

LOW-POWER TRIPLE-CHANNEL DIGITAL ISOLATOR

Features

- High-speed operation
 - DC to 150 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage: 2.70–5.5 V
- Wide Operating Supply Voltage: 2.70–5.5V
- Ultra low power (typical) 5 V Operation:
 - < 1.6 mA per channel at 1 Mbps
 - < 6 mA per channel at 100 Mbps
- 2.70 V Operation:
 - < 1.4 mA per channel at 1 Mbps
 - < 4 mA per channel at 100 Mbps
- High electromagnetic immunity
- Up to 2500 V_{RMS} isolation
- 60-year life at rated working voltage
- Precise timing (typical)
 - <10 ns worst case
 - 1.5 ns pulse width distortion
 - 0.5 ns channel-channel skew
 - 2 ns propagation delay skew
 - 6 ns minimum pulse width
- Transient Immunity 25 kV/μs
- AEC-Q100 qualified
- Wide temperature range
 - –40 to 125 °C at 150 Mbps
- RoHS-compliant packages
 - SOIC-16 wide body
 - SOIC-16 narrow body

Applications

- Industrial automation systems
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Safety Regulatory Approvals

- UL 1577 recognized
 - Up to 2500 V_{RMS} for 1 minute
- CSA component notice 5A approval
 - IEC 60950-1, 61010-1 (reinforced insulation)
- VDE certification conformity
 - IEC 60747-5-2 (VDE0884 Part 2)

Description

Silicon Lab's family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages when compared to legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges throughout their service life, and only VDD bypass capacitors are required.

Data rates up to 150 Mbps are supported, and all devices achieve worst-case propagation delays of less than 10 ns. All products are safety certified by UL, CSA, and VDE and support withstand voltages of up to 2.5 kV_{RMS}. These devices are available in 16-pin wide- and narrow-body SOIC packages.



Ordering Information:
See page 27.

Not Recommended
for New Designs

TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
1. Electrical Specifications	4
2. Functional Description	18
2.1. Theory of Operation	18
2.2. Eye Diagram	19
2.3. Device Operation	20
2.4. Layout Recommendations	22
2.5. Typical Performance Characteristics	23
3. Errata and Design Migration Guidelines	25
3.1. Enable Pin Causes Outputs to Go Low (Revision C Only)	25
3.2. Power Supply Bypass Capacitors (Revision C and Revision D)	25
3.3. Latch Up Immunity (Revision C Only)	25
4. Pin Descriptions	26
5. Ordering Guide	27
6. Package Outline: 16-Pin Wide Body SOIC	29
7. Land Pattern: 16-Pin Wide-Body SOIC	30
8. Package Outline: 16-Pin Narrow Body SOIC	31
9. Land Pattern: 16-Pin Narrow Body SOIC	33
10. Top Marking: 16-Pin Wide Body SOIC	34
10.1. 16-Pin Wide Body SOIC Top Marking	34
10.2. Top Marking Explanation	34
11. Top Marking: 16-Pin Narrow Body SOIC	35
11.1. 16-Pin Narrow Body SOIC Top Marking	35
11.2. Top Marking Explanation	35
Document Change List	36
Contact Information	38

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	150 Mbps, 15 pF, 5 V	-40	25	125*	°C
Supply Voltage	V_{DD1}		2.70	—	5.5	V
	V_{DD2}		2.70	—	5.5	V
*Note: The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.						

Table 2. Absolute Maximum Ratings¹

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature ²	T_{STG}	-65	—	150	°C
Operating Temperature	T_A	-40	—	125	°C
Supply Voltage (Revision C) ³	V_{DD1}, V_{DD2}	-0.5	—	5.75	V
Supply Voltage (Revision D) ³	V_{DD1}, V_{DD2}	-0.5	—	6.0	V
Input Voltage	V_I	-0.5	—	$V_{DD} + 0.5$	V
Output Voltage	V_O	-0.5	—	$V_{DD} + 0.5$	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation Voltage (1 s)		—	—	3600	V_{RMS}
Notes:					
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.					
2. VDE certifies storage temperature from -40 to 150 °C.					
3. See "5. Ordering Guide" on page 27 for more information.					

Table 3. Electrical Characteristics(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = -40 to 125 °C; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V _{IH}		2.0	—	—	V
Low Level Input Voltage	V _{IL}		—	—	0.8	V
High Level Output Voltage	V _{OH}	I _{oh} = −4 mA	V _{DD1} , V _{DD2} − 0.4	4.8	—	V
Low Level Output Voltage	V _{OL}	I _{ol} = 4 mA	—	0.2	0.4	V
Input Leakage Current	I _L		—	—	±10	μA
Output Impedance ¹	Z _O		—	85	—	Ω
Enable Input High Current	I _{ENH}	V _{ENx} = V _{IH}	—	2.0	—	μA
Enable Input Low Current	I _{ENL}	V _{ENx} = V _{IL}	—	2.0	—	μA
DC Supply Current (All inputs 0 V or at Supply)						
Si8430Ax, Bx and Si8435Bx						
V _{DD1}		All inputs 0 DC	—	1.2	1.8	mA
V _{DD2}		All inputs 0 DC	—	1.9	2.9	
V _{DD1}		All inputs 1 DC	—	4.2	6.3	
V _{DD2}		All inputs 1 DC	—	1.9	2.9	
Si8431Ax, Bx						
V _{DD1}		All inputs 0 DC	—	1.7	2.6	mA
V _{DD2}		All inputs 0 DC	—	2.0	3.0	
V _{DD1}		All inputs 1 DC	—	3.7	5.6	
V _{DD2}		All inputs 1 DC	—	3.0	4.5	
1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs)						
Si8430Ax, Bx and Si8435Bx						
V _{DD1}			—	2.7	4.1	mA
V _{DD2}			—	2.2	3.3	
Si8431Ax, Bx						
V _{DD1}			—	2.8	4.2	mA
V _{DD2}			—	2.7	4.1	
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8430Bx, Si8435Bx						
V _{DD1}			—	2.7	4.1	mA
V _{DD2}			—	3.0	4.2	
Si8431Bx						
V _{DD1}			—	3.1	4.3	mA
V _{DD2}			—	3.2	4.5	
Notes:						
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.						
2. t _{PSK(P-P)} is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.						
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.						
4. Start-up time is the time period from the application of power to valid data at the output.						

Table 3. Electrical Characteristics (Continued)(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = -40 to 125 °C; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8430Bx, Si8435Bx						
V _{DD1}			—	2.9	4.4	mA
V _{DD2}			—	14.3	17.9	
Si8431Bx						
V _{DD1}			—	7.0	8.8	mA
V _{DD2}			—	11.0	13.8	
Timing Characteristics						
Si843xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t _{PHL} , t _{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion t _{PLH} - t _{PHL}	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew ²	t _{PSK(P-P)}		—	—	40	ns
Channel-Channel Skew	t _{PSK}		—	—	35	ns
Si843xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t _{PHL} , t _{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion t _{PLH} - t _{PHL}	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew ²	t _{PSK(P-P)}		—	2.0	3.0	ns
Channel-Channel Skew	t _{PSK}		—	0.5	1.8	ns
Notes:						
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.						
2. t _{PSK(P-P)} is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.						
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.						
4. Start-up time is the time period from the application of power to valid data at the output.						

Table 3. Electrical Characteristics (Continued)(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = -40 to 125 °C; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
All Models						
Output Rise Time	t _r	C _L = 15 pF See Figure 2	—	3.8	5.0	ns
Output Fall Time	t _f	C _L = 15 pF See Figure 2	—	2.8	3.7	ns
Common Mode Transient Immunity	CMTI	V _I = V _{DD} or 0 V	—	25	—	kV/μs
Enable to Data Valid ³	t _{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State ³	t _{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time ^{3,4}	t _{SU}		—	15	40	μs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. t_{PSK(P-P)} is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

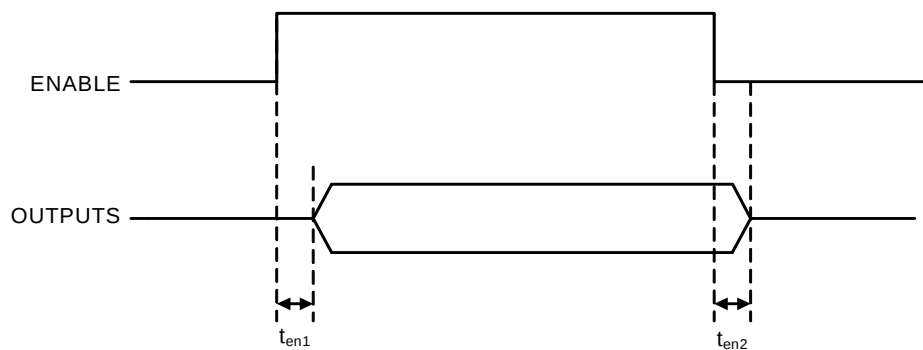


Figure 1. ENABLE Timing Diagram

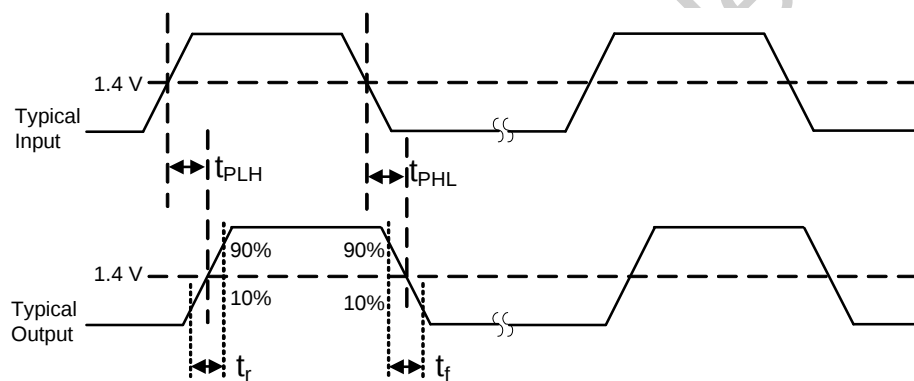


Figure 2. Propagation Delay Timing

Table 4. Electrical Characteristics(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 °C; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V _{IH}		2.0	—	—	V
Low Level Input Voltage	V _{IL}		—	—	0.8	V
High Level Output Voltage	V _{OH}	I _{oh} = −4 mA	V _{DD1} , V _{DD2} − 0.4	3.1	—	V
Low Level Output Voltage	V _{OL}	I _{ol} = 4 mA	—	0.2	0.4	V
Input Leakage Current	I _L		—	—	±10	μA
Output Impedance ¹	Z _O		—	85	—	Ω
Enable Input High Current	I _{ENH}	V _{ENx} = V _{IH}	—	2.0	—	μA
Enable Input Low Current	I _{ENL}	V _{ENx} = V _{IL}	—	2.0	—	μA
DC Supply Current (All inputs 0 V or at supply)						
Si8430Ax, Bx and Si8435Bx						
V _{DD1}		All inputs 0 DC	—	1.2	1.8	mA
V _{DD2}		All inputs 0 DC	—	1.9	2.9	
V _{DD1}		All inputs 1 DC	—	4.2	6.3	
V _{DD2}		All inputs 1 DC	—	1.9	2.9	
Si8431Ax, Bx						
V _{DD1}		All inputs 0 DC	—	1.7	2.6	mA
V _{DD2}		All inputs 0 DC	—	2.0	3.0	
V _{DD1}		All inputs 1 DC	—	3.7	5.6	
V _{DD2}		All inputs 1 DC	—	3.0	4.5	
1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs)						
Si8430Ax, Bx and Si8435Bx						
V _{DD1}			—	2.7	4.1	mA
V _{DD2}			—	2.2	3.3	
Si8431Ax, Bx						
V _{DD1}			—	2.8	4.2	mA
V _{DD2}			—	2.7	4.1	
Notes:						
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.						
2. t _{PSK(P-P)} is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.						
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.						
4. Start-up time is the time period from the application of power to valid data at the output.						

Table 4. Electrical Characteristics (Continued)

($V_{DD1} = 3.3 \text{ V} \pm 10\%$, $V_{DD2} = 3.3 \text{ V} \pm 10\%$, $T_A = -40 \text{ to } 125 \text{ }^\circ\text{C}$; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8430Bx, Si8435Bx			—	2.7	4.1	mA
V _{DD1} V _{DD2}			—	3.0	4.2	
Si8431Bx			—	3.1	4.3	mA
V _{DD1} V _{DD2}			—	3.2	4.5	
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8430Bx, Si8435Bx			—	2.8	4.2	mA
V _{DD1} V _{DD2}			—	10.1	12.6	
Si8431Bx			—	5.5	6.9	mA
V _{DD1} V _{DD2}			—	8.0	10.0	
Timing Characteristics						
Si843xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t _{PHL} , t _{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion t _{PLH} - t _{PHL}	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew ²	t _{PSK(P-P)}		—	—	40	ns
Channel-Channel Skew	t _{PSK}		—	—	35	ns
Notes:						
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.						
2. t _{PSK(P-P)} is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.						
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.						
4. Start-up time is the time period from the application of power to valid data at the output.						

Table 4. Electrical Characteristics (Continued)(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 °C; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si843xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t _{PHL} , t _{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion t _{PLH} - t _{PHL}	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew ²	t _{PSK(P-P)}		—	2.0	3.0	ns
Channel-Channel Skew	t _{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t _r	C _L = 15 pF See Figure 2	—	4.3	6.1	ns
Output Fall Time	t _f	C _L = 15 pF See Figure 2	—	3.0	4.3	ns
Common Mode Transient Immunity	CMTI	V _I = V _{DD} or 0 V	—	25	—	kV/μs
Enable to Data Valid ³	t _{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State ³	t _{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time ^{3,4}	t _{SU}		—	15	40	μs
Notes: 1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. 2. t_{PSK(P-P)} is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. 3. See "3. Errata and Design Migration Guidelines" on page 25 for more details. 4. Start-up time is the time period from the application of power to valid data at the output.						

Table 5. Electrical Characteristics¹

($V_{DD1} = 2.70\text{ V}$, $V_{DD2} = 2.70\text{ V}$, $T_A = -40\text{ to }125\text{ }^{\circ}\text{C}$; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	$I_{OH} = -4\text{ mA}$	$V_{DD1}, V_{DD2} - 0.4$	2.3	—	V
Low Level Output Voltage	V_{OL}	$I_{OL} = 4\text{ mA}$	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	± 10	μA
Output Impedance ²	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	μA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	μA
DC Supply Current (All inputs 0 V or at supply)						
Si8430Ax, Bx and Si8435Bx						
V_{DD1}		All inputs 0 DC	—	1.2	1.8	mA
V_{DD2}		All inputs 0 DC	—	1.9	2.9	
V_{DD1}		All inputs 1 DC	—	4.2	6.3	
V_{DD2}		All inputs 1 DC	—	1.9	2.9	
Si8431Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.7	2.6	mA
V_{DD2}		All inputs 0 DC	—	2.0	3.0	
V_{DD1}		All inputs 1 DC	—	3.7	5.6	
V_{DD2}		All inputs 1 DC	—	3.0	4.5	
1 Mbps Supply Current (All inputs = 500 kHz square wave, $C_I = 15\text{ pF}$ on all outputs)						
Si8430Ax, Bx and Si8435Bx						
V_{DD1}			—	2.7	4.1	mA
V_{DD2}			—	2.2	3.3	
Si8431Ax, Bx						
V_{DD1}			—	2.8	4.2	mA
V_{DD2}			—	2.7	4.1	
Notes:						
1. Specifications in this table are also valid at $V_{DD1} = 2.6\text{ V}$ and $V_{DD2} = 2.6\text{ V}$ when the operating temperature range is constrained to $T_A = 0\text{ to }85\text{ }^{\circ}\text{C}$.						
2. The nominal output impedance of an isolator driver channel is approximately $85\text{ }\Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.						
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.						
4. See "3. Errata and Design Migration Guidelines" on page 25 for more details.						
5. Start-up time is the time period from the application of power to valid data at the output.						

Table 5. Electrical Characteristics¹ (Continued)(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = -40 to 125 °C; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8430Bx, Si8435Bx			—	2.7	4.1	mA
V _{DD1} V _{DD2}			—	3.0	4.2	
Si8431Bx			—	3.1	4.3	mA
V _{DD1} V _{DD2}			—	3.2	4.5	
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8430Bx, Si8435Bx			—	2.8	4.2	mA
V _{DD1} V _{DD2}			—	8.0	10	
Si8431Bx			—	4.7	5.9	mA
V _{DD1} V _{DD2}			—	6.7	8.4	
Timing Characteristics						
Si843xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t _{PHL} , t _{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion t _{PLH} - t _{PHL}	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew ³	t _{PSK(P-P)}		—	—	40	ns
Channel-Channel Skew	t _{PSK}		—	—	35	ns
Notes:						
1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T _A = 0 to 85 °C.						
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.						
3. t _{PSK(P-P)} is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.						
4. See "3. Errata and Design Migration Guidelines" on page 25 for more details.						
5. Start-up time is the time period from the application of power to valid data at the output.						

Table 5. Electrical Characteristics¹ (Continued)

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = -40 to 125 °C; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si843xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t _{PHL} , t _{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion t _{PLH} - t _{PHL}	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew ³	t _{PSK(P-P)}		—	2.0	3.0	ns
Channel-Channel Skew	t _{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t _r	C _L = 15 pF See Figure 2	—	4.8	6.5	ns
Output Fall Time	t _f	C _L = 15 pF See Figure 2	—	3.2	4.6	ns
Common Mode Transient Immunity	CMTI	V _I = V _{DD} or 0 V	—	25	—	kV/μs
Enable to Data Valid ⁴	t _{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State ⁴	t _{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time ^{4,5}	t _{SU}		—	15	40	μs
Notes: - Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C. - The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. - t_{PSK(P-P)} is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature. - See "3. Errata and Design Migration Guidelines" on page 25 for more details. - Start-up time is the time period from the application of power to valid data at the output.						

Table 6. Regulatory Information*

CSA
The Si84xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V _{RMS} reinforced insulation working voltage; up to 600 V _{RMS} basic insulation working voltage.
60950-1: Up to 130 V _{RMS} reinforced insulation working voltage; up to 1000 V _{RMS} basic insulation working voltage.
VDE
The Si84xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 560 V _{peak} for basic insulation working voltage.
UL
The Si84xx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 V _{RMS} isolation voltage for basic insulation.
*Note: Regulatory Certifications apply to 2.5 kV _{RMS} rated devices which are production tested to 3.0 kV _{RMS} for 1 sec. For more information, see "5. Ordering Guide" on page 27.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB SOIC-16	NB SOIC-16	
Nominal Air Gap (Clearance) ¹	L(IO1)		8.0	4.9	mm
Nominal External Tracking (Creepage) ¹	L(IO2)		8.0	4.01	mm
Minimum Internal Gap (Internal Clearance)			0.008	0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	V _{RMS}
Erosion Depth	ED		0.040	0.019	mm
Resistance (Input-Output) ²	R _{IO}		10 ¹²	10 ¹²	Ω
Capacitance (Input-Output) ²	C _{IO}	f = 1 MHz	2.0	2.0	pF
Input Capacitance ³	C _I		4.0	4.0	pF

Notes:

- The values in this table correspond to the nominal creepage and clearance values as detailed in "6. Package Outline: 16-Pin Wide Body SOIC" and "8. Package Outline: 16-Pin Narrow Body SOIC". VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 package and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-16 package and 7.6 mm minimum for the WB SOIC-16 package.
- To determine resistance and capacitance, the Si84xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
- Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Condition	Specification
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages $\leq 150 V_{RMS}$	I-IV
	Rated Mains Voltages $\leq 300 V_{RMS}$	I-III
	Rated Mains Voltages $\leq 400 V_{RMS}$	I-II
	Rated Mains Voltages $\leq 600 V_{RMS}$	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics for Si84xxxB*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 ($V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, $t_m = 1$ sec, Partial Discharge < 5 pC)	1050	V peak
Transient Overvoltage	V_{IOTM}	$t = 60$ sec	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S , $V_{IO} = 500$ V	R_S		$>10^9$	Ω
*Note: Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.				

Table 10. IEC Safety Limiting Values¹

Parameter	Symbol	Test Condition	Min	Typ	Max		Unit
					WB SOIC-16	NB SOIC-16	
Case Temperature	T_S		—	—	150	150	$^{\circ}\text{C}$
Safety input, output, or supply current	I_S	$\theta_{JA} = 100$ $^{\circ}\text{C}/\text{W}$ (WB SOIC-16), 105 $^{\circ}\text{C}/\text{W}$ (NB SOIC-16), $V_I = 5.5$ V, $T_J = 150$ $^{\circ}\text{C}$, $T_A = 25$ $^{\circ}\text{C}$	—	—	220	210	mA
Device Power Dissipation ²	P_D		—	—	275	275	mW
Notes: 1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 3 and 4. 2. The Si843x is tested with $VDD1 = VDD2 = 5.5$ V, $T_J = 150$ $^{\circ}\text{C}$, $CL = 15$ pF, input a 150 Mbps 50% duty cycle square wave.							

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ		Max	Unit
				WB SOIC-16	NB SOIC-16		
IC Junction-to-Air Thermal Resistance	θ_{JA}		—	100	105	—	°C/W

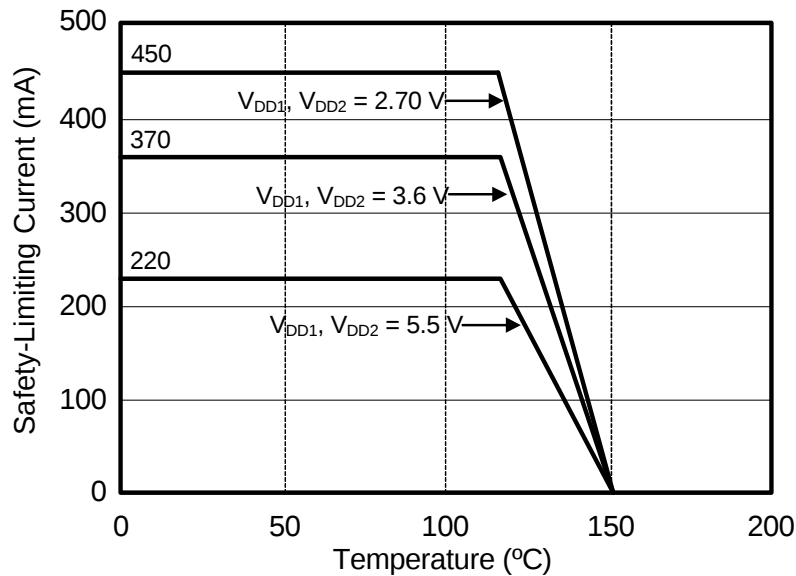


Figure 3. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

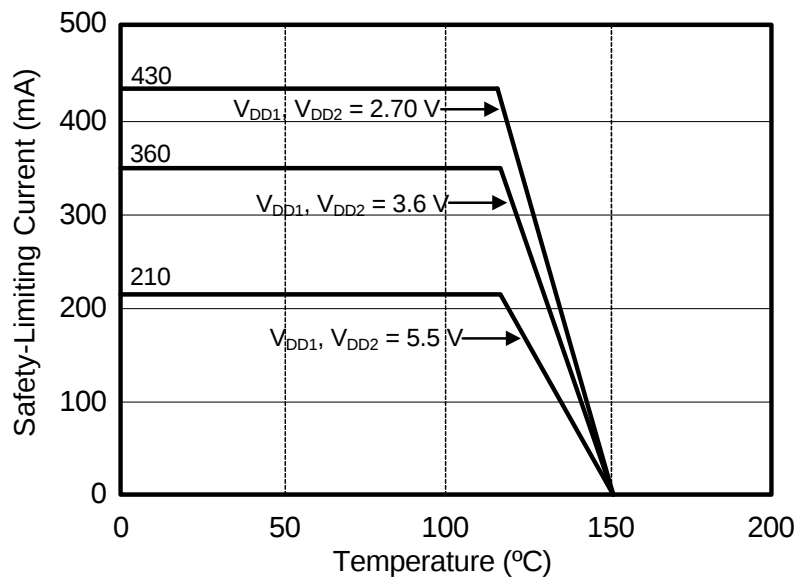


Figure 4. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2. Functional Description

2.1. Theory of Operation

The operation of an Si843x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si843x channel is shown in Figure 5.

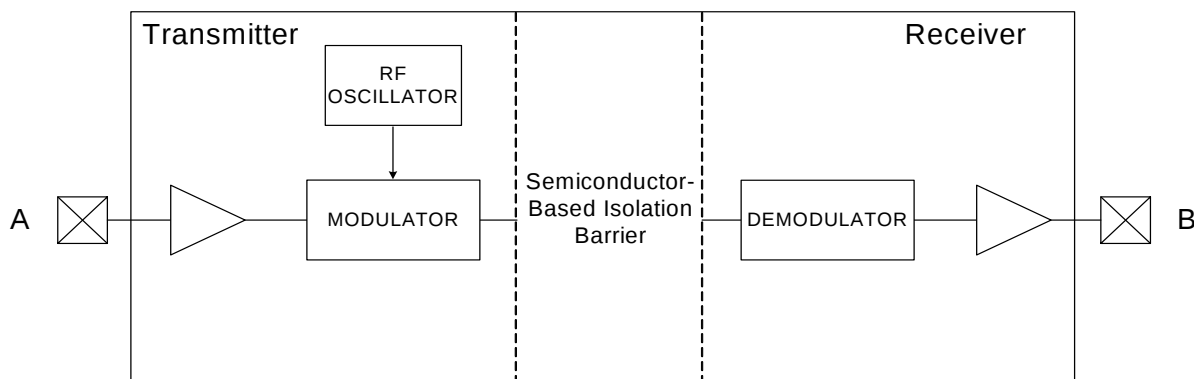


Figure 5. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 6 for more details.

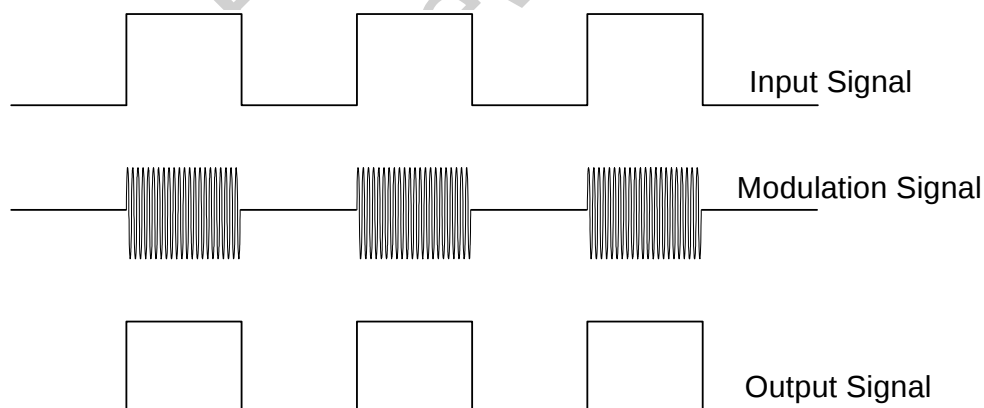


Figure 6. Modulation Scheme

2.2. Eye Diagram

Figure 7 illustrates an eye-diagram taken on an Si8430. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8430 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 250 ps peak jitter were exhibited.

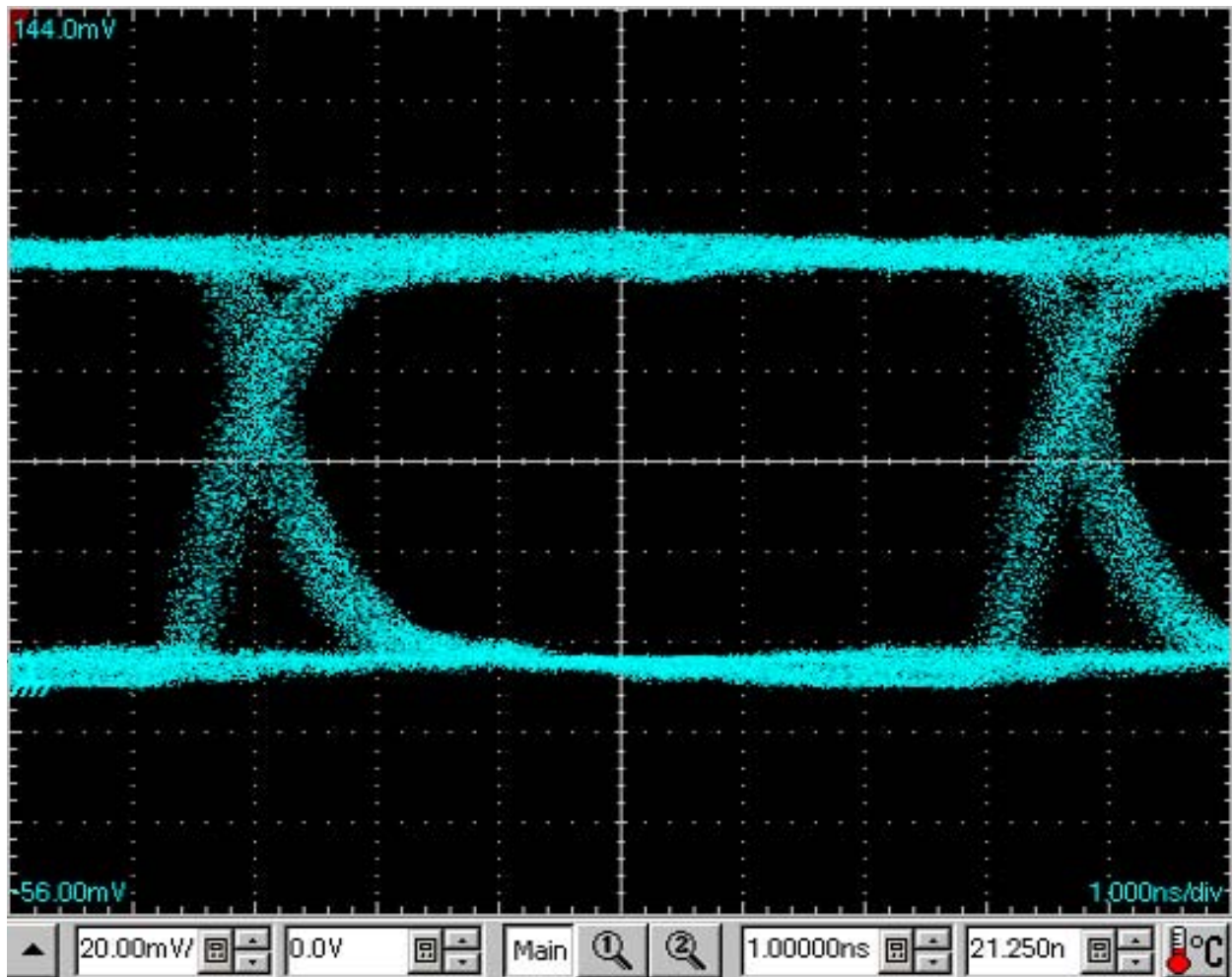


Figure 7. Eye Diagram

2.3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Table 12. Table 13 provides an overview of the output states when the Enable pins are active.

Table 12. Si84xx Logic Operation Table

V _I Input ^{1,2}	EN Input ^{1,2,3,4}	VDDI State ^{1,5,6}	VDDO State ^{1,5,6}	V _O Output ^{1,2}	Comments
H	H or NC	P	P	H	Enabled, normal operation.
L	H or NC	P	P	L	
X ⁷	L	P	P	Hi-Z or L ⁸	Disabled.
X ⁷	H or NC	UP	P	L	Upon transition of VDDI from unpowered to powered, V _O returns to the same state as V _I in less than 1 μ s.
X ⁷	L	UP	P	Hi-Z or L ⁸	Disabled.
X ⁷	X ⁷	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V _O returns to the same state as V _I within 1 μ s, if EN is in either the H or NC state. Upon transition of VDDO from unpowered to powered, V _O returns to Hi-Z with 1 μ s if EN is L.

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals. EN is the enable control input located on the same output side.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the Si84xx is operating in noisy environments.
4. No Connect (NC) replaces EN1 on Si8430/35. No Connect replaces EN2 on the Si8435. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
5. "Powered" state (P) is defined as 2.70 V < VDD < 5.5 V.
6. "Unpowered" state (UP) is defined as VDD = 0 V.
7. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
8. When using the enable pin (EN) function, the output pin state is driven to a logic low state when the EN pin is disabled (EN = 0) in Revision C. Revision D outputs go into a high-impedance state when the EN pin is disabled (EN = 0). See "3. Errata and Design Migration Guidelines" on page 25 for more details.

Table 13. Enable Input Truth Table¹

P/N	EN1 ^{1,2}	EN2 ^{1,2}	Operation
Si8430	—	H	Outputs B1, B2, B3 are enabled and follow input state.
	—	L	Outputs B1, B2, B3 are disabled and Logic Low or in high impedance state. ³
Si8431	H	X	Output A3 enabled and follows input state.
	L	X	Output A3 disabled and Logic Low or in high impedance state. ³
	X	H	Outputs B1, B2 are enabled and follow input state.
	X	L	Outputs B1, B2 are disabled and Logic Low or in high impedance state. ³
Si8435	—	—	Outputs B1, B2, B3 are enabled and follow input state.

Notes:

1. Enable inputs EN1 and EN2 can be used for multiplexing, for clock sync, or other output control. These inputs are internally pulled-up to local VDD by a 3 μ A current source allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating. If EN1, EN2 are unused, it is recommended they be connected to an external logic level, especially if the Si84xx is operating in a noisy environment.
2. X = not applicable; H = Logic High; L = Logic Low.
3. When using the enable pin (EN) function, the output pin state is driven to a logic low state when the EN pin is disabled (EN = 0) in Revision C. Revision D outputs go into a high-impedance state when the EN pin is disabled (EN = 0). See "3. Errata and Design Migration Guidelines" on page 25 for more details.

2.4. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with $>30\text{ V}_{AC}$) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with $<30\text{ V}_{AC}$) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 6 on page 15 and Table 7 on page 15 detail the working voltage and creepage/clearance capabilities of the Si84xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, etc.) requirements before starting any design that uses a digital isolator.

The following sections detail the recommended bypass and decoupling components necessary to ensure robust overall performance and reliability for systems using the Si84xx digital isolators.

2.4.1. Supply Bypass

Digital integrated circuit components typically require $0.1\text{ }\mu\text{F}$ (100 nF) bypass capacitors when used in electrically quiet environments. However, digital isolators are commonly used in hazardous environments with excessively noisy power supplies. To counteract these harsh conditions, it is recommended that an additional $1\text{ }\mu\text{F}$ bypass capacitor be added between VDD and GND on both sides of the package. The capacitors should be placed as close as possible to the package to minimize stray inductance. If the system is excessively noisy, it is recommended that the designer add $50\text{ to }100\text{ }\Omega$ resistors in series with the VDD supply voltage source and $50\text{ to }300\text{ }\Omega$ resistors in series with the digital inputs/outputs (see Figure 8). For more details, see "3. Errata and Design Migration Guidelines" on page 25.

All components upstream or downstream of the isolator should be properly decoupled as well. If these components are not properly decoupled, their supply noise can couple to the isolator inputs and outputs, potentially causing damage if spikes exceed the maximum ratings of the isolator (6 V). In this case, the $50\text{ to }300\text{ }\Omega$ resistors protect the isolator's inputs/outputs (note that permanent device damage may occur if the absolute maximum ratings are exceeded). Functional operation should be restricted to the conditions specified in Table 1, "Recommended Operating Conditions," on page 4.

2.4.2. Pin Connections

No connect pins are not internally connected. They can be left floating, tied to V_{DD} , or tied to GND.

2.4.3. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately $85\text{ }\Omega$, $\pm 40\%$, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. The series termination resistor values should be scaled appropriately while keeping in mind the recommendations described in "2.4.1. Supply Bypass" above.

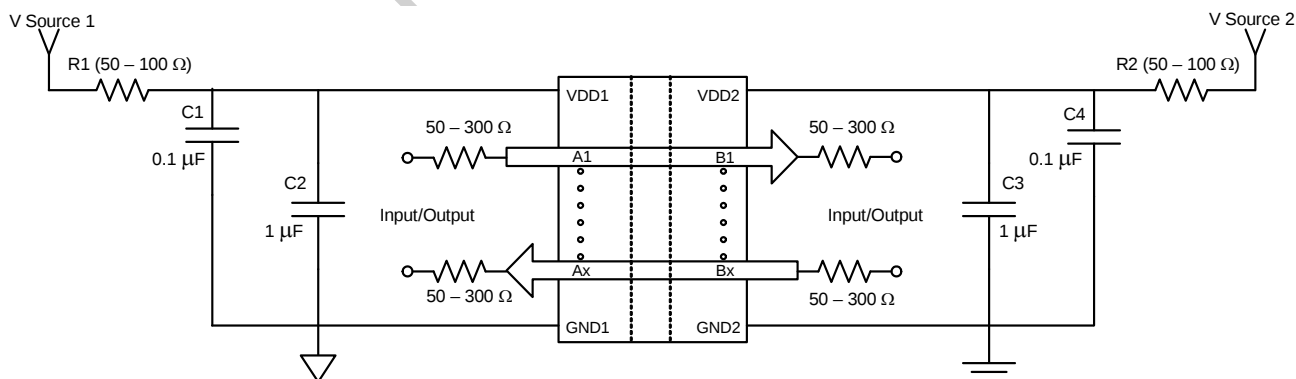


Figure 8. Recommended Bypass Components for the Si84xx Digital Isolator Family

2.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 3, 4, and 5 for actual specification limits.

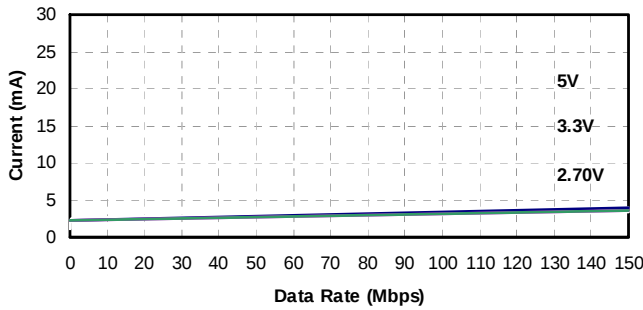


Figure 9. Si8430/35 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

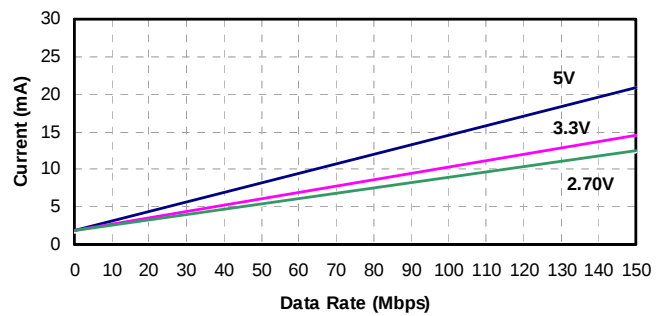


Figure 12. Si8430/35 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

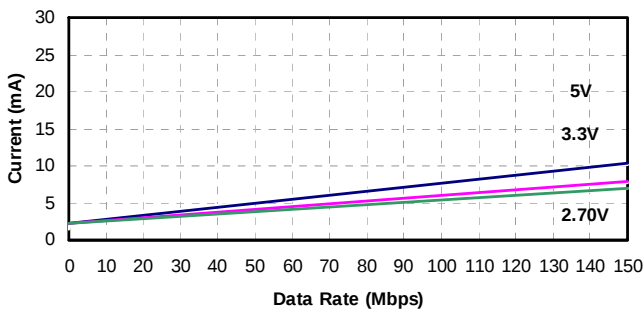


Figure 10. Si8431 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

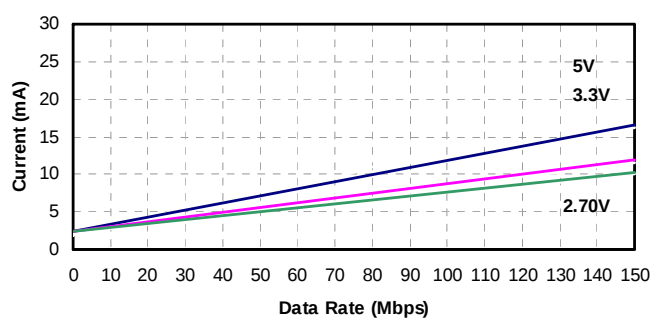


Figure 13. Si8431 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

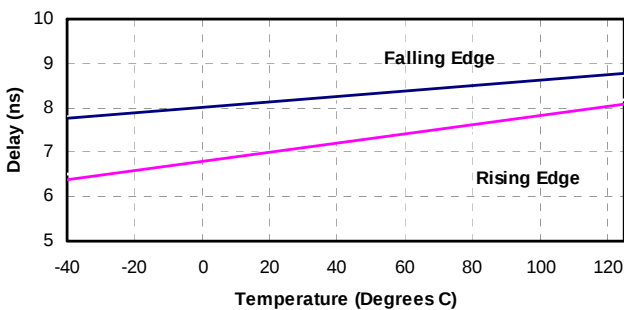


Figure 11. Propagation Delay vs. Temperature

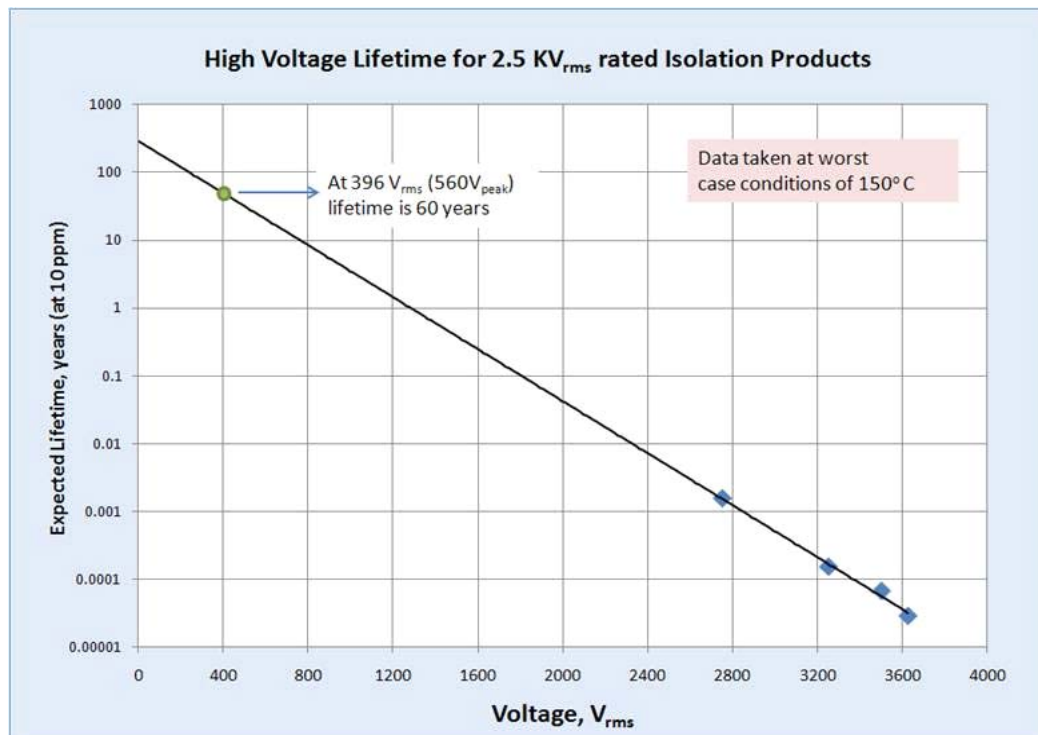


Figure 14. Si84xx Time-Dependent Dielectric Breakdown

3. Errata and Design Migration Guidelines

The following errata apply to Revision C devices only. See "5. Ordering Guide" on page 27 for more details. No errata exist for Revision D devices.

3.1. Enable Pin Causes Outputs to Go Low (Revision C Only)

When using the enable pin (EN1, EN2) function on the 3-channel (Si8430/1) isolators, the corresponding output pin states (pin = An, Bn, where n can be 1...3) are driven to a logic low (to ground) when the enable pin is disabled (EN1 or EN2 = 0). This functionality is different from the legacy 3-channel (Si8430/1) isolators. On those devices, the isolator outputs go into a high-impedance state (Hi-Z) when the enable pin is disabled (EN1 = 0 or EN2 = 0).

3.1.1. Resolution

The enable pin functionality causing the outputs to go low is supported in production for Revision C of the Si84xx devices. Revision D corrects the enable pin functionality (i.e., the outputs will go into the high-impedance state to match the legacy isolator products). Refer to the Ordering Guide sections of the data sheet(s) for current ordering information.

3.2. Power Supply Bypass Capacitors (Revision C and Revision D)

When using the Si84xx isolators with power supplies ≥ 4.5 V, sufficient VDD bypass capacitors must be present on both the VDD1 and VDD2 pins to ensure the VDD rise time is less than $0.5 \text{ V}/\mu\text{s}$ (which is $> 9 \mu\text{s}$ for a ≥ 4.5 V supply). Although rise time is power supply dependent, $\geq 1 \mu\text{F}$ capacitors are required on both power supply pins (VDD1, VDD2) of the isolator device.

3.2.1. Resolution

For recommendations on resolving this issue, see "2.4.1. Supply Bypass" on page 22. Additionally, refer to "5. Ordering Guide" on page 27 for current ordering information.

3.3. Latch Up Immunity (Revision C Only)

Latch up immunity generally exceeds $\pm 200 \text{ mA}$ per pin. Exceptions: Certain pins provide $< 100 \text{ mA}$ of latch-up immunity. To increase latch-up immunity on these pins, 100Ω of equivalent resistance must be included in series with *all* of the pins listed in Table 14. The 100Ω equivalent resistance can be comprised of the source driver's output resistance and a series termination resistor. The Si8431 is not affected when using power supply voltages (VDD1 and VDD2) $\leq 3.5 \text{ V}$.

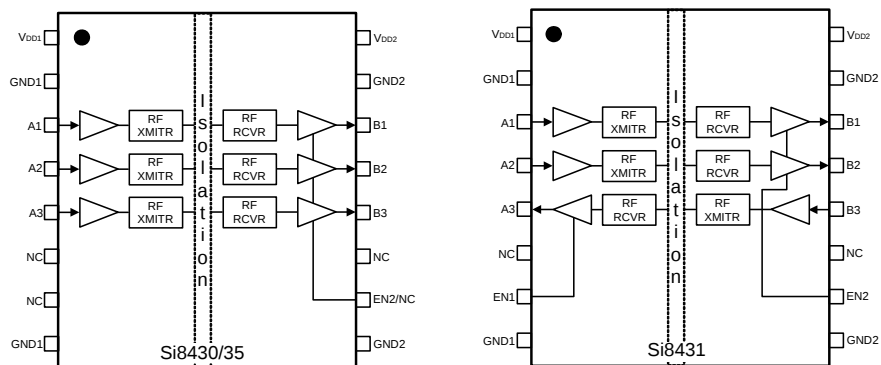
3.3.1. Resolution

This issue has been corrected with Revision D of the device. Refer to "5. Ordering Guide" for current ordering information.

Table 14. Affected Ordering Part Numbers (Revision C Only)

Affected Ordering Part Numbers*	Device Revision	Pin#	Name	Pin Type
SI8430SV-C-IS/IS1, SI8431SV-C-IS/IS1	C	5	A3	Input or Output
		10	EN2	Input
		14	B1	Output
SI8435SV-C-IS/IS1	C	5	A3	Input
		14	B1	Output
*Note: "SV" = Speed Grade/Isolation Rating (AA, AB, BA, BB).				

4. Pin Descriptions



Name	SOIC-16 Pin#	Type	Description ¹
V _{DD1}	1	Supply	Side 1 power supply.
GND1	2	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital I/O	Side 1 digital input or output.
NC	6	NA	No Connect.
EN1/NC ²	7	Digital Input	Side 1 active high enable. NC on Si8430/35
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
EN2/NC ²	10	Digital Input	Side 2 active high enable. NC on Si8435.
NC	11	NA	No Connect.
B3	12	Digital I/O	Side 2 digital input or output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15	Ground	Side 2 ground.
V _{DD2}	16	Supply	Side 2 power supply.

Notes:

- For narrow-body devices, Pin 2 and Pin 8 GND must be externally connected to respective ground. Pin 9 and Pin 15 must also be connected to external ground.
- No Connect. These pins are not internally connected. They can be left floating, tied to VDD or tied to GND.

5. Ordering Guide

These devices are not recommended for new designs. Please see the Si863x data sheet for replacement options.

Table 15. Ordering Guide for Valid OPNs¹

Ordering Part Number (OPN)	Alternative Part Number (APN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Package Type
Revision D Devices ²						
Si8430AB-D-IS	Si8630AB-B-IS	3	0	1	2.5 kVrms	WB SOIC-16 ^{1,3}
Si8430BB-D-IS	Si8630BB-B-IS	3	0	150		
Si8431AB-D-IS	Si8631AB-B-IS	2	1	1		
Si8431BB-D-IS	Si8631BB-B-IS	2	1	150		
Si8435BB-D-IS	Si8635BB-B-IS	3	0	150		
Si8430AB-D-IS1	Si8630AB-B-IS1	3	0	1	2.5 kVrms	NB SOIC-16 ¹
Si8430BB-D-IS1	Si8630BB-B-IS1	3	0	150		
Si8431AB-D-IS1	Si8631AB-B-IS1	2	1	1		
Si8431BB-D-IS1	Si8631BB-B-IS1	2	1	150		
Si8435BB-D-IS1	Si8635BC-B-IS1	3	0	150		
Notes:						
1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures. Moisture sensitivity level is MSL2A for wide-body SOIC-16 packages. Moisture sensitivity level is MSL2A for narrow-body SOIC-16 packages. 2. Revision C and Revision D devices are supported for existing designs. 3. AEC-Q100 qualified.						

Table 15. Ordering Guide for Valid OPNs¹ (Continued)

Ordering Part Number (OPN)	Alternative Part Number (APN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Package Type
Revision C Devices ²						
Si8430AB-C-IS	Si8630AB-B-IS	3	0	1	2.5 kVrms	WB SOIC-16 ¹
Si8430BB-C-IS	Si8630BB-B-IS	3	0	150		
Si8431AB-C-IS	Si8631AB-B-IS	2	1	1		
Si8431BB-C-IS	Si8631BB-B-IS	2	1	150		
Si8435BB-C-IS	Si8635BB-B-IS	3	0	150		
Si8430AB-C-IS1	Si8630AB-B-IS1	3	0	1	2.5 kVrms	NB SOIC-16 ¹
Si8430BB-C-IS1	Si8630BB-B-IS1	3	0	150		
Si8431AB-C-IS1	Si8631AB-B-IS1	2	1	1		
Si8431BB-C-IS1	Si8631BB-B-IS1	2	1	150		
Si8435BB-C-IS1	Si8635BC-B-IS1	3	0	150		
Notes:						
1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures. Moisture sensitivity level is MSL2A for wide-body SOIC-16 packages. Moisture sensitivity level is MSL2A for narrow-body SOIC-16 packages.						
2. Revision C and Revision D devices are supported for existing designs.						
3. AEC-Q100 qualified.						

6. Package Outline: 16-Pin Wide Body SOIC

Figure 15 illustrates the package details for the Triple-Channel Digital Isolator. Table 16 lists the values for the dimensions shown in the illustration.

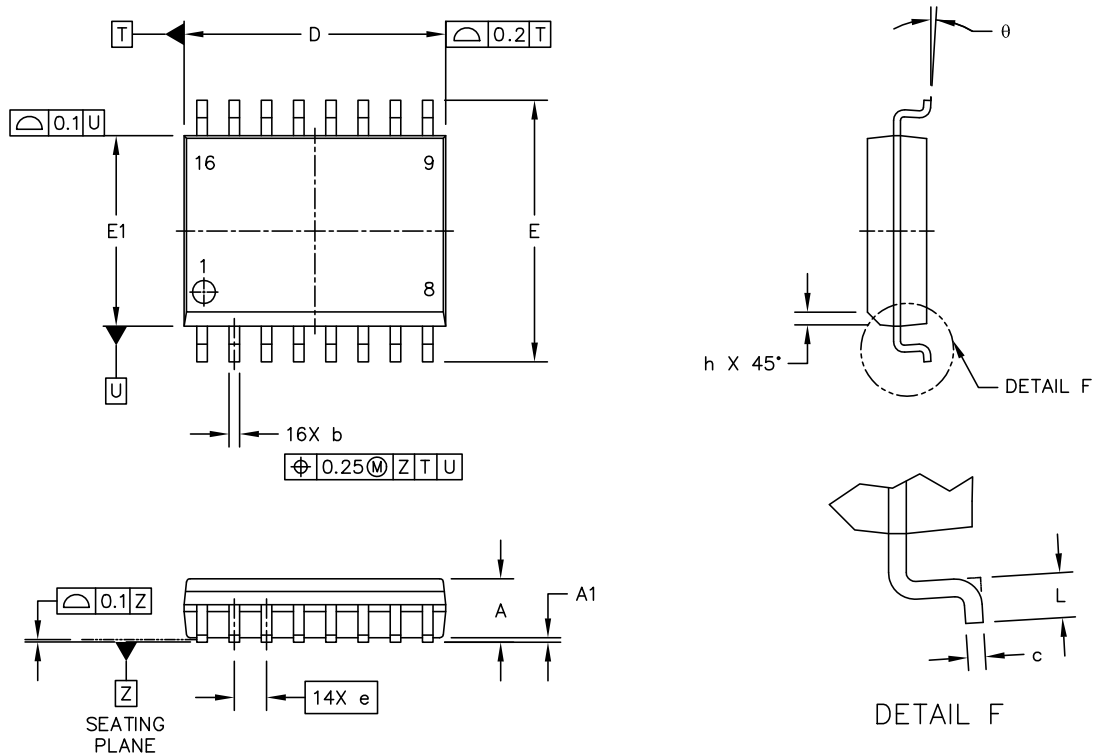


Figure 15. 16-Pin Wide Body SOIC

Table 16. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

7. Land Pattern: 16-Pin Wide-Body SOIC

Figure 16 illustrates the recommended land pattern details for the Si843x in a 16-pin wide-body SOIC. Table 17 lists the values for the dimensions shown in the illustration.

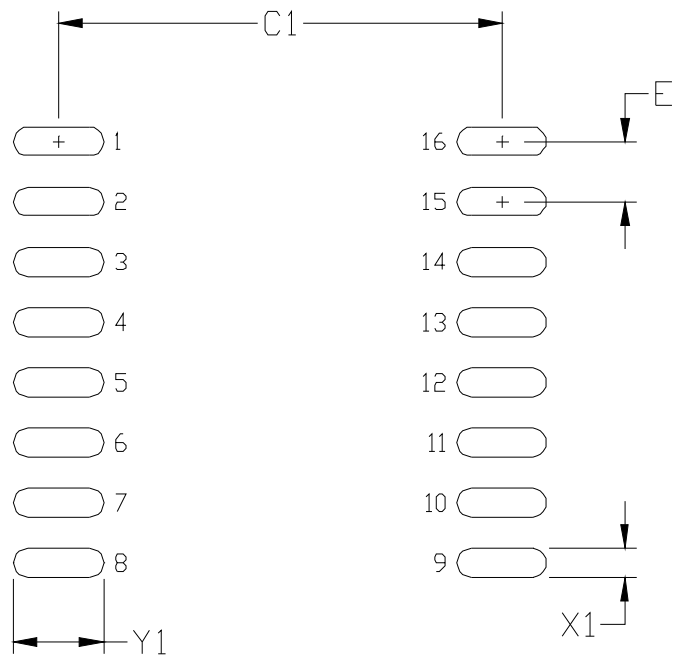


Figure 16. 16-Pin SOIC Land Pattern

Table 17. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90
Notes: 1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion). 2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.		

8. Package Outline: 16-Pin Narrow Body SOIC

Figure 17 illustrates the package details for the Si84xx in a 16-pin narrow-body SOIC (SO-16). Table 18 lists the values for the dimensions shown in the illustration.

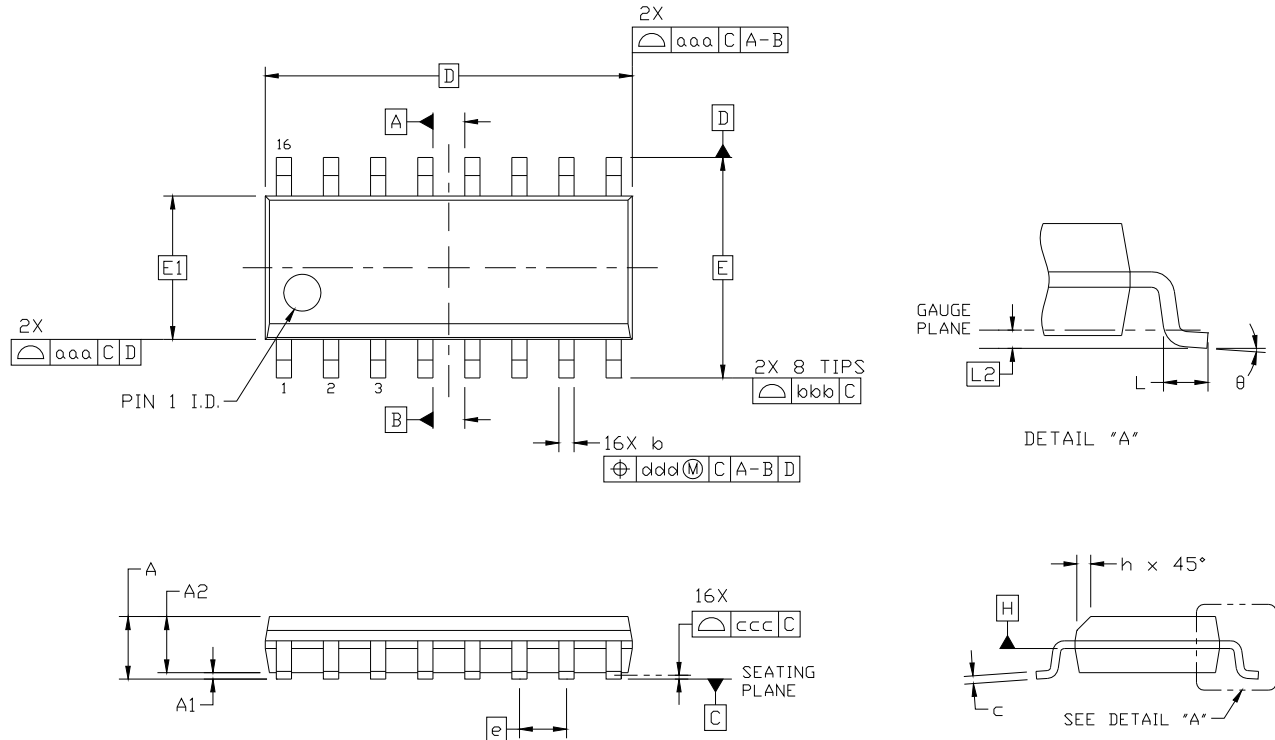


Figure 17. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 18. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	

Table 18. Package Diagram Dimensions (Continued)

Dimension	Min	Max
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	
Notes: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC. 4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

9. Land Pattern: 16-Pin Narrow Body SOIC

Figure 18 illustrates the recommended land pattern details for the Si843x in a 16-pin narrow-body SOIC. Table 19 lists the values for the dimensions shown in the illustration.

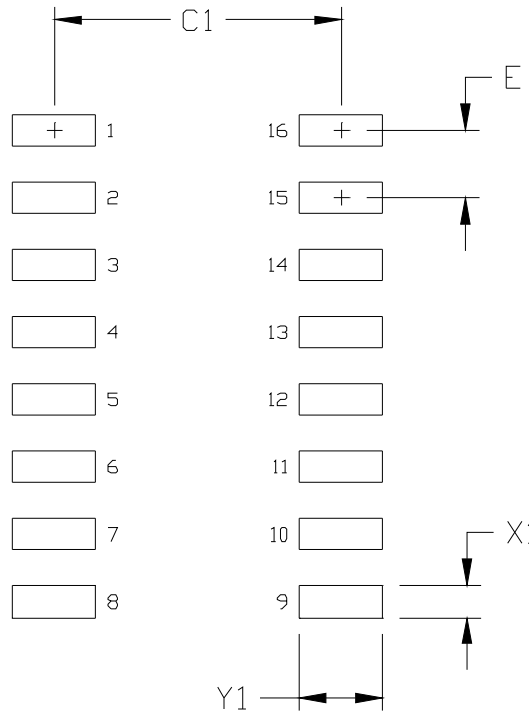


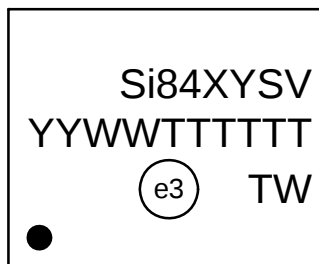
Figure 18. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 19. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55
Notes: 1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion). 2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.		

10. Top Marking: 16-Pin Wide Body SOIC

10.1. 16-Pin Wide Body SOIC Top Marking

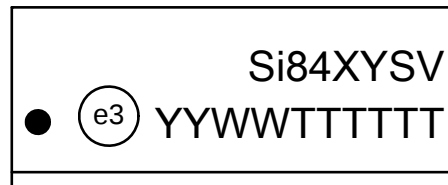


10.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (3, 2, 1) Y = # of reverse channels (1, 0)* S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by Assembly House
	TTTTTT = Mfg Code	Manufacturing Code from Assembly House
Line 3 Marking:	Circle = 1.5 mm Diameter (Center-Justified)	"e3" Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan
*Note: Si8435 has 0 reverse channels.		

11. Top Marking: 16-Pin Narrow Body SOIC

11.1. 16-Pin Narrow Body SOIC Top Marking



11.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (3, 2, 1) Y = # of reverse channels (1, 0)* S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	"e3" Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form.
	Circle = 1.2 mm diameter	"e3" Pb-Free Symbol.
*Note: Si8435 has 0 reverse channels.		

DOCUMENT CHANGE LIST

Revision 0.32 to Revision 0.33

- Rev 0.33 is the first revision of this document that applies to the new series of ultra low power isolators featuring pinout and functional compatibility with previous isolator products.
- Updated "1. Electrical Specifications".
- Updated "5. Ordering Guide".
- Added "10. Top Marking: 16-Pin Wide Body SOIC".

Revision 0.33 to Revision 0.34

- Updated all specs to reflect latest silicon.

Revision 0.34 to Revision 0.35

- Updated all specs to reflect latest silicon.
- Added "3. Errata and Design Migration Guidelines" on page 25.
- Added "11. Top Marking: 16-Pin Narrow Body SOIC" on page 35.

Revision 0.35 to Revision 1.0

- Updated document to reflect availability of Revision D silicon.
- Updated Tables 3,4, and 5.
 - Updated all supply currents and channel-channel skew.
- Updated Table 2.
 - Updated absolute maximum supply voltage.
- Updated Table 7.
 - Updated clearance and creepage dimensions.
- Updated Table 12.
 - Updated Note 7.
- Updated Table 13.
 - Updated Note 3.
- Updated "3. Errata and Design Migration Guidelines" on page 25.
- Updated "5. Ordering Guide" on page 27.

Revision 1.0 to Revision 1.1

- Updated Tables 3, 4, and 5.
 - Updated notes in tables to reflect output impedance of 85 Ω .
 - Updated rise and fall time specifications.
 - Updated CMTI value.

Revision 1.1 to Revision 1.2

- Updated document throughout to include MSL improvements to MSL2A.
- Updated "5. Ordering Guide" on page 27.
 - Updated Note 1 in ordering guide table to reflect improvement and compliance to MSL2A moisture sensitivity level.

Revision 1.2 to Revision 1.3

- Updated "Features" on page 1.
- Moved Tables 1 and 2 to page 4.
- Updated Tables 6, 7, 8, and 9.
- Updated Table 12 footnotes.
- Added Figure 14, "Si84xx Time-Dependent Dielectric Breakdown," on page 24.

Revision 1.3 to Revision 1.4

- Updated "2.4.1. Supply Bypass" on page 22.
- Added Figure 8, "Recommended Bypass Components for the Si84xx Digital Isolator Family," on page 22.
- Updated "3.2. Power Supply Bypass Capacitors (Revision C and Revision D)" on page 25.

Revision 1.4 to Revision 1.5

- Updated "5. Ordering Guide" on page 27 to include MSL2A.

Revision 1.5 to Revision 1.6

- Updated "5. Ordering Guide" on page 27 to include new title note and "Alternative Part Number (APN)" column.

NOTES:

Not Recommended
for New Designs

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
<https://www.silabs.com/support/pages/contacttechnicalsupport.aspx>
and register to submit a technical support request.

Not Recommended
for New Designs

Patent Notice

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.
Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.