MN3664

5000-Bit High-Resolution CCD Linear Image Sensor

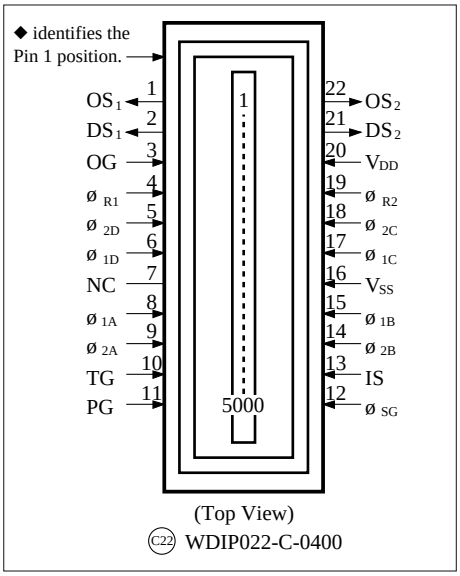
■ Overview

The MN3664 is a 5000-pixel high resolution CCD linear image sensor combining photo-sites using floating photodiodes and CCD analog shift registers for read out. It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

■ Features

- 5000 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- Permits high speed scanning of a data rate of 14MHz.
- High blue responsivity of a maximum responsivity ratio of 40% (typ.) at 400nm, and smooth spectral response over the entire visible region.
- Large signal output of 800mV (typ.) at saturation, and hold type combined odd/even output that makes signal processing easy.
- 64 Black dummy bits and sufficiently low optical response (typ. 0.5%) at the areas other than the photodetector region.
- Operation with a single +12V positive power supply.

■ Pin Assignments



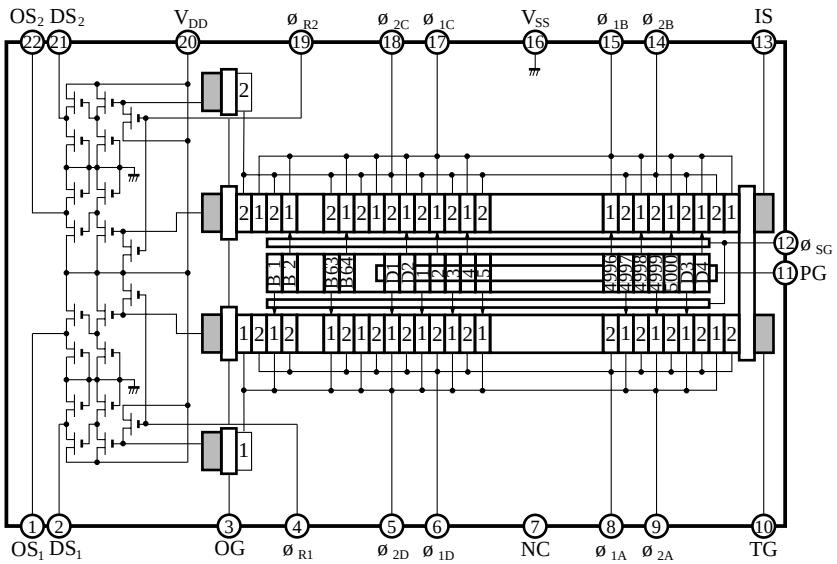
(Top View)

C22 WDIP022-C-0400

■ Application

- Reading out drawings, characters and numerals in copying machines, fax machines, OCRs, etc.
- Measurement of position and dimensions of objects.

■ Block Diagram



B1 to B64 : Black reference pixels

D1 to D 4 : Dummy invalid pixels

■ Absolute Maximum Ratings (Ta=25˚C, V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +17	V
Input voltage	V_I	– 0.3 to +17	V
Output voltage	V_O	– 0.3 to +17	V
Operating temperature range	T_{opr}	–20 to + 60	˚C
Storage temperature range	T_{stg}	–40 to +100	˚C

■ Operating Conditions

• Voltage conditions (Ta=–20 to + 60˚C, V_{SS}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V_{DD}		11.5	12.0	12.5	V
IS test pin voltage	V_{IS}	V_{IS} =V_{DD}	11.5	12.0	12.5	V
Output gate voltage	V_{OG}	V_{DD}=12V, △V_{DD} component is added to V_{OG}.	4.2	4.5	4.8	V
Photostorage gate voltage	V_{PG}	V_{PG}=V_{OG}	4.2	4.5	4.8	V
TG test pin voltage	V_{TG}	V_{TG}=V_{SS}	—	0	—	V
CCD shift register clock High level	$V_{øH}$		8.0	9.0	10.0	V
CCD shift register clock Low level	$V_{øL}$		0	0.5	0.8	V
Reset gate clock High level	V_{RH}		9.0	10.0	12.0	V
Reset gate clock Low level	V_{RL}		0	0.5	0.8	V
Shift gate clock High level	V_{SH}		9.0	10.0	12.0	V
Shift gate clock Low level	V_{SL}		0	0.5	0.8	V

• Timing conditions (Ta=–20 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	f_C=f_R=1/2T	0.1	—	7.0	MHz
Reset clock frequency	f_R		0.1	—	7.0	MHz
Shift clock rise time	t_{Sr}	See timing diagrams (1) to (3).	0	15	50	ns
Shift clock fall time	t_{Sf}		0	15	50	ns
Shift clock set up time	t_{Ss}		250	400	1000	ns
Shift clock pulse width	t_{SW}		1.0	1.8	10	µs
Shift clock hold time	t_{Sh}		0	—	1	µs
Shift register clock rise time	t_{Cr}		0	20	50	ns
Shift register clock fall time	t_{Cf}		0	20	50	ns
Reset clock rise time	t_{Rr}		0	10	20	ns
Reset clock fall time	t_{Rf}		0	10	20	ns
Reset clock pulse width	t_{RW}		20	30	—	ns
Reset clock set up time	t_{Rs}		0.7T	—	—	ns
Reset clock hold time	t_{Rh}		5	10	—	ns

■ Electrical Characteristics

• Clock input capacitance (Ta=–20 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance*	C_{1A}, C_{2A} C_{1B}, C_{2B}	V_{IN}=12V, f=1MHz	—	600	—	pF
Reset clock input capacitance	C_R		—	10	—	pF
Shift clock input capacitance	C_S		—	150	—	pF

*$ø_{1A}$, $ø_{2A}$, $ø_{1B}$, and $ø_{2B}$ are respectively connected to $ø_{1D}$, $ø_{2D}$, $ø_{1C}$, and $ø_{2C}$ internally.

• DC characteristics (Ta=–20 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I_{DD}	V_{IN}=+12V	—	20	50	mA
IS test pin leak current	I_{IS}		—	—	1	mA
Photo storage gate leak current	I_{PG}	V_{IN}=+5V	—	—	50	µA
Output gate pin leak current	I_{OG}		—	—	50	µA

• AC characteristics (Ta=–20 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output set up time	t_{OS}	OS output level=240mV	—	30	—	ns
Signal output hold time	t_{Oh}		—	30	—	ns

■ Optical Characteristics

(Standard operatiing condition, f_R=4MHz, $T_{int.}$=1ms,
Light source: G-54, Green-light fluorescent lamp (peak wavelength=543nm))

Parameter	Symbol	Condition	min	typ	max	Unit
Saturation output voltage	V_{SAT}	STTE≥90%	240	800	—	mV
Saturation exposure	SE		0.4	—	—	lx·s
Minimum saturation exposure output voltage	$V_{SEmin.}$	exposure: 0.4 lx· s	240	—	380	mV
Photoresponse non-uniformity	PRNU	exposure: 0.4 lx· s	—	—	20	%
Bit non-uniformity	BNU	exposure: 0.4 lx· s	—	—	±10	%
Dark signal output voltage	V_d	Dark condition	—	0.4	1.0	mV
Shift register total transfer efficiency	STTE		90	99	—	%
Photodetector response	PPR		—	0.5	3.0	%
Modulation transfer function	MTFR	Nyquist spatial frequency	—	60	—	%
OS-DS DC level difference	△DC	Dark condition	—	—	300	mV
Depth of photodetector	PSU*		—	±20	—	µm
Photodetector linearity	PSL*		—	±10	—	µm

* When there are any problems regarding these parameters, they can be specified again in consultation with the customer.

Note 1) The optical characteristics apply to the 5000 pixels excluding the 4 dummy pixels.

Note 2) Inspection conditions: Using an ND filter (transmissivity of 35%) and a slit of dimensions 40 × 40mm. Distance between sensor and slit is 200mm and the search angle is ±8°.

■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS_1	Signal output	
2	DS_1	Compensation output	
3	OG	Output gate	
4	$ø_{R1}$	Reset clock	
5	$ø_{2D}$	CCD shift register clock	
6	$ø_{1D}$	CCD shift register clock	
7	NC	Non connection	
8	$ø_{1A}$	CCD shift register clock	Internally connected to $ø_{1D}$.
9	$ø_{2A}$	CCD shift register clock	Internally connected to $ø_{2D}$.
10	TG	Test pin	Connect externally to Ground.
11	PG	Photo storage gate	
12	$ø_{SG}$	Shift gate clock	
13	IS	Test pin	Connect externally to V_{DD}.
14	$ø_{2B}$	CCD shift register clock	Internally connected to $ø_{2C}$.
15	$ø_{1B}$	CCD shift register clock	Internally connected to $ø_{1C}$.
16	V_{SS}	Ground	Internally connected to the substrate.
17	$ø_{1C}$	CCD shift register clock	
18	$ø_{2C}$	CCD shift register clock	
19	$ø_{R2}$	Reeset clock	
20	V_{DD}	Power supply	
21	DS_2	Compensation output	
22	OS_2	Signal output	

Note) Connect the NC pin externally to Ground.

■ Construction of the Image Sensor

The MN3664 can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of a 5µm floating photodiode and a 2µm channel stopper for each pixel, and 5000 of these devices are linearly arranged side by side at a pitch of 7µm.
- The photo detector's windows are 7µm × 7µm squares and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 64 optically shielded pixels which serve as the black reference.

b) CCD Transfer region (shift register)

- The optical output after photoelectric conversion is transferred respectively to the odd and even CCD transfer region at the timing of the shift gate electrode ($ø_{SG}$), the photoelectric converted output transferred to this analog shift register is transferred successively to the output region.
- A buried type CCD that can be driven by a 2-phase clock is used as the analog shift register.

c) Output region

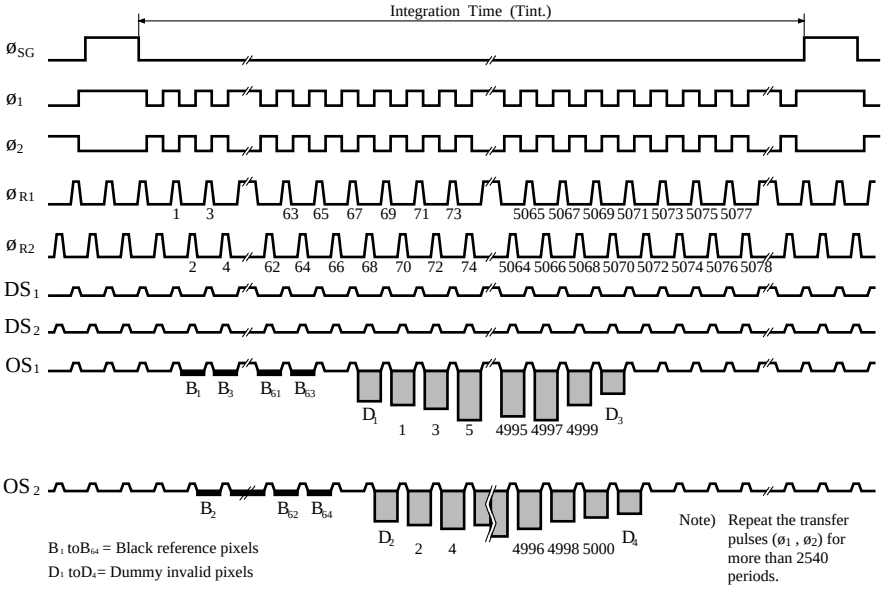
- The signal transferred to this region is sent to the detector region and is amplified by a two stage source follower amplifier.

Evaluation board

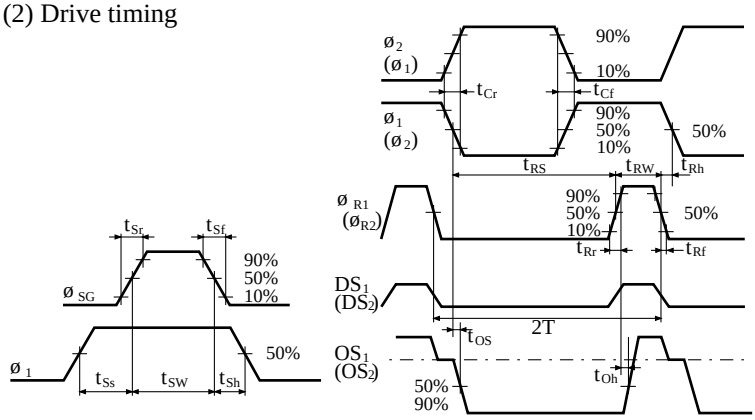
The placement of the each component is very important in order to get a good output signal. The evaluation board BS803 is available for evaluating the MN3664.

■ Timing Diagram

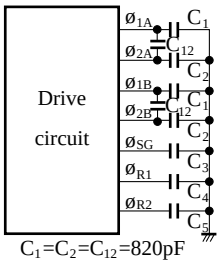
(1) I/O timing



(2) Drive timing



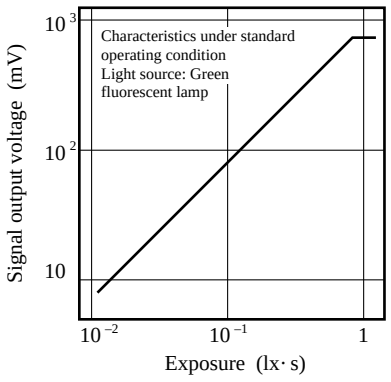
(3) Timing condition measuring circuit



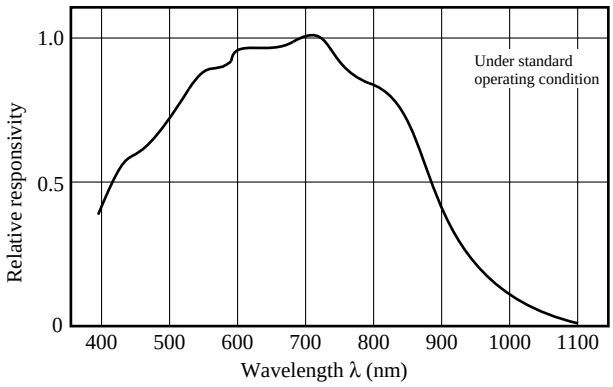
C1=C2=C12=820pF
C3=150pF
C4=C5=10pF

■ Graphs and Characteristics

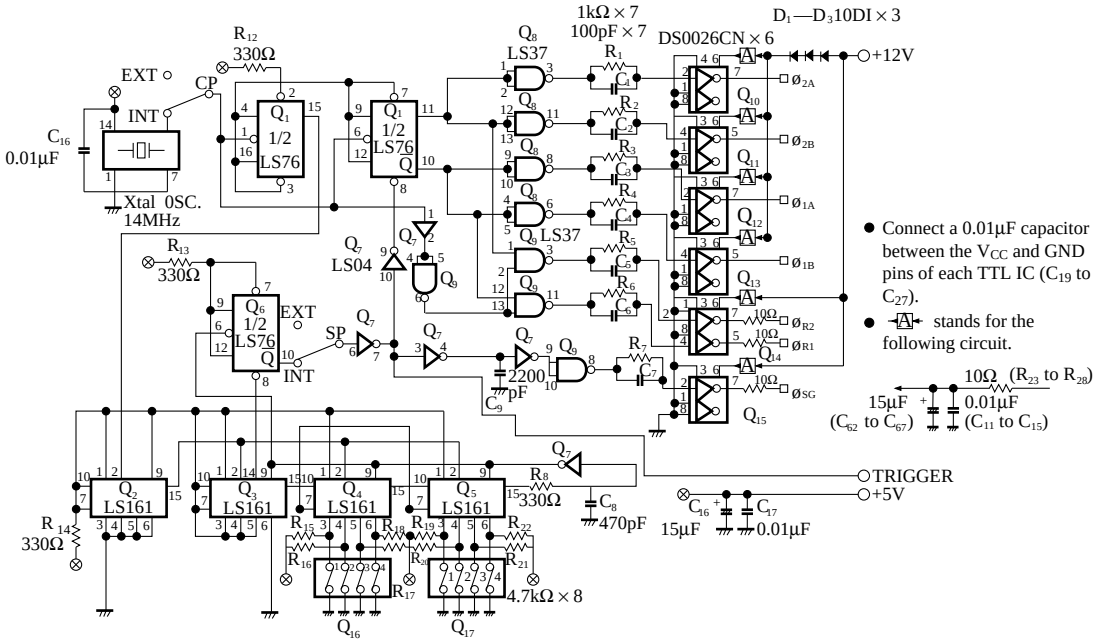
Photoelectric Conversion Characteristics



Spectral Response Characteristics



■ Drive Circuit Diagram (Digital Section)



■ Drive Circuit Diagram (Analog Section)