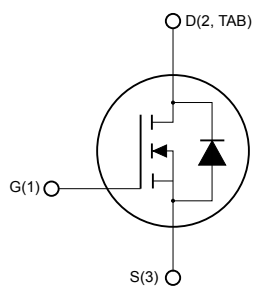
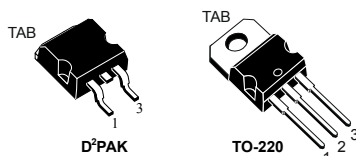


Automotive N-channel 55 V, 6.5 mΩ typ., 80 A STripFET II Power MOSFETs in D²PAK and TO-220 packages



NG1D2TS3



Features

Order codes	V _{DSS}	R _{DS(on)}	I _D
STB141NF55	55 V	< 8 mΩ	80 A
STP141NF55			

- AEC-Q101 qualified
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge



Applications

- Switching applications

Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status links

[STB141NF55](#)

[STP141NF55](#)

Product summary

Order code	STB141NF55
Marking	B141NF55
Package	D ² PAK
Packing	Tape and reel
Order code	STP141NF55
Marking	P141NF55
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	55	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	80	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2	W/°C
$dv/dt^{(3)}$	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.3	J
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Operating junction temperature range		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 80\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$
4. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 40\text{ A}$, $V_{DD} = 30\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO -220	D ² PAK	
$R_{thj-case}$	Thermal resistance junction-case max	0.5		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	-	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	-	35	°C/W
T_l	Maximum lead temperature for soldering purpose (for 10 sec, 1.6 mm from case)	300		°C

1. When mounted on 1 inch², FR4 board, 2 oz Cu

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	55			V
I_{DSS}	Zero gate voltage drain ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$			1	μA
		$V_{DS} = \text{Max rating}$, $T_C = 125\text{ }^{\circ}\text{C}$			10	
I_{GSS}	Gate-body leakage ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$		6.5	8	m Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 40\text{ A}$	-	100	-	S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$ $V_{GS} = 0$	-	5300	-	pF
C_{oss}	Output capacitance		-	1000	-	
C_{rss}	Reverse transfer capacitance		-	290	-	
Q_g	Total gate charge	$V_{DD} = 44\text{ V}$, $I_D = 80\text{ A}$	-	142	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$	-	27	-	
Q_{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	55	-	

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5 %

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 27.5\text{ V}$, $I_D = 40\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	30	-	ns
t_r	Rise time		-	150	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times)	-	125	-	ns
t_f	Fall time		-	45	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	90		ns
Q_{rr}	Reverse recovery charge		-	275		nC
I_{RRM}	Reverse recovery current		-	6.5		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

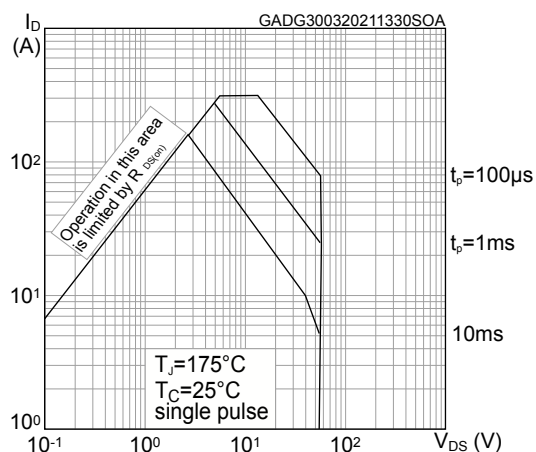
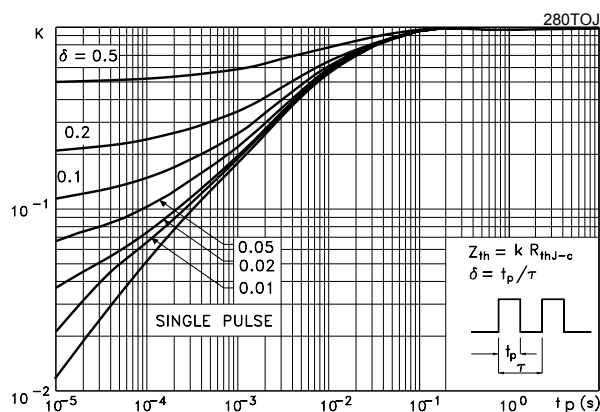
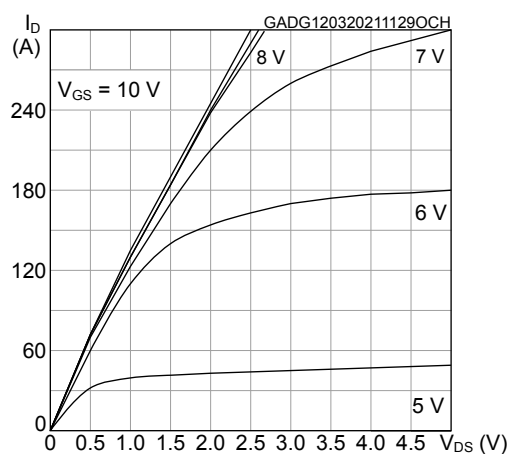
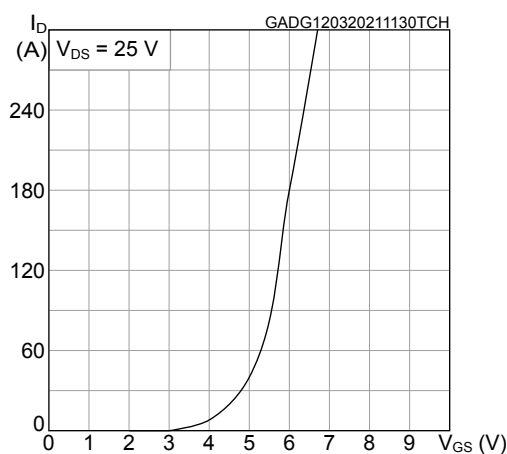
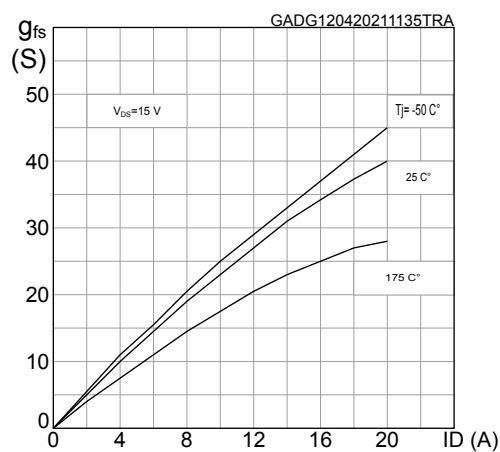
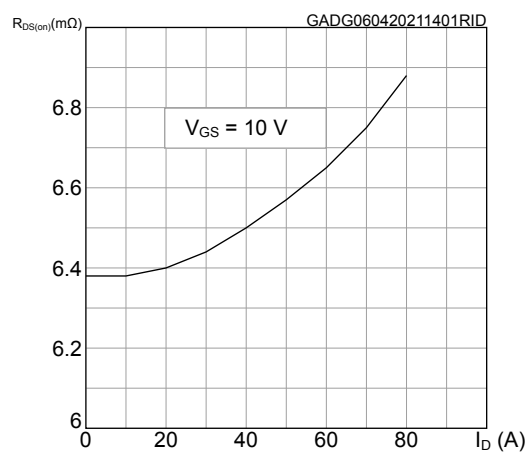
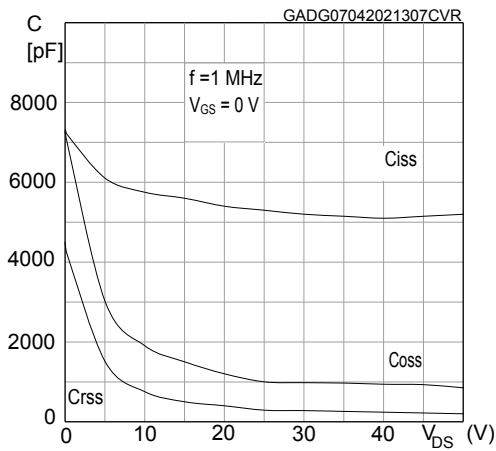
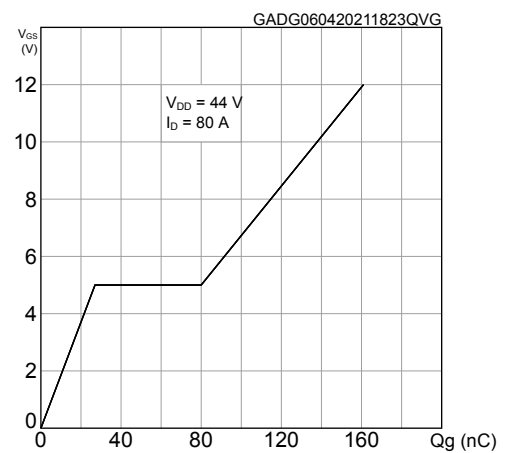
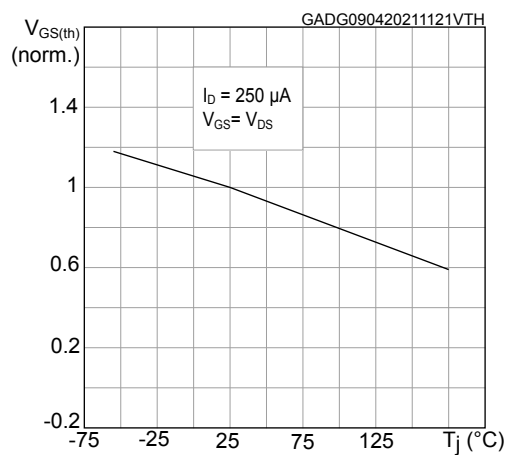
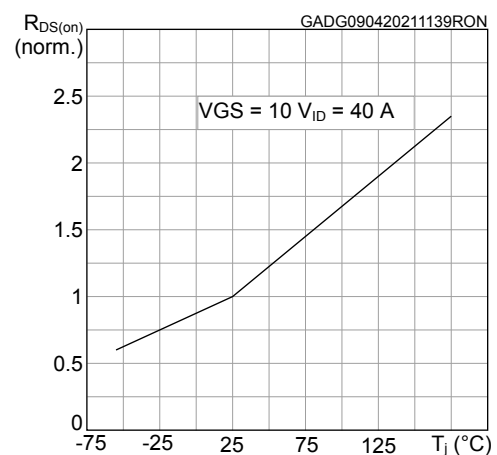
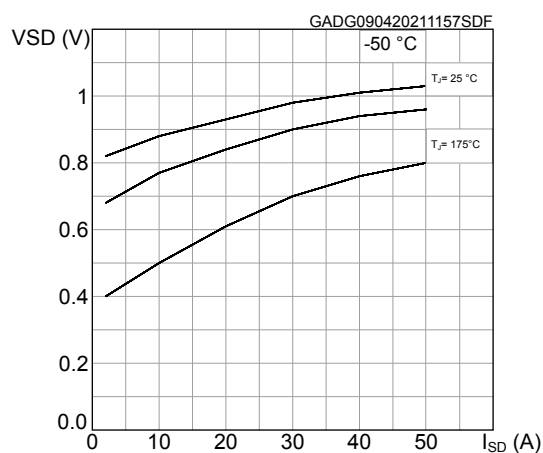
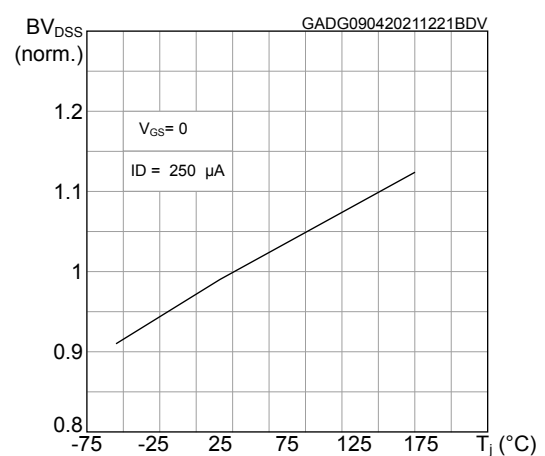
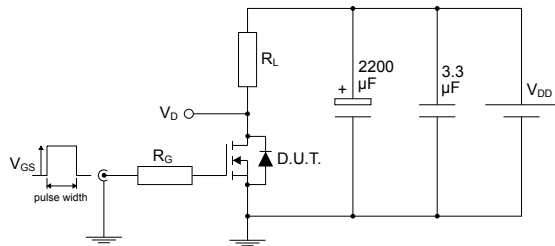
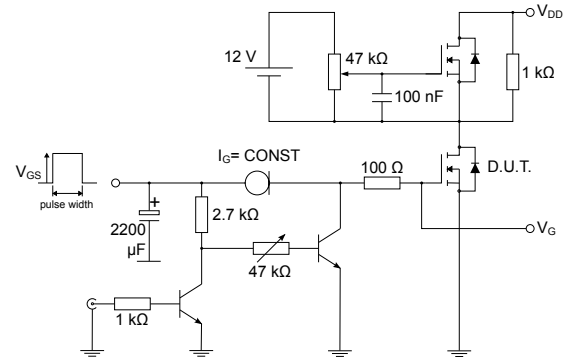
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Transconductance

Figure 6. Static drain-source on resistance


Figure 7. Capacitance variations

Figure 8. Gate charge vs gate-source voltage

Figure 9. Normalized breakdown voltage vs temperature

Figure 10. Normalized on resistance vs temperature

Figure 11. Source-drain diode forward characteristics

Figure 12. Normalized BV_{DSS} vs temperature


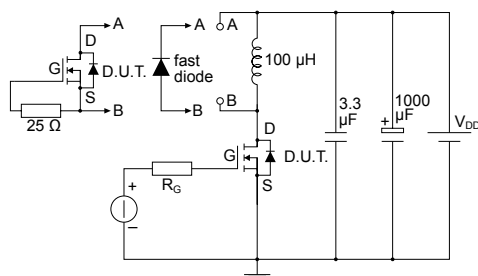
3 Test circuits

Figure 13. Test circuit for resistive load switching times


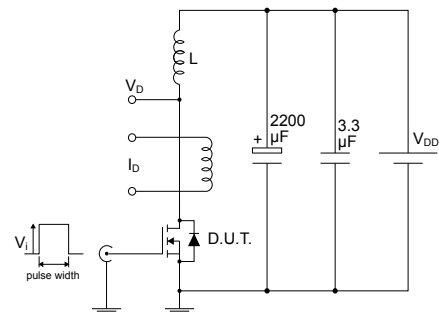
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Figure 14. Test circuit for gate charge behavior


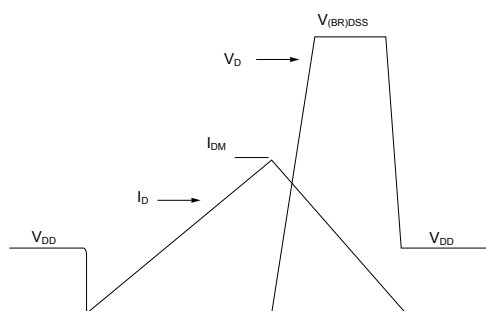
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Figure 15. Test circuit for inductive load switching and diode recovery times


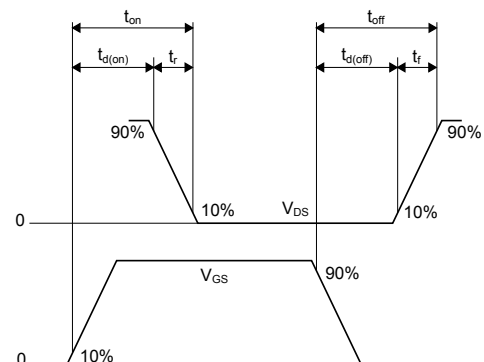
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Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


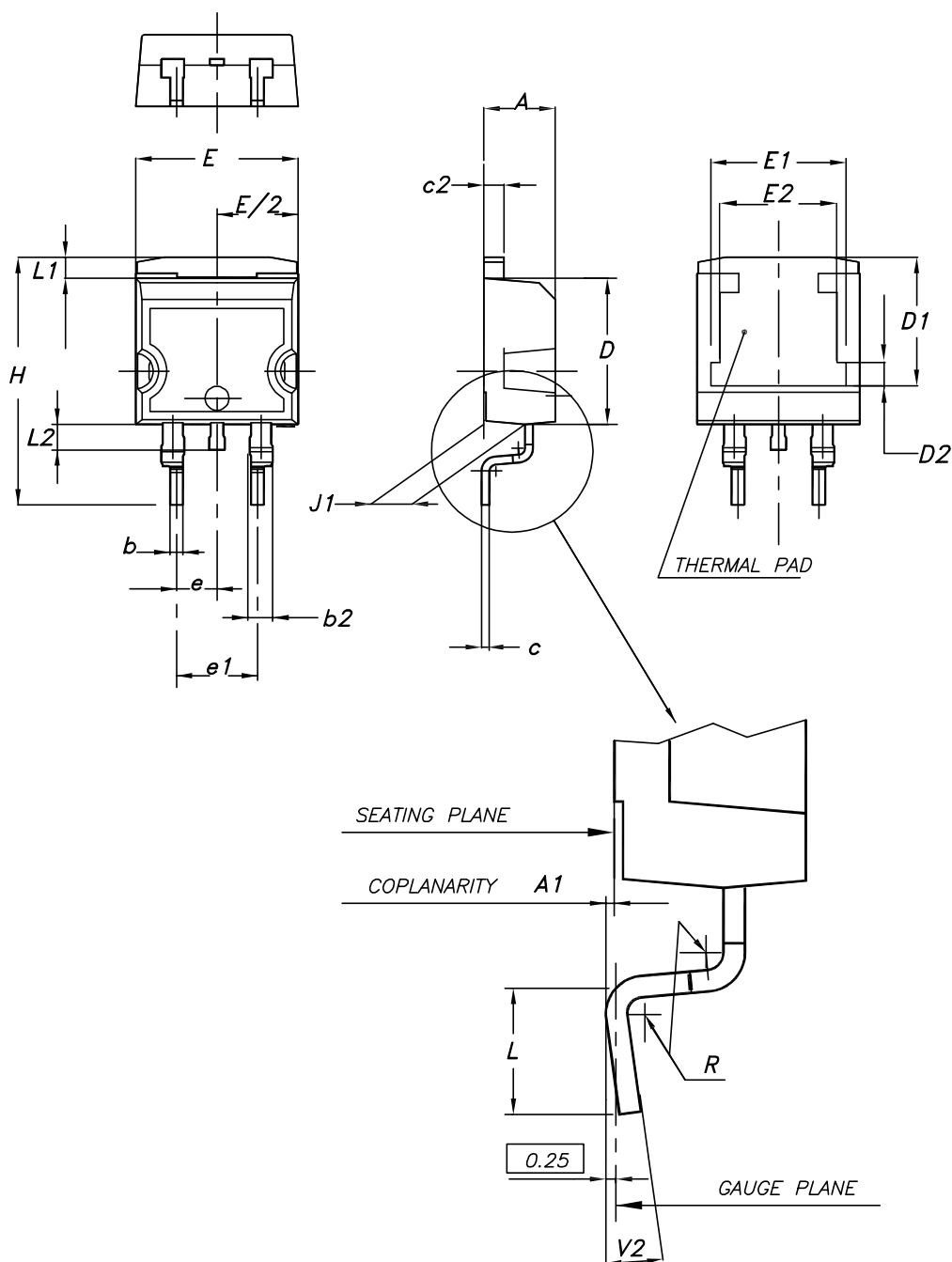
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 19. D²PAK (TO-263) type A package outline

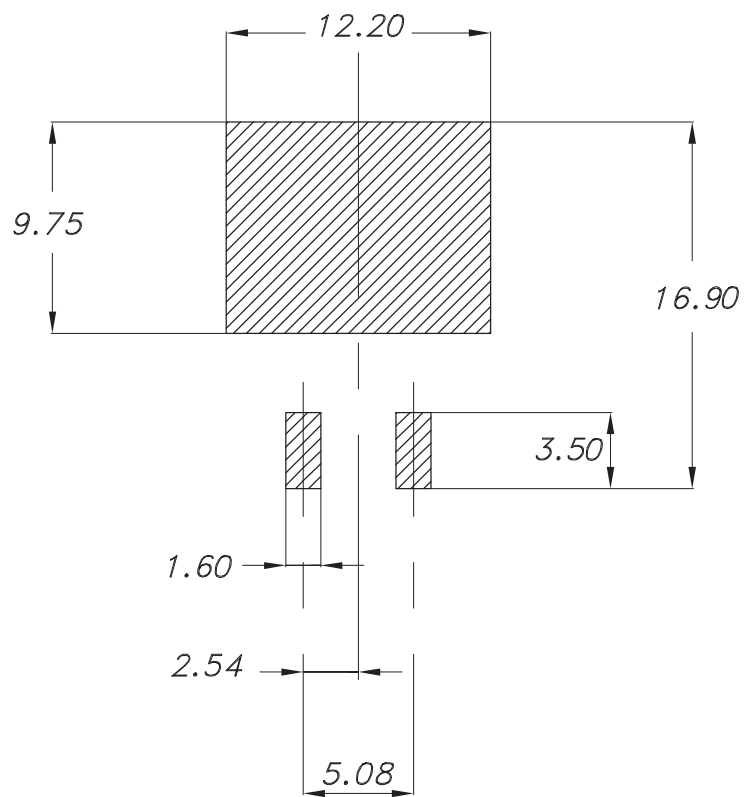


0079457_26

Table 7. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

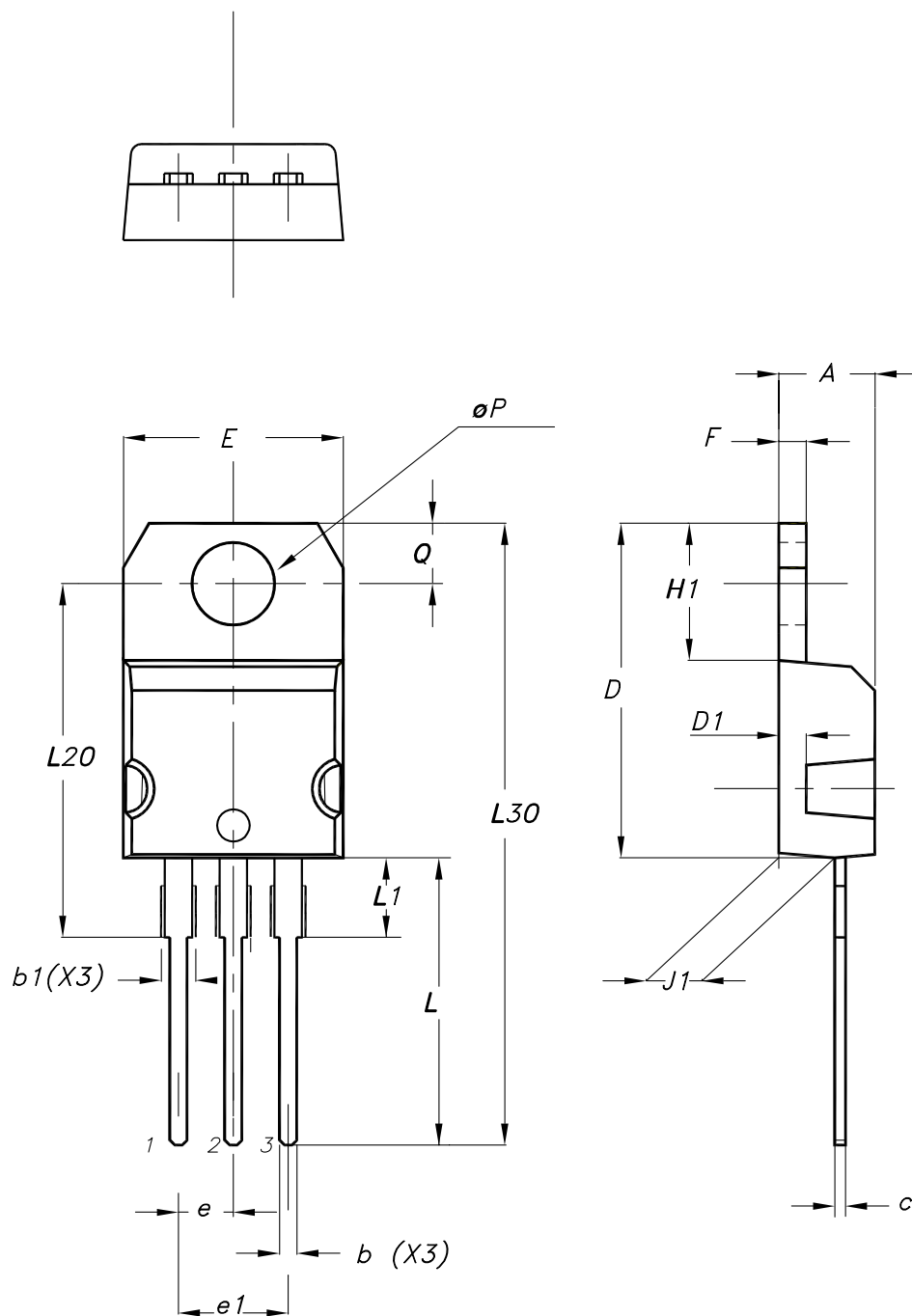
Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev26_footprint

4.2 TO-220 type A package information

Figure 21. TO-220 type A package outline



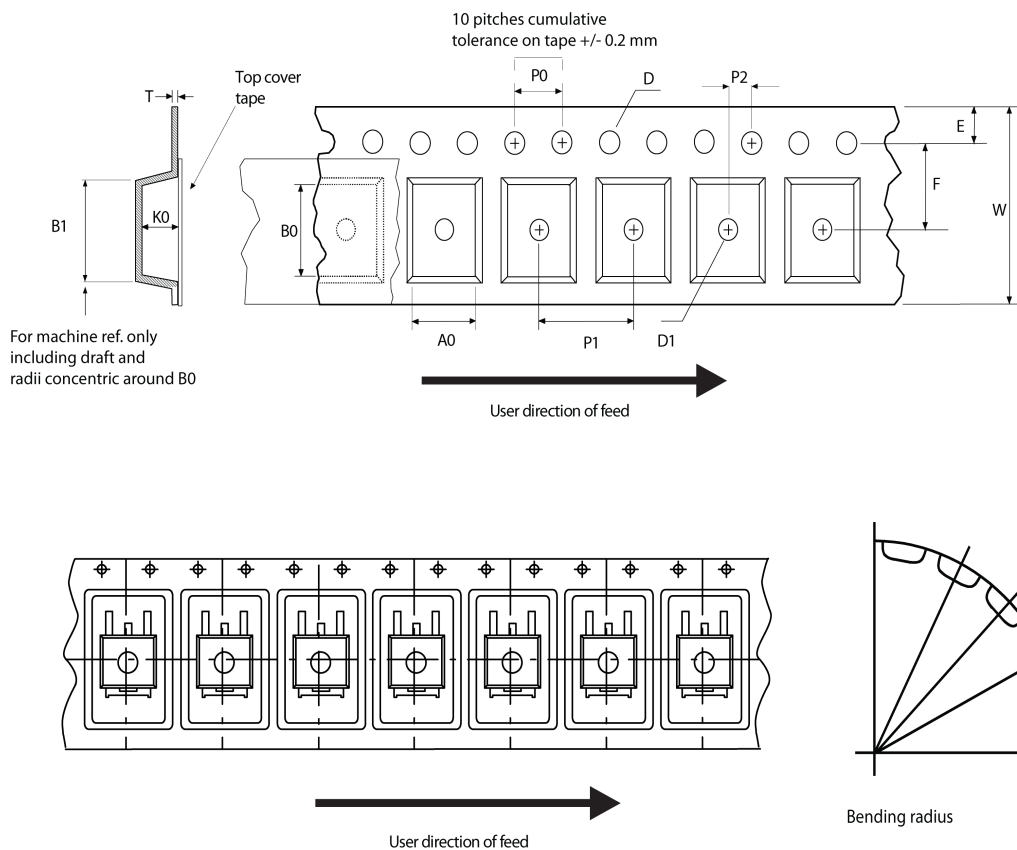
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Table 8. TO-220 type A package mechanical data

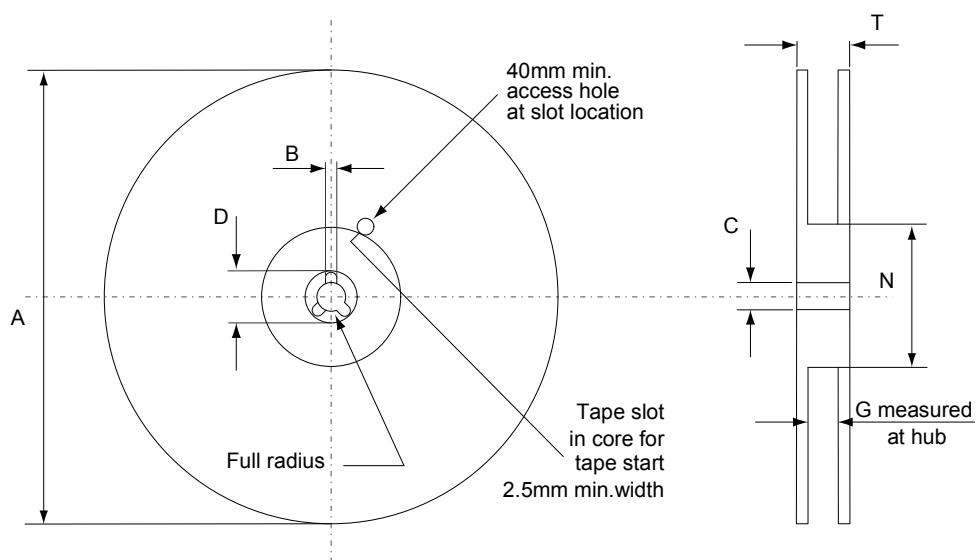
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.3 D²PAK packing information

Figure 22. D²PAK tape outline



AM08852v1

Figure 23. D²PAK reel outline


AM06038v1

Table 9. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 10. Document revision history

Date	Version	Changes
01-Aug-2007	1	First release.
03-Jan-2022	2	The part number in IPAK package has been removed.

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