

# 74LV244

## Octal buffer/line driver (3-state)

Rev. 3 — 11 March 2014

Product data sheet

### 1. General description

The 74LV244 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC244 and 74HCT244.

The 74LV244 is an octal non-inverting buffer/line driver with 3-state outputs. The output enable inputs  $1\overline{OE}$  and  $2\overline{OE}$  control the 3-state outputs. A HIGH on  $n\overline{OE}$  causes the outputs to assume a high impedance OFF-state. The 74LV244 is identical to the 74LV240 but has non-inverting outputs.

### 2. Features and benefits

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce) < 0.8 V at  $V_{CC} = 3.3$  V;  $T_{amb} = 25$  °C
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot) > 2 V at  $V_{CC} = 3.3$  V;  $T_{amb} = 25$  °C
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V

### 3. Ordering information

Table 1. Ordering information

Type number	Package		Description	Version
	Temperature range	Name		
74LV244N	−40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74LV244D	−40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LV244DB	−40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LV244PW	−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1



#### 4. Block diagram

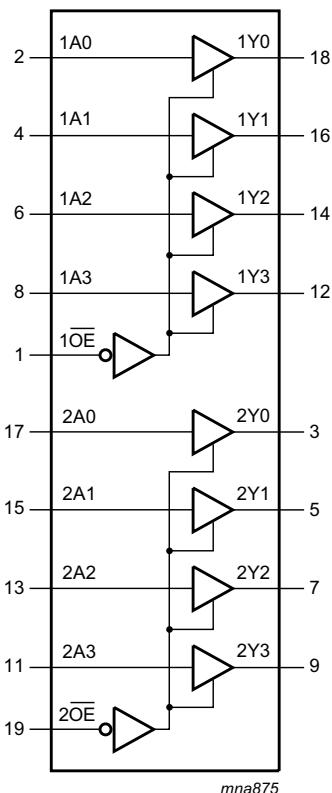


Fig 1. Functional diagram

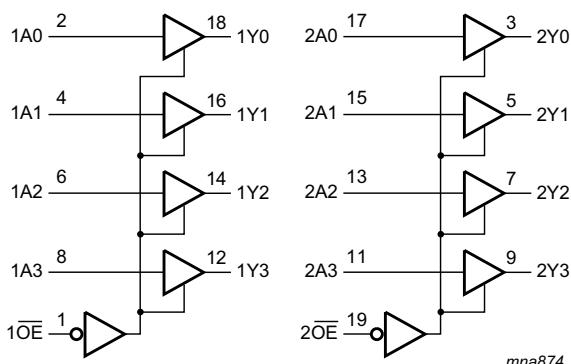


Fig 2. Logic symbol

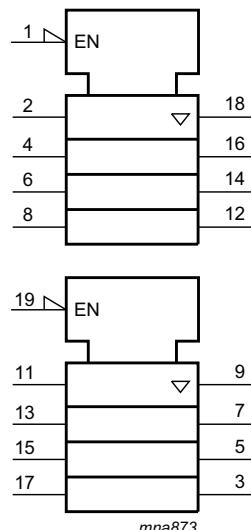


Fig 3. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning

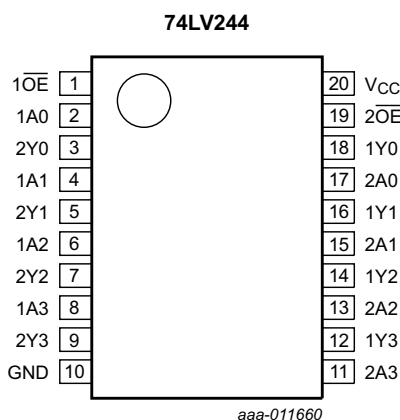


Fig 4. Pin configuration DIP20, SO20, SSOP20 and TSSOP20

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	bus output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	bus output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input		Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	-	±50	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±35	mA
I <sub>CC</sub>	supply current		-	70	mA
I <sub>GND</sub>	ground current		-70	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
		DIP20 package	[1]	-	750 mW
		SO20	[2]	-	500 mW
		SSOP20 and TSSOP20	[3]	-	400 mW

[1] For DIP20 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

[2] For SO20 packages: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

[3] For SSOP20 and TSSOP20 packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V <sub>CC</sub>	supply voltage		[1]	1.0	3.3	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V	
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V	
T <sub>amb</sub>	ambient temperature		-40	-	+85	°C	
			-40	-	+125	°C	
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.0 V to 2.0 V	0	-	500	ns/V	
		V <sub>CC</sub> = 2.0 V to 2.7 V	0	-	200	ns/V	
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	100	ns/V	
		V <sub>CC</sub> = 3.6 V to 5.5 V	0	-	50	ns/V	

[1] The LV is guaranteed to function down to V<sub>CC</sub> = 1.0 V (input levels GND or V<sub>CC</sub>). DC characteristics are guaranteed from V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 5.5 V.

## 9. Static characteristics

**Table 6. Static characteristics**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9		V
		V <sub>CC</sub> = 2.0 V	1.4	-	-	1.4		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0		V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	0.7V <sub>CC</sub>		V
V <sub>IL</sub>	LOW level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3		0.3	V
		V <sub>CC</sub> = 2.0 V	-	-	0.6		0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>		0.3V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100 µA						
		V <sub>CC</sub> = 1.2 V	-	1.2	-	-	-	V
		V <sub>CC</sub> = 2.0 V	1.8	2.0	-	1.8	-	V
		V <sub>CC</sub> = 2.7 V	2.5	2.7	-	2.5	-	V
		V <sub>CC</sub> = 3.0 V	2.8	3.0	-	2.8	-	V
		V <sub>CC</sub> = 4.5 V	4.3	4.5	-	4.3	-	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		V <sub>CC</sub> = 3.0 V; I <sub>O</sub> = -8 mA	2.40	2.82	-	2.20	-	V
		V <sub>CC</sub> = 4.5 V; I <sub>O</sub> = -16 mA	3.60	4.20	-	3.50	-	V
V <sub>OL</sub>	LOW level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 µA						
		V <sub>CC</sub> = 1.2 V	-	0	-	-	-	V
		V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V
		V <sub>CC</sub> = 2.7 V	-	0	0.2	-	0.2	V
		V <sub>CC</sub> = 3.0 V	-	0	0.2	-	0.2	V
		V <sub>CC</sub> = 4.5 V	-	0	0.2	-	0.2	V
		V <sub>CC</sub> = 3.0 V; I <sub>O</sub> = 8 mA	-	0.25	0.40	-	0.50	V
		V <sub>CC</sub> = 4.5 V; I <sub>O</sub> = 16 mA	-	0.35	0.55	-	0.65	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	-	1.0	-	1.0	µA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	5	-	10	µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	-	20	-	160	µA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V	-	-	500	-	850	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND (ground = 0 V); for test circuit, see [Figure 7](#)

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	1An to 1Yn; 2An to 2Yn; see <a href="#">Figure 5</a>	[2]					
		V <sub>CC</sub> = 1.2 V	-	50		-	-	ns
		V <sub>CC</sub> = 2.0 V	-	17	24	-	31	ns
		V <sub>CC</sub> = 2.7 V	-	13	17	-	23	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	9	14	-	18	ns
		V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF	-	8.0	-	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	12	-	15	ns
t <sub>en</sub>	enable time	1 $\overline{OE}$ to 1Yn; 2 $\overline{OE}$ to 2Yn; see <a href="#">Figure 6</a>	[2]					
		V <sub>CC</sub> = 1.2 V	-	65	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	22	39	-	49	ns
		V <sub>CC</sub> = 2.7 V	-	16	29	-	36	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	12	23	-	29	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	19	-	24	ns
t <sub>dis</sub>	disable time	1 $\overline{OE}$ to 1Yn; 2 $\overline{OE}$ to 2Yn; see <a href="#">Figure 6</a>	[2]					
		V <sub>CC</sub> = 1.2 V	-	60		-	-	ns
		V <sub>CC</sub> = 2.0 V	-	22	34	-	43	ns
		V <sub>CC</sub> = 2.7 V	-	17	24	-	32	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	13	21	-	26	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	16	-	19	ns
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V	[3]	-	35	-	-	ns

[1] Unless otherwise stated, all typical values are measured at T<sub>amb</sub> = 25 °C and nominal V<sub>CC</sub>.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> + Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) (P<sub>D</sub> in  $\mu$ W), where:

f<sub>i</sub> = input frequency in MHz;

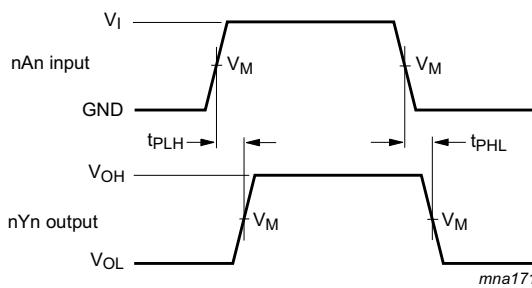
f<sub>o</sub> = output frequency in MHz;

Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V.

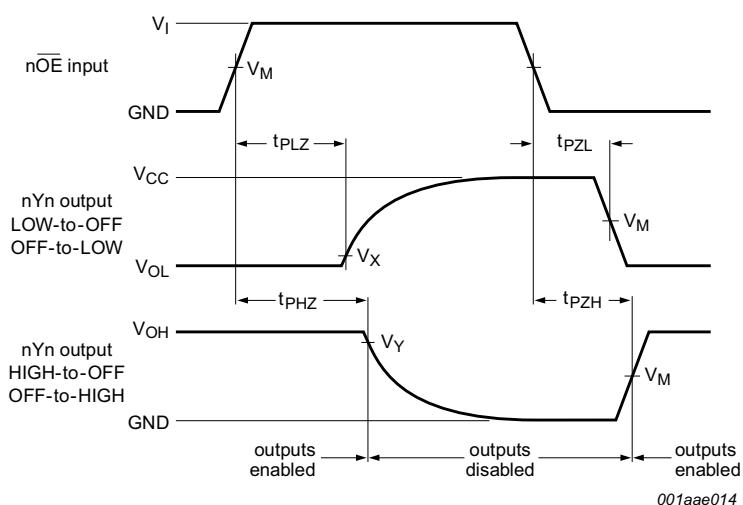
## 11. Waveforms



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 5. Input (nAn) to output (nYn) propagation delays**



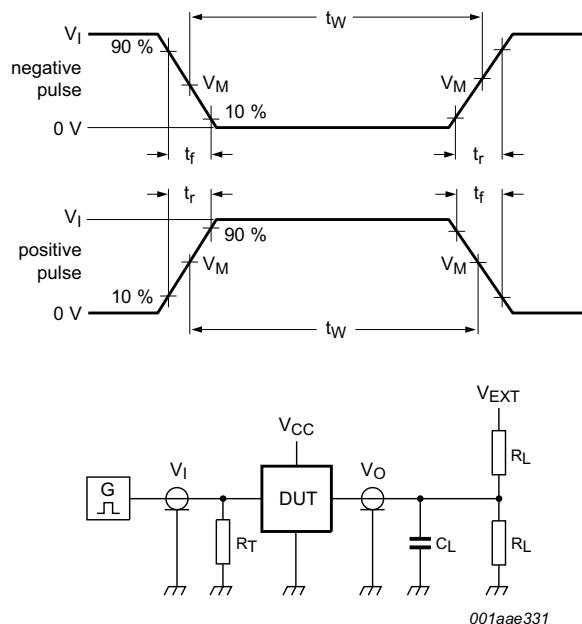
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. 3-state enable and disable times**

**Table 8. Measurement points**

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
< 2.7 V	0.5 $V_{CC}$	0.5 $V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
$\geq 4.5 V$	0.5 $V_{CC}$	0.5 $V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

$S1$  = Test selection switch.

**Fig 7. Test circuit for measuring switching times**

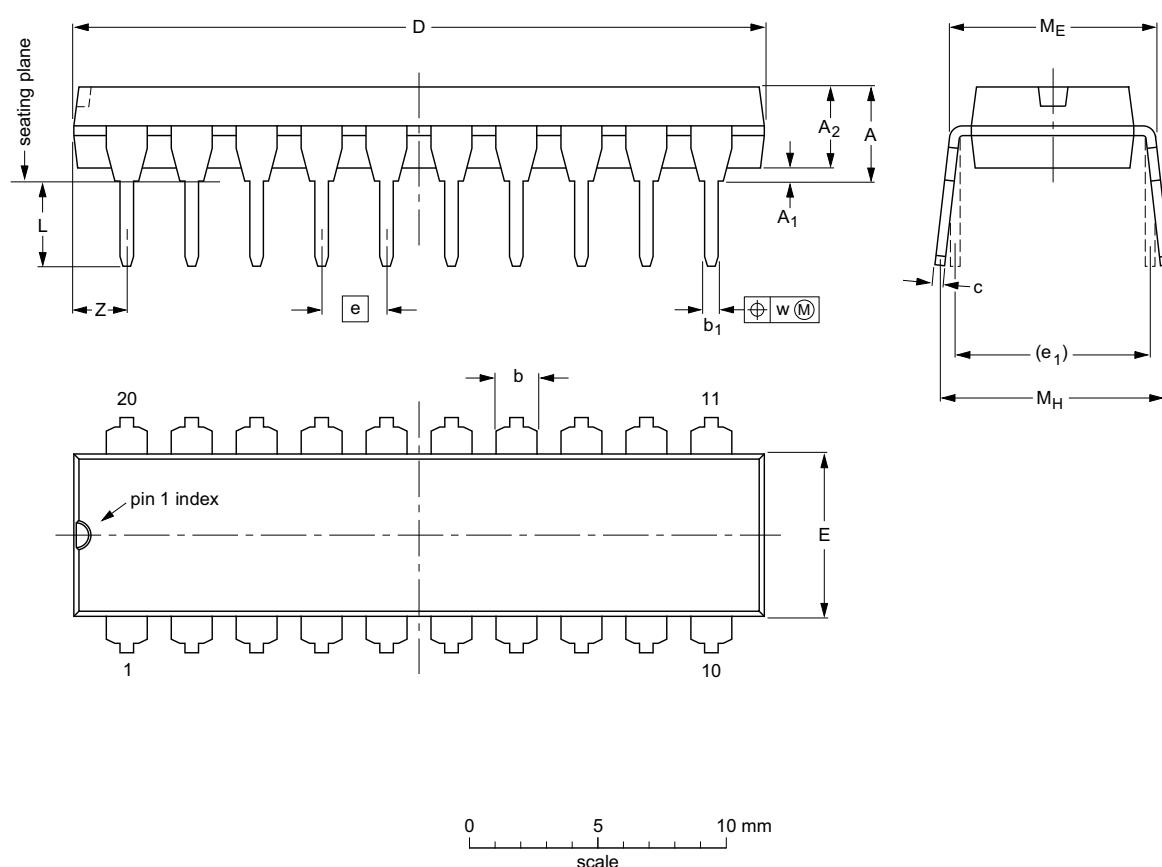
**Table 9. Test data**

Supply voltage	Input	Load		$V_{EXT}$				
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$	
< 2.7 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open	GND	$2V_{CC}$	
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$2V_{CC}$	
$\geq 4.5$ V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open	GND	$2V_{CC}$	

## 12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

### Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			99-12-27 03-02-13

Fig 8. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

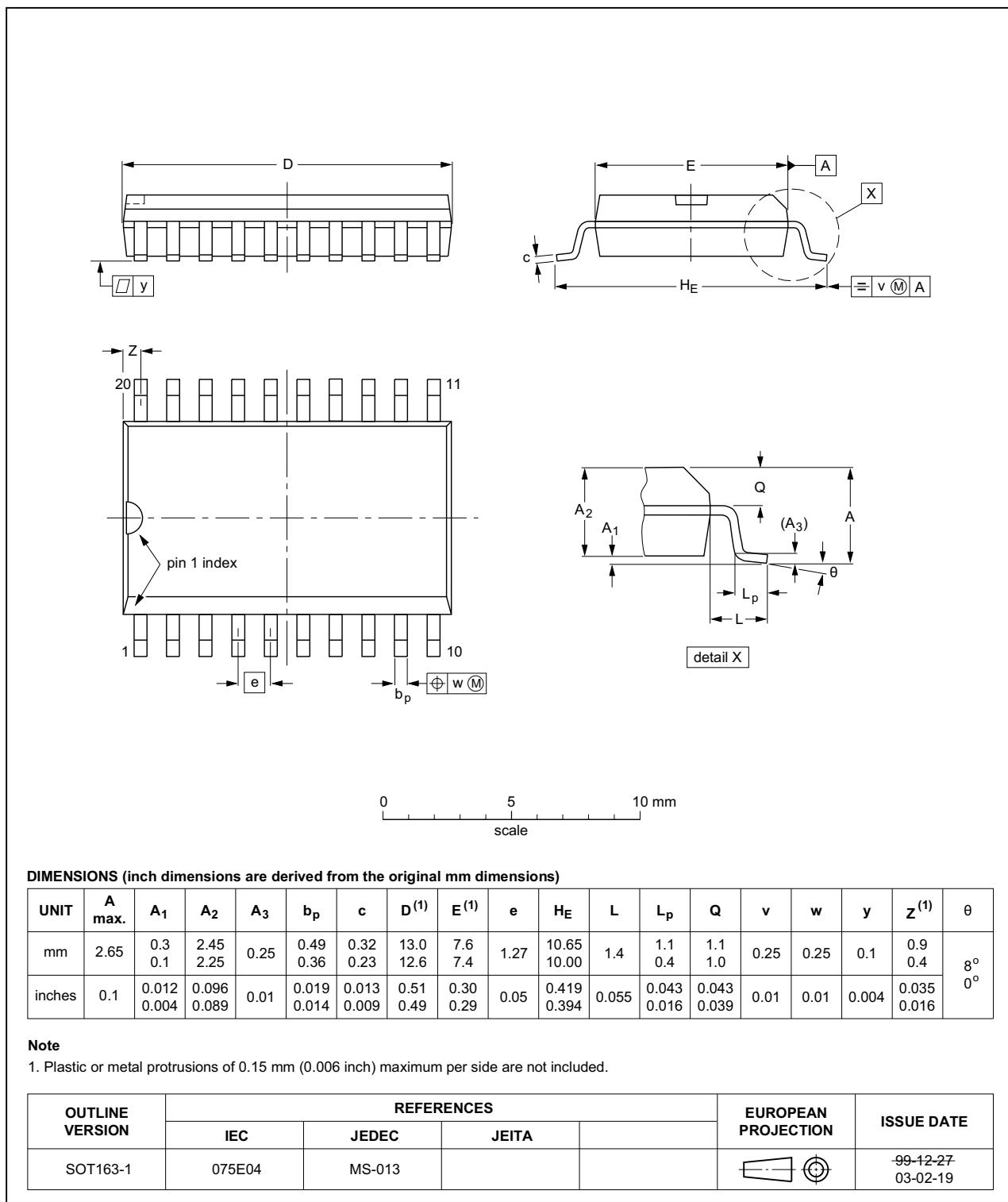


Fig 9. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

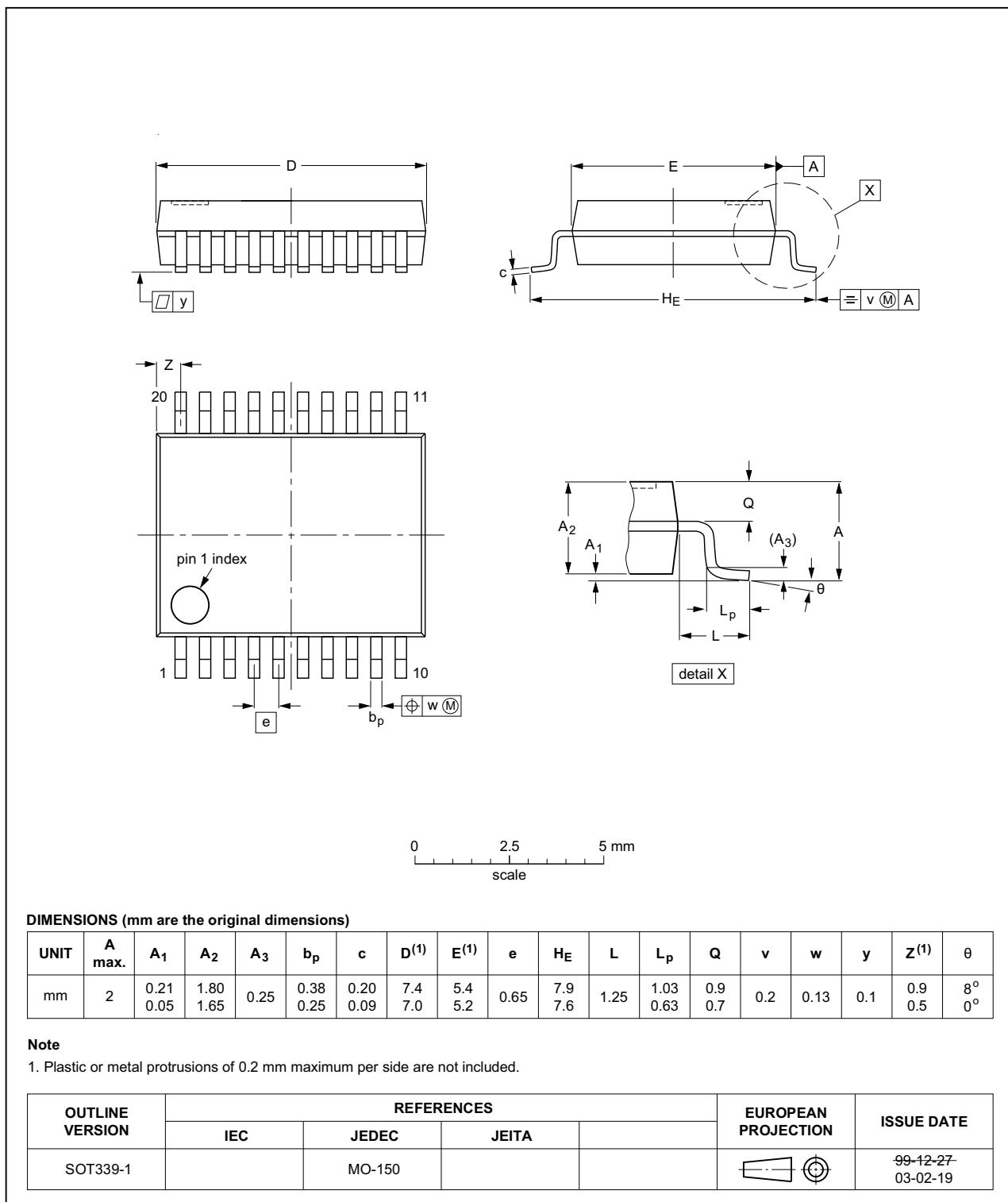


Fig 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

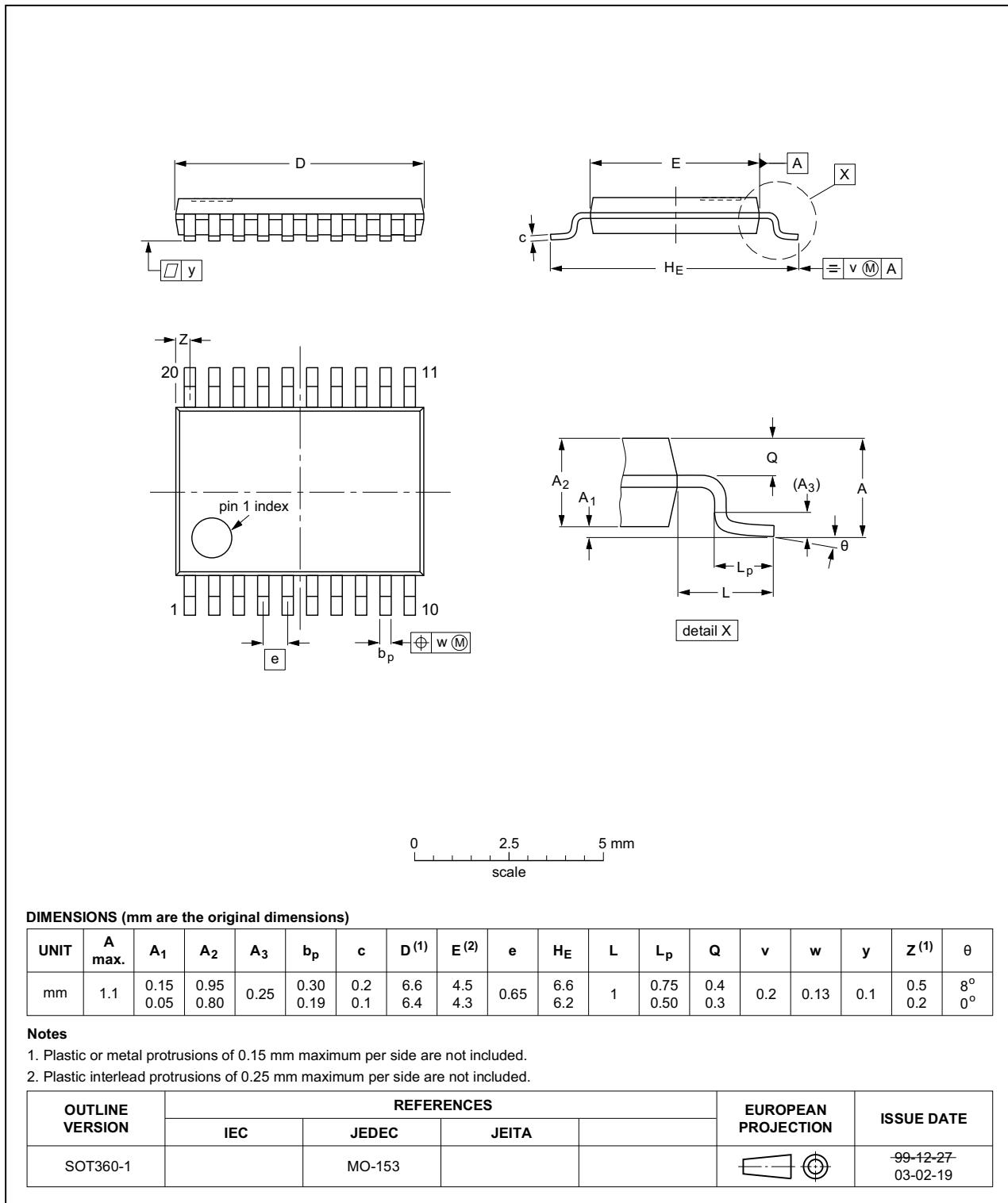


Fig 11. Package outline SOT360-1 (TSSOP20)

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV244 v.3	20140311	Product data sheet	-	74LV244 v.2
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul>			
74LV244 v.2	19980520	Product specification	-	74LV244 v.1
74LV244 v.1	-	-	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 17. Contents

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<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>1</b>
<b>4</b>	<b>Block diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>3</b>
5.1	Pinning .....	3
5.2	Pin description .....	3
<b>6</b>	<b>Functional description</b> .....	<b>3</b>
<b>7</b>	<b>Limiting values</b> .....	<b>4</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>4</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>5</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>6</b>
<b>11</b>	<b>Waveforms</b> .....	<b>7</b>
<b>12</b>	<b>Package outline</b> .....	<b>9</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>13</b>
<b>14</b>	<b>Revision history</b> .....	<b>13</b>
<b>15</b>	<b>Legal information</b> .....	<b>14</b>
15.1	Data sheet status .....	14
15.2	Definitions.....	14
15.3	Disclaimers.....	14
15.4	Trademarks.....	15
<b>16</b>	<b>Contact information</b> .....	<b>15</b>
<b>17</b>	<b>Contents</b> .....	<b>16</b>

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