



STD20NF06L STD20NF06L-1

N-channel 60V - 0.032Ω - 24A - DPAK - IPAK
STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STD20NF06L	60V	<0.040Ω	24A
STD20NF06L-1	60V	<0.040Ω	24A

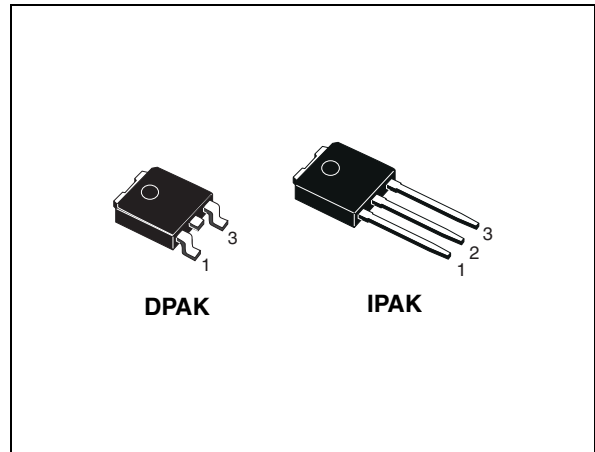
- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

Description

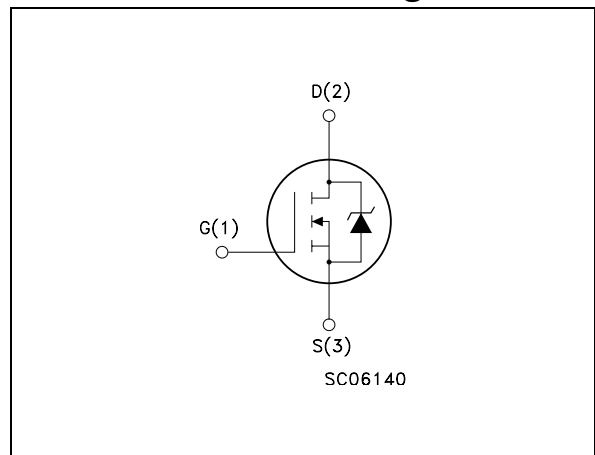
This Power MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” stripbased process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD20NF06L	D20NF06L	DPAK	Tape & reel
STD20NF06L-1	D20NF06L-1	IPAK	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V_{GS}	Gate-source voltage	± 18	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	24	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	17	A
$I_{DM}^{(1)}$	Drain current (pulsed)	96	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
	Derating factor	0.4	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	225	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 24\text{A}$, $di/dt \leq 300\text{A/ns}$, $V_{DD} = 80\% V_{(BR)DSS}$
3. Starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 60\text{V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	2.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb Max	50	$^\circ\text{C/W}$
T_l	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

1. When mounted on 1 inch² FR-4 board, 2 oz of Cu

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250μA, V _{GS} = 0	60			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating, V _{DS} = Max rating, T _c = 125°C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±18V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250μA	1		2.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 12A V _{GS} = 5V, I _D = 12A		0.032	0.040 0.050	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 25V, I _D = 12A		20		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1MHz, V _{GS} = 0		660 170 70		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 30V, I _D = 20A V _{GS} = 10V (see Figure 12)		13 3.5 8		nC nC nC

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=30V$, $I_D=10A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 13)		11		ns
t_r	Rise time			50		ns
$t_{d(off)}$	Turn-off delay time			20		ns
t_f	Fall time			12		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				24	A
I_{SDM}	Source-drain current (pulsed)				96	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD}=20A$, $V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=20A$, $di/dt = 100A/\mu s$, $V_{DD}=20V$, $T_j=150^\circ C$ (see Figure 16)		56		ns
Q_{rr}	Reverse recovery charge			108		nC
I_{RRM}	Reverse recovery current			4		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

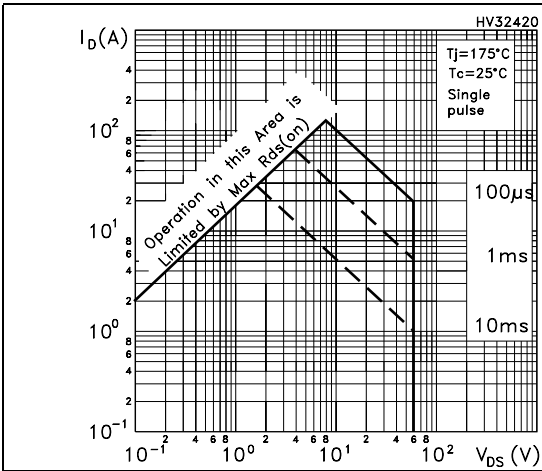


Figure 2. Thermal impedance

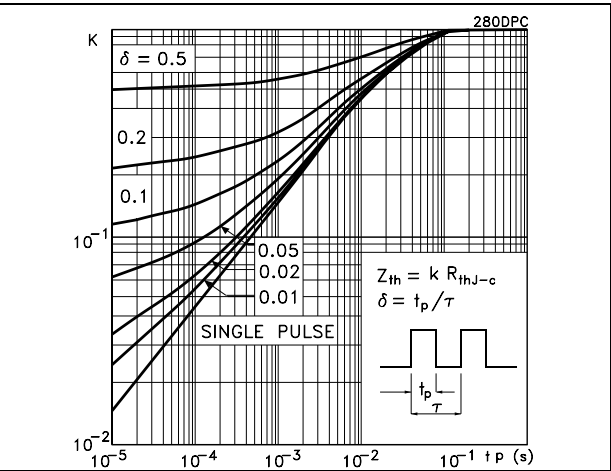


Figure 3. Output characteristics

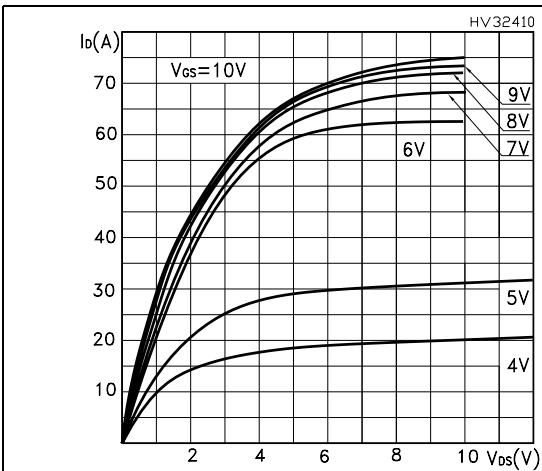


Figure 4. Transfer characteristics

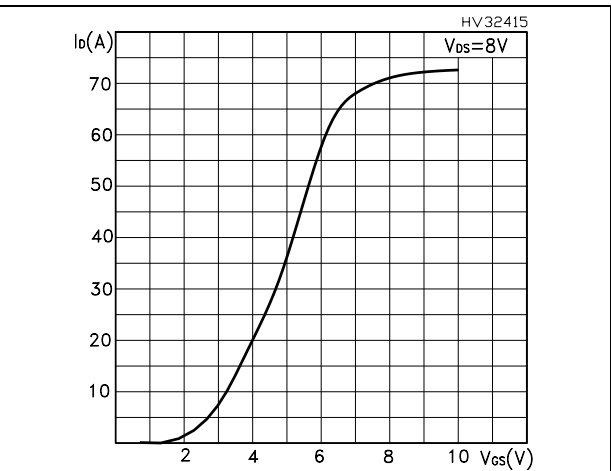


Figure 5. Normalized B_VDSS vs temperature

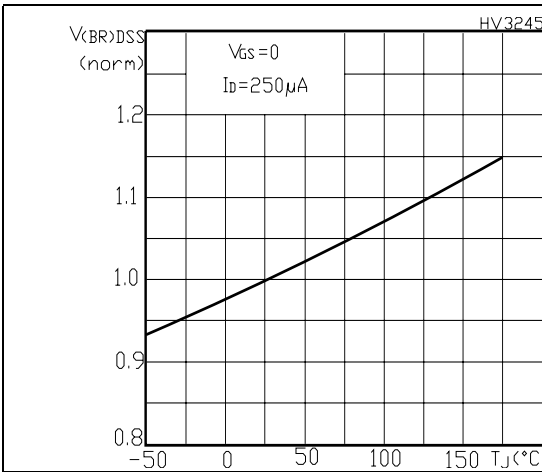


Figure 6. Static drain-source on resistance

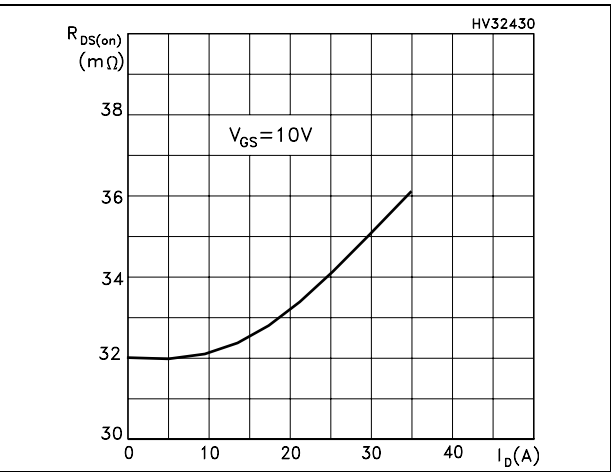


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

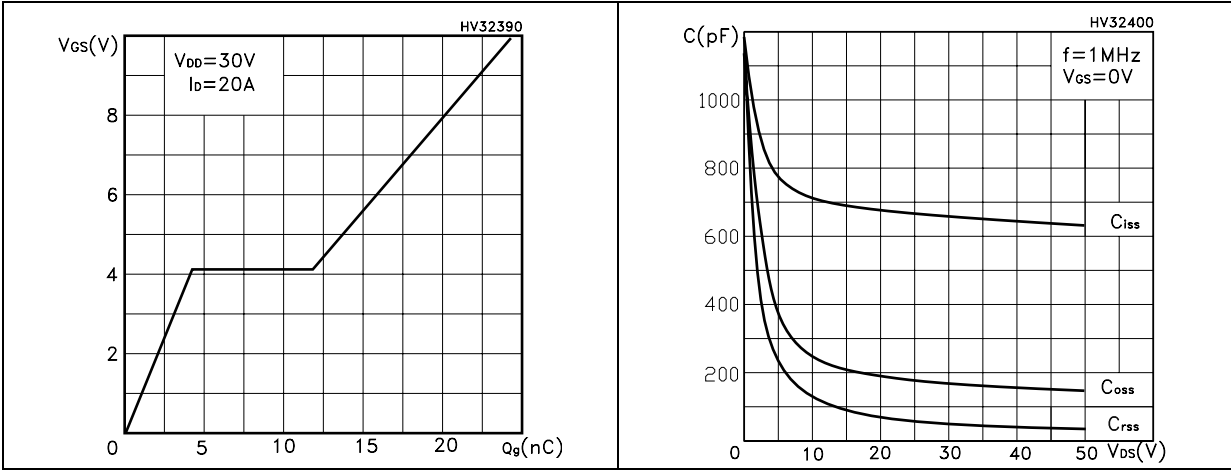
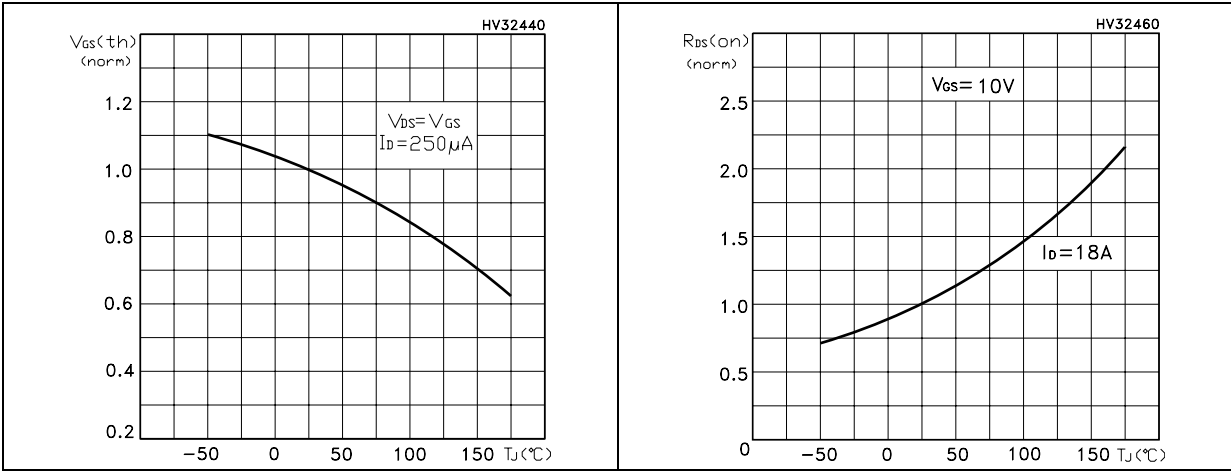


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature



3 Test circuits

Figure 11. Switching times test circuit for resistive load

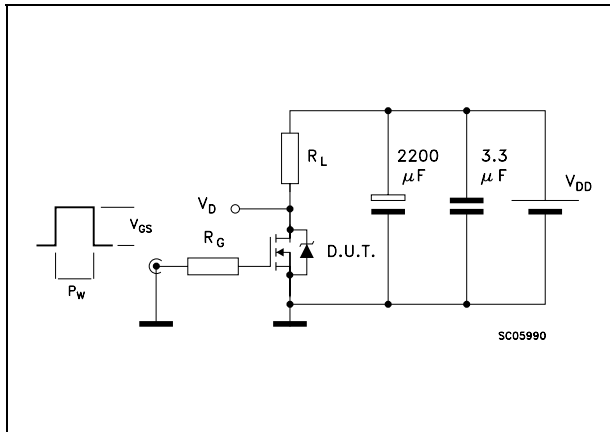


Figure 12. Gate charge test circuit

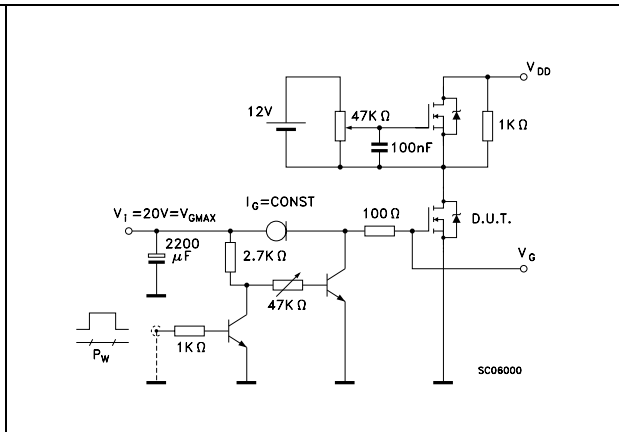


Figure 13. Test circuit for inductive load switching and diode recovery times

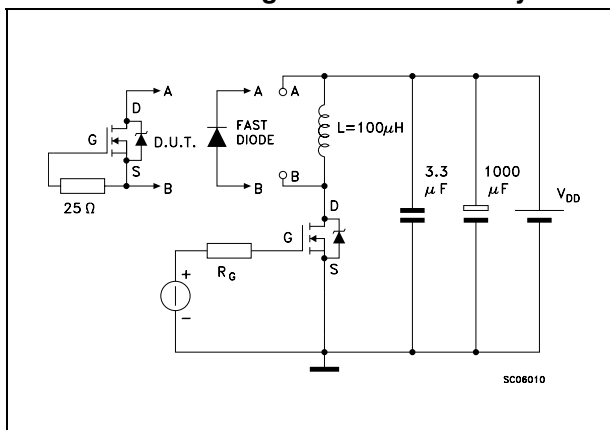


Figure 14. Unclamped inductive load test circuit

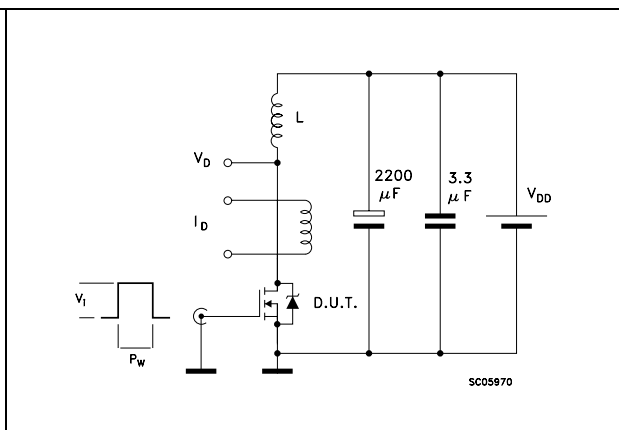


Figure 15. Unclamped inductive waveform

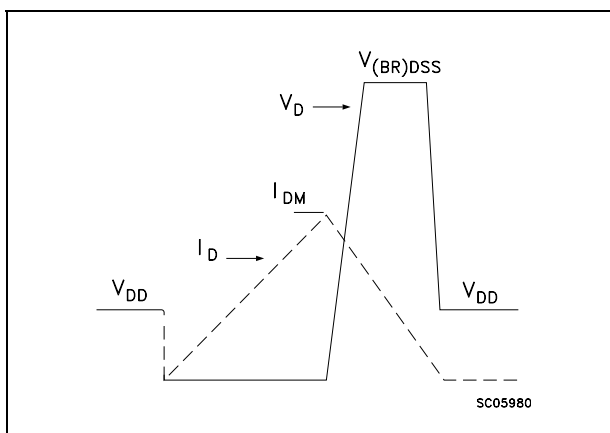
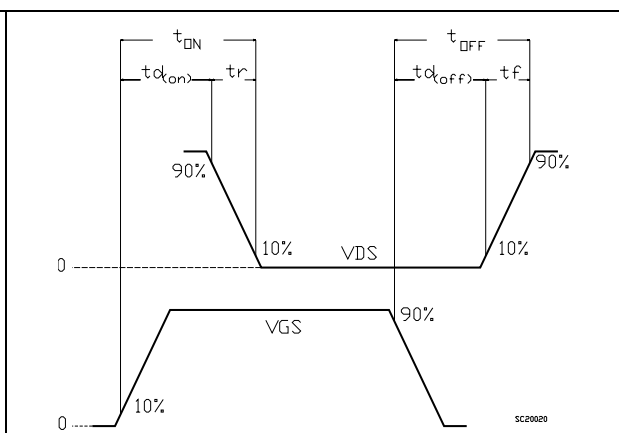


Figure 16. Switching time waveform

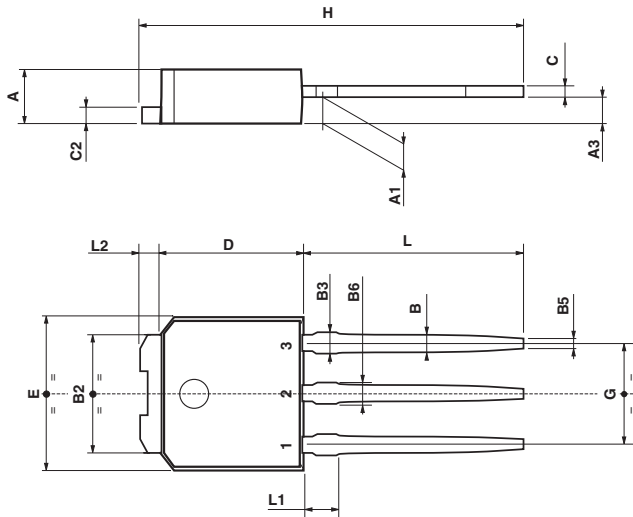


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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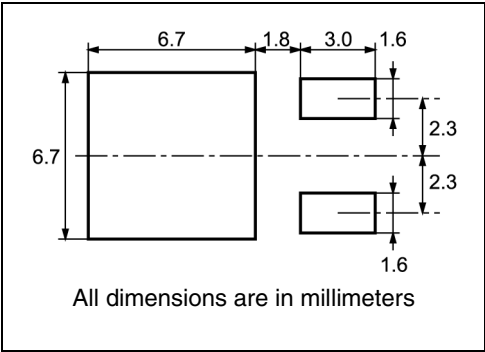
DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

The mechanical drawing illustrates the DPAK package geometry. It includes a top view showing dimensions E, b4, L2, L4, H, e, e1, and b(2x). A side view shows dimensions A, c2, D, A1, c, and R. A detail view of the thermal pad shows dimensions E1, D1, and L1. A circular detail view shows the lead profile with dimensions A2, L, (L1), V2, and a 0.25 gauge plane. The text 'SEATING PLANE' and 'THERMAL PAD' are also present.

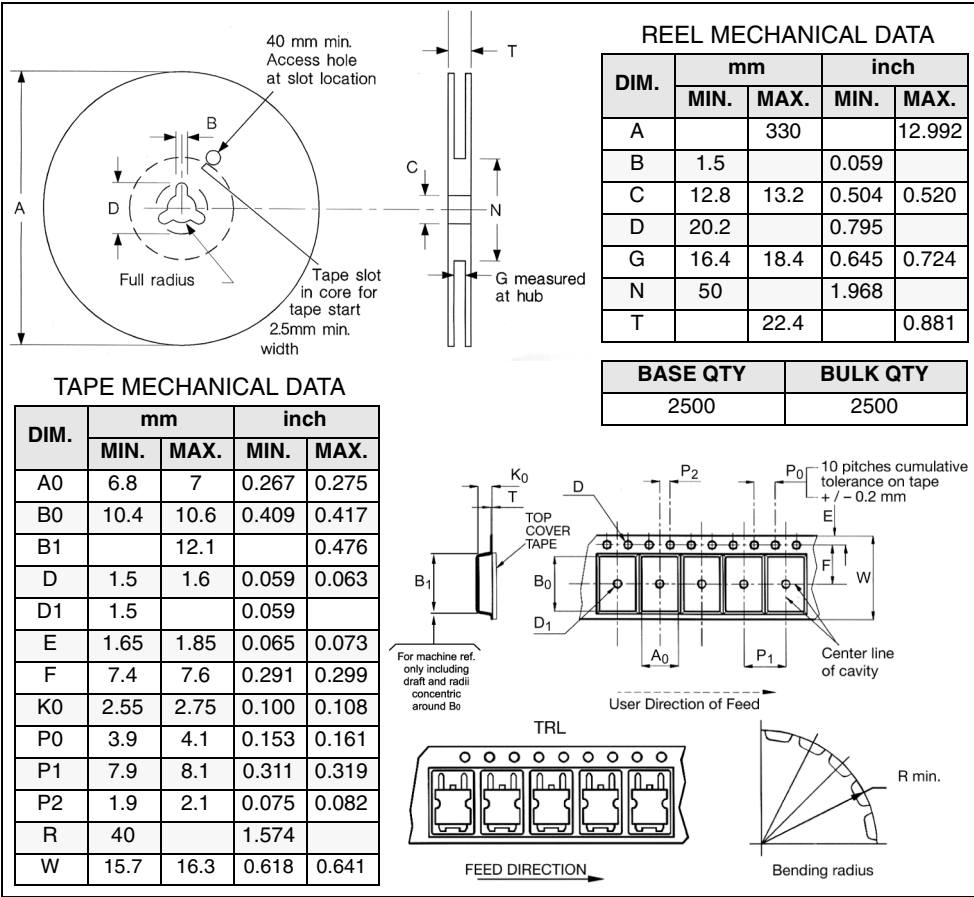
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5 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 7. Revision history

Date	Revision	Changes
19-Apr-2005	2	Added package IPAK
08-Jun-2006	3	Graphical updates
03-Jul-2006	4	New template, no content change

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