

2.5 Gbps x2 Lane Serial PCI Express Repeater/Equalizer with Signal Detect feature

Features

- Two High Speed PCI Express lanes
- Supports PCI Express data rates (2.5 Gbps) on each lane
- Adjustable Transmitter De-Emphasis & Amplitude
- Adjustable Receiver Equalization
- Input Signal Level Detect & Output Squelch on all Channels
- Two Spread Spectrum Reference Clock Buffer Outputs
- 100Ω Differential CML I/O's
- Low Power (100mW per Channel)
- Standby Mode – Power Down State
- V_{DD} Operating Range: 1.8V +/-0.1V
- Packaging (Pb-free & Green): 84-ball LFBGA (NB84)

Description

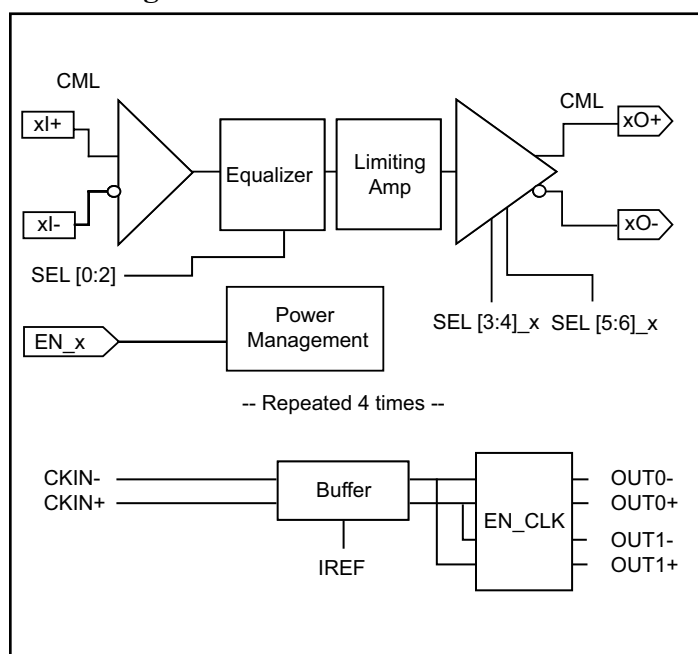
Pericom Semiconductor's PI2EQX4402D is a low power, PCI Express compliant signal Re-Driver. The device provides programmable equalization, amplification, and de-emphasis by using 7 select bits, SEL[0:6], to optimize performance over a variety of physical mediums by reducing Inter-symbol interference. PI2EQX4402D supports four 100-ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or extends the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the PCI Express signal before the Re-Driver. Whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the PCI Express signal after the Re-Driver.

A low-level input signal detection and output squelch function is provided for all four channels. Each channel operates fully independantly. When a channel is enabled (EN_x=1) and operating, that channel input signal level (on xI+/-) determines whether the output is enabled. If the input level of the channel falls below the active threshold level (V_{th}-) then the output driver switches off, and the pin is pulled to VDD via a high impedance resistor.

In addition to providing signal re-conditioning, Pericom's PI2EQX4402D also provides power management Stand-by mode operated by an Enable pin. A differential clock buffer is provided for test and other system requirements. This clock function is not used by the data channels.

Block Diagram



Pin Description (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|----------|-----------------|-----------------|-----------------|-----------------|--------|--------|--------|-----------------|--------|-----------------|
| A | SD_C | SD_D | SEL0_A | SEL0_B | SEL4_A | SEL4_B | SEL6_A | SEL6_B | EN_A | EN_B |
| B | V _{DD} | SD_B | V _{DD} | SEL1_A | SEL2_A | SEL3_A | SEL5_A | V _{DD} | EN_C | V _{DD} |
| C | BO+ | SD_A | AI+ | SEL1_B | SEL2_B | SEL3_B | SEL5_B | BI+ | EN_D | AO+ |
| D | BO- | V _{DD} | AI- | 84-Ball LFBGA | | | | BI- | GND | AO- |
| E | GND | V _{DD} | GND | | | | | GND | GND | GND |
| F | V _{DD} | GND | V _{DD} | | | | | V _{DD} | GND | V _{DD} |
| G | DO+ | SEL0_C | CI+ | | | | | DI+ | SEL6_C | CO+ |
| H | DO- | SEL0_D | CI- | V _{DD} | CKIN+ | CKIN- | GND | DI- | SEL6_D | CO- |
| J | GND | SEL1_C | GND | SEL2_C | SEL2_D | SEL3_D | IREF | GND | SEL4_D | GND |
| K | EN_CLK | SEL1_D | SEL3_C | SEL4_C | OUT0+ | OUT0- | OUT1+ | OUT1- | SEL5_C | SEL5_D |

Pin Description

| Pin # | Pin Name | I/O | Description |
|--|-----------------|-----|---|
| B1, F1, D2, E2, B3, F3, H4, B8, F8, B10, F10 | V _{DD} | PWR | 1.8V Supply Voltage |
| C3 | AI+ | I | Positive CML Input Channel A with internal 50Ω pull down during normal operation (EN_A=1). When EN_A=0, this pin is high impedance. |
| D3 | AI- | I | Negative CML Input Channel A with internal 50Ω pull down during normal operation (EN_A=1). When EN_A=0, this pin is high impedance. |
| E1, J1, F2, E3, J3, H7, E8, J8, D9, E9, F9, E10, J10 | GND | PWR | Supply Ground |
| C8 | BI+ | I | Positive CML Input Channel B with internal 50Ω pull down during normal operation (EN_B=1). When EN_B=0, this pin is high impedance. |
| D8 | BI- | I | Negative CML Input Channel B with internal 50Ω pull down during normal operation (EN_B=1). When EN_B=0, this pin is high impedance. |
| G3 | CI+ | I | Positive CML Input Channel C with internal 50Ω pull down during normal operation (EN_C=1). When EN_C=0, this pin is high impedance. |
| H3 | CI- | I | Negative CML Input Channel C with internal 50Ω pull down during normal operation (EN_C=1). When EN_C=0, this pin is high impedance. |
| G8 | DI+ | I | Positive CML Input Channel D with internal 50Ω pull down during normal operation (EN_D=1). When EN_D=0, this pin is high impedance. |
| H8 | DI- | I | Negative CML Input Channel D with internal 50Ω pull down during normal operation (EN_D=1). When EN_D=0, this pin is high impedance. |
| A3, B4, B5 | SEL[0:2]_A | I | Selection pins for equalizer (see Amplifier Configuration Table) w/ 50KΩ internal pull up |
| A4, C4, C5 | SEL[0:2]_B | I | |
| G2, J2, J4 | SEL[0:2]_C | I | |
| H2, K2, J5 | SEL[0:2]_D | I | |
| B6, A5 | SEL[3:4]_A | I | Selection pins for amplifier (see Amplifier Configuration Table) w/ 50KΩ internal pull up |
| C6, A6 | SEL[3:4]_B | I | |
| K3, K4 | SEL[3:4]_C | I | |
| J6, J9 | SEL[3:4]_D | I | |
| B7, A7 | SEL[5:6]_A | I | Selection pins for De-Emphasis (See De-Emphasis Configuration Table) w/ 50KΩ internal pull up |
| C7, A8 | SEL[5:6]_B | I | |
| K9, G9 | SEL[5:6]_C | I | |
| K10, H9 | SEL[5:6]_D | I | |
| C10 | AO+ | O | Positive CML Output Channel A internal 50Ω pull up during normal operation and 2KΩ pull up otherwise. |
| D10 | AO- | O | Negative CML Output Channel A with internal 50Ω pull up during normal operation and 2KΩ pull up otherwise. |
| C1 | BO+ | O | Positive CML Output Channel B with internal 50Ω pull up during normal operation and 2KΩ pull up otherwise. |
| D1 | BO- | O | Negative CML Output Channel B with internal 50Ω pull up during normal operation and 2KΩ pull up otherwise. |
| G10 | CO+ | O | Positive CML Output Channel C with internal 50Ω pull up during normal operation and 2KΩ pull up otherwise. |
| H10 | CO- | O | Negative CML Output Channel C with internal 50Ω pull up during normal operation and 2KΩ pull up otherwise. |

Pin Description (Continued)

| Pin # | Pin Name | I/O | Description |
|-----------------|------------------|-----|---|
| GI | DO+ | O | Positive CML Output Channel D with internal 50Ω pull up during normal operation and 2KΩ pull up otherwise. |
| HI | DO- | O | Negative CML Output Channel D with internal 50Ω pull up during normal operation and 2KΩ pull up otherwise. |
| A9, A10, B9, C9 | EN_ [A,B,C,D] | I | EN_[A:D] is the enable pin with internal 50KΩ pull up resistor. A LVCMOS high provides normal operation. A LVCMOS low selects a low power down mode. |
| H6 | CKIN- | I | Differential Input Reference Clock |
| H5 | CKIN+ | I | |
| K5, K6 | OUT0+, OUT0- | O | Differential Reference Clock Output |
| K7, K8 | OUT1+, OUT1- | O | |
| J7 | IREF | O | External 475Ω resistor connection to set the differential output current |
| K1 | EN_CLK | I | Enable output clock pin with internal 50kΩ pull up resistor. When EN_CLK is LVCMOS high level, the clock output operates normally. When EN_CLK = low, the clock outputs are turned off for power savings. A clock is not required by the data channels for operation. |
| C2, B2, A1, A2 | SD [A,B,C,D] | N/A | Signal detected, channels A, B, C, D. Indicated a valid signal level on the channels input pin pair when active high. When low, SD indicates the input signal level is below the signal detect threshold level. |

| Inputs | Outputs |
|-----------------|---------------|
| EN_[A, B, C, D] | O+ / O- |
| High | Normal output |
| Low | No output |

| Inputs | Clock Outputs |
|--------|-----------------|
| EN_CLK | |
| High | Clock output |
| Low | No clock output |

Output Swing Control

| SEL3_[A:D] | SEL4_[A:D] | Swing |
|------------|------------|-------|
| 0 | 0 | 1x |
| 0 | 1 | 0.8x |
| 1 | 0 | 1.2x |
| 1 | 1 | 1.4x |

Output De-emphasis Adjustment

| SEL5_[A:D] | SEL6_[A:D] | De-emphasis |
|------------|------------|-------------|
| 0 | 0 | 0dB |
| 0 | 1 | -2.5dB |
| 1 | 0 | -3.5dB |
| 1 | 1 | -4.5dB |

Equalizer Selection

| SEL0_[A:D] | SEL1_[A:D] | SEL2_[A:D] | Compliance Channel |
|------------|------------|------------|----------------------|
| 0 | 0 | 0 | No Equalization |
| 0 | 0 | 1 | [0:1.5dB] @ 1.25 GHz |
| 0 | 1 | 0 | [0:2.5dB] @ 1.25 GHz |
| 0 | 1 | 1 | [0:3.5dB] @ 1.25 GHz |
| 1 | 0 | 0 | [0:4.5dB] @ 1.25 GHz |
| 1 | 0 | 1 | [0:5.5dB] @ 1.25 GHz |
| 1 | 1 | 0 | [0:6.5dB] @ 1.25 GHz |
| 1 | 1 | 1 | [0:7.5dB] @ 1.25 GHz |

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| | |
|--|--------------------------------|
| Storage Temperature..... | –65°C to +150°C |
| Supply Voltage to Ground Potential | –0.5V to +2.5V |
| DC SIG Voltage..... | –0.5V to V _{DD} +0.5V |
| Current Output | –25mA to +25mA |
| Power Dissipation Continuous | 800mW |
| Operating Temperature..... | 0 to +70°C |

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics for 2.5 Gbps Quad Repeater/Equalizer (V_{DD} = 1.8 ±0.1V)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-------------------------|---|-------------------------|-------|------|-------|-------|
| Ps | Supply Power | EN = LVCMOS Low | | | 0.1 | W |
| | | EN = LVCMOS High | | | 0.6 | |
| | Latency | From input to output | | 2.0 | | ns |
| CML Receiver Input | | | | | | |
| V _{RX-DIFFP-P} | Differential Input Peak-to-peak Voltage | | 0.175 | | 1.200 | V |
| V _{RX-CM-ACP} | AC Peak Common Mode Input Voltage | | | | 150 | mV |
| V _{TH-} | Signal Detect Threshold | E _{N_X} = High | | 120 | 175 | mV |
| Z _{RX-DIFF-DC} | DC Differential Input Impedance | | 80 | 100 | 120 | Ω |
| Z _{RX-DC} | DC Input Impedance | | 40 | 50 | 60 | |
| Equalization | | | | | | |
| J _{RS} | Residual Jitter ^(1,2) | Total Jitter | | | 0.3 | Ulp-p |
| | | Deterministic jitter | | | 0.2 | |
| J _{RM} | Random Jitter ^(1,2) | | | 1.5 | | psrms |

Notes

- K28.7 pattern is applied differentially at point A as shown in Figure 1.
- Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of Figure 1.

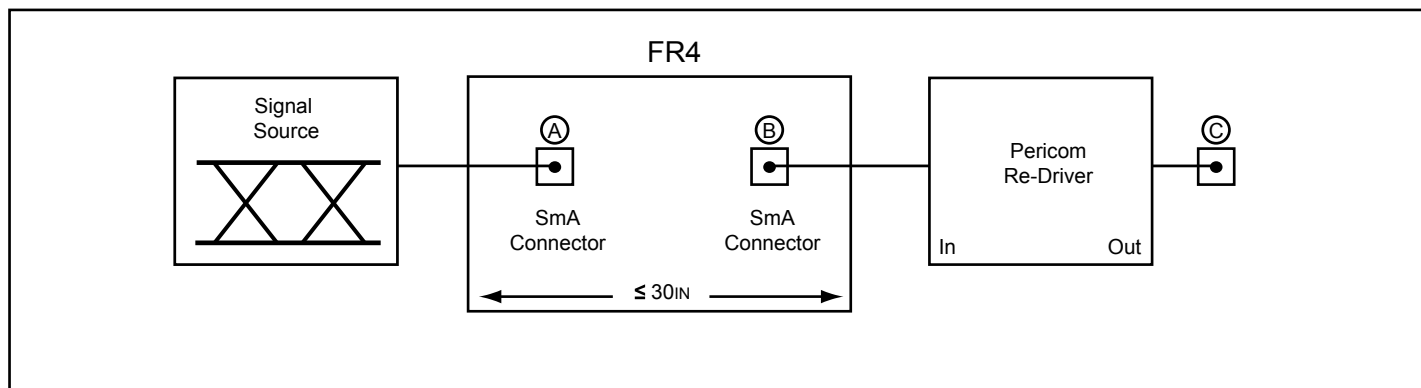


Figure 1. Test Condition Referenced in the Electrical Characteristic Table

AC/DC Electrical Characteristics for 2.5 Gbps x2 Lane Repeater/Equalizer (TA = 0 to 70°C)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|--|---|------------------------|----------------------|------------------------|-------|
| CML Transmitter Output (100Ω differential) | | | | | | |
| V _{DIFFP} | Output Voltage Swing | Differential Swing V _{TX-D+} - V _{TX-D-} | 400 | | 900 | mVp-p |
| V _{TX-C} | Common-Mode Voltage | V _{TX-D+} + V _{TX-D-} / 2 | | V _{DD} -0.3 | | |
| t _F , t _R | Transition Time | 20% to 80% ⁽¹⁾ | | | 150 | ps |
| Z _{OUT} | Output resistance | Single ended | 40 | 50 | 60 | Ω |
| Z _{TX-DIFF-DC} | DC Differential TX Impedance | | 80 | 100 | 120 | Ω |
| C _{TX} | AC Coupling Capacitor | | 75 | | 200 | nF |
| V _{TX-DIFFP-P} | Differential Peak-to-peak Output Voltage | V _{TX-DIFFP-P} = 2 * V _{TX-D+} - V _{TX-D-} | 0.8 | | 1.8 | V |
| LVC MOS Control Pins | | | | | | |
| V _{IH} | Input High Voltage | | 0.65 × V _{DD} | | V _{DD} | V |
| V _{IL} | Input Low Voltage | | | | 0.35 × V _{DD} | |
| I _{IH} | Input High Current | | | | 250 | μA |
| I _{IL} | Input Low Current | | | | 500 | |

Note:

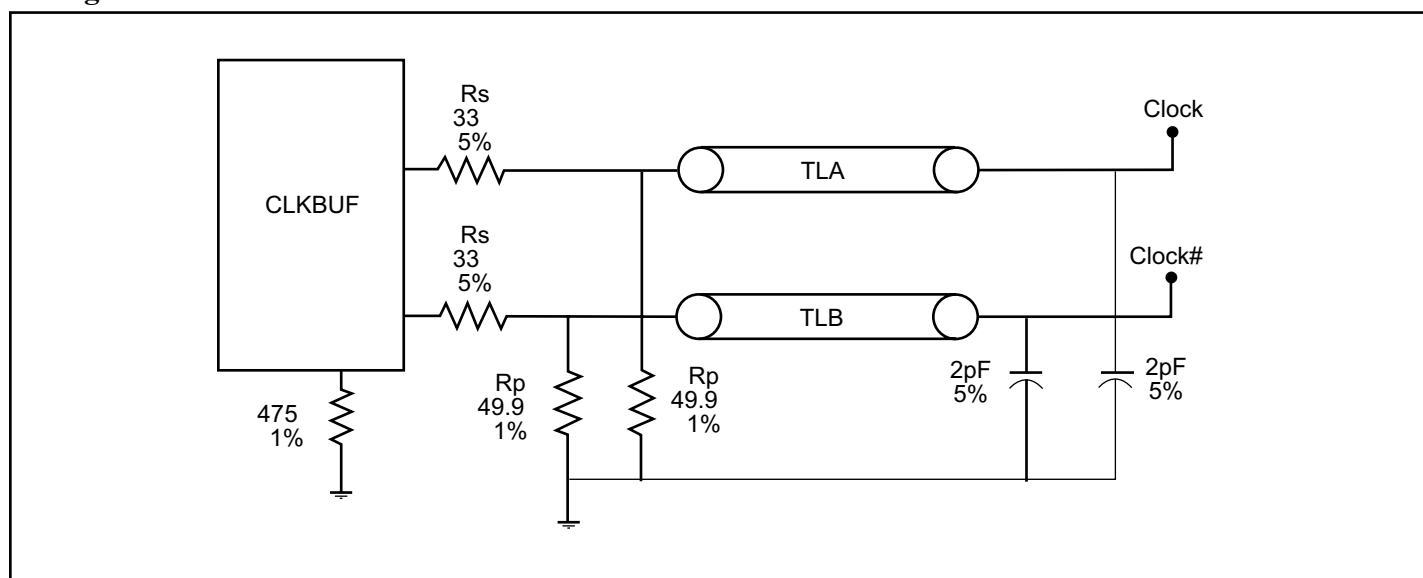
- Using K28.7 (0011111000) pattern)

AC Switching Characteristics for Clock Buffer ($V_{DD} = 1.8 \pm 0.1V$, $AV_{DD} = 1.8 \pm 0.1V$) ⁽³⁾

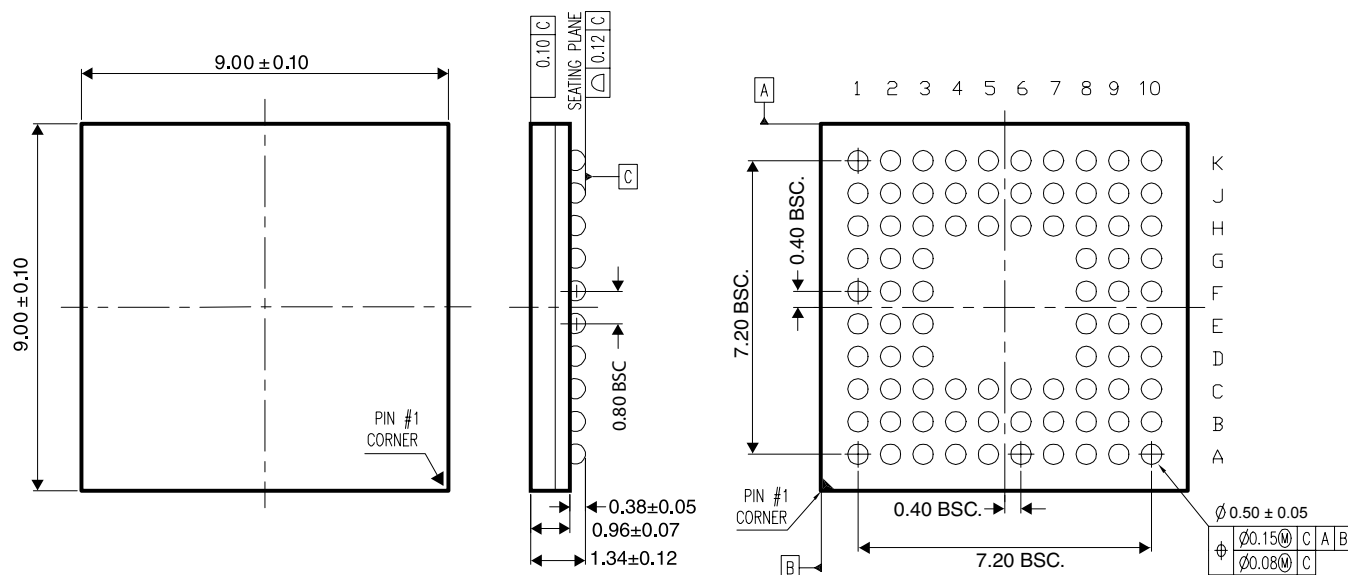
| Symbol | Parameters | Min | Max. | Units | Notes |
|-------------------------------------|---|------|------|-------|-------|
| T_{rise} / T_{fall} | Rise and Fall Time (measured between 0.175V to 0.525V) ⁽¹⁾ | 125 | 525 | ps | 1 |
| $\Delta T_{rise} / \Delta T_{fall}$ | Rise and Fall Time Variation | | 75 | | 1 |
| V_{HIGH} | Voltage High including overshoot | 660 | 900 | mV | 1 |
| V_{LOW} | Voltage Low including undershoot | -200 | | | 1 |
| V_{CROSS} | Absolute crossing point voltages | 200 | 550 | | 1 |
| ΔV_{CROSS} | Total Variation of Vcross over all edges | | 250 | | 1 |
| T_{DC} | Duty Cycle (input duty cycle = 50%) ⁽²⁾ | 45 | 55 | % | 2 |

Notes:

1. Measurement taken from Single Ended waveform.
2. Measurement taken from Differential waveform.
3. Test configuration is $R_S = 33.2\Omega$, $R_P = 49.9\Omega$, and 2pF.

Configuration Test Load Board Termination

Figure 2. Configuration test load board termination
Note:

- TLA and TLB are 3" transmission lines.



Notes:

- 1) All dimensions are in millimeters
- 2) JEDEC: MO-205F (Ref.)



DATE: 08/19/05

DESCRIPTION: 84-Ball LFBGA

PACKAGE CODE: NB-84

DOCUMENT CONTROL #: PD-2038

REVISION: C

Ordering Information

| Ordering Number | Package Code | Package Description |
|-----------------|--------------|-------------------------------|
| PI2EQX4402DNBE | NB | Pb-free & Green 84-Ball LFBGA |

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- X suffix = Tape/Reel