

150 mA, Tiny CMOS LDO With Shutdown

Features:

- Space-saving 5-Pin SC-70 and SOT-23 Packages
- Extremely Low Operating Current for Longer Battery Life: 53 μ A (typ.)
- Very Low Dropout Voltage
- Rated 150 mA Output Current
- Requires Only 1 μ F Ceramic Output Capacitance
- High Output Voltage Accuracy: $\pm 0.5\%$ (typical)
- 10 μ s (typ.) Wake-Up Time from $\overline{\text{SHDN}}$
- Power-Saving Shutdown Mode: 0.05 μ A (typ.)
- Overcurrent and Overtemperature Protection
- Pin-Compatible Upgrade for Bipolar Regulators

Applications:

- Cellular/GSM/PHS Phones
- Battery-Operated Systems
- Portable Computers
- Medical Instruments
- Electronic Games
- Pagers

General Description:

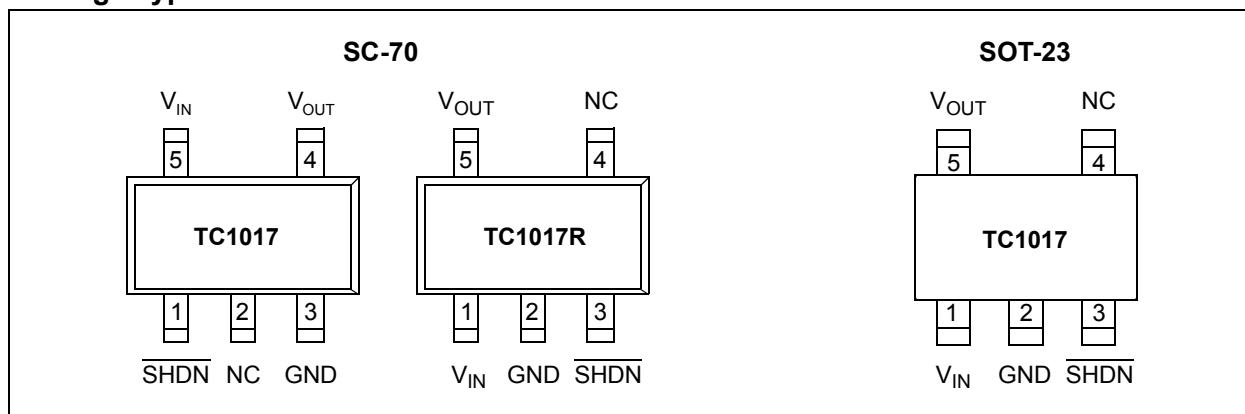
The TC1017 is a high-accuracy (typically $\pm 0.5\%$) CMOS upgrade for bipolar Low Dropout regulators (LDOs). It is offered in a SC-70 or SOT-23 package. The SC-70 package represents a 50% footprint reduction versus the popular SOT-23 package and is offered in two pinouts to make board layout easier.

Developed specifically for battery-powered systems, the TC1017's CMOS construction consumes only 53 μ A typical supply current over the entire 150 mA operating load range. This can be as much as 60 times less than the quiescent operating current consumed by bipolar LDOs.

The TC1017 is designed to be stable, over the entire input voltage and output current range, with low-value (1 μ F) ceramic or tantalum capacitors. This helps to reduce board space and save cost. Additional integrated features, such as shutdown, overcurrent and overtemperature protection, further reduce the board space and cost of the entire voltage-regulating application.

Key performance parameters for the TC1017 include low dropout voltage (285 mV typical at 150 mA output current), low supply current while shutdown (0.05 μ A typical) and fast stable response to sudden input voltage and load changes.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage6.5V

Power Dissipation Internally Limited (**Note 7**)

Maximum Voltage On Any Pin $V_{IN} + 0.3V$ to $-0.3V$

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
SHDN	Shutdown control input.
NC	No connect
GND	Ground terminal
V_{OUT}	Regulated voltage output
V_{IN}	Unregulated supply input

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100 \mu A$, $C_L = 1.0 \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25^\circ C$ Boldface type specifications apply for junction temperatures of $-40^\circ C$ to $+125^\circ C$.						
Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Input Operating Voltage	V_{IN}	2.7	—	6.0	V	Note 1
Maximum Output Current	I_{OUTMAX}	100	—	—	mA	Note 1
		150	—	—		$V_{IN} \geq 3V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUTMAX}$
Output Voltage	V_{OUT}	$V_R - 2.5\%$	$V_R \pm 0.5\%$	$V_R + 2.5\%$	V	Note 2
V_{OUT} Temperature Coefficient	TCV_{OUT}	—	40	—	ppm/ $^\circ C$	Note 3
Line Regulation	$[(\Delta V_{OUT}/\Delta V_{IN}) / V_R]$	—	0.04	0.2	%/V	$(V_R + 1V) < V_{IN} < 6V$
Load Regulation (Note 4)	$ \Delta V_{OUT} / V_R$	—	0.38	1.5	%	$I_L = 0.1 \text{ mA to } I_{OUTMAX}$
Dropout Voltage (Note 5)	$V_{IN} - V_{OUT}$	—	2	—	mV	$I_L = 100 \mu A$
		—	90	200		$I_L = 50 \text{ mA}$
		—	180	350		$I_L = 100 \text{ mA}$
		—	285	500		$I_L = 150 \text{ mA}$
Supply Current	I_{IN}	—	53	90	μA	$\overline{SHDN} = V_{IH}$, $I_L = 0$
Shutdown Supply Current	I_{INSD}	—	0.05	2	μA	$\overline{SHDN} = 0V$
Power Supply Rejection Ratio	PSRR	—	58	—	dB	$f = 1 \text{ kHz}$, $I_L = 50 \text{ mA}$

Note 1: The minimum V_{IN} has to meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$.

2: V_R is the regulator voltage setting. For example: $V_R = 1.8V, 2.7V, 2.8V, 3.0V$.

3:

$$TCV_{OUT} = \frac{(V_{OUTMAX} - V_{OUTMIN}) \times 10^6}{V_{OUT} \times \Delta T}$$

4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

5: Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value at a 1V differential.

6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at $V_{IN} = 6V$ for $t = 10 \text{ msec}$.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see **Section 5.1 “Thermal Shutdown”**, for more details.

8: Output current is limited to 120 mA (typ) when V_{OUT} is less than 0.5V due to a load fault or short-circuit condition.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100 \mu A$, $C_L = 1.0 \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25^\circ C$ Boldface type specifications apply for junction temperatures of $-40^\circ C$ to $+125^\circ C$.						
Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Wake-Up Time (from Shutdown mode)	t_{WK}	—	10	—	μs	$V_{IN} = 5V$, $I_L = 60 mA$, $C_{IN} = C_{OUT} = 1 \mu F$, $f = 100 Hz$
Settling Time (from Shutdown mode)	t_S	—	32	—	μs	$V_{IN} = 5V$, $I_L = 60 mA$, $C_{IN} = 1 \mu F$, $C_{OUT} = 1 \mu F$, $f = 100 Hz$
Output Short-Circuit Current	I_{OUTSC}	—	120	—	mA	$V_{OUT} = 0V$, Average Current (Note 8)
Thermal Regulation	V_{OUT}/P_D	—	0.04	—	V/W	Notes 6, 7
Thermal Shutdown Die Temperature	T_{SD}	—	160	—	$^\circ C$	
Thermal Shutdown Hysteresis	ΔT_{SD}	—	10	—	$^\circ C$	
Output Noise	eN	—	800	—	nV/ $\sqrt{Hz}$	$f = 10 kHz$
SHDN Input High Threshold	V_{IH}	45	—	—	% V_{IN}	$V_{IN} = 2.7V$ to $6.0V$
SHDN Input Low Threshold	V_{IL}	—	—	15	% V_{IN}	$V_{IN} = 2.7V$ to $6.0V$

Note 1: The minimum V_{IN} has to meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$.

2: V_R is the regulator voltage setting. For example: $V_R = 1.8V$, $2.7V$, $2.8V$, $3.0V$.

3:

$$TCV_{OUT} = \frac{(V_{OUTMAX} - V_{OUTMIN}) \times 10^6}{V_{OUT} \times \Delta T}$$

4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from $0.1 mA$ to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

5: Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value at a $1V$ differential.

6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at $V_{IN} = 6V$ for $t = 10 msec$.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see **Section 5.1 "Thermal Shutdown"**, for more details.

8: Output current is limited to $120 mA$ (typ) when V_{OUT} is less than $0.5V$ due to a load fault or short-circuit condition.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{DD} = +2.7V$ to $+6.0V$ and $V_{SS} = GND$.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	$^\circ C$	Extended Temperature parts
Operating Temperature Range	T_A	-40	—	+125	$^\circ C$	
Storage Temperature Range	T_A	-65	—	+150	$^\circ C$	
Thermal Package Resistances³						
Thermal Resistance, 5L-SOT23	θ_{JA}	—	255	—	$^\circ C/W$	
Thermal Resistance, 5L-SC-70	θ_{JA}	—	450	—	$^\circ C/W$	

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100 \mu A$, $C_L = 1.0 \mu F$, $SHDN > V_{IH}$, $T_A = +25^\circ C$.

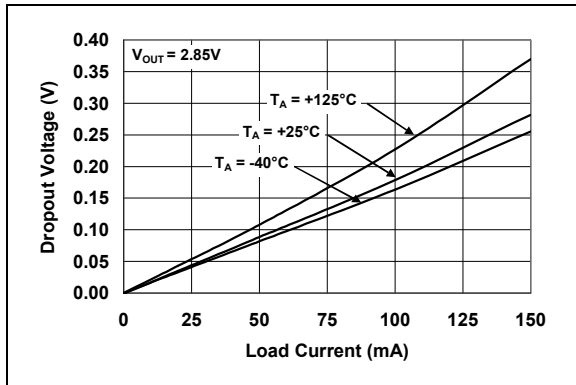


FIGURE 2-1: Dropout Voltage vs. Output Current.

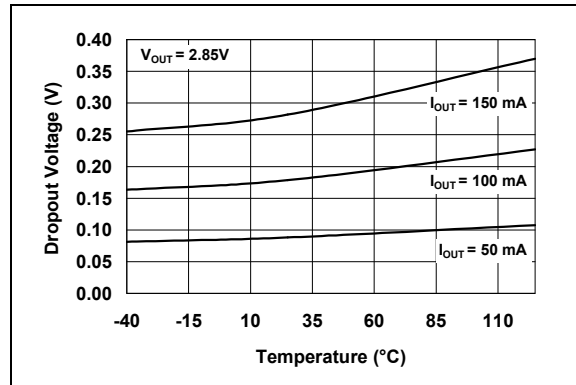


FIGURE 2-4: Dropout Voltage vs. Temperature.

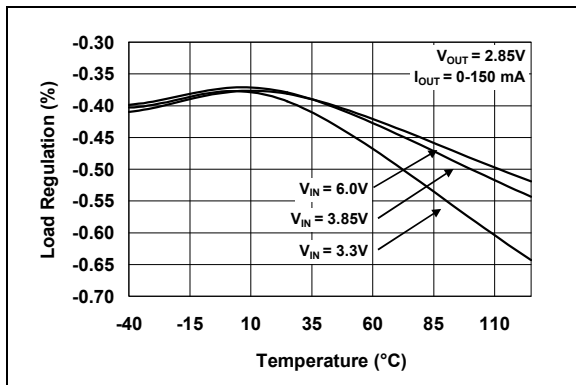


FIGURE 2-2: Load Regulation vs. Temperature.

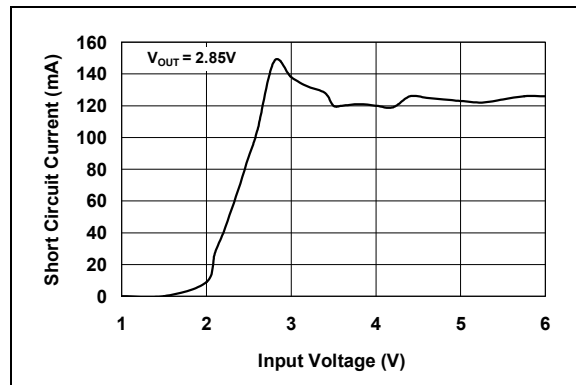


FIGURE 2-5: Short-Circuit Current vs. Input Voltage.

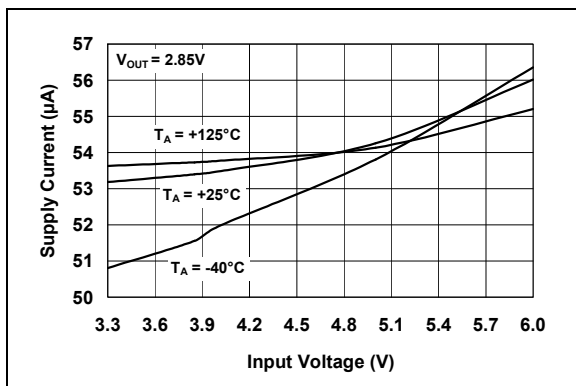


FIGURE 2-3: Supply Current vs. Input Voltage.

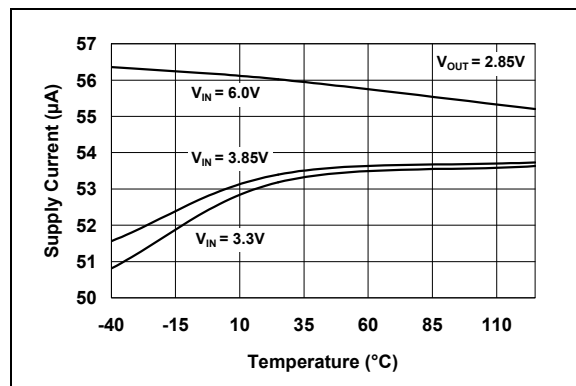


FIGURE 2-6: Supply Current vs. Temperature.

Note: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100 \mu A$, $C_L = 1.0 \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25^\circ C$.

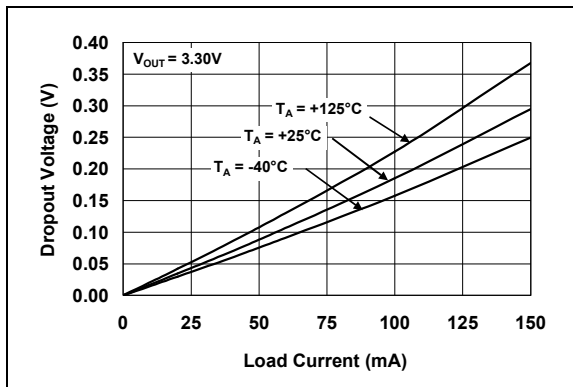


FIGURE 2-7: Dropout Voltage vs. Output Current.

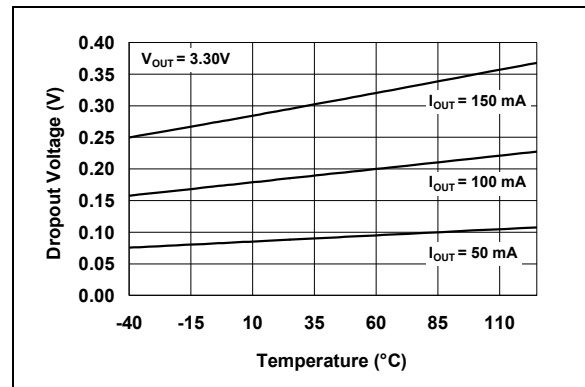


FIGURE 2-10: Dropout Voltage vs. Temperature.

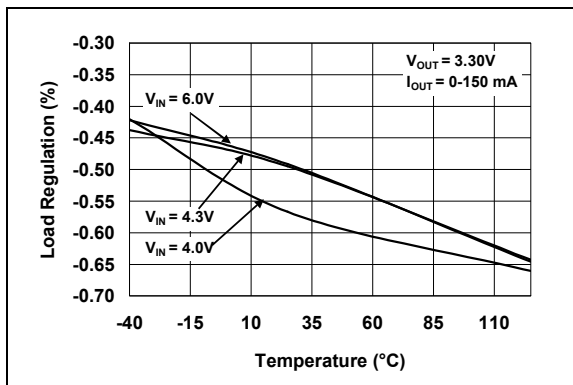


FIGURE 2-8: Load Regulation vs. Temperature.

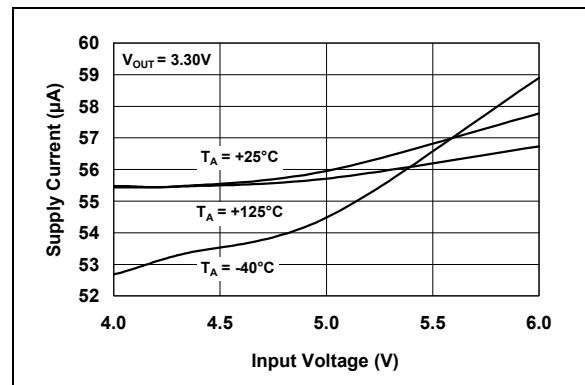


FIGURE 2-11: Supply Current vs. Input Voltage.

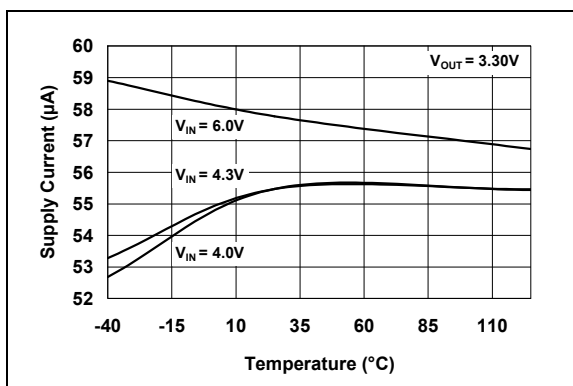


FIGURE 2-9: Supply Current vs. Temperature.

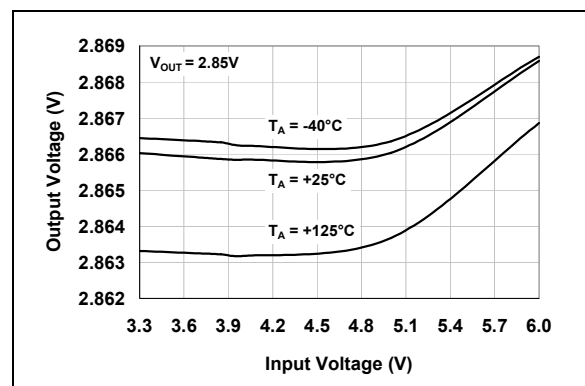


FIGURE 2-12: Output Voltage vs. Supply Voltage.

Note: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100 \mu A$, $C_L = 1.0 \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25^\circ C$.

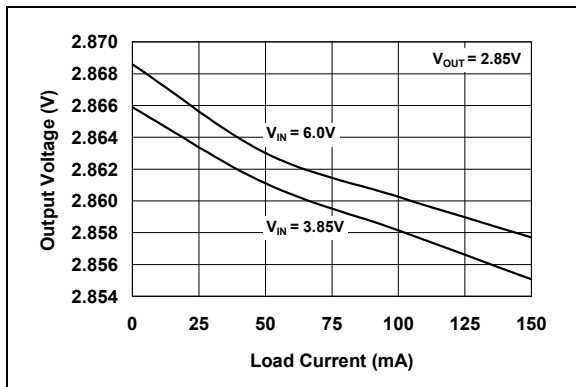


FIGURE 2-13: Output Voltage vs. Output Current.

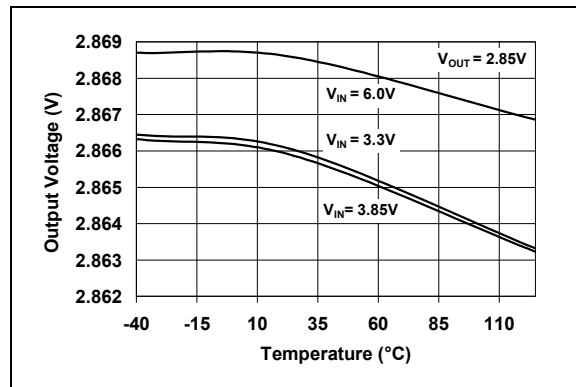


FIGURE 2-16: Output Voltage vs. Temperature.

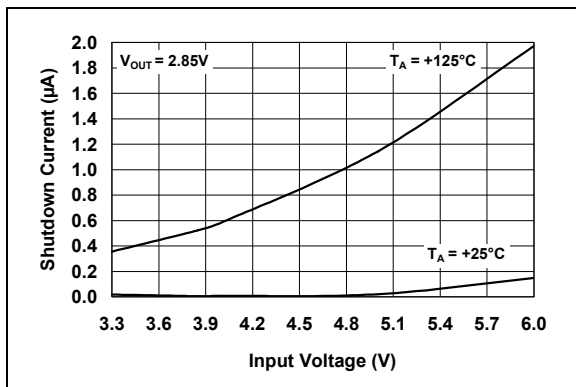


FIGURE 2-14: Shutdown Current vs. Input Voltage.

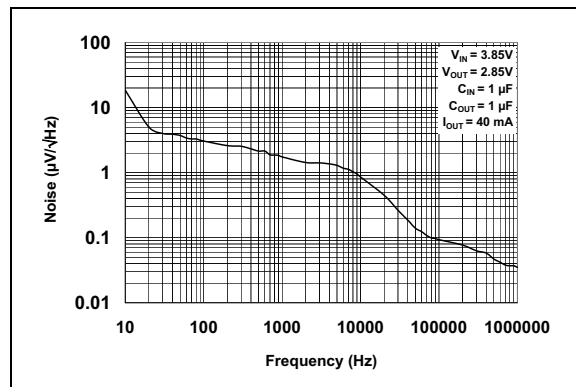


FIGURE 2-17: Output Noise vs. Frequency.

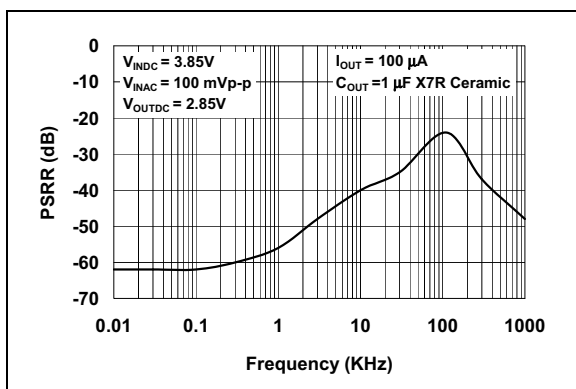


FIGURE 2-15: Power Supply Rejection Ratio vs. Frequency.

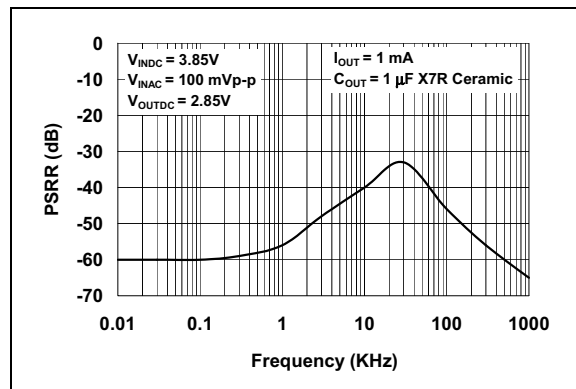


FIGURE 2-18: Power Supply Rejection Ratio vs. Frequency.

Note: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100 \mu A$, $C_L = 1.0 \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25^\circ C$.

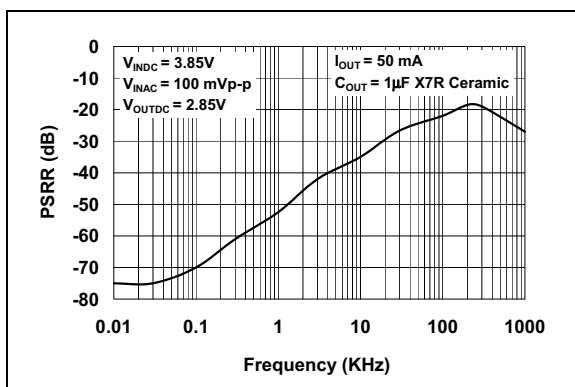


FIGURE 2-19: Power Supply Rejection Ratio vs. Frequency.

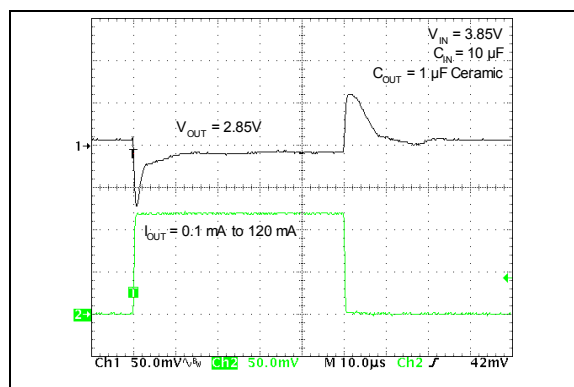


FIGURE 2-22: Load Transient Response.

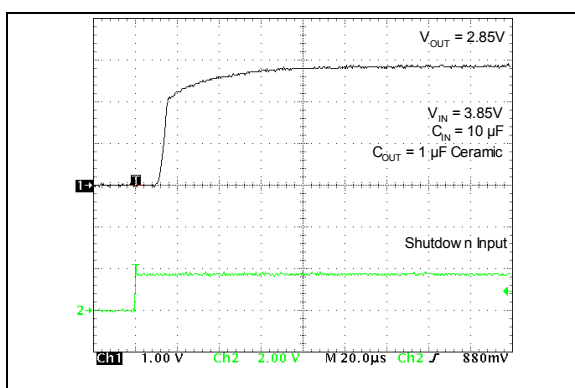


FIGURE 2-20: Wake-Up Response.

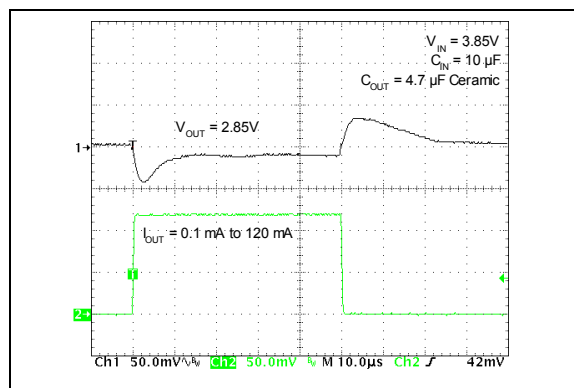


FIGURE 2-23: Load Transient Response.

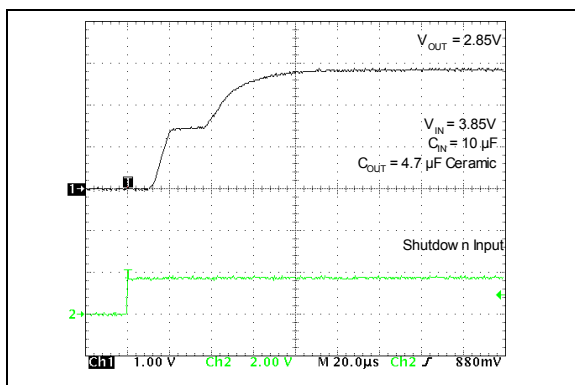


FIGURE 2-21: Wake-Up Response.

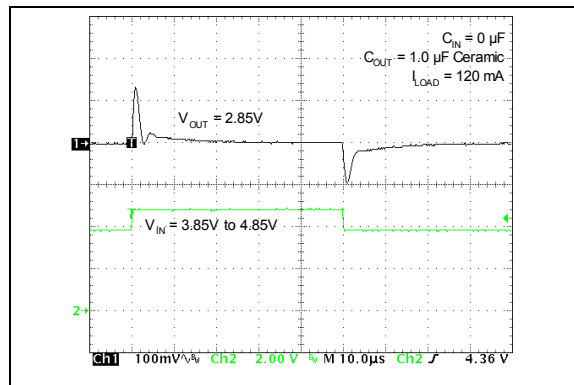


FIGURE 2-24: Line Transient Response.

Note: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100 \mu A$, $C_L = 1.0 \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25^\circ C$.

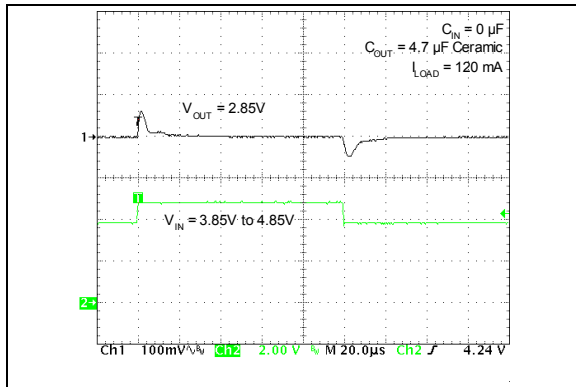


FIGURE 2-25: Line Transient Response.

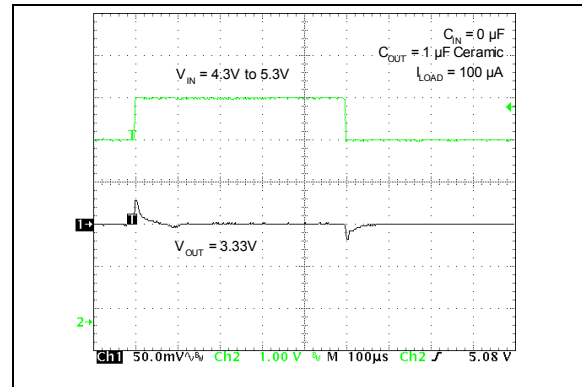


FIGURE 2-26: Line Transient Response.

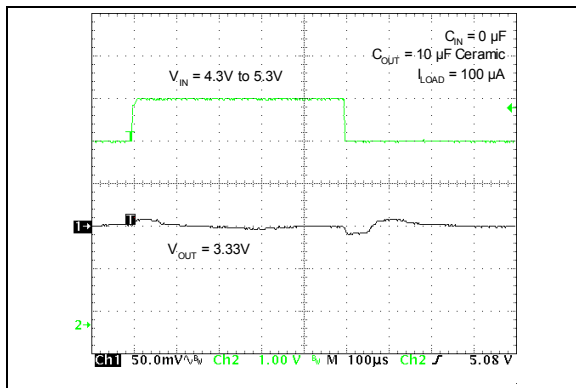


FIGURE 2-27: Line Transient Response.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin No. 5-Pin SC-70	Pin No. 5-Pin SOT-23 5-Pin SC-70R	Symbol	Description
1	3	$\overline{\text{SHDN}}$	Shutdown Control Input
2	4	NC	No Connect
3	2	GND	Ground Terminal
4	5	V_{OUT}	Regulated Voltage Output
5	1	V_{IN}	Unregulated Supply Input

3.1 Shutdown Control Input ($\overline{\text{SHDN}}$)

The regulator is fully enabled when a logic-high is applied to $\overline{\text{SHDN}}$. The regulator enters shutdown when a logic-low is applied to this input. During shutdown, the output voltage falls to zero and the supply current is reduced to 0.05 μA (typ.)

3.2 Ground Terminal

For best performance, it is recommended that the ground pin be tied to a ground plane.

3.3 Regulated Voltage Output (V_{OUT})

Bypass the regulated voltage output to GND with a minimum capacitance of 1 μF . A ceramic bypass capacitor is recommended for best performance.

3.4 Unregulated Supply Input (V_{IN})

The minimum V_{IN} has to meet two conditions in order to ensure that the output maintains regulation: $V_{\text{IN}} \geq 2.7\text{V}$ and $V_{\text{IN}} \geq [(V_{\text{R}} + 2.5\%) + V_{\text{DROPOUT}}]$. The maximum V_{IN} should be less than or equal to 6V. Power dissipation may limit V_{IN} to a lower potential in order to maintain a junction temperature below 125°C. Refer to [Section 5.0 "Thermal Considerations"](#), for determining junction temperature.

It is recommended that V_{IN} be bypassed to GND with a ceramic capacitor.

4.0 DETAILED DESCRIPTION

The TC1017 is a precision, fixed-output, linear voltage regulator. The internal linear pass element is a P-channel MOSFET. As with all P-channel CMOS LDOs, there is a body drain diode with the cathode connected to V_{IN} and the anode connected to V_{OUT} (Figure 4-1).

As is shown in Figure 4-1, the output voltage of the LDO is sensed and divided down internally to reduce external component count. The internal error amplifier has a fixed bandgap reference on the inverting input and the sensed output voltage on the non-inverting input. The error amplifier output will pull the gate voltage down until the inputs of the error amplifier are equal to regulate the output voltage.

Output overload protection is implemented by sensing the current in the P-channel MOSFET. During a shorted or faulted load condition in which the output voltage falls to less than 0.5V, the output current is limited to a typical value of 120 mA. The current-limit protection helps prevent excessive current from damaging the Printed Circuit Board (PCB).

An internal thermal sensing device is used to monitor the junction temperature of the LDO. When the sensed temperature is over the set threshold of 160°C (typical), the P-channel MOSFET is turned off. When the P-channel is off, the power dissipation internal to the device is almost zero. The device cools until the junction tem-

perature is approximately 150°C and the P-channel is turned on. If the internal power dissipation is still high enough for the junction to rise to 160°C, it will again shut off and cool. The maximum operating junction temperature of the device is 125°C. Steady-state operation at or near the 160°C overtemperature point can lead to permanent damage of the device.

The output voltage V_{OUT} remains stable over the entire input operating voltage range (2.7V to 6.0V) and the entire load range (0 mA to 150 mA). The output voltage is sensed through an internal resistor divider and compared with a precision internal voltage reference. Several fixed-output voltages are available by changing the value of the internal resistor divider.

Figure 4-2 shows a typical application circuit. The regulator is enabled any time the shutdown input pin is at or above V_{IH} . It is shut down (disabled) any time the shutdown input pin is below V_{IL} . For applications where the SHDN feature is not used, tie the SHDN pin directly to the input supply voltage source. While in shutdown, the supply current decreases to 0.006 μ A (typical) and the P-channel MOSFET is turned off.

As shown in Figure 4-2, batteries have internal source impedance. An input capacitor is used to lower the input impedance of the LDO. In some applications, high input impedance can cause the LDO to become unstable. Adding more input capacitance can compensate for this.

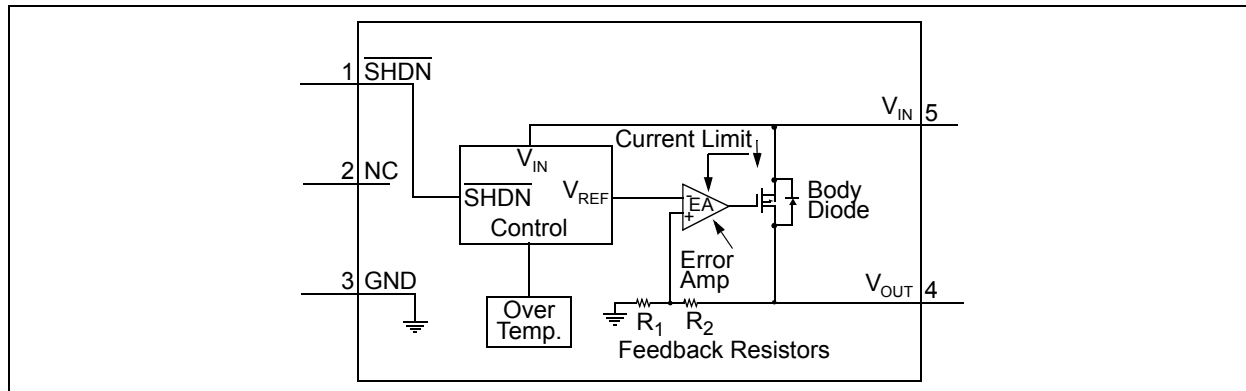


FIGURE 4-1: TC1017 Block Diagram (5-Pin SC-70 Pinout).

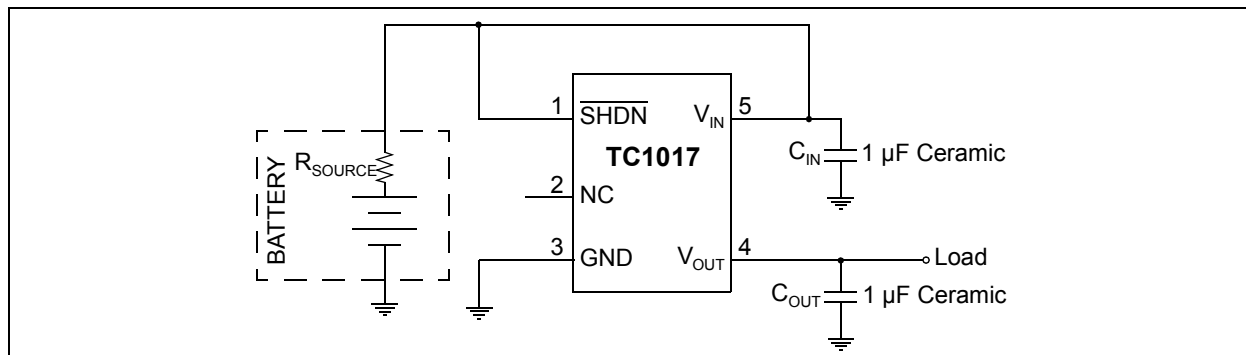


FIGURE 4-2: Typical Application Circuit (5-Pin SC-70 Pinout).

4.1 Input Capacitor

Low input source impedance is necessary for the LDO to operate properly. When operating from batteries, or in applications with long lead length ($> 10''$) between the input source and the LDO, some input capacitance is required. A minimum of $0.1\ \mu\text{F}$ is recommended for most applications and the capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will help reduce the input impedance and further reduce any high-frequency noise on the input and output of the LDO.

4.2 Output Capacitor

A minimum output capacitance of $1\ \mu\text{F}$ for the TC1017 is required for stability. The Equivalent Series Resistance (ESR) requirements on the output capacitor are between 0 and 2 ohms. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical $1\ \mu\text{F}$ X5R 0805 capacitor has an ESR of 50 milli-ohms. Larger output capacitors can be used with the TC1017 to improve dynamic behavior and input ripple-rejection performance.

Ceramic, aluminum electrolytic or tantalum capacitor types can be used. Since many aluminum electrolytic capacitors freeze at approximately -30°C , ceramic or solid tantalums are recommended for applications operating below -25°C . When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the value of the input and output capacitors and employing passive filtering techniques.

4.3 Turn-On Response

The turn-on response is defined as two separate response categories, wake-up time (t_{WK}) and settling time (t_{S}).

The TC1017 has a fast wake-up time (10 μsec , typical) when released from shutdown. See Figure 4-3 for the wake-up time designated as t_{WK} . The wake-up time is defined as the time it takes for the output to rise to 2% of the V_{OUT} value after being released from shutdown.

The total turn-on response is defined as the settling time (t_{S}) (see Figure 4-3). Settling time (inclusive with t_{WK}) is defined as the condition when the output is within 98% of its fully-enabled value (32 μsec , typical) when released from shutdown. The settling time of the output voltage is dependent on load conditions and output capacitance on V_{OUT} (RC response).

The table below demonstrates the typical turn-on response timing for different input voltage power-up frequencies: $V_{\text{OUT}} = 2.85\text{V}$, $V_{\text{IN}} = 5.0\text{V}$, $I_{\text{OUT}} = 60\text{ mA}$ and $C_{\text{OUT}} = 1\ \mu\text{F}$.

Frequency	Typical (t_{WK})	Typical (t_{S})
1000 Hz	5.3 μsec	14 μsec
500 Hz	5.9 μsec	16 μsec
100 Hz	9.8 μsec	32 μsec
50 Hz	14.5 μsec	52 μsec
10 Hz	17.2 μsec	77 μsec

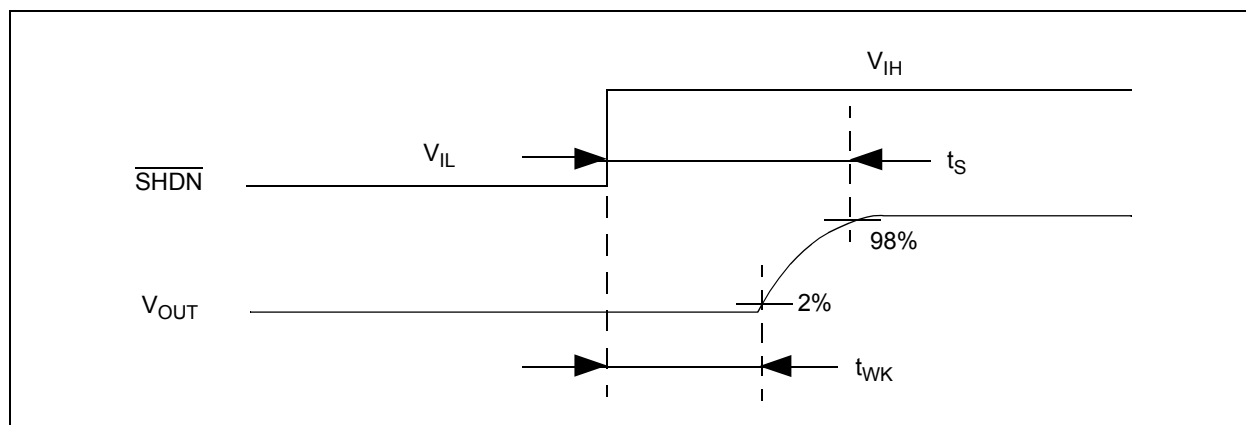


FIGURE 4-3: Wake-Up Time from Shutdown.

5.0 THERMAL CONSIDERATIONS

5.1 Thermal Shutdown

Integrated thermal protection circuitry shuts the regulator off when the die temperature exceeds approximately 160°C. The regulator remains off until the die temperature drops to approximately 150°C.

5.2 Power Dissipation: SC-70

The TC1017 is available in the SC-70 package. The thermal resistance for the SC-70 package is approximately 450°C/W when the copper area used in the PCB layout is similar to the JEDEC J51-7 high thermal conductivity standard or semi-G42-88 standard. For applications with a larger or thicker copper area, the thermal resistance can be lowered. See AN792, "A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application" (DS00792), for a method to determine the thermal resistance for a particular application.

The TC1017 power dissipation capability is dependant upon several variables: input voltage, output voltage, load current, ambient temperature and maximum junction temperature. The absolute maximum steady-state junction temperature is rated at +125°C. The power dissipation within the device is equal to:

EQUATION 5-1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD} + V_{IN} \times I_{GND}$$

The $V_{IN} \times I_{GND}$ term is typically very small when compared to the $(V_{IN} - V_{OUT}) \times I_{LOAD}$ term, simplifying the power dissipation within the LDO to be:

EQUATION 5-2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

To determine the maximum power dissipation capability, the following equation is used:

EQUATION 5-3:

$$P_{D_{MAX}} = \frac{(T_{J_{MAX}} - T_{A_{MAX}})}{R\theta_{JA}}$$

Where:

$T_{J_{MAX}}$ = the maximum junction temperature allowed

$T_{A_{MAX}}$ = the maximum ambient temperature

$R\theta_{JA}$ = the thermal resistance from junction to air

Given the following example:

$$\begin{aligned} V_{IN} &= 3.0V \text{ to } 4.1V \\ V_{OUT} &= 2.85V \pm 2.5\% \\ I_{LOAD} &= 120 \text{ mA (output current)} \\ T_A &= 55^\circ\text{C (max. desired ambient)} \end{aligned}$$

Find:

1. Internal power dissipation:

$$\begin{aligned} P_{D_{MAX}} &= (V_{IN_{MAX}} - V_{OUT_{MIN}}) \times I_{LOAD} \\ &= (4.1V - 2.85 \times (0.975)) \times 120\text{mA} \\ &= 158.5\text{mW} \end{aligned}$$

2. Maximum allowable ambient temperature:

$$\begin{aligned} T_{A_{MAX}} &= T_{J_{MAX}} - P_{D_{MAX}} \times R\theta_{JA} \\ &= (125^\circ\text{C} - 158.5\text{mW} \times 450^\circ\text{C/W}) \\ &= (125^\circ\text{C} - 71^\circ\text{C}) \\ &= 54^\circ\text{C} \end{aligned}$$

3. Maximum allowable power dissipation at desired ambient:

$$\begin{aligned} P_D &= \frac{T_{J_{MAX}} - T_A}{R\theta_{JA}} \\ &= \frac{125^\circ\text{C} - 55^\circ\text{C}}{450^\circ\text{C/W}} \\ &= 155\text{mW} \end{aligned}$$

In this example, the TC1017 dissipates approximately 158.5 mW and the junction temperature is raised 71°C over the ambient. The absolute maximum power dissipation is 155 mW when given a maximum ambient temperature of 55°C.

Input voltage, output voltage or load current limits can also be determined by substituting known values in the power dissipation equations.

Figure 5-1 and Figure 5-2 depict typical maximum power dissipation versus ambient temperature, as well as typical maximum current versus ambient temperature, with a 1V input voltage to output voltage differential, respectively.

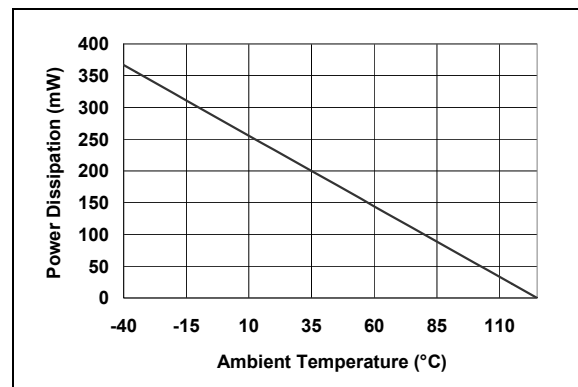


FIGURE 5-1: Power Dissipation vs. Ambient Temperature (SC-70 package).

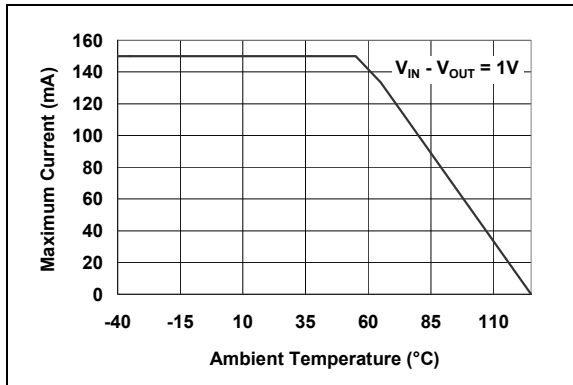


FIGURE 5-2: Maximum Current vs. Ambient Temperature (SC-70 package).

5.3 Power Dissipation: SOT-23

The TC1017 is also available in a SOT-23 package for improved thermal performance. The thermal resistance for the SOT-23 package is approximately 255°C/W when the copper area used in the printed circuit board layout is similar to the JEDEC J51-7 low thermal conductivity standard or semi-G42-88 standard. For applications with a larger or thicker copper area, the thermal resistance can be lowered. See AN792, "A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application" (DS00792), for a method to determine the thermal resistance for a particular application.

The TC1017 power dissipation capability is dependant upon several variables: input voltage, output voltage, load current, ambient temperature and maximum junction temperature. The absolute maximum steady-state junction temperature is rated at +125°C. The power dissipation within the device is equal to:

EQUATION 5-4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD} + V_{IN} \times I_{GND}$$

The $V_{IN} \times I_{GND}$ term is typically very small when compared to the $(V_{IN} - V_{OUT}) \times I_{LOAD}$ term, simplifying the power dissipation within the LDO to be:

EQUATION 5-5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

To determine the maximum power dissipation capability, the following equation is used:

EQUATION 5-6:

$$P_{D_{MAX}} = \frac{(T_{J_MAX} - T_{A_MAX})}{R\theta_{JA}}$$

Where:

T_{J_MAX} = the maximum junction temperature allowed

T_{A_MAX} = the maximum ambient temperature

$R\theta_{JA}$ = the thermal resistance from junction to air

Given the following example:

$$V_{IN} = 3.0V \text{ to } 4.1V$$

$$V_{OUT} = 2.85V \pm 2.5\%$$

$$I_{LOAD} = 120 \text{ mA (output current)}$$

$$T_A = +85^\circ\text{C (max. desired ambient)}$$

Find:

1. Internal power dissipation:

$$\begin{aligned} P_{D_{MAX}} &= (V_{IN_MAX} - V_{OUT_MIN}) \times I_{LOAD} \\ &= (4.1V - 2.85 \times (0.975)) \times 120mA \\ &= 158.5mW \end{aligned}$$

2. Maximum allowable ambient temperature:

$$\begin{aligned} T_{A_MAX} &= T_{J_MAX} - P_{D_{MAX}} \times R\theta_{JA} \\ &= (125^\circ\text{C} - 158.5mW \times 255^\circ\text{C/W}) \\ &= (125^\circ\text{C} - 40.5^\circ\text{C}) \\ &= 84.5^\circ\text{C} \end{aligned}$$

3. Maximum allowable power dissipation at desired ambient:

$$\begin{aligned} P_D &= \frac{T_{J_MAX} - T_A}{R\theta_{JA}} \\ &= \frac{125^\circ\text{C} - 85^\circ\text{C}}{255^\circ\text{C/W}} \\ &= 157mW \end{aligned}$$

In this example, the TC1017 dissipates approximately 158.5mW and the junction temperature is raised 40.5°C over the ambient. The absolute maximum power dissipation is 157 mW when given a maximum ambient temperature of +85°C.

Input voltage, output voltage or load current limits can also be determined by substituting known values in the power dissipation equations.

Figure 5-3 and Figure 5-4 depict typical maximum power dissipation versus ambient temperature, as well as typical maximum current versus ambient temperature with a 1V input voltage to output voltage differential, respectively.

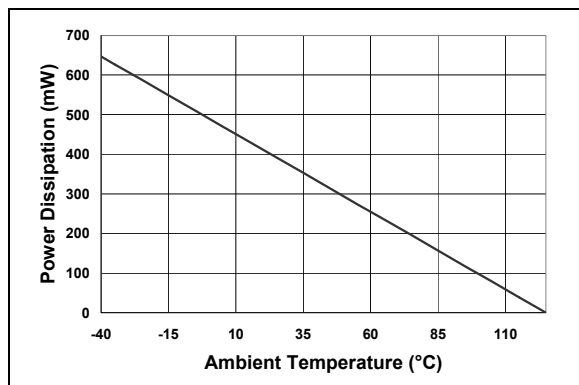


FIGURE 5-3: Power Dissipation vs. Ambient Temperature (SOT-23 Package).

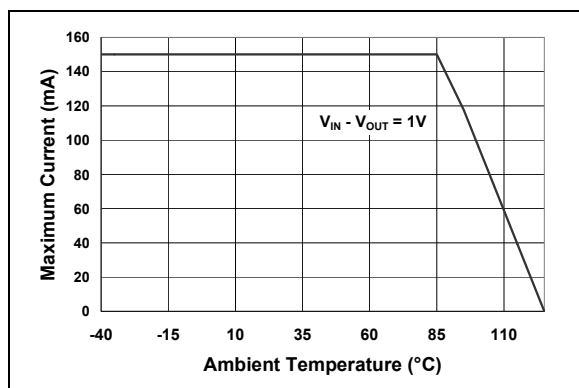


FIGURE 5-4: Maximum Current vs. Ambient Temperature (SOT-23 Package).

5.4 Layout Considerations

The primary path for heat conduction out of the SC-70/SOT-23 package is through the package leads. Using heavy, wide traces at the pads of the device will facilitate the removal of the heat within the package, thus lowering the thermal resistance $R\theta_{JA}$. By lowering the thermal resistance, the maximum internal power dissipation capability of the package is increased.

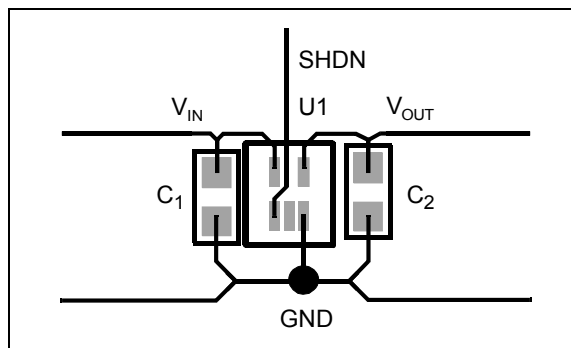
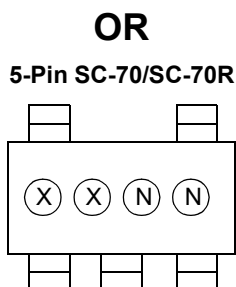
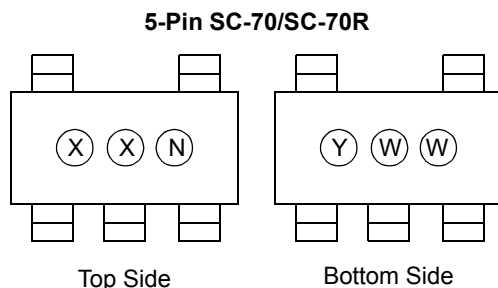


FIGURE 5-5: SC-70 Package Suggested Layout.

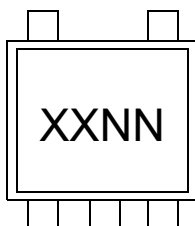
6.0 PACKAGE INFORMATION

6.1 Package Marking Information



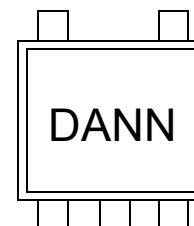
Part Number	TC1017 Pinout Code	TC1017R Pinout Code
TC1017 – 1.8VLT	CE	CU
TC1017 – 1.85VLT	CQ	DF
TC1017 – 1.9VLT	CB	
TC1017 – 2.5VLT	CR	CV
TC1017 – 2.6VLT	CF	CW
TC1017 – 2.7VLT	CG	CX
TC1017 – 2.8VLT	CH	CY
TC1017 – 2.85VLT	CJ	CZ
TC1017 – 2.9VLT	CK	DA
TC1017 – 3.0VLT	CL	DB
TC1017 – 3.2VLT	CC	DC
TC1017 – 3.3VLT	CM	DD
TC1017 – 4.0VLT	CP	DE

5-Lead SOT-23



Part Number	Code
TC1017 – 1.8VCT	DA
TC1017 – 1.85VCT	DK
TC1017 – 2.6VCT	DB
TC1017 – 2.7VCT	DC
TC1017 – 2.8VCT	DD
TC1017 – 2.85VCT	DE
TC1017 – 2.9VCT	DF
TC1017 – 3.0VCT	DG
TC1017 – 3.3VCT	DH
TC1017 – 4.0VCT	DJ

Example:

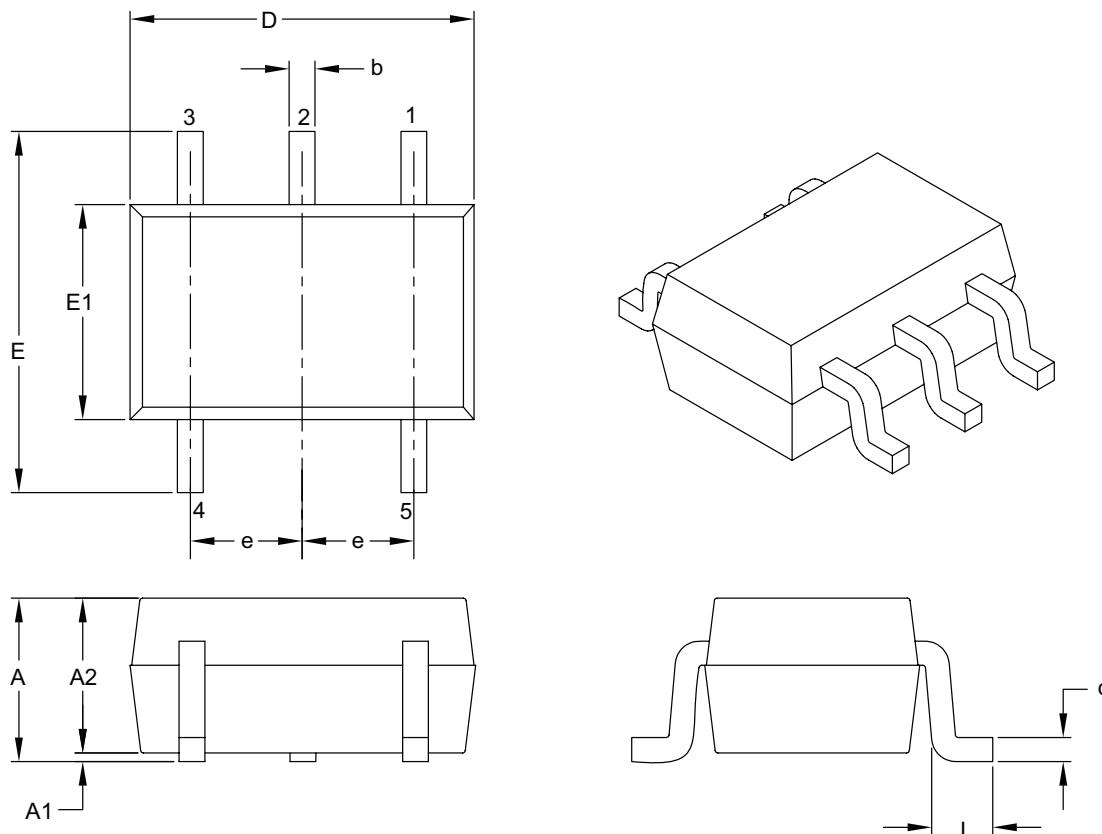


Legend:	XX...X	Customer-specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

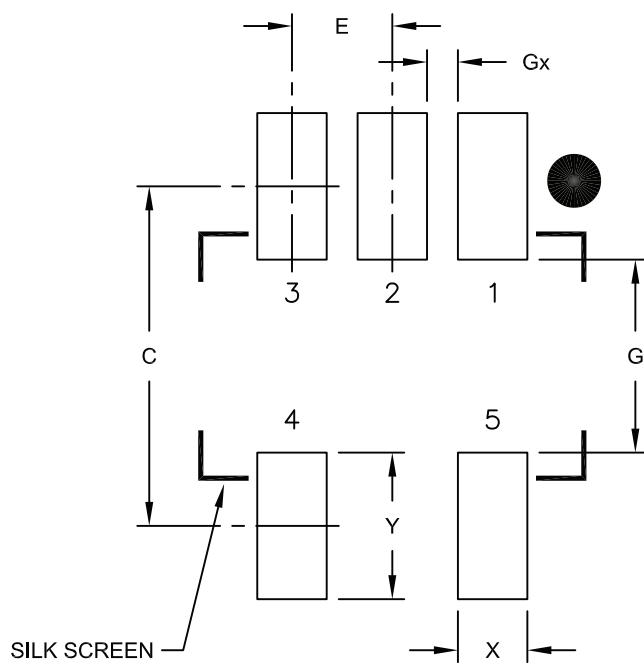
Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

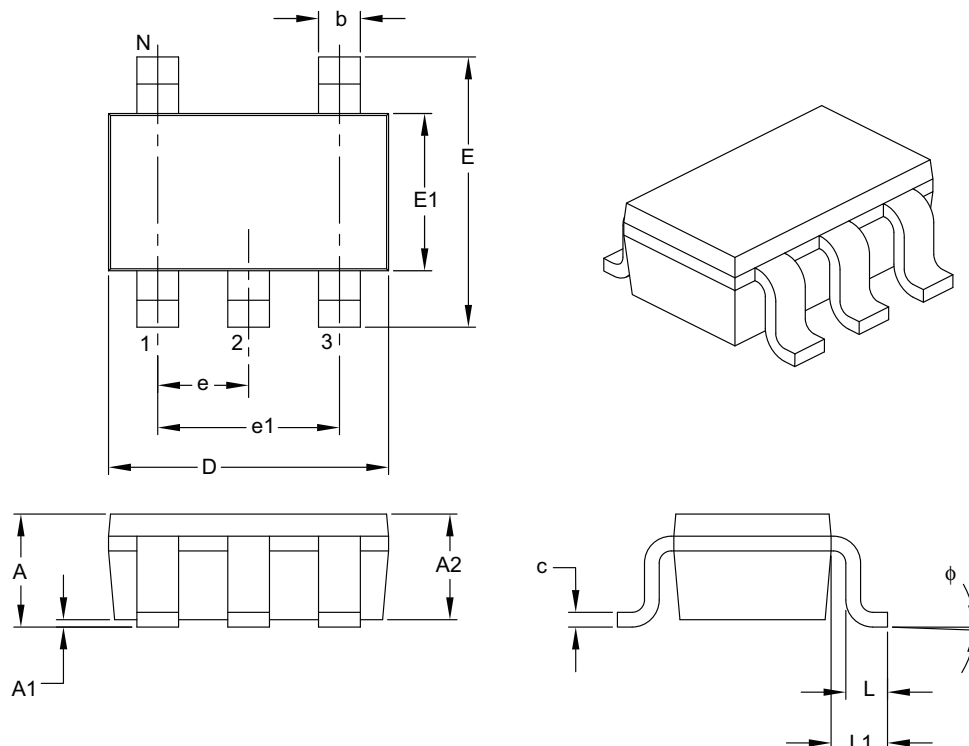
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		5		
Lead Pitch	e		0.95 BSC		
Outside Lead Pitch	e1		1.90 BSC		
Overall Height	A		0.90	—	1.45
Molded Package Thickness	A2		0.89	—	1.30
Standoff	A1		0.00	—	0.15
Overall Width	E		2.20	—	3.20
Molded Package Width	E1		1.30	—	1.80
Overall Length	D		2.70	—	3.10
Foot Length	L		0.10	—	0.60
Footprint	L1		0.35	—	0.80
Foot Angle	φ		0°	—	30°
Lead Thickness	c		0.08	—	0.26
Lead Width	b		0.20	—	0.51

Notes:

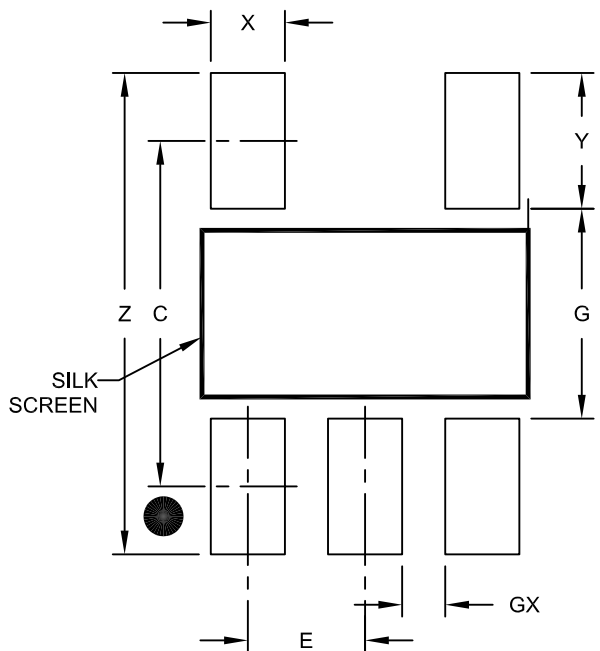
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

NOTES:

APPENDIX A: REVISION HISTORY

Revision F (April 2013)

The following is the list of modifications:

- Updated the information for the Maximum Output Current parameter in the [Electrical Characteristics](#) table.

Revision E (January 2013)

- Added a note to each package outline drawing.

Revision D (February 2005)

- Undocumented changes.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X.XX</u>	<u>X</u>	<u>XXXX</u>	Examples:
Device	Voltage Options	Temperature Range	Package	
Device:	TC1017: 150 mA Tiny CMOS LDO with Shutdown TC1017R: 150 mA Tiny CMOS LDO with Shutdown (SC-70 only)			a) TC1017-1.8VLTTTR: 150 mA, Tiny CMOS LDO with Shutdown, SC-70 package.
Voltage Options:* (Standard)	1.8V 1.85V 2.5V 2.6V 2.7V 2.8V 2.85V 2.9V 3.0V 3.2V 3.3V 4.0V	SC-70 only SC-70 only		b) TC1017R-1.8VLTTTR: 150mA, Tiny CMOS LDO with Shutdown, SC-70R package. c) TC1017-2.6VCTTTR: 150 mA, Tiny CMOS LDO with Shutdown, SOT-23 package. d) TC1017-2.7VLTTTR: 150 mA, Tiny CMOS LDO with Shutdown, SC-70 package. e) TC1017-2.8VCTTTR: 150 mA, Tiny CMOS LDO with Shutdown, SOT-23 package. f) TC1017-2.85VLTTTR: 150 mA, Tiny CMOS LDO with Shutdown, SC-70 package. g) TC1017-2.9VCTTTR: 150 mA, Tiny CMOS LDO with Shutdown, SOT-23 package. h) TC1017-3.0VLTTTR: 150 mA, Tiny CMOS LDO with Shutdown, SC-70 package. i) TC1017-3.3VCTTTR: 150 mA, Tiny CMOS LDO with Shutdown, SOT-23 package. j) TC1017-4.0VLTTTR: 150 mA, Tiny CMOS LDO with Shutdown, SC-70 package.
* Other voltage options available. Please contact your local Microchip sales office for details.				
Temperature Range:	V = -40°C to +125°C			
Package:	LTTR = 5-pin SC-70 (Tape and Reel) CTTR = 5-pin SOT-23 (Tape and Reel)			

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICTail, REAL ICE, rLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2005-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 9781620771440

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820