To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HAT1036R

Silicon P Channel Power MOS FET
Power Switching

ADE-208-662E (Z)

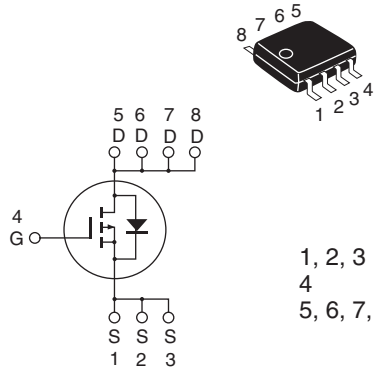
6th. Edition
Dec. 2002

Features

- Low on-resistance
  $R_{DS(on)}$ = 11 m• typ
- Capable of -4 V gate drive
- Low drive current
- High density mounting

Outline

SOP-8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	-12	A
Drain peak current	$I_{D(pulse)}$ Note1	-96	A
Body-drain diode reverse drain current	I_{DR}	-12	A
Channel dissipation	Pch Note2	2.5	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW • 10 s

Electrical Characteristics

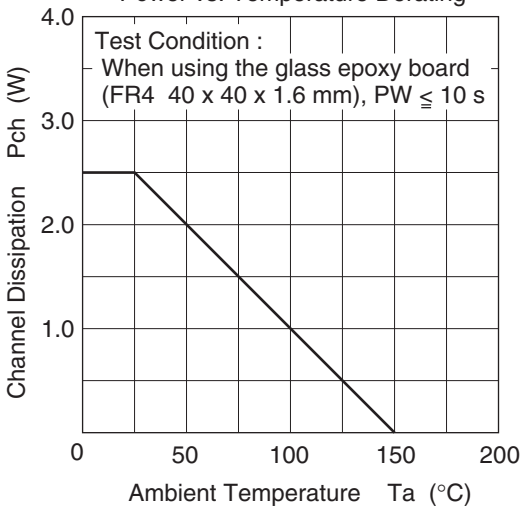
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	I_D = -10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	µA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	-1	µA	V_{DS} = -30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	V_{DS} = -10 V, I_D = -1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	11	14	mΩ	I_D = -6 A, V_{GS} = -10 V [Note1]
	$R_{DS(on)}$	—	21	34	mΩ	I_D = -6 A, V_{GS} = -4 V [Note1]
Forward transfer admittance	$\|y_{fs}\|$	12	20	—	S	I_D = -6 A, V_{DS} = -10 V [Note1]
Input capacitance	Ciss	—	4200	—	pF	V_{DS} = -10 V
Output capacitance	Coss	—	870	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	360	—	pF	f = 1 MHz
Total gate charge	Qg	—	70	—	nc	V_{DD} = -10 V
Gate to source charge	Qgs	—	12	—	nc	V_{GS} = -10 V
Gate to drain charge	Qgd	—	14	—	nc	I_D = -12 A
Turn-on delay time	$t_{d(on)}$	—	120	—	ns	V_{GS} = -4 V, I_D = -6 A
Rise time	t_r	—	350	—	ns	$V_{DD} \cong$ -10 V
Turn-off delay time	$t_{d(off)}$	—	100	—	ns	
Fall time	t_f	—	120	—	ns	
Body–drain diode forward voltage	V_{DF}	—	-0.85	-1.11	V	I_F = -12 A, V_{GS} = 0 [Note1]
Body–drain diode reverse recovery time	t_{rr}	—	55	—	ns	I_F = -12 A, V_{GS} = 0 diF/ dt = 20 A/ µs

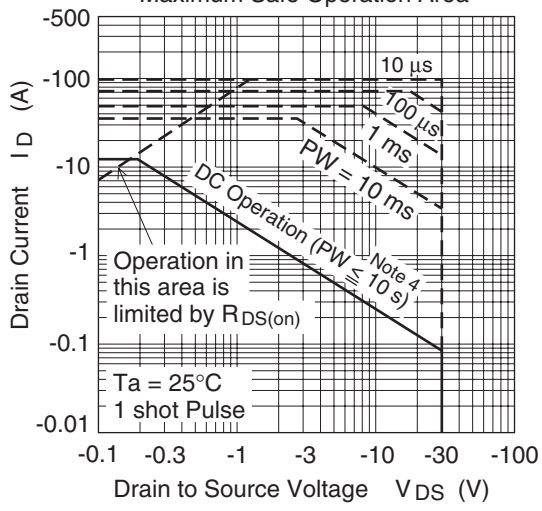
Note: 1. Pulse test

Main Characteristics

Power vs. Temperature Derating

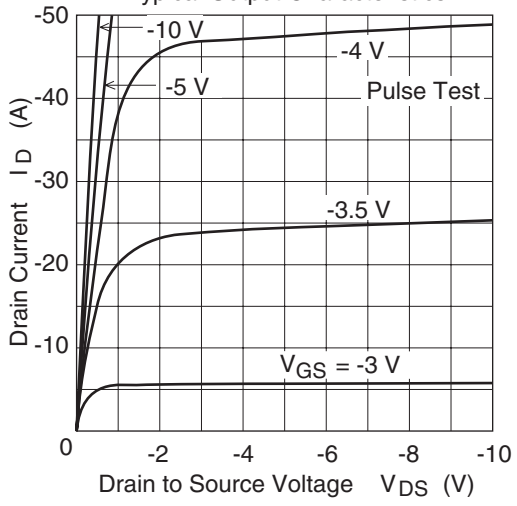


Maximum Safe Operation Area

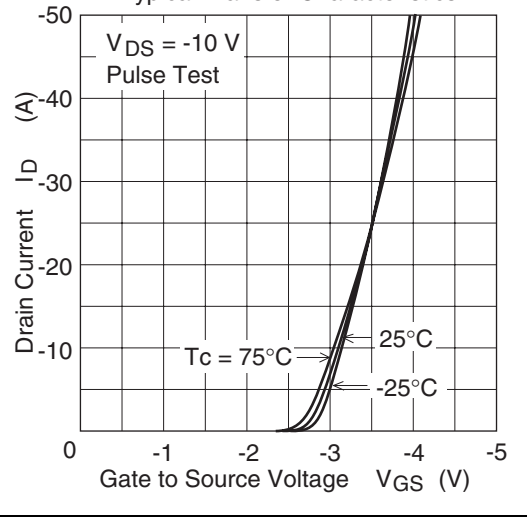


Note 4 :
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)

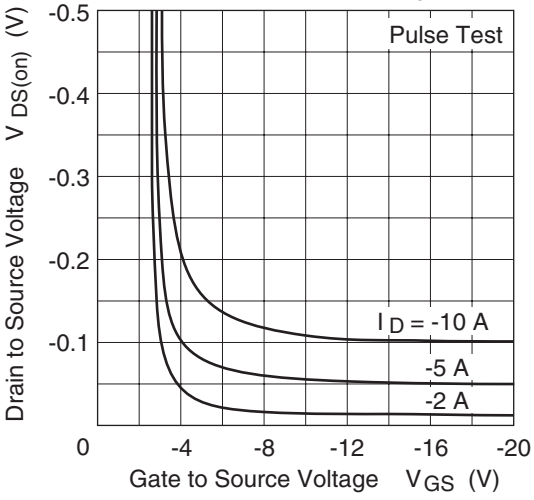
Typical Output Characteristics



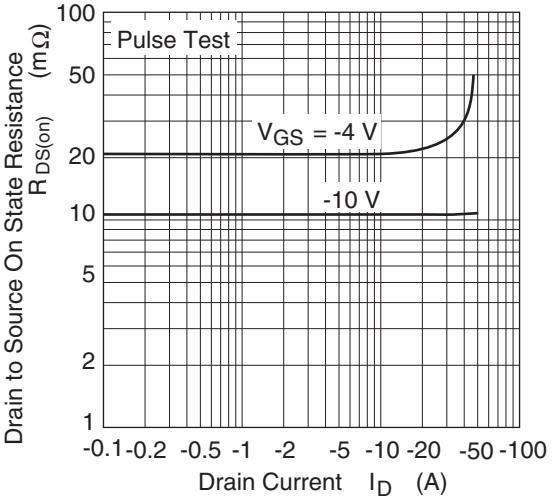
Typical Transfer Characteristics



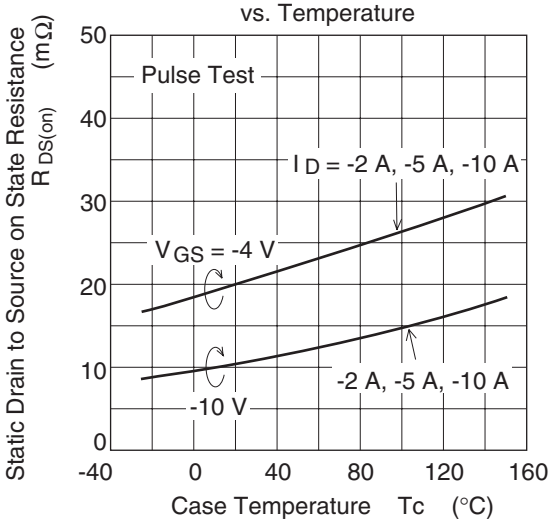
Drain to Source Saturation Voltage vs. Gate to Source Voltage



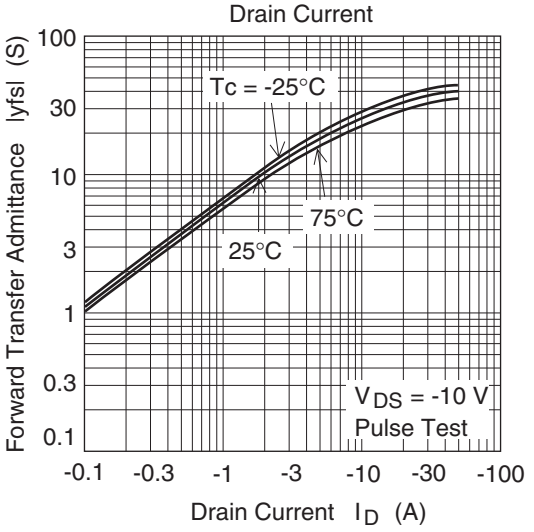
Static Drain to Source on State Resistance vs. Drain Current



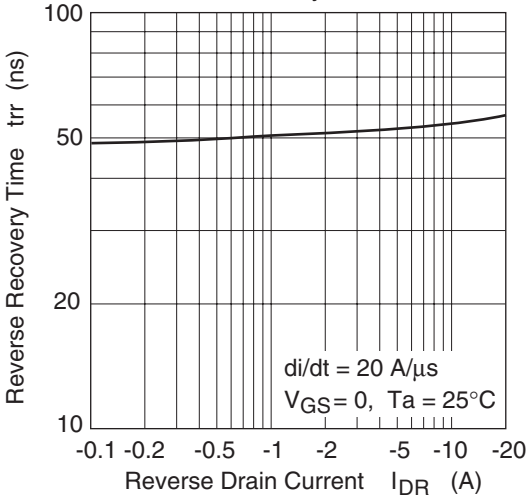
Static Drain to Source on State Resistance vs. Temperature



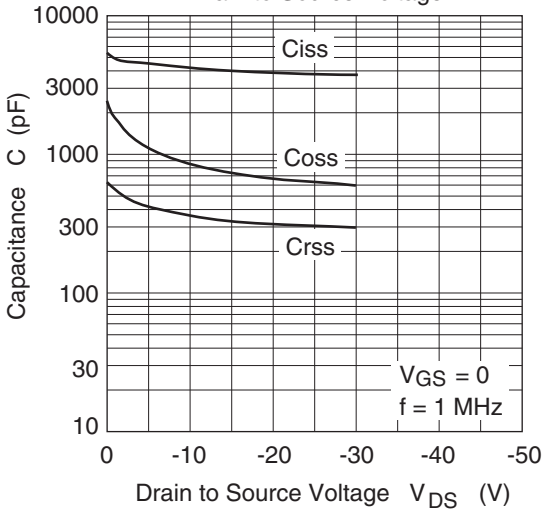
Forward Transfer Admittance vs. Drain Current



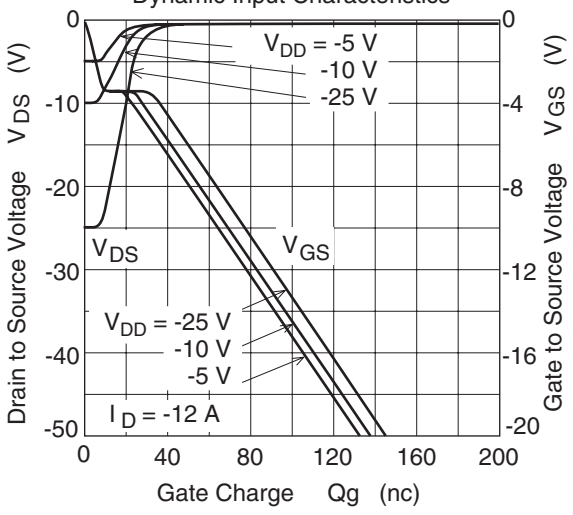
Body-Drain Diode Reverse Recovery Time



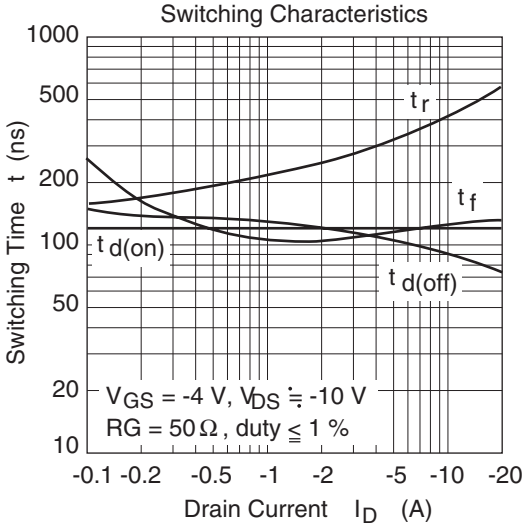
Typical Capacitance vs. Drain to Source Voltage



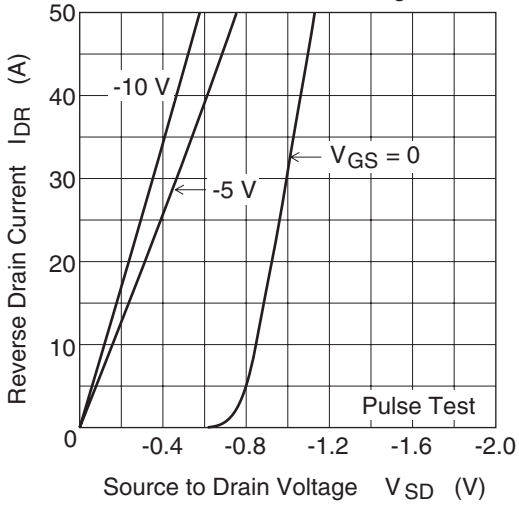
Dynamic Input Characteristics



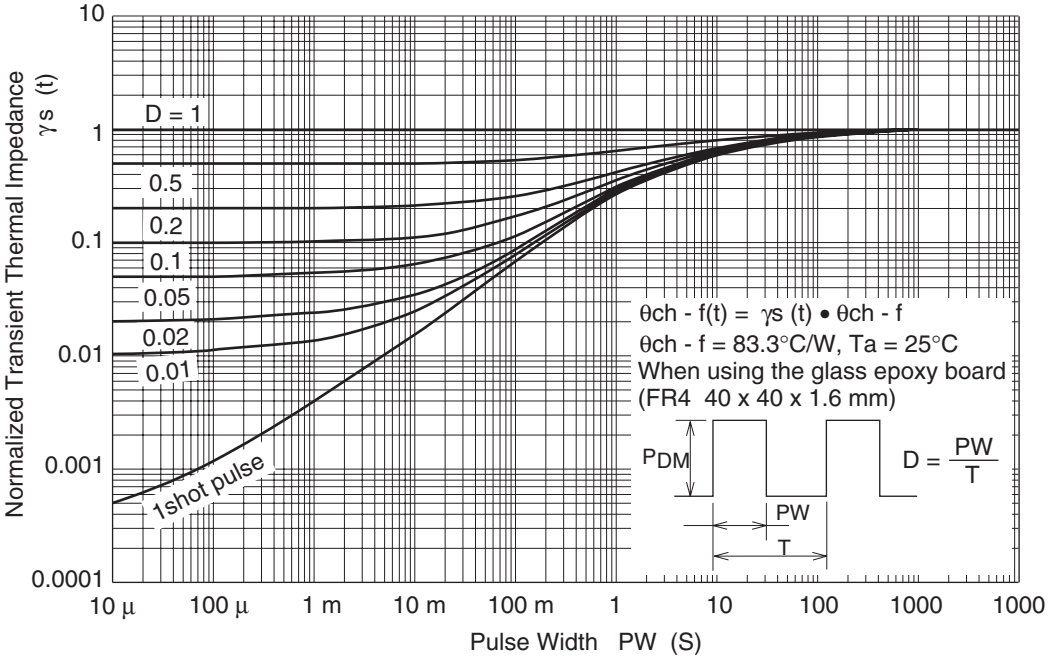
Switching Characteristics



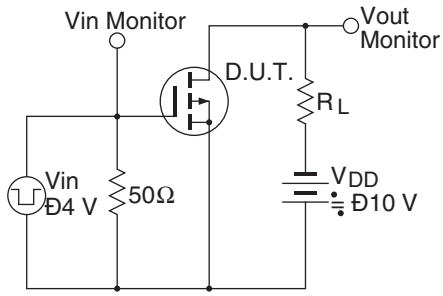
Reverse Drain Current vs.
Source to Drain Voltage



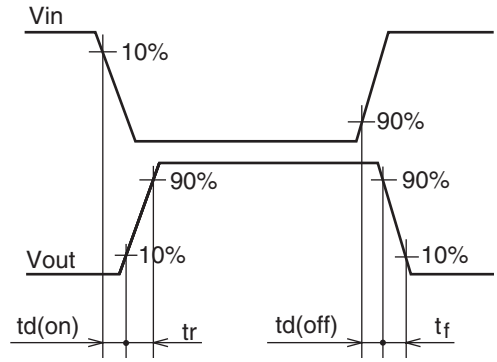
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



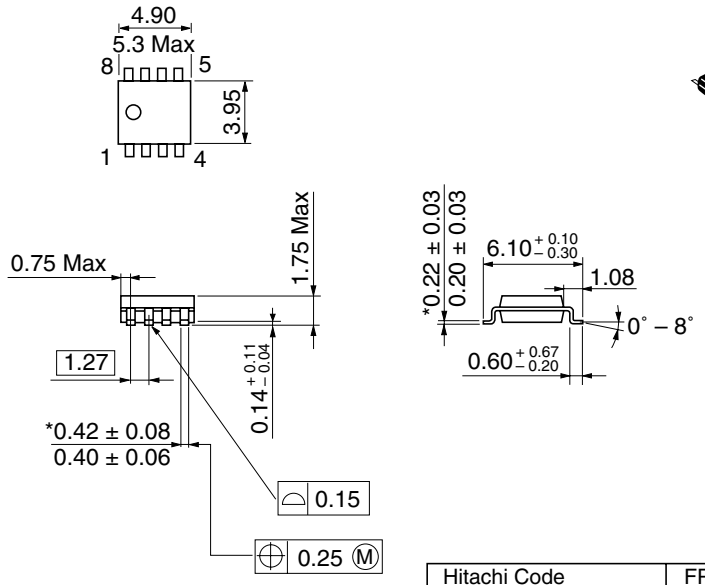
Switching Time Waveforms



Package Dimensions

As of July, 2002

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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