FAIRCHILD SEMICONDUCTOR™

May 1995
Revised April 1999

# 74LCX16543
# Low Voltage 16-Bit Registered Transceiver with 5V Tolerant Inputs and Outputs

## General Description

The LCX16543 contains sixteen non-inverting transceivers containing two sets of D-type registers for temporary storage of data flowing in either direction. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

The LCX16543 is designed for low voltage (2.5V or 3.3V) $V_{CC}$ applications with capability of interfacing to a 5V signal environment.

The LCX16543 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

## Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V $V_{CC}$ specifications provided
- 5.2 ns $t_{PD}$ max ($V_{CC}$ = 3.3V), 20 µA $I_{CC}$ max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA Output Drive ($V_{CC}$ = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human Body Model > 2000V
  - Machine Model > 200V

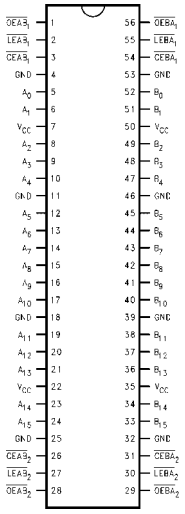
**Note 1:** To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

## Ordering Code:

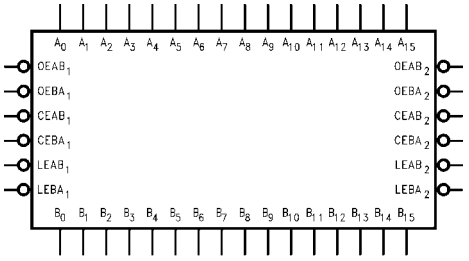
| Order Number | Package Number | Package Description |
|---|---|---|
| 74LCX16543MEA | MS56A | 56-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide |
| 74LCX16543MTD | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram




## Logic Symbol



## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OEAB}_n$ | A-to-B Output Enable Input (Active LOW) |
| $\overline{OEBA}_n$ | B-to-A Output Enable Input (Active LOW) |
| $\overline{CEAB}_n$ | A-to-B Enable Input (Active LOW) |
| $\overline{CEBA}_n$ | B-to-A Enable Input (Active LOW) |
| $\overline{LEAB}_n$ | A-to-B Latch Enable Input (Active LOW) |
| $\overline{LEBA}_n$ | B-to-A Latch Enable Input (Active LOW) |
| $A_0$–$A_{15}$ | A-to-B Data Inputs or B-to-A 3-STATE Outputs |
| $B_0$–$B_{15}$ | B-to-A Data Inputs or A-to-B 3-STATE Outputs |

## Data I/O Control Table

| Inputs | | | Latch Status | Output Buffers |
|---|---|---|---|---|
| $\overline{CEAB}_n$ | $\overline{LEAB}_n$ | $\overline{OEAB}_n$ | (Byte n) | (Byte n) |
| H | X | X | Latched | High Z |
| X | H | X | Latched | — |
| L | L | X | Transparent | — |
| X | X | H | — | High Z |
| L | X | L | — | Driving |

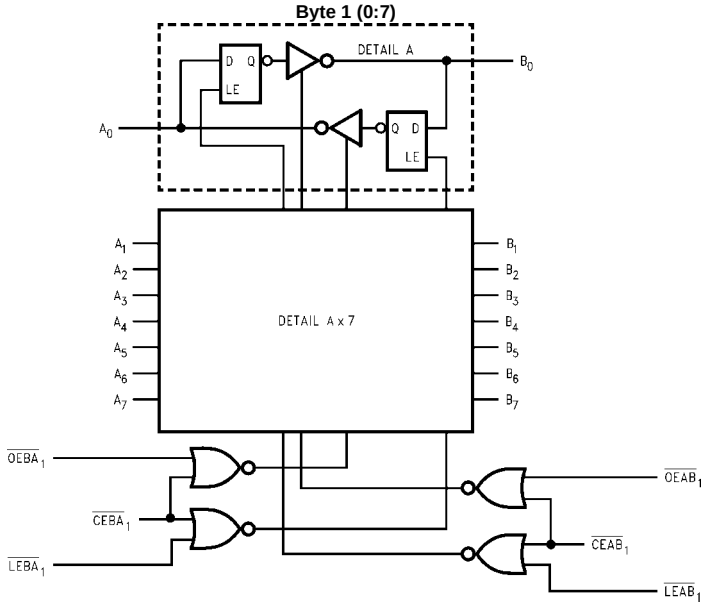
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$

## Functional Description

The LCX16543 contains sixteen non-inverting transceivers with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The following description applies to each byte. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}_n$) input must be LOW in order to enter data from $A_0$–$A_{15}$ or take data from $B_0$–$B_{15}$, as indicated in the Data I/O Control Table. With $\overline{CEAB}_n$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}_n$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}_n$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}_n$ and $\overline{OEAB}_n$ both LOW, the 3-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$ inputs.

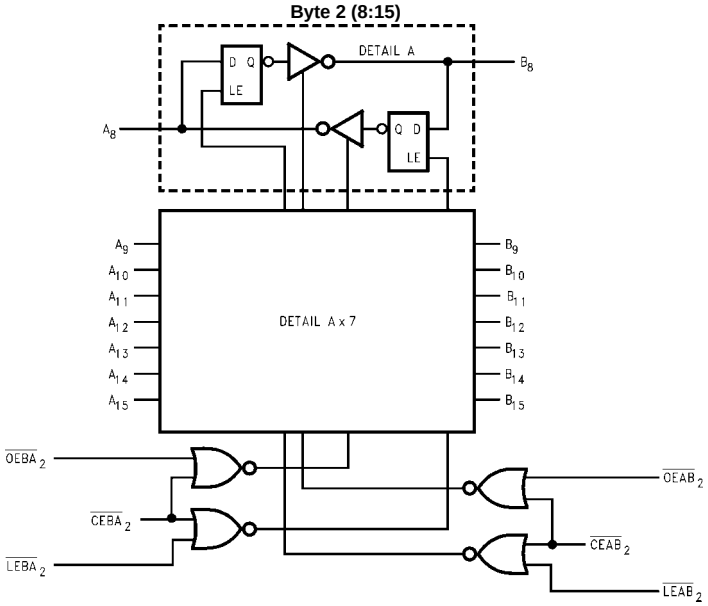
## Logic Diagrams

**Byte 1 (0:7)**




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Byte 2 (8:15)**




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 2)

| Symbol | Parameter | Value | Conditions | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.5 to +7.0 | | V |
| $V_I$ | DC Input Voltage | –0.5 to +7.0 | | V |
| $V_O$ | DC Output Voltage | –0.5 to +7.0<br>–0.5 to $V_{CC}$ + 0.5 | Output in 3-STATE<br>Output in HIGH or LOW State (Note 3) | V |
| $I_{IK}$ | DC Input Diode Current | –50 | $V_I$ < GND | mA |
| $I_{OK}$ | DC Output Diode Current | –50<br>+50 | $V_O$ < GND<br>$V_O$ > $V_{CC}$ | mA |
| $I_O$ | DC Output Source/Sink Current | ±50 | | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | ±100 | | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | ±100 | | mA |
| $T_{STG}$ | Storage Temperature | –65 to +150 | | °C |

## Recommended Operating Conditions (Note 4)

| Symbol | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Operating | 2.0 | 3.6 | V |
| | | Data Retention | 1.5 | 3.6 | |
| $V_I$ | Input Voltage | | 0 | 5.5 | V |
| $V_O$ | Output Voltage | HIGH or LOW State | 0 | $V_{CC}$ | V |
| | | 3-STATE | 0 | 5.5 | |
| $I_{OH}/I_{OL}$ | Output Current | $V_{CC}$ = 3.0V – 3.6V | | ±24 | mA |
| | | $V_{CC}$ = 2.7V – 3.0V | | ±12 | |
| | | $V_{CC}$ = 2.3V – 2.7V | | ±8 | |
| $T_A$ | Free-Air Operating Temperature | | –40 | 85 | °C |
| $\Delta t/\Delta V$ | Input Edge Rate, $V_{IN}$ = 0.8V–2.0V, $V_{CC}$ = 3.0V | | 0 | 10 | ns/V |

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** $I_O$ Absolute Maximum Rating must be observed.

**Note 4:** Unused (inputs or I/Os) must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = –40°C to +85°C | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | | 2.3 – 2.7 | 1.7 | | V |
| | | | 2.7 – 3.6 | 2.0 | | |
| $V_{IL}$ | LOW Level Input Voltage | | 2.3 – 2.7 | | 0.7 | V |
| | | | 2.7 – 3.6 | | 0.8 | |
| $V_{OH}$ | HIGH Level Output Voltage | $I_{OH}$ = –100 µA | 2.3 – 3.6 | $V_{CC}$ – 0.2 | | V |
| | | $I_{OH}$ = –8 mA | 2.3 | 1.8 | | |
| | | $I_{OH}$ = –12 mA | 2.7 | 2.2 | | |
| | | $I_{OH}$ = –18 mA | 3.0 | 2.4 | | |
| | | $I_{OH}$ = –24 mA | 3.0 | 2.2 | | |
| $V_{OL}$ | LOW Level Output Voltage | $I_{OL}$ = 100 µA | 2.3 – 3.6 | | 0.2 | V |
| | | $I_{OL}$ = 8 mA | 2.3 | | 0.6 | |
| | | $I_{OL}$ = 12 mA | 2.7 | | 0.4 | |
| | | $I_{OL}$ = 16 mA | 3.0 | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3.0 | | 0.55 | |
| $I_I$ | Input Leakage Current | 0 ≤ $V_I$ ≤ 5.5V | 2.3 – 3.6 | | ±5.0 | µA |
| $I_{OZ}$ | 3-STATE I/O Leakage | 0 ≤ $V_O$ ≤ 5.5V<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | 2.3 – 3.6 | | ±5.0 | µA |
| $I_{OFF}$ | Power-Off Leakage Current | $V_I$ or $V_O$ = 5.5V | 0 | | 10 | µA |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = -40°C$ to $+85°C$ | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $I_{CC}$ | Quiescent Supply Current | $V_I = V_{CC}$ or GND | 2.3 – 3.6 | | 20 | µA |
| | | $3.6V \le V_I$, $V_O \le 5.5V$ (Note 5) | 2.3 – 3.6 | | ±20 | |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH} = V_{CC} - 0.6V$ | 2.3 – 3.6 | | 500 | µA |

**Note 5:** Outputs in disabled or 3-STATE only.

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $R_L = 500\ \Omega$ | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | $V_{CC} = 3.3V \pm 0.3V$ | | $V_{CC} = 2.7V$ | | $V_{CC} = 2.5V \pm 0.2V$ | | |
| | | $C_L = 50$ pF | | $C_L = 50$ pF | | $C_L = 30$ pF | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{PHL}$ | Propagation Delay | 1.5 | 5.2 | 1.5 | 6.0 | 1.5 | 6.2 | ns |
| $t_{PLH}$ | $A_n$ to $B_n$ or $B_n$ to $A_n$ | 1.5 | 5.2 | 1.5 | 6.0 | 1.5 | 6.2 | |
| $t_{PHL}$ | Propagation Delay | 1.5 | 6.5 | 1.5 | 7.5 | 1.5 | 7.8 | ns |
| $t_{PLH}$ | $\overline{LEBA}_n$ to $A_n$ or $\overline{LEAB}_n$ to $B_n$ | 1.5 | 6.5 | 1.5 | 7.5 | 1.5 | 7.8 | |
| $t_{PZL}$ | Output Enable Time | | | | | | | ns |
| $t_{PZH}$ | $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to $A_n$ or $B_n$ | 1.5 | 6.5 | 1.5 | 7.0 | 1.5 | 8.5 | |
| | $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to $A_n$ or $B_n$ | 1.5 | 6.5 | 1.5 | 7.0 | 1.5 | 8.5 | |
| $t_{PLZ}$ | Output Disable Time | | | | | | | ns |
| $t_{PHZ}$ | $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to $A_n$ or $B_n$ | 1.5 | 6.5 | 1.5 | 7.0 | 1.5 | 7.8 | |
| | $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to $A_n$ or $B_n$ | 1.5 | 6.5 | 1.5 | 7.0 | 1.5 | 7.8 | |
| $t_S$ | Setup Time, HIGH or LOW, Data to $\overline{LEXX}_n$ | 2.5 | | 2.5 | | 3.0 | | ns |
| $t_H$ | Hold Time, HIGH or LOW, Data to $\overline{LEXX}_n$ | 1.5 | | 1.5 | | 2.0 | | ns |
| $t_W$ | Pulse Width, Latch Enable, LOW | 3.0 | | 3.0 | | 3.5 | | ns |
| $t_{OSHL}$ | Output to Output Skew (Note 6) | | 1.0 | | | | | ns |
| $t_{OSLH}$ | | | 1.0 | | | | | |

**Note 6:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$). Parameter guaranteed by design.

## Dynamic Switching Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = 25°C$ | Units |
|---|---|---|---|---|---|
| | | | | Typical | |
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | 0.8 | V |
| | | $C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$ | 2.5 | 0.6 | |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | –0.8 | V |
| | | $C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$ | 2.5 | –0.6 | |

## Capacitance

| Symbol | Parameter | Conditions | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = Open, $V_I = 0V$ or $V_{CC}$ | 7 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$, f = 10 MHz | 20 | pF |

## AC LOADING and WAVEFORMS Generic for LCX Family

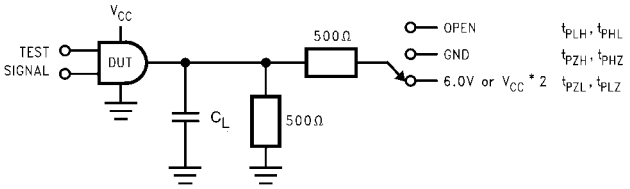
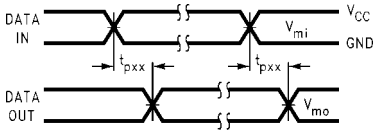
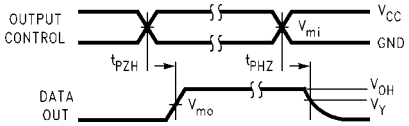



**FIGURE 1. AC Test Circuit ($C_L$ includes probe and jig capacitance)**

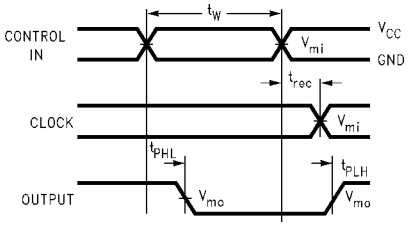
| Test | Switch |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6V at $V_{CC}$ = 3.3 ± 0.3V<br>$V_{CC}$ x 2 at $V_{CC}$ = 2.5 ± 0.2V |
| $t_{PZH}$,$t_{PHZ}$ | GND |



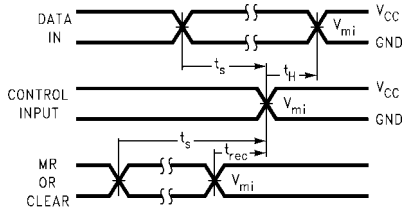

**Waveform for Inverting and Non-Inverting Functions**



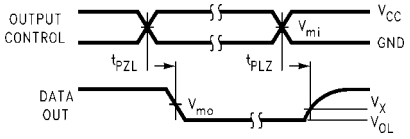

**3-STATE Output High Enable and Disable Times for Logic**



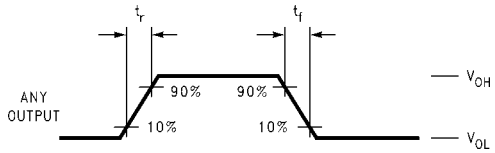

**Propagation Delay. Pulse Width and $t_{rec}$ Waveforms**




**Setup Time, Hold Time and Recovery Time for Logic**




**3-STATE Output Low Enable and Disable Times for Logic**

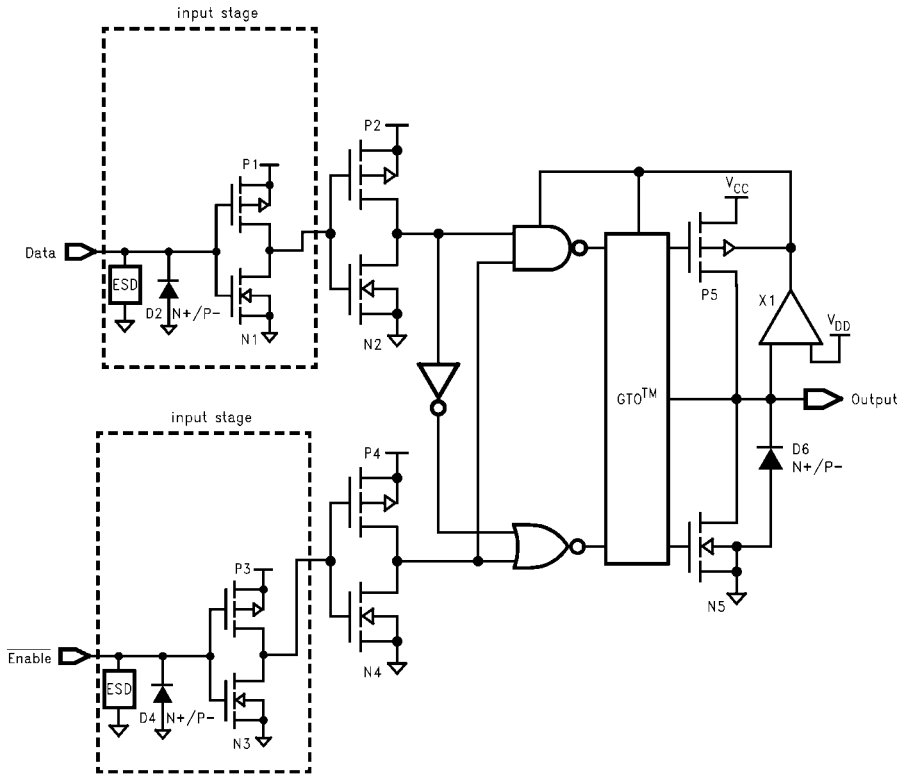



**$t_{rise}$ and $t_{fall}$**

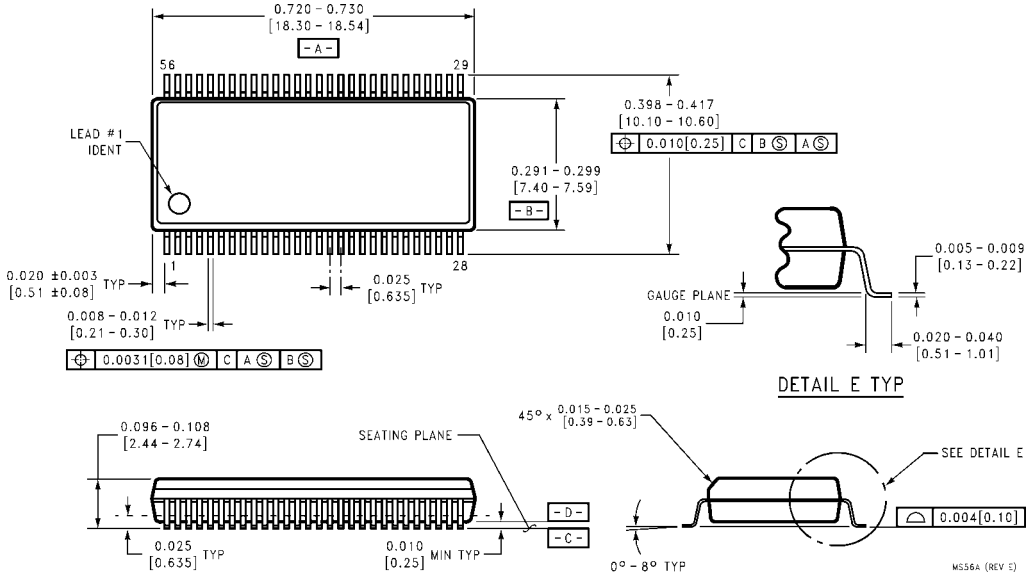
**FIGURE 2. Waveforms**
**(Input Characteristics; f =1MHz, $t_R$ = $t_F$ = 3ns)**

| Symbol | $V_{CC}$ | | |
|---|---|---|---|
| | **3.3V ± 0.3V** | **2.7V** | **2.5V ± 0.2V** |
| $V_{mi}$ | 1.5V | 1.5V | $V_{CC}$/2 |
| $V_{mo}$ | 1.5V | 1.5V | $V_{CC}$/2 |
| $V_x$ | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.15V |
| $V_y$ | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.15V |

## Schematic Diagram Generic for LCX Family

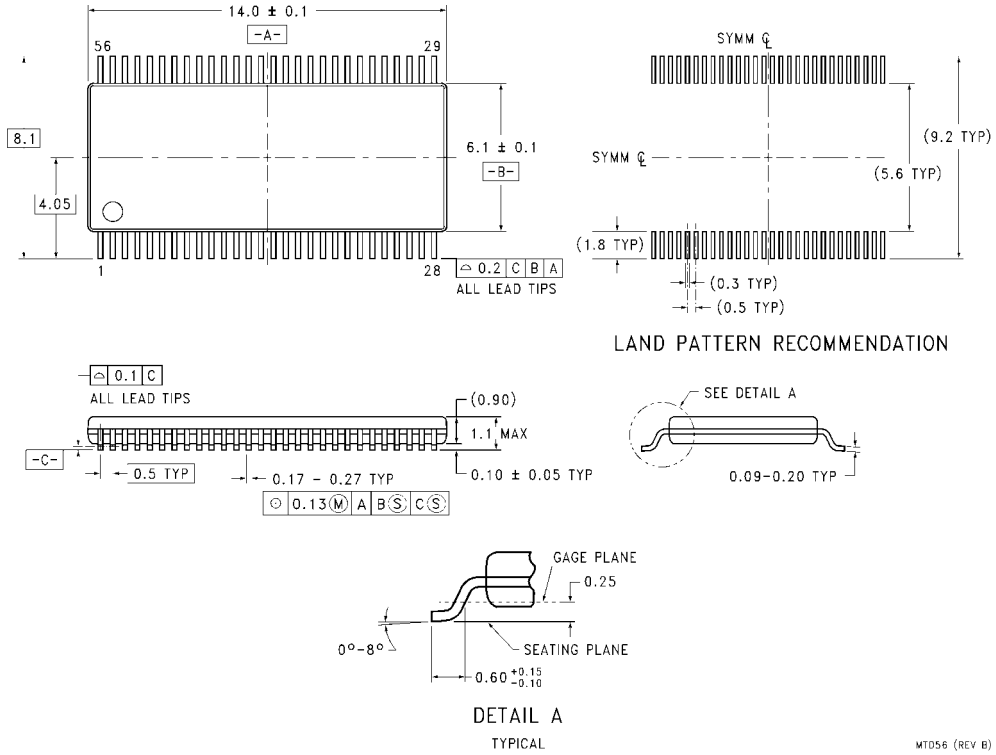


## Physical Dimensions inches (millimeters) unless otherwise noted




**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide**
**Package Number MS56A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD56**

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**www.fairchildsemi.com**