DATA SHEET

74AHC14; 74AHCT14
Hex inverting Schmitt trigger

Product specification
Supersedes data of 1999 Sep 27

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Philips Semiconductors

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FEATURES

- Balanced propagation delays
- Inputs accepts voltages higher than V_{CC}
- For 74AHC only: operates with CMOS input levels
- For 74AHCT only: operates with TTL input levels
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74AHC14 and 74AHCT14 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC14 and 74AHCT14 provide six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	3.2	4.0	ns
C_I	input capacitance	$V_I = V_{CC}$ or GND	3.0	3.0	pF
C_O	output capacitance		4.0	4.0	pF
C_{PD}	power dissipation capacitance per buffer	C_L = 50 pF; f = 1 MHz; notes 1 and 2	10	12	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	nY
L	H
H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74AHC14D	–40 to +125 °C	14	SO14	plastic	SOT108-1
74AHCT14D	–40 to +125 °C	14	SO14	plastic	SOT108-1
74AHC14PW	–40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74AHCT14PW	–40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74AHC14BQ	–40 to +125 °C	14	DHVQFN14	plastic	SOT762-1
74AHCT14BQ	–40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1Y	data output
3	2A	data input
4	2Y	data output
5	3A	data input
6	3Y	data output
7	GND	ground (0 V)
8	4Y	data output
9	4A	data input
10	5Y	data output
11	5A	data input
12	6Y	data output
13	6A	data input
14	V_{CC}	supply voltage

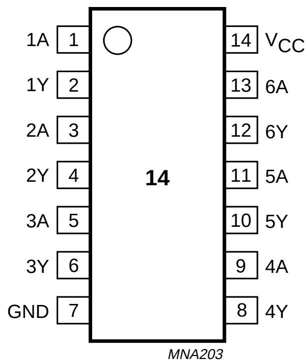
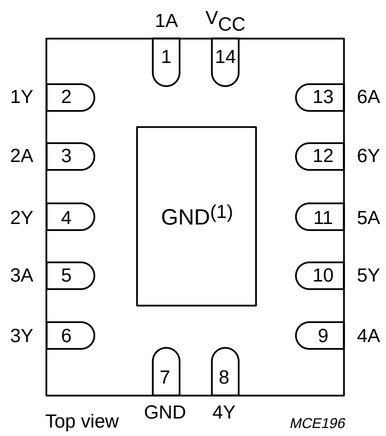


Fig.1 Pin configuration SO14 and TSSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

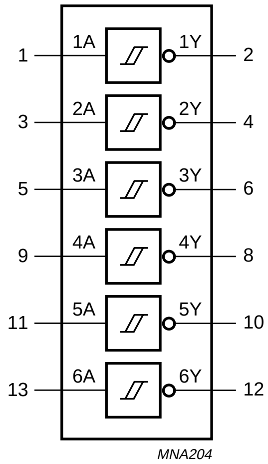


Fig.3 Logic symbol.

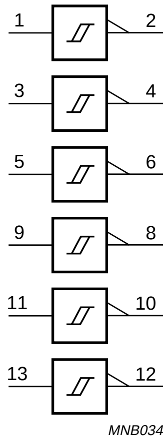


Fig.4 IEC logic symbol.

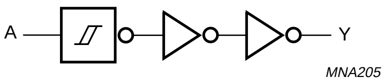


Fig.5 Logic diagram (one Schmitt trigger).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–	+25	–	–	+25	–	°C
			–40	–	+125	–40	–	+125	°C
			–40	–	+125	–40	–	+125	°C

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	input diode current	V_I < –0.5 V; note 1	–	–20	mA
I_{OK}	output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	output source or sink current	–0.5 V < V_O < V_{CC} + 0.5 V	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO14 packages: above 70 °C the value of P_D derates linearly with 8 mW/K.
   For TSSOP14 packages: above 60 °C the value of P_D derates linearly with 5.5 mW/K.
   For DHVQFN14 packages: above 60 °C the value of P_D derates linearly with 4.5 mW/K.

DC CHARACTERISTICS

Type 74AHC14

At recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{T+}	positive going threshold		3.0	–	–	2.2	V
			4.5	–	–	3.15	V
			5.5	–	–	3.85	V
V_{T-}	negative going threshold		3.0	0.9	–	–	V
			4.5	1.35	–	–	V
			5.5	1.65	–	–	V
V_H	hysteresis (V_{T+} – V_{T-})		3.0	0.3	–	1.2	V
			4.5	0.4	–	1.4	V
			5.5	0.5	–	1.6	V
V_{OH}	HIGH-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = –50 µA	2.0	1.9	2.0	–	V
			3.0	2.9	3.0	–	V
			4.5	4.4	4.5	–	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –4.0 mA	3.0	2.58	–	–	V
		I_O = –8.0 mA	4.5	3.94	–	–	V
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = 50 µA	2.0	–	0	0.1	V
			3.0	–	0	0.1	V
			4.5	–	0	0.1	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 4.0 mA	3.0	–	–	0.36	V
		I_O = 8.0 mA	4.5	–	–	0.36	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	5.5	–	–	2.0	µA
C_I	input capacitance			–	3	10	pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 to +85 °C							
V_{T+}	positive going threshold		3.0	–	–	2.2	V
			4.5	–	–	3.15	V
			5.5	–	–	3.85	V
V_{T-}	negative going threshold		3.0	0.9	–	–	V
			4.5	1.35	–	–	V
			5.5	1.65	–	–	V
V_H	hysteresis ($V_{T+} - V_{T-}$)		3.0	0.3	–	1.2	V
			4.5	0.4	–	1.4	V
			5.5	0.5	–	1.6	V
V_{OH}	HIGH-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = –50 μA	2.0	1.9	–	–	V
			3.0	2.9	–	–	V
			4.5	4.4	–	–	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –4.0 mA	3.0	2.48	–	–	V
		I_O = –8.0 mA	4.5	3.8	–	–	V
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = 50 μA	2.0	–	–	0.1	V
			3.0	–	–	0.1	V
			4.5	–	–	0.1	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 4.0 mA	3.0	–	–	0.44	V
		I_O = 8.0 mA	4.5	–	–	0.44	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	5.5	–	–	20	μA
C_I	input capacitance			–	–	10	pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 to +125 °C							
V_{T+}	positive going threshold		3.0	–	–	2.2	V
			4.5	–	–	3.15	V
			5.5	–	–	3.85	V
V_{T-}	negative going threshold		3.0	0.9	–	–	V
			4.5	1.35	–	–	V
			5.5	1.65	–	–	V
V_H	hysteresis ($V_{T+} - V_{T-}$)		3.0	0.25	–	1.2	V
			4.5	0.35	–	1.4	V
			5.5	0.45	–	1.6	V
V_{OH}	HIGH-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = –50 μA	2.0	1.9	–	–	V
			3.0	2.9	–	–	V
			4.5	4.4	–	–	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –4.0 mA	3.0	2.40	–	–	V
		I_O = –8.0 mA	4.5	3.70	–	–	V
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = 50 μA	2.0	–	–	0.1	V
			3.0	–	–	0.1	V
			4.5	–	–	0.1	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 4.0 mA	3.0	–	–	0.55	V
		I_O = 8.0 mA	4.5	–	–	0.55	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	2.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	5.5	–	–	40	μA
C_I	input capacitance			–	–	10	pF

Type 74AHCT14

At recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{T+}	positive going threshold		4.5	–	–	1.9	V
			5.5	–	–	2.1	V
V_{T-}	negative going threshold		4.5	0.5	–	–	V
			5.5	0.6	–	–	V
V_H	hysteresis (V_{T+} – V_{T-})		4.5	0.4	–	1.4	V
			5.5	0.4	–	1.5	V
V_{OH}	HIGH-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = –50 μA	4.5	4.4	4.5	–	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = –8.0 mA	4.5	3.94	–	–	V
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = 50 μA	4.5	–	0	0.1	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = 8 mA	4.5	–	–	0.36	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	5.5	–	–	2.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 2.1 V other inputs at V_{CC} or GND; I_O = 0	4.5 to 5.5	–	–	1.35	mA
C_I	input capacitance			–	3	10	pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 to +85 °C							
V_{T+}	positive going threshold		4.5	–	–	1.9	V
			5.5	–	–	2.1	V
V_{T-}	negative going threshold		4.5	0.5	–	–	V
			5.5	0.6	–	–	V
V_H	hysteresis ($V_{T+} – V_{T-}$)		4.5	0.4	–	1.4	V
			5.5	0.4	–	1.5	V
V_{OH}	HIGH-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = –50 µA	4.5	4.4	–	–	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = –8.0 mA	4.5	3.8	–	–	V
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = 50 µA	4.5	–	–	0.1	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = 8 mA	4.5	–	–	0.44	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	5.5	–	–	20	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 2.1 V other inputs at V_{CC} or GND; I_O = 0	4.5 to 5.5	–	–	1.5	mA
C_I	input capacitance			–	–	10	pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 to +125 °C							
V_{T+}	positive going threshold		4.5	–	–	1.9	V
			5.5	–	–	2.1	V
V_{T-}	negative going threshold		4.5	0.5	–	–	V
			5.5	0.6	–	–	V
V_H	hysteresis ($V_{T+} – V_{T-}$)		4.5	0.35	–	1.4	V
			5.5	0.35	–	1.5	V
V_{OH}	HIGH-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = –50 µA	4.5	4.4	–	–	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = –8.0 mA	4.5	3.7	–	–	V
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL}; I_O = 50 µA	4.5	–	–	0.1	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = 8 mA	4.5	–	–	0.55	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	2.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	5.5	–	–	40	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 2.1 V other inputs at V_{CC} or GND; I_O = 0	4.5 to 5.5	–	–	1.5	mA
C_I	input capacitance			–	–	10	pF

AC CHARACTERISTICS

Type 74AHC14

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

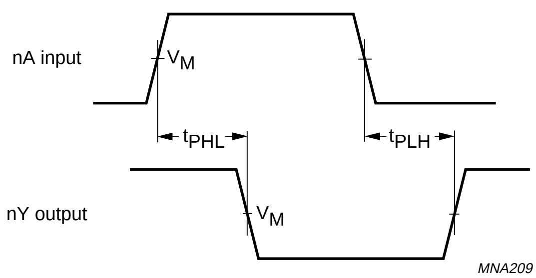
SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	C_L (pF)	V_{CC} (V)				
T_{amb} = 25 °C								
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	15	3.3	–	4.3	–	ns
			15	3.0 to 3.6	–	–	12.8	ns
			50	3.3	–	5.8	–	ns
			50	3.0 to 3.6	–	–	16.3	ns
			15	5.0	–	3.2	–	ns
			15	4.5 to 5.5	–	–	8.6	ns
			50	5.0	–	4.2	–	ns
			50	4.5 to 5.5	–	–	10.6	ns
T_{amb} = –40 to +85 °C								
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	15	3.0 to 3.6	1.0	–	15.0	ns
			50	3.0 to 3.6	1.0	–	18.0	ns
			15	4.5 to 5.5	1.0	–	10.0	ns
			50	4.5 to 5.5	1.0	–	12.0	ns
T_{amb} = –40 to +125 °C								
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	15	3.0 to 3.6	1.0	–	16.0	ns
			50	3.0 to 3.6	1.0	–	20.5	ns
			15	4.5 to 5.5	1.0	–	11.0	ns
			50	4.5 to 5.5	1.0	–	13.5	ns

Type 74AHCT14

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

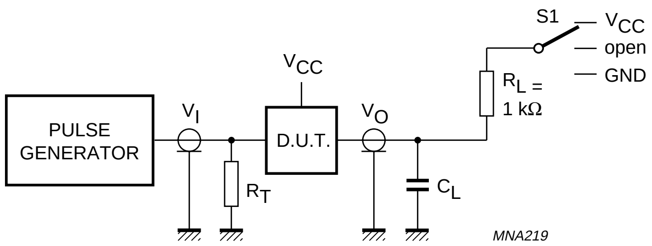
SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	C_L (pF)	V_{CC} (V)				
T_{amb} = 25 °C								
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	15	5.0	–	4.0	–	ns
			15	4.5 to 5.5	–	–	7.0	ns
			50	5.0	–	5.4	–	ns
			50	4.5 to 5.5	–	–	8.0	ns
T_{amb} = −40 to +85 °C								
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	15	4.5 to 5.5	1.0	–	8.0	ns
			50	4.5 to 5.5	1.0	–	9.0	ns
T_{amb} = −40 to +125 °C								
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	15	4.5 to 5.5	1.0	–	9.0	ns
			50	4.5 to 5.5	1.0	–	10.0	ns

AC WAVEFORMS



FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
74AHC14	GND to V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74AHCT14	GND to 3.0 V	1.5 V	$0.5V_{CC}$

Fig.6 The input (nA) to output (nY) propagation delays.



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

TRANSFER CHARACTERISTIC WAVEFORMS

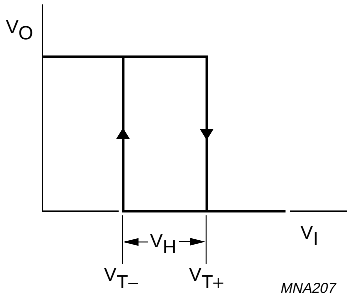
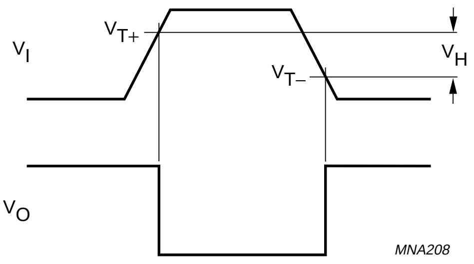
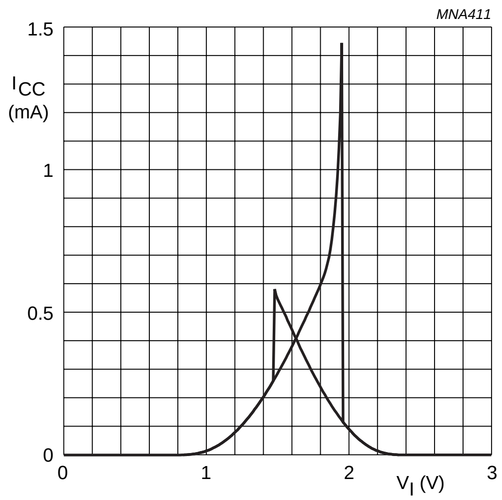


Fig.8 Transfer characteristic.



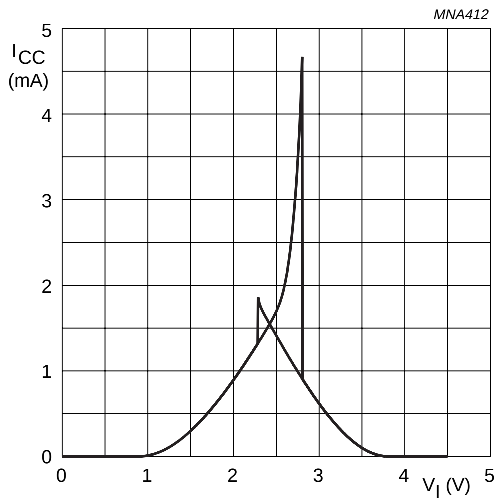
V_{T+} and V_{T-} are between limits of 20% and 70%.

Fig.9 The definition of V_{T+}, V_{T-} and V_H.



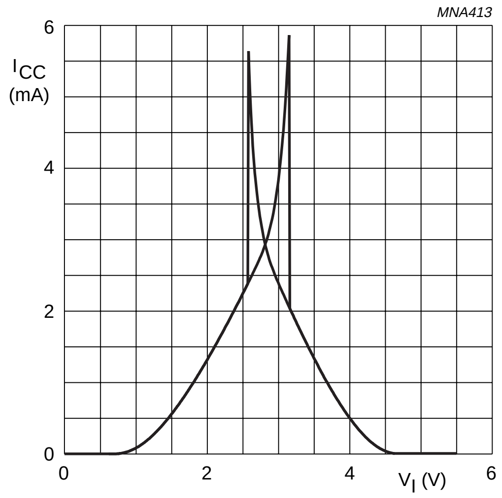
V_{CC} = 3.0 V.

Fig.10 Typical 74AHC transfer characteristic.



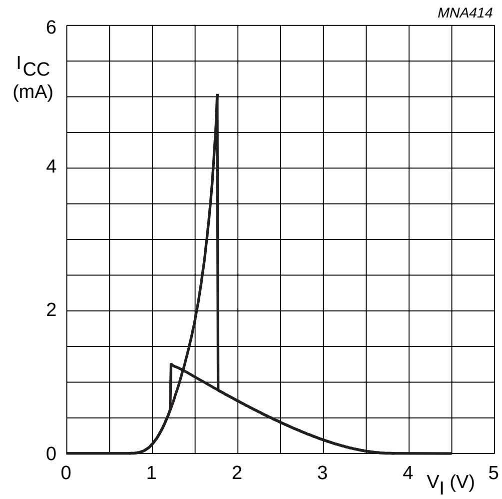
V_{CC} = 4.5 V.

Fig.11 Typical 74AHC transfer characteristic.



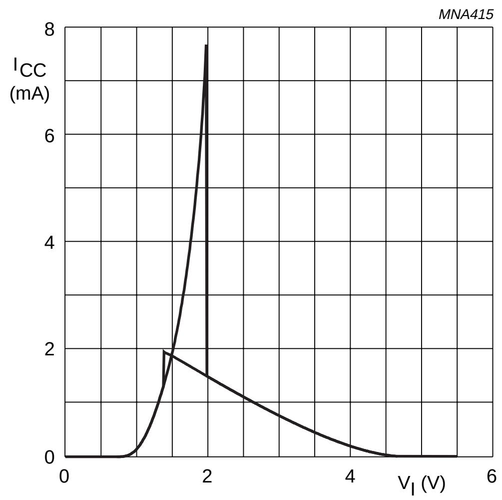
V_{CC} = 5.5 V.

Fig.12 Typical AHC transfer characteristic.



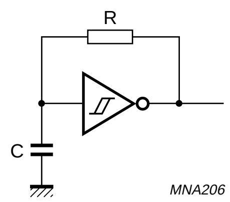
V_{CC} = 4.5 V.

Fig.13 Typical 74AHCT transfer characteristic.



V_{CC} = 5.5 V.

Fig.14 Typical 74AHCT transfer characteristics.



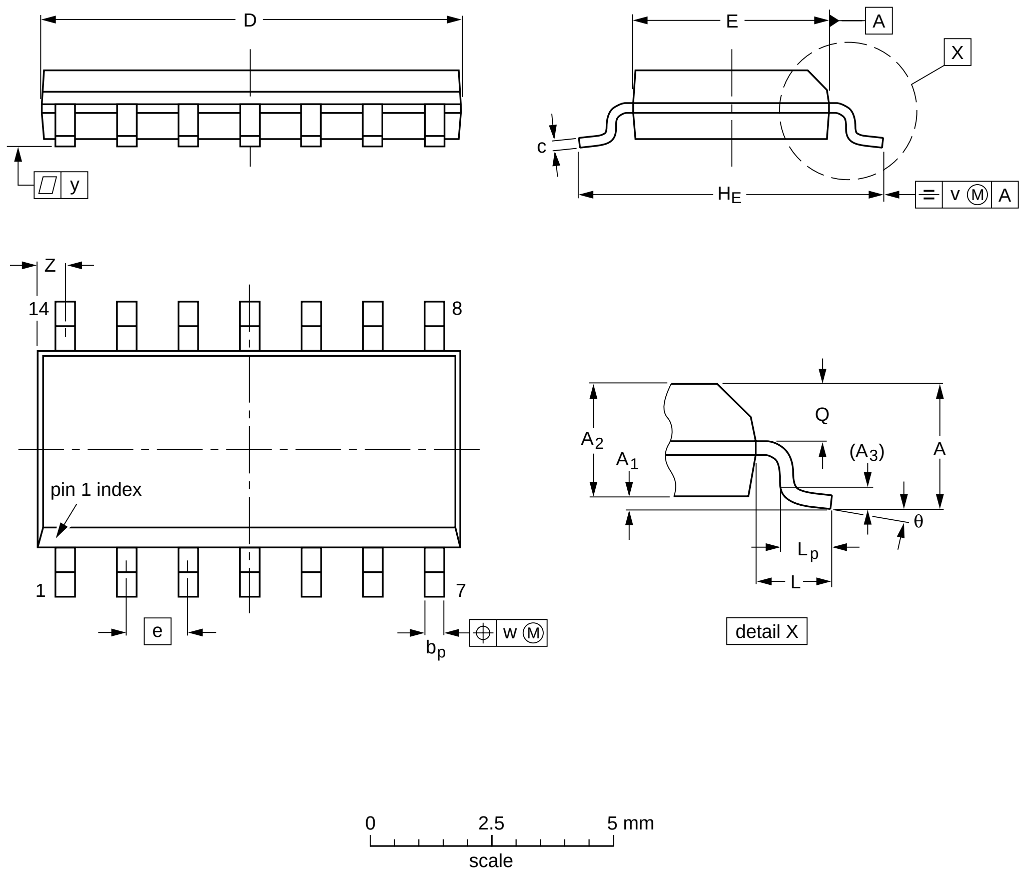
74AHC14: $f = \frac{1}{T} \cong \frac{1}{0.55RC}$

74AHCT14: $f = \frac{1}{T} \cong \frac{1}{0.60RC}$

Fig.15 Relaxation oscillator.

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

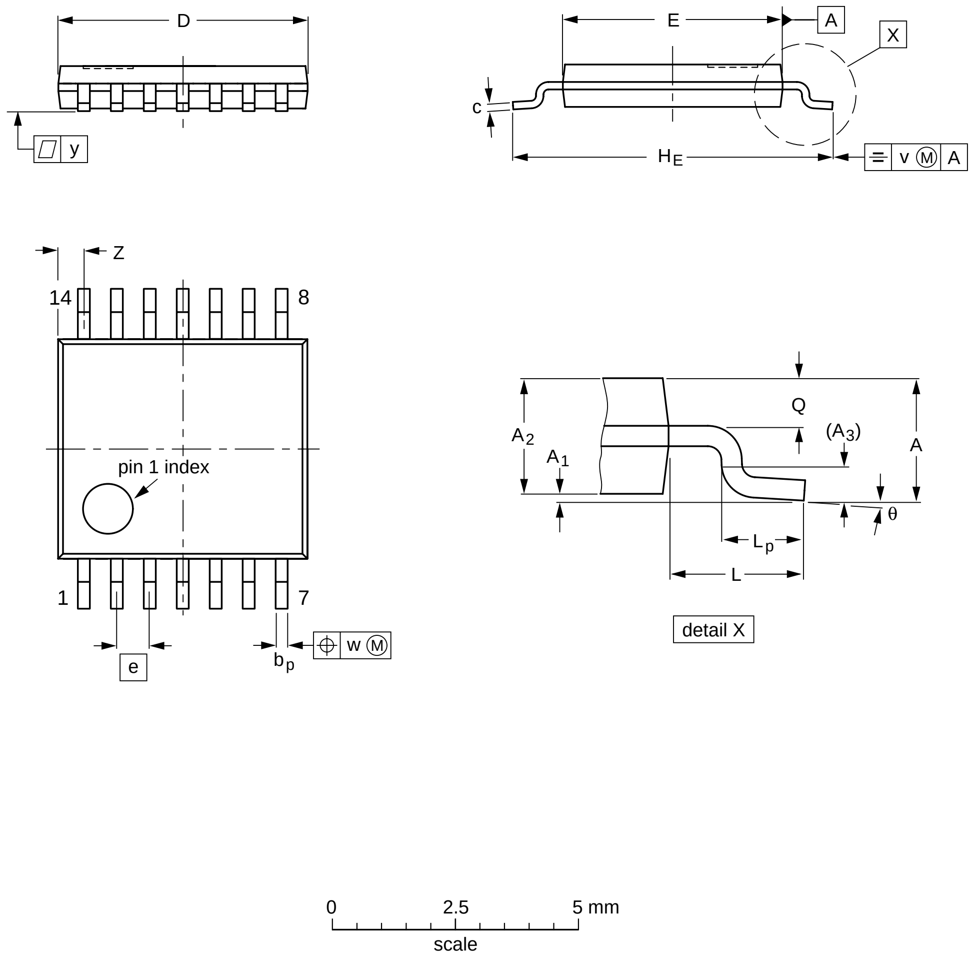
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

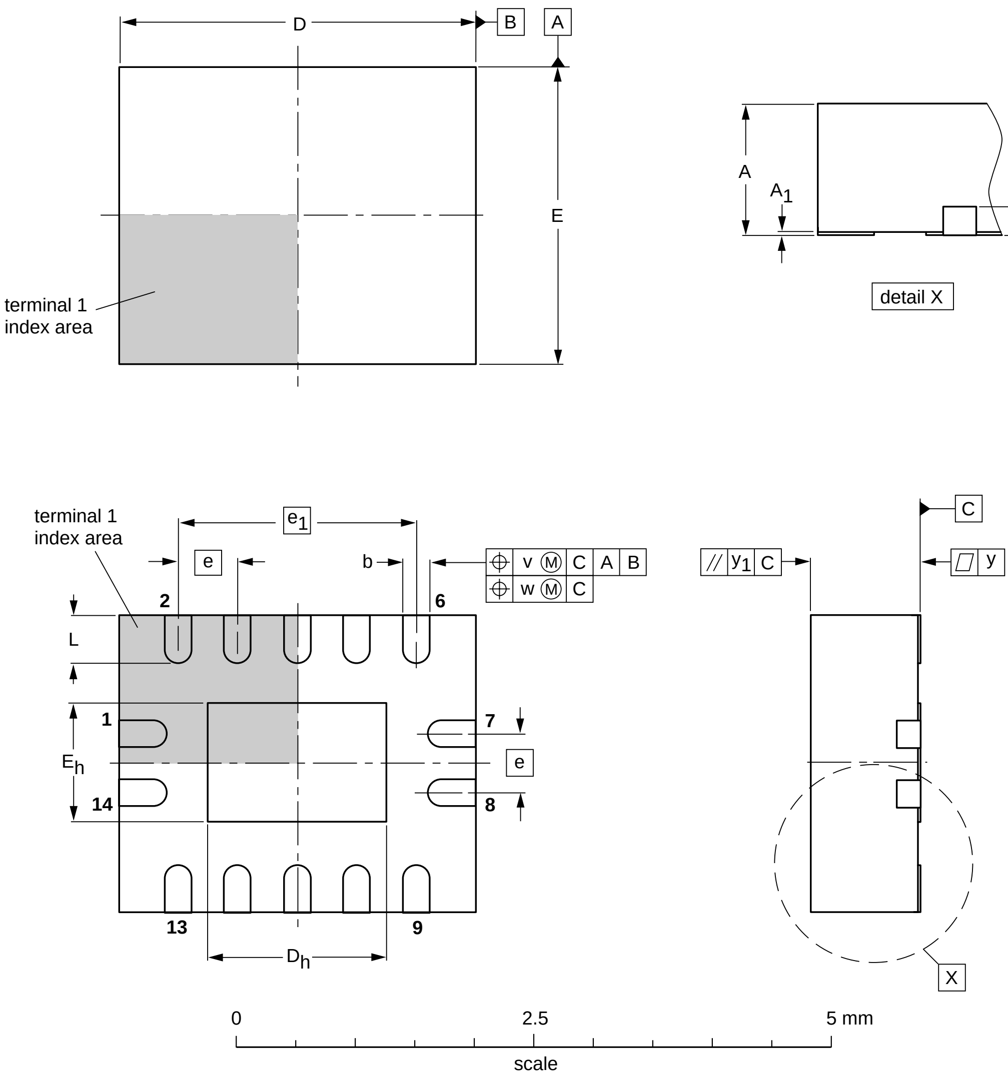
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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