LP2982 Micropower 50 mA Ultra Low-Dropout Regulator in SOT-23 Package

Check for Samples: LP2982

FEATURES

- **Ultra Low Dropout Voltage**
- **Ensured 50 mA Output Current**
- **Typical Dropout Voltage 180 mV @ 80 mA**
- **Requires Minimum External Components**
- **< 1 μA Quiescent Current when Shutdown**
- **Low Ground Pin Current at All Loads**
- **Output Voltage Accuracy 1.0% (A Grade)**
- **High Peak Current Capability (150 mA Typical)**
- **Wide Supply Voltage Range (16V Max)**
- **Low Z_{OUT} 0.3Ω Typical (10 Hz to 1 MHz)**
- **Over-Temperature/Over-Current Protection**
- **−40°C to +125°C Junction Temperature Range**

APPLICATIONS

- **Cellular Phone**
- **Palmtop/Laptop Computer**
- **Personal Digital Assistant (PDA)**
- **Camcorder, Personal Stereo, Camera**

DESCRIPTION

The LP2982 is a 50 mA, fixed-output voltage regulator designed to provide ultra low dropout and lower noise in battery powered applications.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2982 delivers unequaled performance in all specifications critical to battery-powered designs:

Dropout Voltage: Typically 120 mV @ 50 mA load, and 7 mV @ 1 mA load.

Ground Pin Current: Typically 375 μA @ 50 mA load, and 80 μA @ 1 mA load.

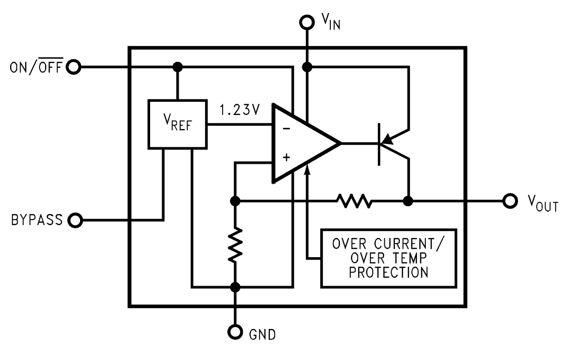
Sleep Mode: Less than 1 μA quiescent current when on/off pin is pulled low.

Precision Output: 1.0% tolerance output voltages available (A grade).

Low Noise: By adding an external bypass capacitor, output noise can be reduced to 30 μV (typical).

Four output voltage versions, from 3.0V to 5.0V, are available as standard products.

Block Diagram



Connection Diagram

Top View

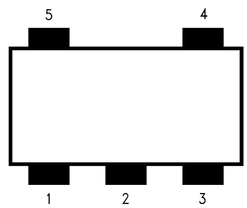


Figure 1. 5-Lead Small Outline SOT-23 Package
See Package Number DBV0005A

Pin Descriptions

Name	Pin Number	Function
V_{IN}	1	Input Voltage
GND	2	Common Ground (device substrate)
ON/OFF	3	Logic high enable input
BYPASS	4	Bypass capacitor for low noise operation
V_{OUT}	5	Regulated output voltage

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)]

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 5 sec.)	260°C
ESD Rating[(3)]	2 kV
Power Dissipation[(4)]	Internally Limited
Input Supply Voltage (Survival)	−0.3V to +16V
Input Supply Voltage (Operating)	2.1V to +16V
Shutdown Input Voltage (Survival)	−0.3V to +16V
Output Voltage (Survival[(5)])	−0.3V to +9V
I_{OUT} (Survival)	Short Circuit Protected
Input-Output Voltage (Survival[(6)])	−0.3V to +16V

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The ESD rating of pins 3 and 4 for the SOT-23 package, or pins 5 and 2 for the DSBGA package, is 1 kV.
(4) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P(MAX) = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$ The value of θ_{JA} for the SOT-23 package is 220°C/W. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2982 output must be diode-clamped to ground.
(6) The output PNP structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Reversing the polarity from V_{IN} to V_{OUT} will turn on this diode. (See REVERSE CURRENT PATH.)

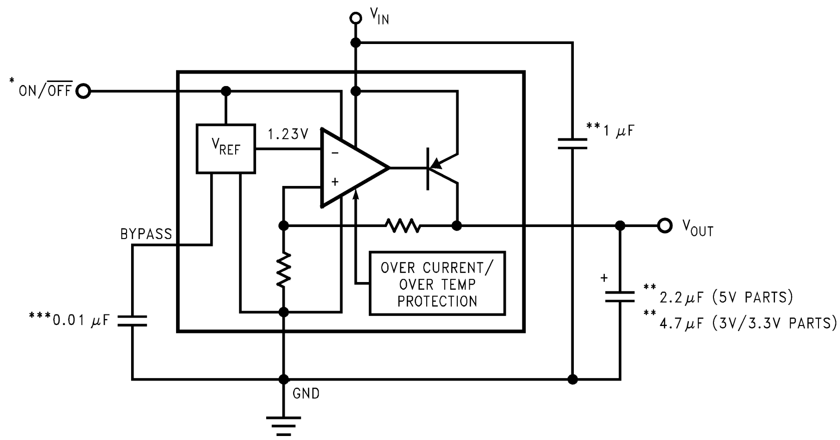
Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 1 mA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, $V_{ON/OFF}$ = 2V.

Symbol	Parameter	Conditions	Typ	LP2982AI-X.X(1)		LP2982I-X.X(1)		Units
				Min	Max	Min	Max	
ΔV_O	Output Voltage Tolerance	I_L = 1 mA		−1.0	+1.0	−1.5	+1.5	$\%V_{NOM}$
		1 mA < I_L < 50 mA		−1.5 **−2.0**	+1.5 **+2.0**	−2.0 **−3.5**	+2.0 **+3.5**	
$\frac{\Delta V_O}{\Delta V_{IN}}$	Output Voltage Line Regulation	$V_{O(NOM)} + 1V \le V_{IN} \le 16V$	0.007		0.014 **0.032**		0.014 **0.032**	%/V
$V_{IN}–V_O$	Dropout Voltage(2)	I_L = 0	1		3 **5**		3 **5**	mV
		I_L = 1 mA	7		10 **15**		10 **15**	
		I_L = 10 mA	40		60 **90**		60 **90**	
		I_L = 50 mA	120		150 **225**		150 **225**	
I_{GND}	Ground Pin Current	I_L = 0	65		95 **125**		95 **125**	µA
		I_L = 1 mA	80		110 **170**		110 **170**	
		I_L = 10 mA	140		220 **460**		220 **460**	
		I_L = 50 mA	375		600 **1200**		600 **1200**	
		$V_{ON/OFF}$ < 0.3V $V_{ON/OFF}$ < 0.15V	0.01 **0.10**		0.8 **2.0**		0.8 **2.0**	
$V_{ON/OFF}$	ON/OFF Input Voltage(3)	High = O/P ON	1.4	**1.6**		**1.6**		V
		Low = O/P OFF	0.55		**0.15**		**0.15**	
$I_{ON/OFF}$	ON/OFF Input Current	$V_{ON/OFF}$ = 0	0.01		**−2**		**−2**	µA
		$V_{ON/OFF}$ = 5V	5		**15**		**15**	
$I_{O(PK)}$	Peak Output Current	$V_{OUT} \ge V_{O(NOM)}$ − 5%	150	100		100		mA
$V_{IN}–V_O$	Dropout Voltage	I_L = 80 mA	180		225 **325**		225 **325**	mV
I_{GND}	Ground Pin Current	I_L = 80 mA	525		750 **1400**		750 **1400**	µA
e_n	Output Noise Voltage (RMS)	BW = 300 Hz–50 kHz, C_{OUT} = 10 µF C_{BYPASS} = 0.01 µF	30					µV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Ripple Rejection	f = 1 kHz C_{OUT} = 10 µF	45					dB
$I_{O(MAX)}$	Short Circuit Current	R_L = 0 (Steady State)(4)	150					mA

(1) Temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential.
(3) The ON/OFF inputs must be properly driven to prevent possible misoperation. For details, refer to Application Hints.
(4) See Typical Performance Characteristics curve(s).

Typical Application Circuit



*ON/OFF input must be actively terminated. Tie to V_{IN} if this function is not to be used.
**Minimum capacitance is shown to insure stability over full load current range. More capacitance provides superior dynamic performance (see Application Hints).
***See Application Hints.

Typical Performance Characteristics

Unless otherwise specified: T_A = 25°C, $V_{IN} = V_{O(NOM)}$ + 1V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

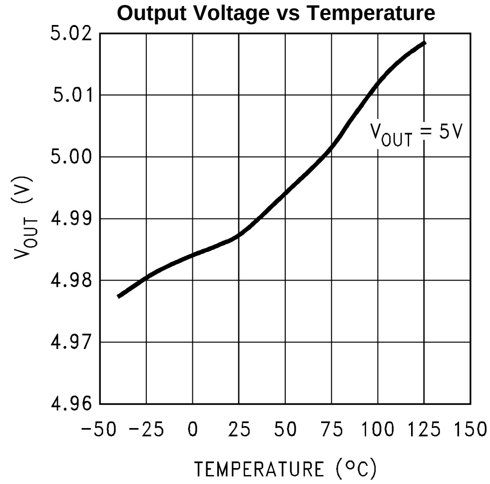


Figure 2.

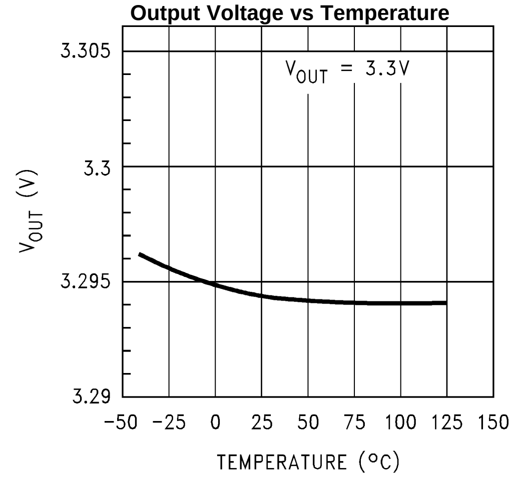


Figure 3.

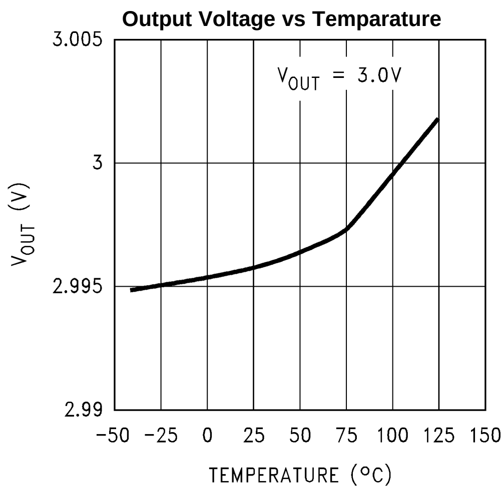


Figure 4.

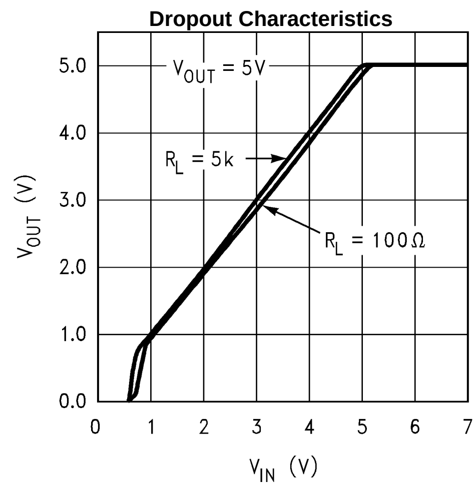


Figure 5.

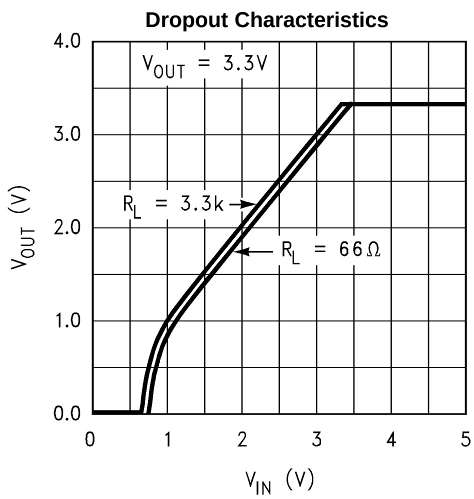


Figure 6.

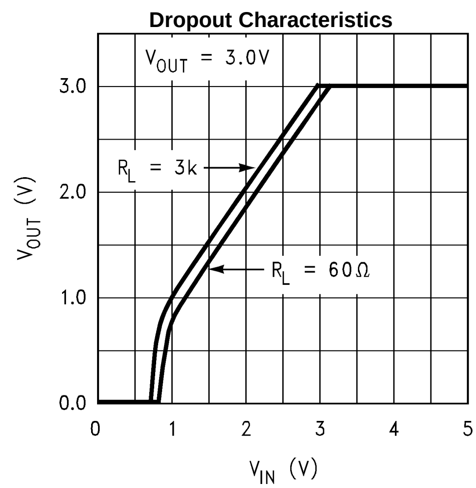


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, $V_{IN} = V_{O(NOM)}$ + 1V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

Dropout Voltage vs Temperature

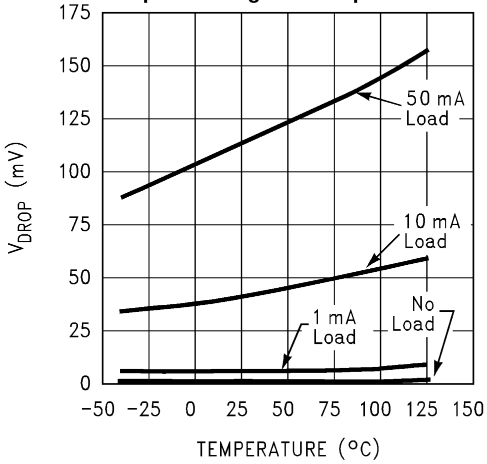


Figure 8.

Dropout Voltage vs Load Current

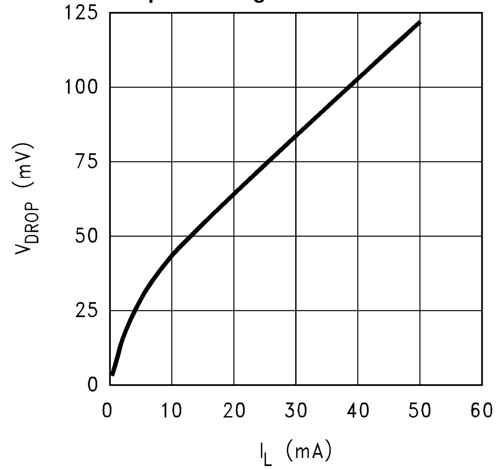


Figure 9.

Ground Pin Current vs Temperature

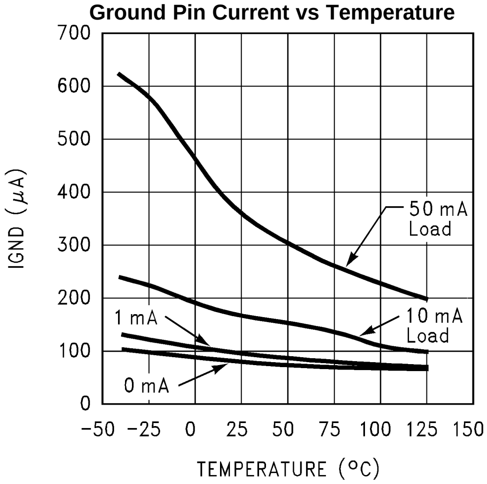


Figure 10.

Ground Pin Current vs Load Current

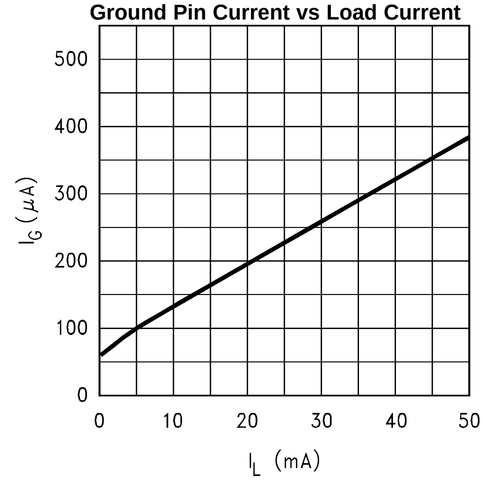


Figure 11.

Input Current vs V_{IN}

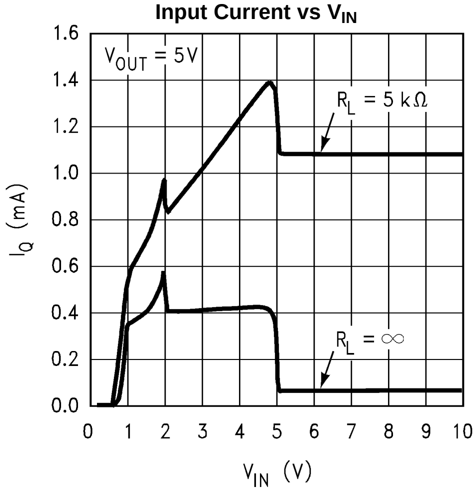


Figure 12.

Input Current vs V_{IN}

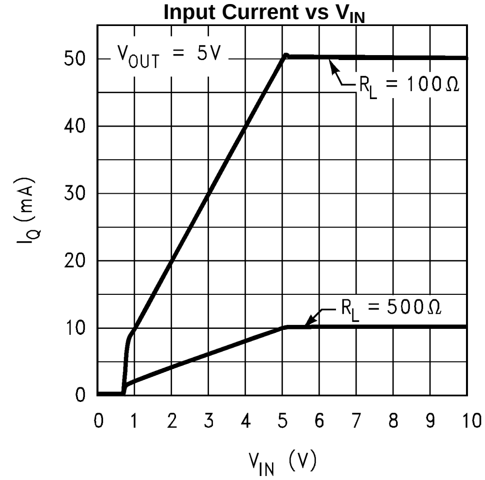


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

Line Transient Response

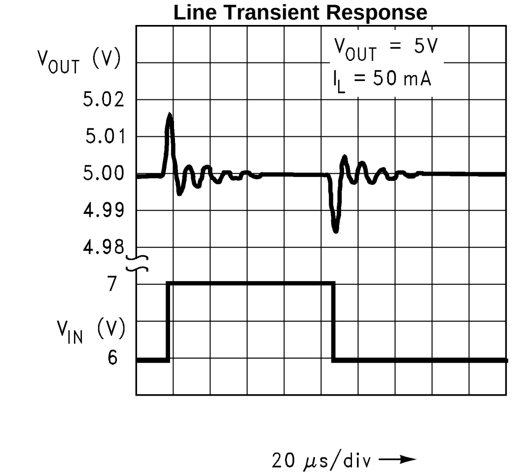


Figure 14.

Line Transient Response

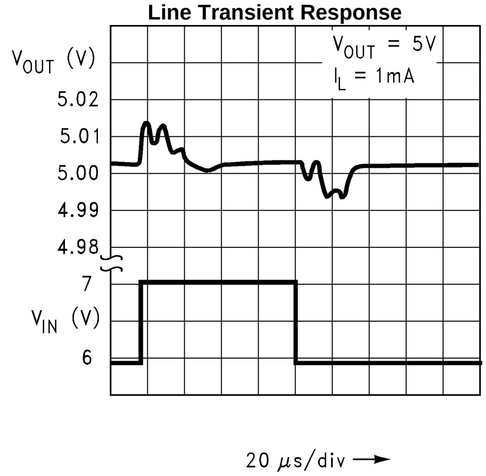


Figure 15.

Load Transient Response

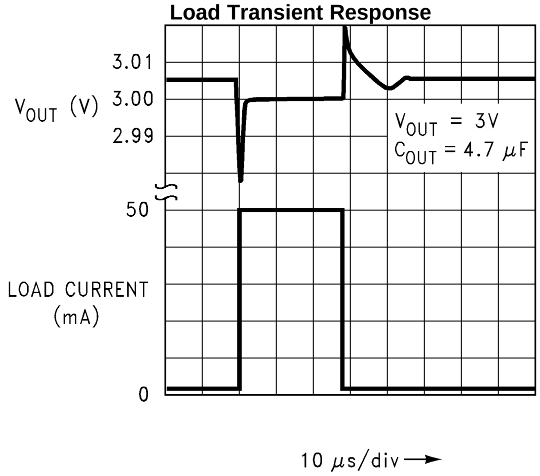


Figure 16.

Load Transient Response

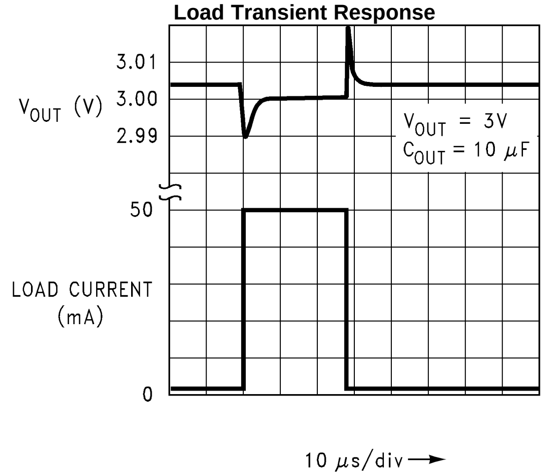


Figure 17.

Load Transient Response

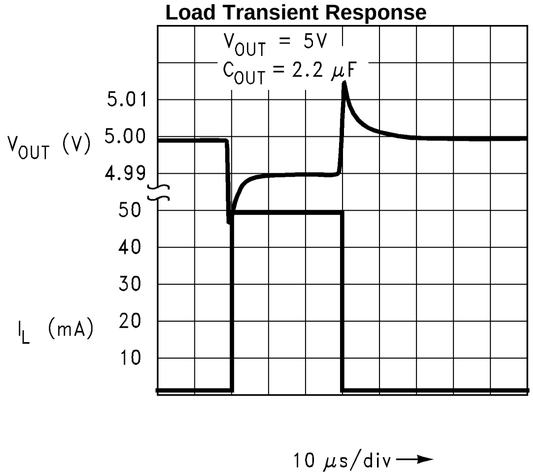


Figure 18.

Load Transient Response

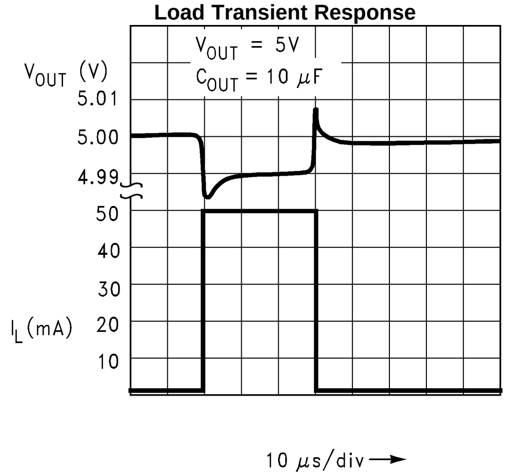


Figure 19.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1V, C_{OUT} = 4.7 μF, C_{IN} = 1 μF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

Short Circuit Current

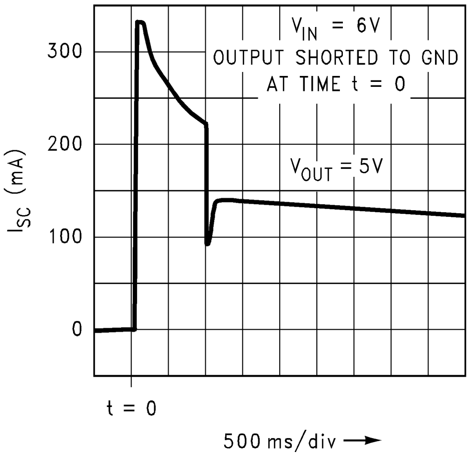


Figure 20.

Instantaneous Short Circuit Current vs Temperature

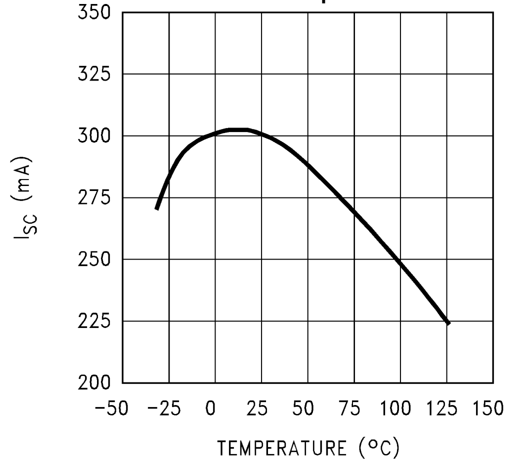


Figure 21.

Short Circuit Current

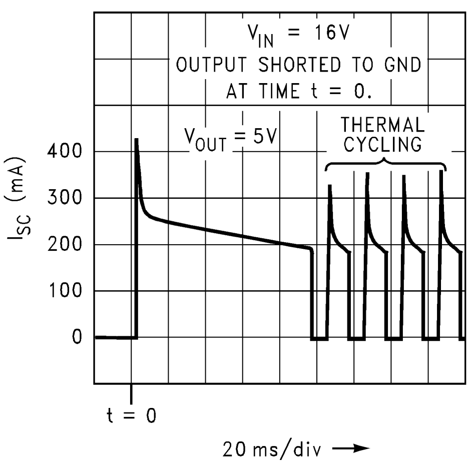


Figure 22.

Instantaneous Short Circuit Current vs Output Voltage

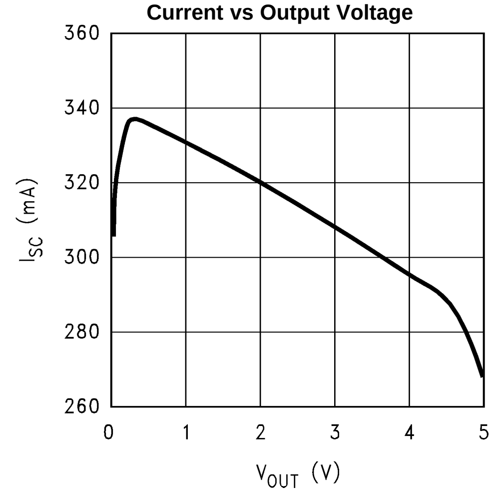


Figure 23.

Output Impedance vs Frequency

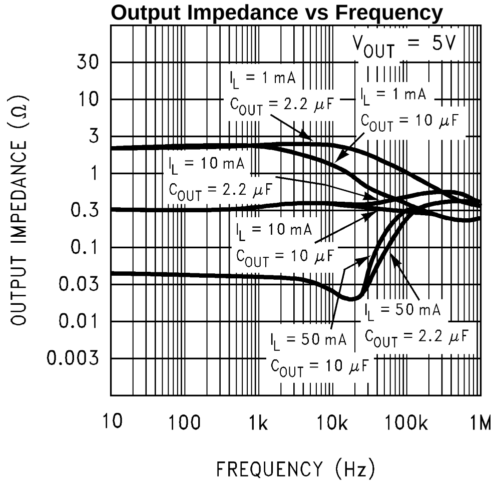


Figure 24.

Output Impedance vs Frequency

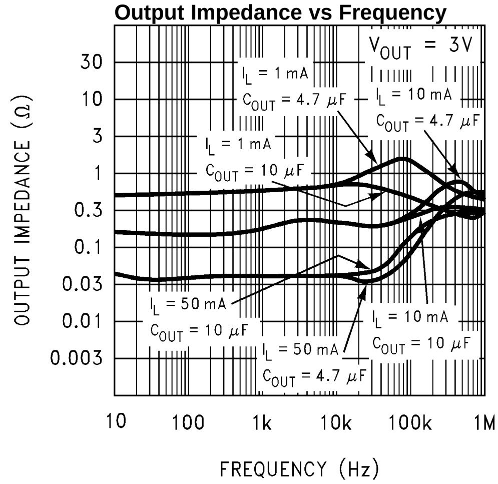


Figure 25.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, $V_{IN} = V_{O(NOM)}$ + 1V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

ON/OFF Pin Current vs $V_{ON/OFF}$

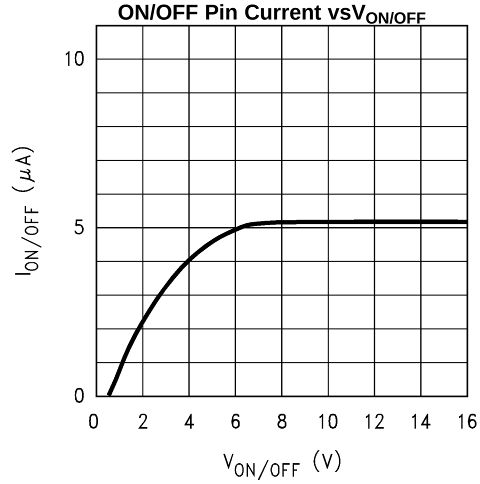


Figure 26.

ON/OFF Threshold vs Temperature

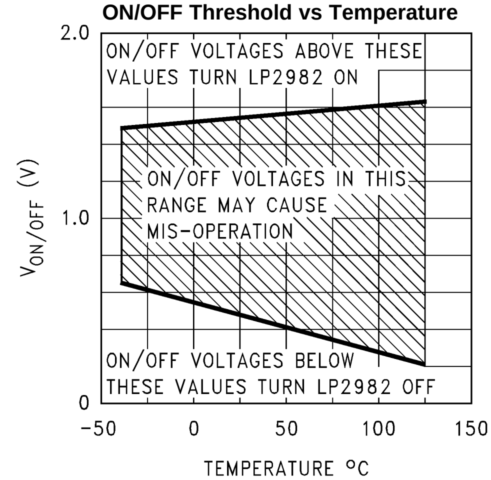


Figure 27.

Input to Output Leakage vs Temperature

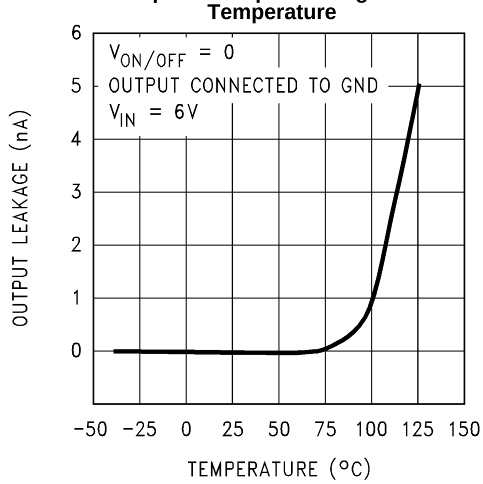


Figure 28.

Output Reverse Leakage vs Temperature

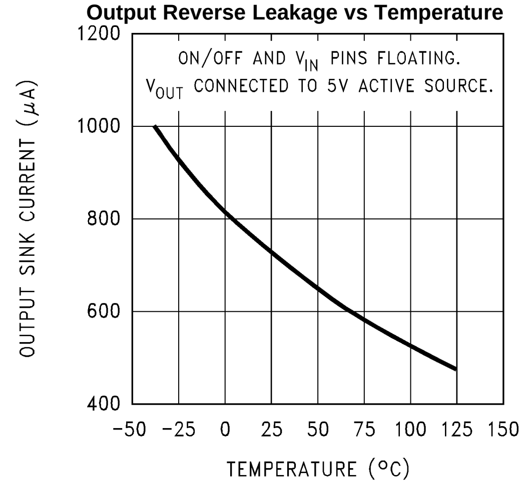


Figure 29.

Output Noise Density

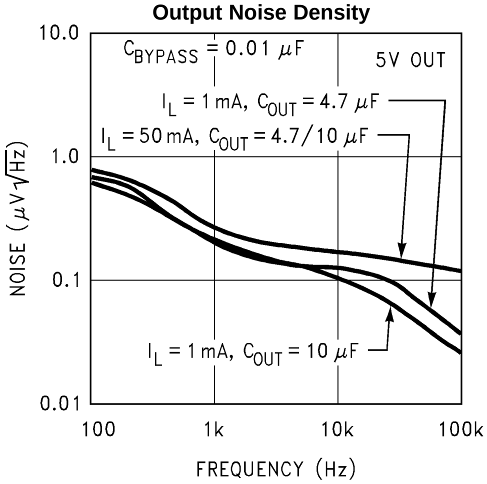


Figure 30.

Output Noise Density

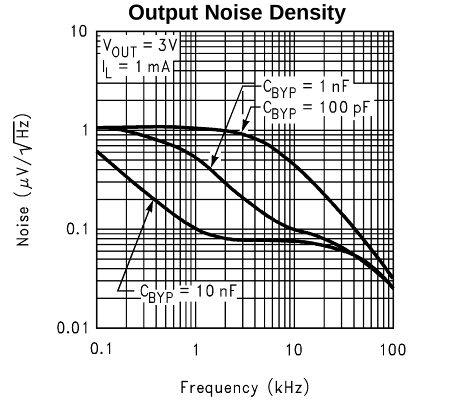


Figure 31.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, $V_{IN} = V_{O(NOM)}$ + 1V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

Output Noise Density

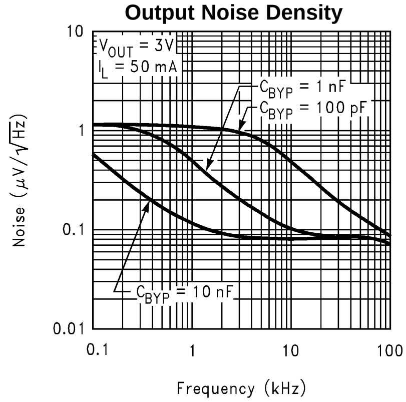


Figure 32.

Ripple Rejection

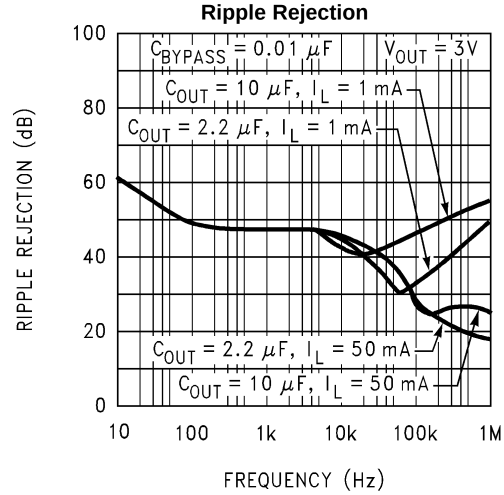


Figure 33.

Turn-ON Waveform

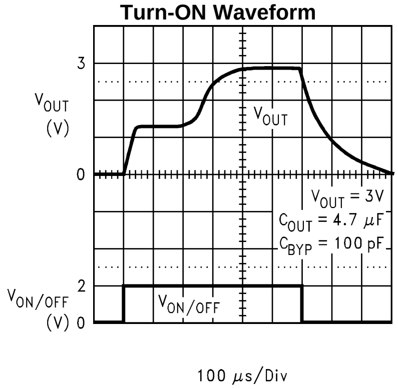


Figure 34.

Turn-ON Waveform

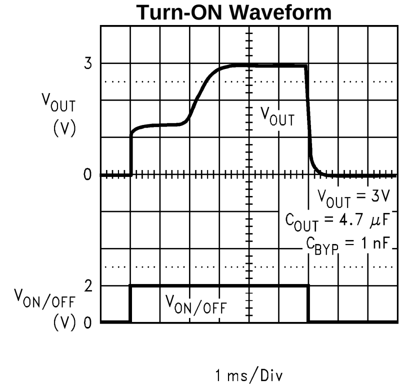


Figure 35.

Turn-ON Waveform

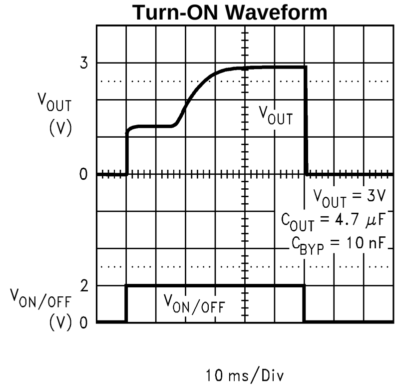


Figure 36.

APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, the external capacitors used with the LP2982 must be carefully selected to assure regulator loop stability.

Input Capacitor: An input capacitor whose value is ≥ 1 µF is required with the LP2982 (amount of capacitance can be increased without limit).

This capacitor must be located a distance of not more than 0.5″ from the input pin of the LP2982 and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor.

Output Capacitor: The output capacitor must meet both the requirement for minimum amount of capacitance and E.S.R. (equivalent series resistance) value. Curves are provided which show the allowable ESR range as a function of load current for various output voltages and capacitor values (refer to Figure 37 and Figure 38).

Important: The output capacitor must maintain its ESR in the stable region over the full operating temperature to assure stability. Also, capacitor tolerance and variation with temperature must be considered to assure the minimum amount of capacitance is provided at all times.

This capacitor should be located not more than 0.5″ from the output pin of the LP2982 and returned to a clean analog ground.

Low-current Operation: In applications where the load current is < 1 mA, special consideration must be given to the output capacitor.

Circuitry inside the LP2982 is specially designed to reduce operating (quiescent) current at light loads down to about 65 µA.

The mode of operation which yields this very low quiescent current also means that the output capacitor ESR is critical.

For optimum stability and minimum output noise, it is recommended that a 10Ω resistor be placed in series with the output capacitor in any applications where $I_L < 1$ mA.

CAPACITOR CHARACTERISTICS

Tantalum: Tantalum capacitors are the best choice for use with the LP2982. Most good quality tantalum can be used with the LP2982, but check the manufacturer's data sheet to be sure the ESR is in range.

It is important to remember that ESR increases sharply at lower temperatures (< 10°C) and a capacitor that is near the upper limit for stability at room temperature can cause instability when it gets cold.

In applications which must operate at very low temperatures, it may be necessary to parallel the output tantalum capacitor with a ceramic capacitor to prevent the ESR from going up too high (see next section for important information on ceramic capacitors).

Ceramic: Ceramic capacitors are not recommended for use at the output of the LP2982. This is because the ESR of a ceramic can be low enough to go below the minimum stable value for the LP2982. A good 2.2 µF ceramic was measured and found to have an ESR of about 15 mΩ, which is low enough to cause oscillations.

If a ceramic capacitor is used on the output, a 1Ω resistor should be placed in series with the capacitor.

Aluminum: Because of large physical size, aluminum electrolytic are not typically used with the LP2982. They must meet the same ESR requirements over the operating temperature range, which is more difficult because of their large increase in ESR at cold temperature.

An aluminum electrolytic can exhibit an ESR increase of as much as 50X when going from 20°C to −40°C. Also, some aluminum electrolytic are not operational below −25°C because the electrolyte can freeze.

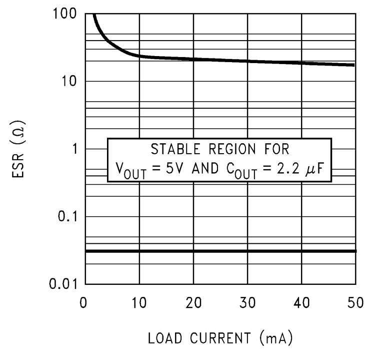


Figure 37. 5V/2.2 μF ESR Curves

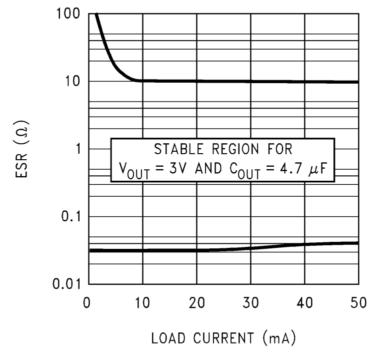


Figure 38. 3V/4.7 μF ESR Curves

BYPASS CAPACITOR

The 0.01 μF capacitor connected to the bypass pin to reduce noise must have very low leakage.

The current flowing out of the bypass pin comes from the bandgap reference, which is used to set the output voltage.

This capacitor leakage current causes the output voltage to decline by an amount proportional to the current. Typical values are −0.015%/nA @ −40°C, −0.021%/nA @ 25°C, and −0.035%/nA @ +125°C.

This data is valid up to a maximum leakage current of about 500 nA, beyond which the bandgap is so severely loaded that it can not function.

Care must be taken to ensure that the capacitor selected will not have excessive leakage current over the operating temperature range of the application.

A high quality ceramic capacitor which uses either NPO or COG type dielectric material will typically have very low leakage. Small surface mount polypropylene or polycarbonate film capacitors also have extremely low leakage, but are slightly larger than ceramics.

REVERSE CURRENT PATH

The internal PNP power transistor used as the pass element in the LP2982 has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse biased (See Figure 39).

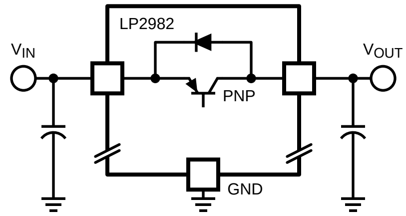


Figure 39. LP2982 Reverse Current Path

However, if the input voltage is more than a V_{BE} below the output voltage, this diode will turn ON and current will flow into the regulator output. In such cases, a parasitic SCR can latch which will allow a high current to flow into the V_{IN} pin and out the ground pin, which can damage the part.

The internal diode can also be turned on if the input voltage is abruptly stepped down to a voltage which is a V_{BE} below the output voltage.

In any application where the output voltage may be higher than the input voltage, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}. See Figure 40), to limit the reverse voltage across the LP2982 to 0.3V (see Absolute Maximum Ratings).

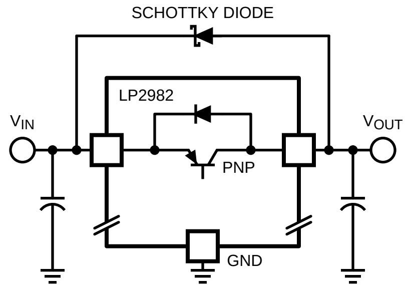


Figure 40. Adding External Schottky Diode Protection

ON/OFF INPUT OPERATION

The LP2982 is shut off by pulling the ON/OFF input low, and turned on by driving the input high. If this feature is not to be used, the ON/OFF input should be tied to V_{IN} to keep the regulator on at all times (the ON/OFF input must **not** be left floating).

To ensure proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on/turn-off voltage thresholds which ensure an ON or OFF state (see Electrical Characteristics).

The ON/OFF signal may come from either a totem-pole output, or an open-collector output with pull-up resistor to the LP2982 input voltage or another logic supply. The high-level voltage may exceed the LP2982 input voltage, but must remain within the Absolute Maximum Ratings for the ON/OFF pin.

It is also important that the turn-on/turn-off voltage signals applied to the ON/OFF input have a slew rate which is greater than 40 mV/µs.

IMPORTANT: The regulator shutdown function will not operate correctly if a slow-moving signal is applied to the ON/OFF input.

REVISION HISTORY

Changes from Revision I (April 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2982AIM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L20A	Samples
LP2982AIM5-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L19A	
LP2982AIM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L19A	Samples
LP2982AIM5-5.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L18A	
LP2982AIM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L18A	Samples
LP2982AIM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L20A	Samples
LP2982AIM5X-3.3	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	L19A	
LP2982AIM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L19A	Samples
LP2982AIM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L18A	Samples
LP2982IM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L20B	Samples
LP2982IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L19B	Samples
LP2982IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L18B	Samples
LP2982IM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L20B	Samples
LP2982IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L19B	Samples
LP2982IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L18B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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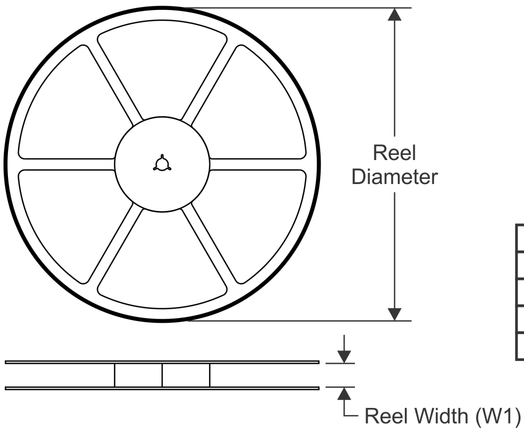
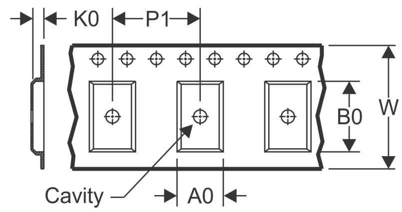
TAPE AND REEL INFORMATION

REEL DIMENSIONS

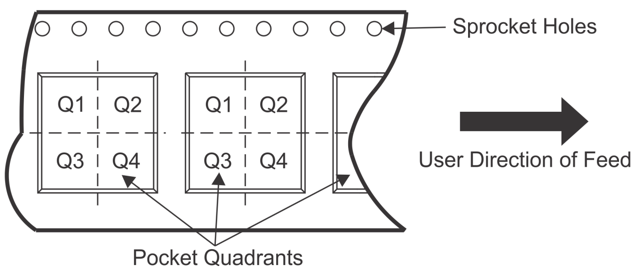


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

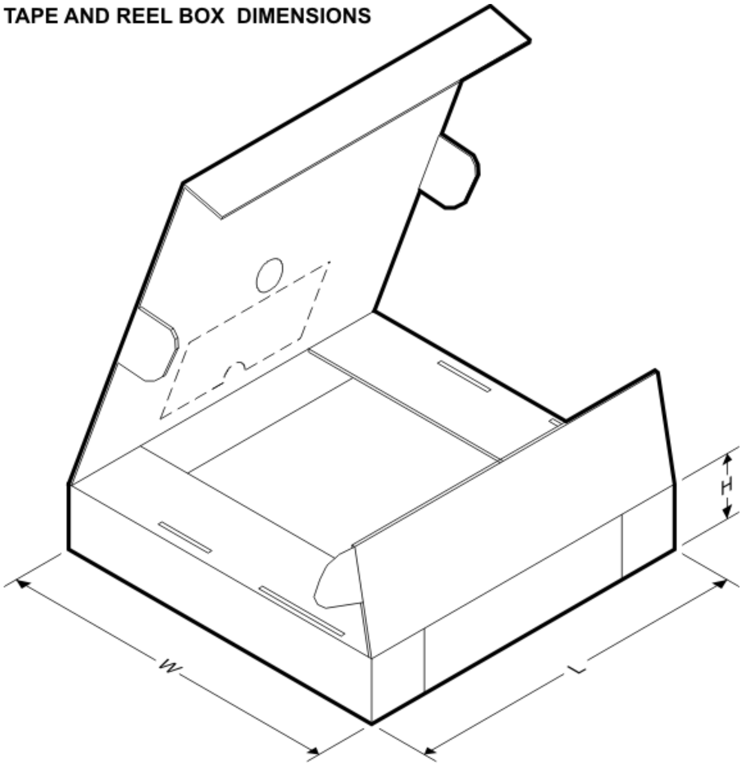
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2982AIM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-3.3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

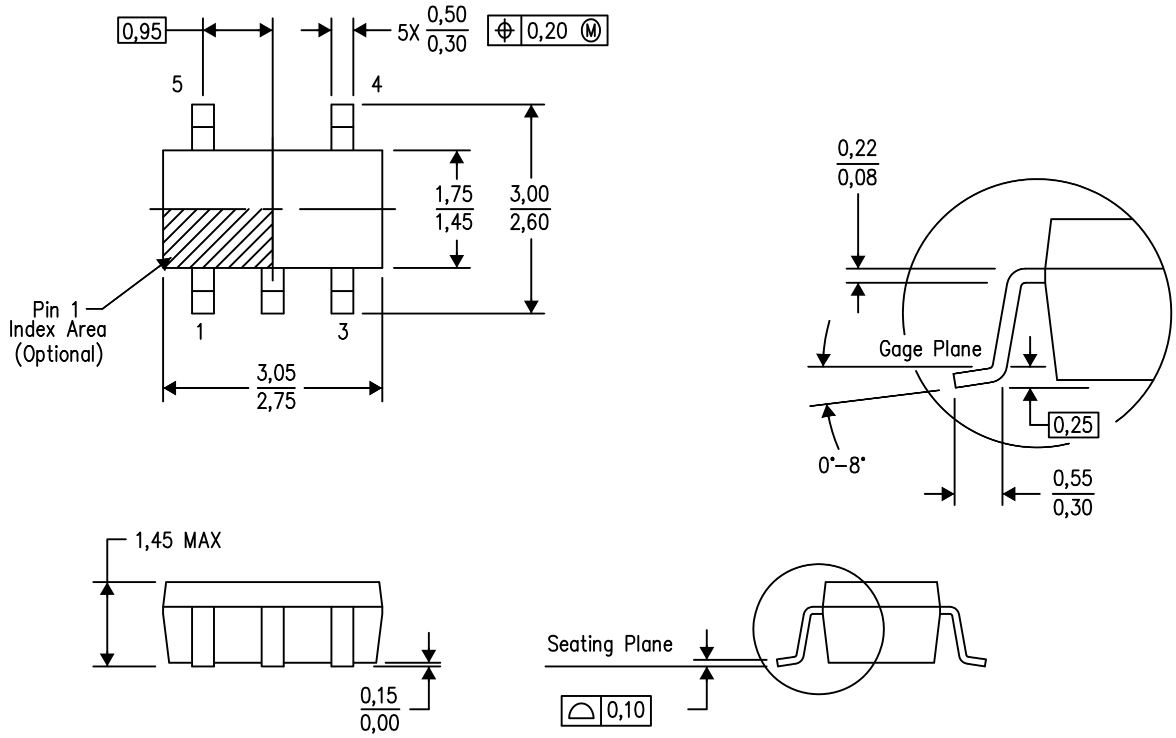
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2982AIM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982AIM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982AIM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982AIM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982AIM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982AIM5X-3.3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982IM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982IM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982IM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

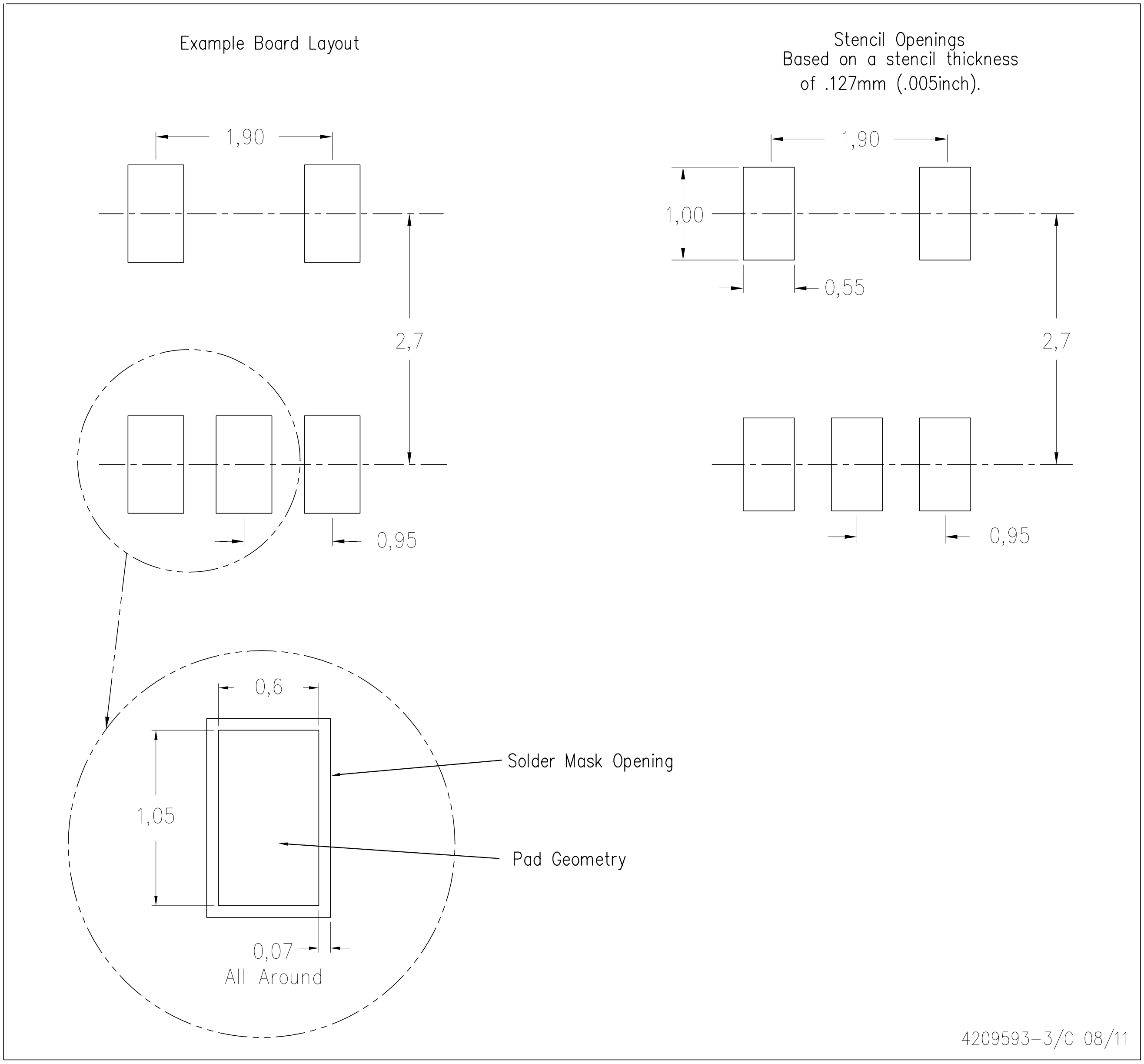
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/L 08/2013

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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