SAF1562

Hi-Speed Universal Serial Bus PCI Host Controller

Rev. 3 — 19 June 2012 Product data sheet

1. General description

The SAF1562HL is a Peripheral Component Interconnect (PCI)-based, single-chip Universal Serial Bus (USB) Host Controller. It integrates two Original USB Open Host Controller Interface (OHCI) cores, one Hi-Speed USB Enhanced Host Controller Interface (EHCI) core, and two transceivers that are compliant with Hi-Speed USB and Original USB. The functional parts of the SAF1562HL are fully compliant with *Universal Serial Bus Specification Rev. 2.0*, *Open Host Controller Interface Specification for USB Rev. 1.0a*, *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*, *PCI Local Bus Specification Rev. 2.2*, and *PCI Bus Power Management Interface Specification Rev. 1.1*.

The integrated high performance USB transceivers allow the SAF1562HL to handle all Hi-Speed USB transfer speed modes: high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s). The SAF1562HL provides two downstream ports, allowing simultaneous connection of USB devices at different speeds.

The SAF1562HL is fully compatible with various operating system drivers, such as Microsoft Windows standard OHCI and EHCI drivers that are present in Windows XP, Windows 2000 and Red Hat Linux.

The SAF1562HL directly interfaces to any 32-bit, 33 MHz PCI bus. Its PCI pins can source 3.3 V. The PCI interface fully complies with *PCI Local Bus Specification Rev. 2.2*.

The SAF1562HL is ideally suited for use in Hi-Speed USB mobile applications and embedded solutions. The SAF1562HL uses a 12 MHz crystal.

2. Features and benefits

- Complies with *Universal Serial Bus Specification Rev. 2.0*
- Supports data transfer at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
- Two Original USB OHCI cores comply with *Open Host Controller Interface Specification for USB Rev. 1.0a*
- One Hi-Speed USB EHCI core complies with *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*
- Supports PCI 32-bit, 33 MHz interface compliant with *PCI Local Bus Specification Rev. 2.2*, with support for $D3_{cold}$ standby and wake-up modes; all I/O pins are 3.3 V standard

- Compliant with *PCI Bus Power Management Interface Specification Rev. 1.1* for all hosts (EHCI and OHCI), and supports all power states: D0, D1, D2, $D3_{hot}$ and $D3_{cold}$
- CLKRUN support for mobile applications, such as internal notebook design
- Configurable subsystem ID and subsystem vendor ID through external EEPROM
- Digital and analog power separation for better Electro-Magnetic Interference (EMI) and ElectroStatic Discharge (ESD) protection
- Supports hot plug and play and remote wake-up of peripherals
- Supports individual power switching and individual overcurrent protection for downstream ports
- Supports partial dynamic port-routing capability for downstream ports that allows sharing of the same physical downstream ports between the Original USB Host Controller and the Hi-Speed USB Host Controller
- Uses 12 MHz crystal oscillator to reduce system cost and EMI emissions
- Supports dual power supply: PCI $V_{aux(3V3)}$ and V_{CC}
- Operates at +3.3 V power supply input
- Low power consumption
- Qualified in accordance with AEC-Q100
- Operating temperature range from –40 °C to +85 °C
- Available in LQFP100 package

3. Applications

This NXP USB product can only be used in automotive applications. Inclusion or use of the NXP USB products in other than automotive applications is not permitted and for your company's own risk. Your company agrees to full indemnify NXP for any damages resulting from such inclusion or use.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SAF1562HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

5. Block diagram

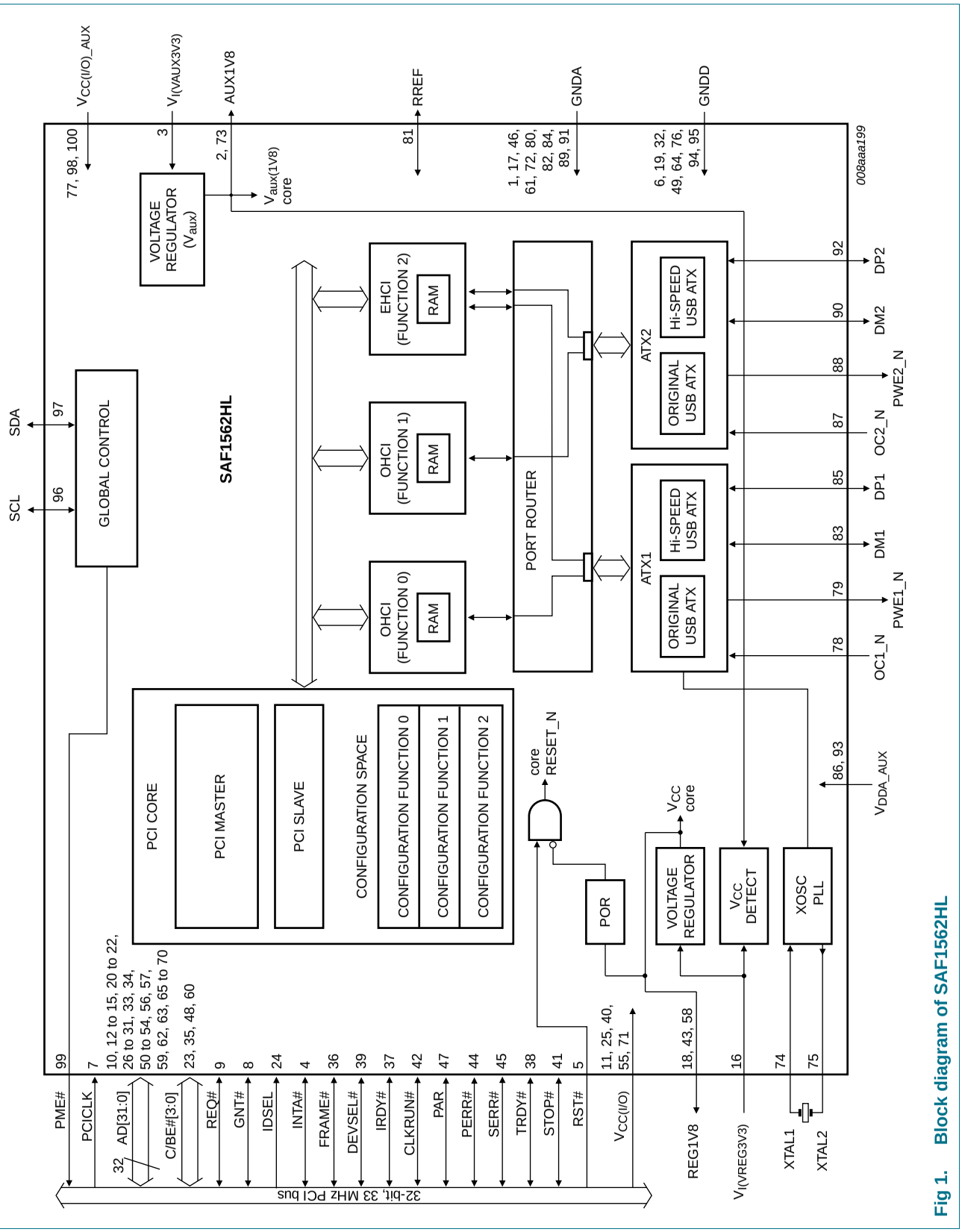


Fig 1. Block diagram of SAF1562HL

6. Pinning information

6.1 Pinning

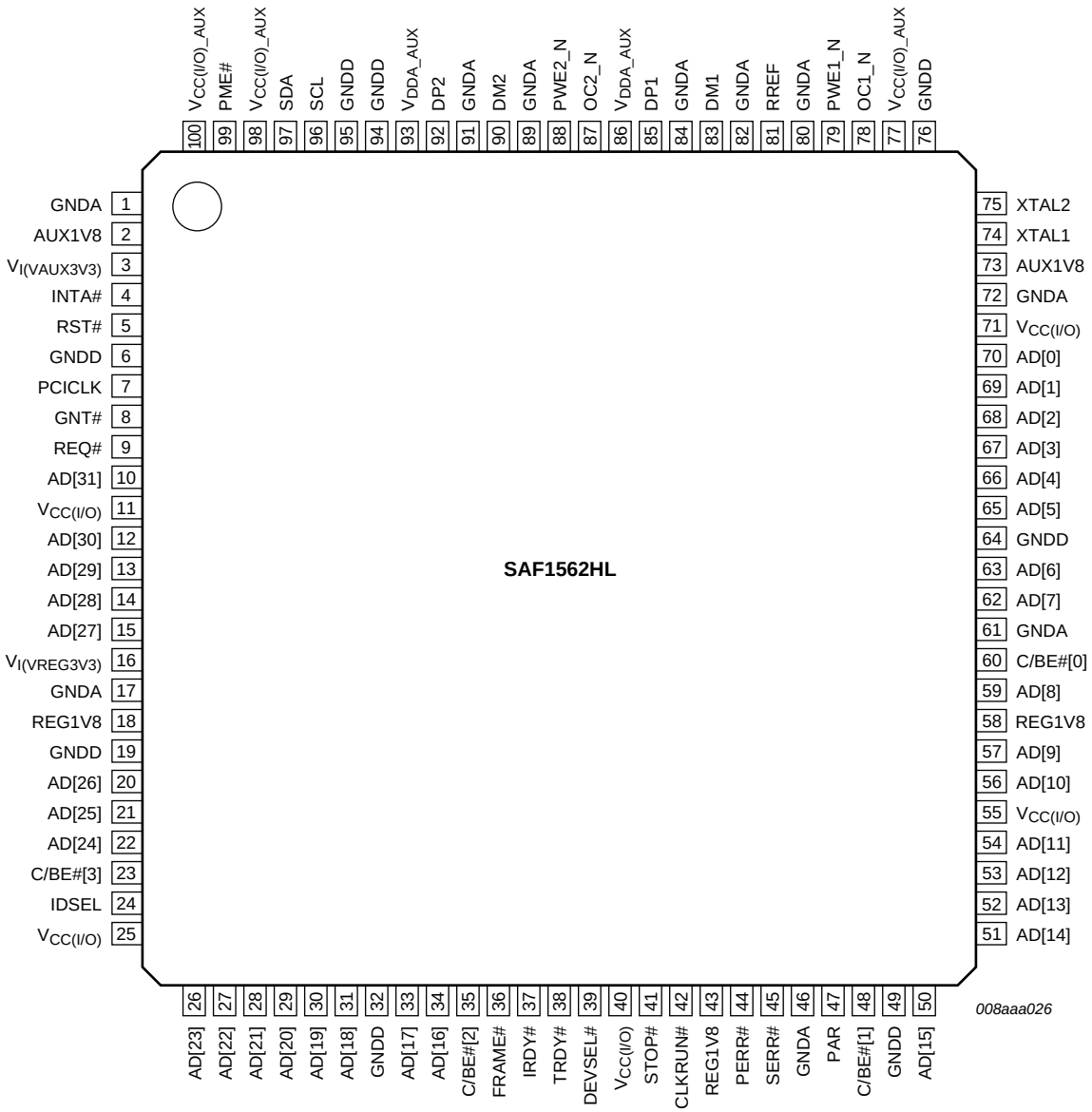


Fig 2. Pin configuration for LQFP100

6.2 Pin description

Table 2. Pin description

Symbol[1]	Pin	Type	Description
GNDA	1	-	analog ground
AUX1V8	2	-	1.8 V auxiliary output voltage; only for voltage conditioning; cannot be used to supply power to external components; connected to 100 nF and 4.7 μF capacitors
$V_{I(VAUX3V3)}$	3	-	3.3 V auxiliary input voltage; add a 100 nF decoupling capacitor
INTA#	4	O	PCI interrupt PCI pad; 3.3 V signaling; open-drain
RST#	5	I	PCI reset; used to bring PCI-specific registers, sequencers and signals to a consistent state 3.3 V input pad; push-pull
GNDD	6	-	digital ground
PCICLK	7	I	PCI system clock (33 MHz) PCI pad; 3.3 V signaling
GNT#	8	I/O	PCI grant; indicates to the agent that access to the bus is granted PCI pad; 3.3 V signaling
REQ#	9	I/O	PCI request; indicates to the arbitrator that the agent wants to use the bus PCI pad; 3.3 V signaling
AD[31]	10	I/O	bit 31 of multiplexed PCI address and data PCI pad; 3.3 V signaling
$V_{CC(I/O)}$	11	-	3.3 V supply voltage; used to power pads; add a 100 nF decoupling capacitor
AD[30]	12	I/O	bit 30 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[29]	13	I/O	bit 29 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[28]	14	I/O	bit 28 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[27]	15	I/O	bit 27 of multiplexed PCI address and data PCI pad; 3.3 V signaling
$V_{I(VREG3V3)}$	16	-	3.3 V regulator input voltage; add a 100 nF decoupling capacitor
GNDA	17	-	analog ground
REG1V8	18	-	1.8 V regulator output voltage; only for voltage conditioning; cannot be used to supply power to external components; connected to 100 nF and 4.7 μF capacitors
GNDD	19	-	digital ground
AD[26]	20	I/O	bit 26 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[25]	21	I/O	bit 25 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[24]	22	I/O	bit 24 of multiplexed PCI address and data PCI pad; 3.3 V signaling

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type	Description
C/BE#[3]	23	I/O	byte 3 of multiplexed PCI bus command and byte enable PCI pad; 3.3 V signaling
IDSEL	24	I	PCI initialization device select; used as a chip select during configuration read and write transactions PCI pad; 3.3 V signaling
$V_{CC(I/O)}$	25	-	3.3 V supply voltage; used to power pads; add a 100 nF decoupling capacitor
AD[23]	26	I/O	bit 23 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[22]	27	I/O	bit 22 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[21]	28	I/O	bit 21 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[20]	29	I/O	bit 20 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[19]	30	I/O	bit 19 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[18]	31	I/O	bit 18 of multiplexed PCI address and data PCI pad; 3.3 V signaling
GNDD	32	-	digital ground
AD[17]	33	I/O	bit 17 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[16]	34	I/O	bit 16 of multiplexed PCI address and data PCI pad; 3.3 V signaling
C/BE#[2]	35	I/O	byte 2 of multiplexed PCI bus command and byte enable PCI pad; 3.3 V signaling
FRAME#	36	I/O	PCI cycle frame; driven by the master to indicate the beginning and duration of an access PCI pad; 3.3 V signaling
IRDY#	37	I/O	PCI initiator ready; indicates the ability of the initiating agent to complete the current data phase of a transaction PCI pad; 3.3 V signaling
TRDY#	38	I/O	PCI target ready; indicates the ability of the target agent to complete the current data phase of a transaction PCI pad; 3.3 V signaling
DEVSEL#	39	I/O	PCI device select; indicates if any device is selected on the bus PCI pad; 3.3 V signaling
$V_{CC(I/O)}$	40	-	3.3 V supply voltage; used to power pads; add a 100 nF decoupling capacitor
STOP#	41	I/O	PCI stop; indicates that the current target is requesting the master to stop the current transaction PCI pad; 3.3 V signaling
CLKRUN#	42	I/O	PCI CLKRUN signal; pull-down to ground through a 10 kΩ resistor PCI pad; 3.3 V signaling; open-drain

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type	Description
REG1V8	43	-	1.8 V regulator output voltage; only for voltage conditioning; cannot be used to supply power to external components; add a 100 nF decoupling capacitor
PERR#	44	I/O	PCI parity error; used to report data parity errors during all PCI transactions, except a Special Cycle PCI pad; 3.3 V signaling
SERR#	45	O	PCI system error; used to report address parity errors and data parity errors on the Special Cycle command, or any other system error in which the result will be catastrophic PCI pad; 3.3 V signaling; open-drain
GNDA	46	-	analog ground
PAR	47	I/O	PCI parity PCI pad; 3.3 V signaling
C/BE#[1]	48	I/O	byte 1 of multiplexed PCI bus command and byte enable PCI pad; 3.3 V signaling
GNDD	49	-	digital ground
AD[15]	50	I/O	bit 15 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[14]	51	I/O	bit 14 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[13]	52	I/O	bit 13 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[12]	53	I/O	bit 12 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[11]	54	I/O	bit 11 of multiplexed PCI address and data PCI pad; 3.3 V signaling
$V_{CC(I/O)}$	55	-	3.3 V supply voltage; used to power pads; add a 100 nF decoupling capacitor
AD[10]	56	I/O	bit 10 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[9]	57	I/O	bit 9 of multiplexed PCI address and data PCI pad; 3.3 V signaling
REG1V8	58	-	1.8 V regulator output voltage; only for voltage conditioning; cannot be used to supply power to external components; add a 100 nF decoupling capacitor
AD[8]	59	I/O	bit 8 of multiplexed PCI address and data PCI pad; 3.3 V signaling
C/BE#[0]	60	I/O	byte 0 of multiplexed PCI bus command and byte enable PCI pad; 3.3 V signaling
GNDA	61	-	analog ground
AD[7]	62	I/O	bit 7 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[6]	63	I/O	bit 6 of multiplexed PCI address and data PCI pad; 3.3 V signaling

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type	Description
GNDD	64	-	digital ground
AD[5]	65	I/O	bit 5 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[4]	66	I/O	bit 4 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[3]	67	I/O	bit 3 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[2]	68	I/O	bit 2 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[1]	69	I/O	bit 1 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[0]	70	I/O	bit 0 of multiplexed PCI address and data PCI pad; 3.3 V signaling
$V_{CC(I/O)}$	71	-	3.3 V supply voltage; used to power pads; add a 100 nF decoupling capacitor
GNDA	72	-	analog ground
AUX1V8	73	-	1.8 V auxiliary output voltage; only for voltage conditioning; cannot be used to supply power to external components; add a 100 nF decoupling capacitor
XTAL1	74	AI	crystal oscillator input; this can also be a 12 MHz clock input
XTAL2	75	AO	crystal oscillator output (12 MHz); leave open when clock is used
GNDD	76	-	digital ground
$V_{CC(I/O)\_AUX}$	77	-	3.3 V auxiliary supply voltage; used to power pads; add a 100 nF decoupling capacitor
OC1_N	78	I	overcurrent sense input for the USB downstream port 1 (digital) 3.3 V input pad; push-pull; CMOS
PWE1_N	79	O	power enable for the USB downstream port 1 3.3 V output pad; 3 ns slew rate control; CMOS; open-drain
GNDA	80	-	analog ground
RREF	81	AI/O	analog connection for the external resistor (12 kΩ ± 1 %)
GNDA	82	-	analog ground
DM1	83	AI/O	D–; analog connection for the USB downstream port 1; pull down to ground through 15 kΩ resistor, even when the port is not used
GNDA	84	-	analog ground
DP1	85	AI/O	D+; analog connection for the USB downstream port 1; pull down to ground through 15 kΩ resistor, even when the port is not used
V_{DDA_AUX}	86	-	auxiliary analog supply voltage; add a 100 nF decoupling capacitor
OC2_N	87	I	overcurrent sense input for the USB downstream port 2 (digital) 3.3 V input pad; push-pull; CMOS
PWE2_N	88	O	power enable for the USB downstream port 2 3.3 V output pad; 3 ns slew rate control; CMOS; open-drain
GNDA	89	-	analog ground

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type	Description
DM2	90	AI/O	D–; analog connection for the USB downstream port 2; pull down to ground through 15 kΩ resistor, even when the port is not used
GNDA	91	-	analog ground
DP2	92	AI/O	D+; analog connection for the USB downstream port 2; pull down to ground through 15 kΩ resistor, even when the port is not used
V_{DDA_AUX}	93	-	auxiliary analog supply voltage; add a 100 nF decoupling capacitor
GNDD	94	-	digital ground
GNDD	95	-	digital ground
SCL	96	I/O	I^2C-bus clock; pull-up to 3.3 V through a 10 kΩ resistor[2] I^2C-bus pad; clock signal
SDA	97	I/O	I^2C-bus data; pull-up to 3.3 V through a 10 kΩ resistor[2] I^2C-bus pad; data signal
$V_{CC(I/O)\_AUX}$	98	-	3.3 V auxiliary supply voltage; used to power pads; add a 100 nF decoupling capacitor
PME#	99	O	PCI Power Management Event; used by a device to request a change in the device or system power state PCI pad; 3.3 V signaling; open-drain
$V_{CC(I/O)\_AUX}$	100	-	3.3 V auxiliary supply voltage; used to power pads; add a 100 nF decoupling capacitor

[1] Symbol names ending with # represent active LOW signals for PCI pins, for example: NAME#. Symbol names ending with underscore N represent active LOW signals for USB pins, for example: NAME_N.

[2] Connect to ground if I^2C-bus is not used.

7. Functional description

7.1 OHCI Host Controller

An OHCI Host Controller per port transfers data to devices at the Original USB defined bit rate of 12 Mbit/s or 1.5 Mbit/s.

7.2 EHCI Host Controller

The EHCI Host Controller transfers data to a Hi-Speed USB compliant device at the Hi-Speed USB defined bit rate of 480 Mbit/s. When the EHCI Host Controller has the ownership of a port, the OHCI Host Controllers are not allowed to modify the port register. All additional port bit definitions required for the Enhanced Host Controller are not visible to the OHCI Host Controller.

7.3 Dynamic port-routing logic

The port-routing feature allows sharing of the same physical downstream ports between the Original USB Host Controller and the Hi-Speed USB Host Controller. This requirement of the *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0* provides ports that are multiplexed with the ports of the OHCI.

The EHCI is responsible for the port-routing switching mechanism. Two register bits are used for ownership switching. During power-on and system reset, the default ownership of all downstream ports is the OHCI. The Enhanced Host Controller Driver (EHCD) controls the ownership during normal functionality.

7.4 Hi-Speed USB analog transceivers

The Hi-Speed USB analog transceivers directly interface to the USB cables through integrated termination resistors. These transceivers can transmit and receive serial data at all data rates: high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s).

7.5 Power management

The SAF1562HL provides an advanced power management capability interface that is compliant with *PCI Bus Power Management Interface Specification Rev. 1.1*. Power is controlled and managed by the interaction between drivers and PCI registers.

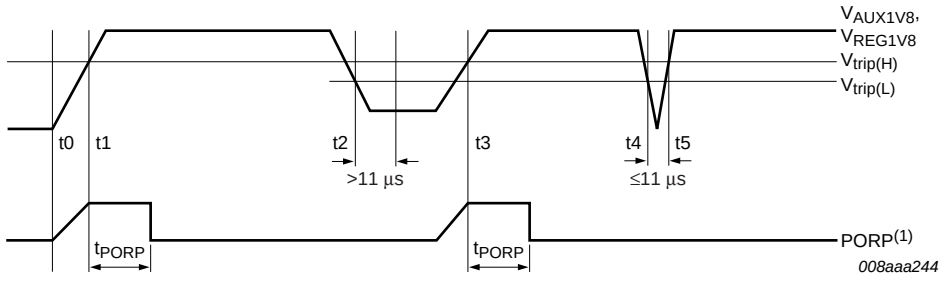
For a detailed description on power management, see Section 10.

7.6 Phase-Locked Loop (PLL)

A 12 MHz-to-30 MHz and 48 MHz clock multiplier PLL is integrated on-chip. This allows the use of a low-cost 12 MHz crystal, which also minimizes EMI. No external components are required for the PLL to operate.

7.7 Power-On Reset (POR)

Figure 3 shows a possible curve of V_{AUX1V8}, V_{REG1V8} with dips at t2 to t3 and t4 to t5. The internal Power-On Reset Pulse (PORP) starts at t0 and follows the curve of V_{AUX1V8}, V_{REG1V8} until t1. At t1, the detector will detect the passing of the trip level $V_{trip(H)}$ (maximum 1.4 V) and a delay element will add another t_{PORP} (minimum 200 ns) before the PORP drops to LOW. If the dip at t4 to t5 is too short (less than or equal 11 µs), the PORP will not react and will remain LOW. A HIGH on PORP will be generated whenever V_{AUX1V8}, V_{REG1V8} drops below $V_{trip(L)}$ (minimum 0.95 V) for more than 11 µs. The $V_{I(VAUX3V3)}$, $V_{CC(I/O)}$, $V_{I(VREG3V3)}$ and $V_{CC(I/O)\_AUX}$ during power on should ramp up linearly from 0 V to 3.3 V with the rise time between 5 ms and 11 ms.



(1) PORP = internal power-on reset pulse.

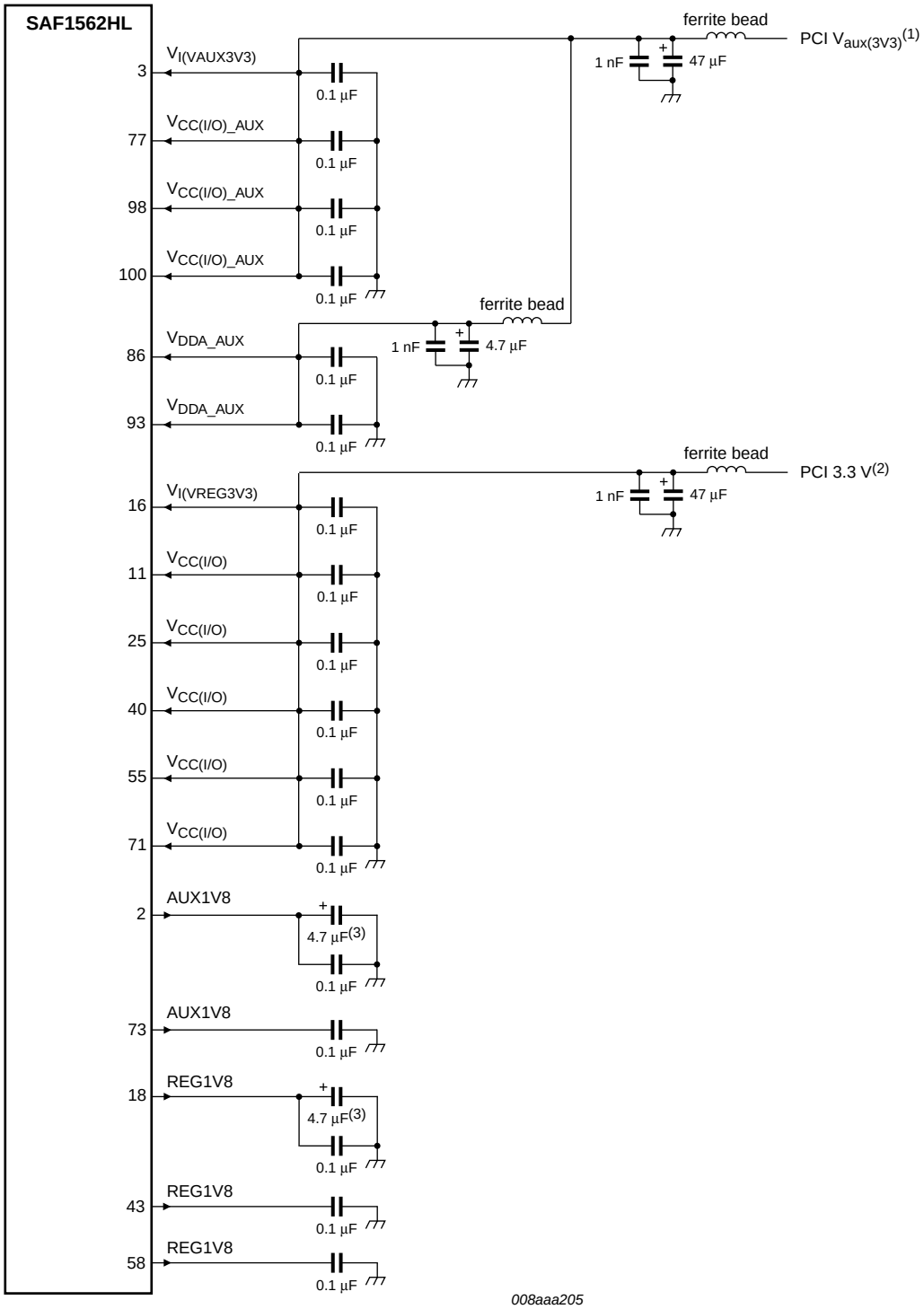
Fig 3. Power-on reset

7.8 Power supply

The SAF1562 supports both single power supply and dual power supply.

Figure 4 shows the SAF1562HL voltage pins connection with dual power supply.

Figure 5 shows the SAF1562HL voltage pins connection with single power supply.



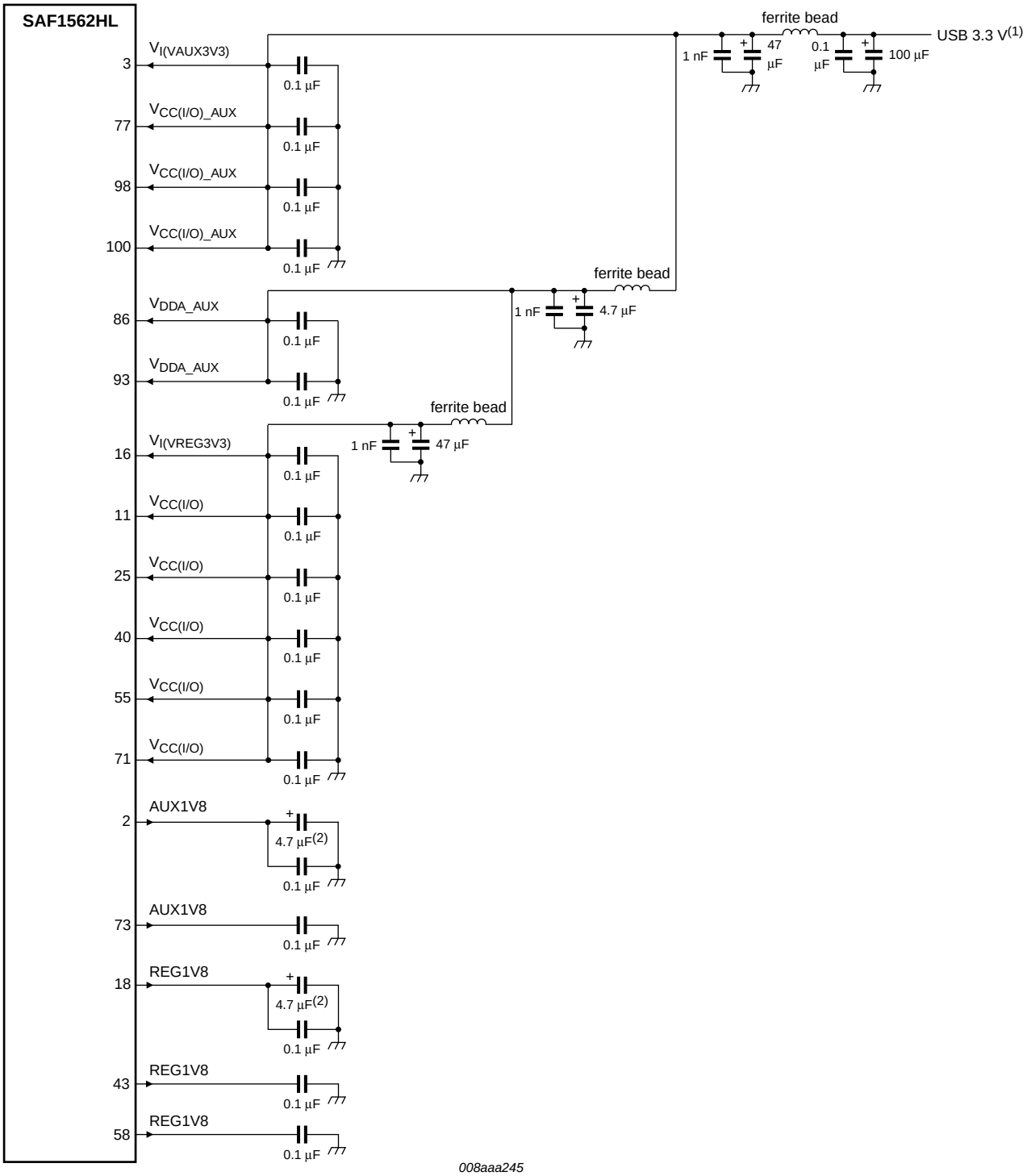
Remark: Connect the decoupling capacitor very close to the supply pins.

(1) The PCI $V_{aux(3V3)}$ during power on should ramp up linearly from 0 V to 3.3 V with the rise time between 5 ms and 11 ms.

(2) PCI 3.3 V is turned on much later after the PCI $V_{I(VAUX3V3)}$ is powered.

(3) This electrolytic or tantalum capacitor must be a low Equivalent Series Resistance (ESR) type (0.2 Ω to 2 Ω).

Fig 4. SAF1562HL voltage pins connection with dual power supply



Remark: Connect the decoupling capacitor very close to the supply pins.

(1) The USB 3.3 V power supply during power on should ramp up linearly from 0 V to 3.3 V with the rise time between 5 ms and 11 ms.

(2) This electrolytic or tantalum capacitor must be a low ESR type (0.2 Ω to 2 Ω).

Fig 5. SAF1562HL voltage pins connection with single power supply

8. PCI

8.1 PCI interface

The PCI interface has three functions. The first function (#0) and the second function (#1) are for the OHCI Host Controllers, and the third function (#2) is for the EHCI Host Controller. All functions support both master and target accesses, and share the same PCI interrupt signal INTA#. These functions provide memory-mapped, addressable operational registers as required in *Open Host Controller Interface Specification for USB Rev. 1.0a* and *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*.

Each function has its own configuration space. The PCI enumerator should allocate the memory address space for each of these functions. Power management is implemented in each PCI function and all power states are provided. This allows the system to achieve low power consumption by switching off the functions that are not required.

8.1.1 PCI configuration space

PCI Local Bus Specification Rev. 2.2 requires that each of the three PCI functions of the SAF1562HL provides its own PCI configuration registers, which can vary in size. In addition to the basic PCI configuration header registers, these functions implement capability registers to support power management.

The registers of each of these functions are accessed by the respective driver. Section 8.2 provides a detailed description of the various PCI configuration registers.

8.1.2 PCI initiator and target

A PCI initiator initiates PCI transactions to the PCI bus. A PCI target responds to PCI transactions as a slave. In the case of the SAF1562HL, the two Open Host Controllers and the Enhanced Host Controller function as both initiators or targets of PCI transactions issued by the host CPU.

All USB Host Controllers have their own operational registers that can be accessed by the system driver software. Drivers use these registers to configure the Host Controller hardware system, issue commands to it, and monitor the status of the current hardware operation. The Host Controller plays the role of a PCI target. All operational registers of the Host Controllers are the PCI transaction targets of the CPU.

Normal USB transfers require the Host Controller to access system memory fields, which are allocated by USB HCDs and PCI drivers. The Host Controller hardware interacts with the HCD by accessing these buffers. The Host Controller works as an initiator in this case and becomes a PCI master.

8.2 PCI configuration registers

The OHCI USB Host Controllers and the EHCI USB Host Controller contain two sets of software-accessible hardware registers: PCI configuration registers and memory-mapped Host Controller registers.

A set of configuration registers is implemented for each of the three PCI functions of the SAF1562HL, see Table 3.

Remark: In addition to the normal PCI header, from offset index 00h to 3Fh, implementation-specific registers are defined to support power management and function-specific features.

Table 3. PCI configuration space registers of OHCI1, OHCI2 and EHCI

Address	Bits 31 to 24	Bits 23 to 16	Bits 15 to 8	Bits 7 to 0	Reset value[1]		
					Func0 OHCI1	Func1 OHCI2	Func2 EHCI
PCI configuration header registers							
00h	Device ID[15:0]		Vendor ID[15:0]		1561 1131h	1561 1131h	1562 1131h
04h	Status[15:0]		Command[15:0]		0210 **0000**h	0210 **0000**h	0210 **0000**h
08h	Class Code[23:0]			Revision ID[7:0]	0C03 1012h	0C03 1012h	0C03 2012h
0Ch	reserved	Header Type[7:0]	Latency Timer[7:0]	Cache Line Size[7:0]	0080 **0000**h	0080 **0000**h	0080 **0000**h
10h	Base Address 0[31:0]				**0000 0**000h	**0000 0**000h	**0000 00**00h
14h	reserved				0000 0000h	0000 0000h	0000 0000h
18h							
1Ch							
20h							
24h							
28h							
2Ch	Subsystem ID[15:0]		Subsystem Vendor ID[15:0]		1561 1131h	1561 1131h	1562 1131h
30h	reserved				0000 0000h	0000 0000h	0000 0000h
34h	reserved			Capabilities Pointer[7:0]	0000 00DCh	0000 00DCh	0000 00DCh
38h	reserved				0000 0000h	0000 0000h	0000 0000h
3Ch	Max_ Lat[7:0]	Min_Gnt[7:0]	Interrupt Pin[7:0]	Interrupt Line[7:0]	2A01 01**00**h	2A01 01**00**h	1002 01**00**h
40h	reserved		Retry time-out	TRDY time-out	0000 **8000**h	0000 **8000**h	0000 **8000**h
Enhanced Host Controller-specific PCI registers							
60h	PORTWAKECAP[15:0]		FLADJ[7:0]	SBRN[7:0]	-	-	**0007 20**20h
Power management registers							
DCh	PMC[15:0]		Next_Item_Ptr [7:0]	Cap_ID[7:0]	D282 0001h	D282 0001h	FE82 0001h
E0h	Data[7:0]	PMCSR_BSE [7:0]	PMCSR[15:0]		0000 **XX00**h[2]	0000 **XX00**h[2]	0000 **XX00**h[2]

[1] Reset values that are highlighted—for example, **0**—indicate read and write accesses; and reset values that are not highlighted—for example, 0—indicate read-only.

[2] See Section 8.2.3.4.

The HCD does not usually interact with the PCI configuration space. The configuration space is used only by the PCI enumerator to identify the USB Host Controller and assign appropriate system resources by reading the Vendor ID (VID) and the Device ID (DID).

8.2.1 PCI configuration header registers

The Enhanced Host Controller implements the normal PCI header register values, except the values for the memory-mapping base address register, serial bus number and Device ID.

8.2.1.1 Vendor ID register

This read-only register identifies the manufacturer of the device. PCI Special Interest Group (PCI-SIG) assigns valid vendor identifiers to ensure the uniqueness of the identifier. The bit description is shown in Table 4.

Table 4. VID - Vendor ID register (address 00h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	VID[15:0]	R	1131h*	**Vendor ID**: This read-only register value is assigned to NXP Semiconductors by PCI-SIG as 1131h.

8.2.1.2 Device ID register

This is a 2 B read-only register that identifies a particular device. The identifier is allocated by NXP Semiconductors. Table 5 shows the bit description of the register.

Table 5. DID - Device ID register (address 02h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	DID[15:0]	R	156Xh*[1]	**Device ID**: This register value is defined by NXP Semiconductors to identify the USB Host Controller IC product.

[1] X is 1h for OHCI1 and OHCI2; X is 2h for EHCI.

8.2.1.3 Command register

This is a 2 B register that provides coarse control over the ability of a device to generate and respond to PCI cycles. The bit allocation of the Command register is given in Table 6. When logic 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses, except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command register may or may not support this base level of functionality.

Table 6. Command register (address 04h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved[1]						FBBE	SERRE
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SCTRL	PER	VGAPS	MWIE	SC	BM	MS	IOS
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R	R/W	R	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 7. Command register (address 04h) bit description

Bit	Symbol	Description
15 to 10	reserved	-
9	FBBE	**Fast Back-to-Back Enable**: This bit controls whether a master can do fast back-to-back transactions to various devices. The initialization software must set this bit if all targets are fast back-to-back capable. **0 —** Fast back-to-back transactions are only allowed to the same agent (value after RST#). **1 —** The master is allowed to generate fast back-to-back transactions to different agents.
8	SERRE	**SERR# Enable**: This bit is an enable bit for the SERR# driver. All devices that have an SERR# pin must implement this bit. Address parity errors are reported only if this bit and the PER bit are logic 1. **0 —** Disable the SERR# driver. **1 —** Enable the SERR# driver.
7	SCTRL	**Stepping Control**: This bit controls whether a device does address and data stepping. Devices that never do stepping must clear this bit. Devices that always do stepping must set this bit. Devices that can do either, must make this bit read and write, and initialize it to logic 1 after RST#.
6	PER	**Parity Error Response**: This bit controls the response of a device to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is logic 0, the device sets DPE (bit 15 in the Status register) when an error is detected, but does not assert PERR# and continues normal operation. The state of this bit after RST# is logic 0. Devices that check parity must implement this bit. Devices are required to generate parity, even if parity checking is disabled.
5	VGAPS	**VGA Palette Snoop**: This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. **0 —** The device should treat palette write accesses like all other accesses. **1 —** Palette snooping is enabled, that is, the device does not respond to palette register writes and snoops data. VGA compatible devices should implement this bit.
4	MWIE	**Memory Write and Invalidate Enable**: This is an enable bit for using the Memory Write and Invalidate command. **0 —** Memory Writes must be used instead. State after RST# is logic 0. **1 —** Masters may generate the command. This bit must be implemented by master devices that can generate the Memory Write and Invalidate command.
3	SC	**Special Cycles**: Controls the action of a device on Special Cycle operations. **0 —** Causes the device to ignore all Special Cycle operations. State after RST# is logic 0. **1 —** Allows the device to monitor Special Cycle operations.

Table 7. Command register (address 04h) bit description *...continued*

Bit	Symbol	Description
2	BM	**Bus Master**: Controls the ability of a device to act as a master on the PCI bus. **0 —** Disables the device from generating PCI accesses. State after RST# is logic 0. **1 —** Allows the device to behave as a bus master.
1	MS	**Memory Space**: Controls the response of a device to Memory Space accesses. **0 —** Disables the device response. State after RST# is logic 0. **1 —** Allows the device to respond to memory space accesses.
0	IOS	**IO Space**: Controls the response of a device to I/O space accesses. **0 —** Disables the device response. State after RST# is logic 0. **1 —** Allows the device to respond to I/O space accesses.

8.2.1.4 Status register

The Status register is a 2 B read-only register used to record status information on PCI bus-related events. For bit allocation, see Table 8.

Table 8. Status register (address 06h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	DPE	SSE	RMA	RTA	STA	DEVSELT[1:0]		MDPE
Reset	0	0	0	0	0	0	1	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FBBC	reserved	66MC	CL	reserved			
Reset	0	0	0	1	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 9. Status register (address 06h) bit description

Bit	Symbol	Description
15	DPE	**Detected Parity Error**: This bit must be set by the device whenever it detects a parity error, even if the parity error handling is disabled.
14	SSE	**Signaled System Error**: This bit must be set whenever the device asserts SERR#. Devices that never assert SERR# do not need to implement this bit.
13	RMA	**Received Master Abort**: This bit must be set by a master device whenever its transaction, except for Special Cycle, is terminated with Master-Abort. All master devices must implement this bit.
12	RTA	**Received Target Abort**: This bit must be set by a master device whenever its transaction is terminated with Target-Abort. All master devices must implement this bit.
11	STA	**Signaled Target Abort**: This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that never signal Target-Abort do not need to implement this bit.

Table 9. Status register (address 06h) bit description *...continued*

Bit	Symbol	Description
10 and 9	DEVSELT [1:0]	**DEVSEL Timing**: These bits encode the timing of DEVSEL#. There are three allowable timing to assert DEVSEL#: **00b —** Fast **01b —** Medium **10b —** Slow **11b —** Reserved These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command, except Configuration Read and Configuration Write.
8	MDPE	**Master Data Parity Error**: This bit is implemented by bus masters. It is set when the following three conditions are met: • The bus agent asserted PERR# itself, on a read; or observed PERR# asserted, on a write • The agent setting the bit acted as the bus master for the operation in which error occurred • PER (bit 6 in the Command register) is set
7	FBBC	**Fast Back-to-Back Capable**: This read-only bit indicates whether the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to logic 1, if the device can accept these transactions; and must be set to logic 0 otherwise.
6	reserved	-
5	66MC	**66 MHz Capable**: This read-only bit indicates whether this device is capable of running at 66 MHz. **0 —** 33 MHz **1 —** 66 MHz
4	CL	**Capabilities List**: This read-only bit indicates whether this device implements the pointer for a new capabilities linked list at offset 34h. **0 —** No new capabilities linked list is available **1 —** The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities
3 to 0	reserved	-

8.2.1.5 Revision ID register

This 1 B read-only register indicates a device-specific revision identifier. The value is chosen by the vendor. This field is a vendor-defined extension of the Device ID. The Revision ID register bit description is given in Table 10.

Table 10. REVID - Revision ID register (address 08h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	REVID[7:0]	R	12h*	**Revision ID**: This byte specifies the design revision number of functions.

8.2.1.6 Class Code register

Class Code is a 24-bit read-only register used to identify the generic function of the device, and in some cases, a specific register-level programming interface. Table 11 shows the bit allocation of the register.

The Class Code register is divided into three byte-size fields. The upper byte is a base class code that broadly classifies the type of function the device performs. The middle byte is a sub-class code that identifies more specifically the function of the device. The lower byte identifies a specific register-level programming interface, if any, so that device-independent software can interact with the device.

Table 11. Class Code register (address 09h) bit allocation

Bit	23	22	21	20	19	18	17	16
Symbol	BCC[7:0]							
Reset	0Ch							
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	SCC[7:0]							
Reset	03h							
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RLPI[7:0]							
Reset	X0h[1]							
Access	R	R	R	R	R	R	R	R

[1] X is 1h for OHCI1 and OHCI2; X is 2h for EHCI.

Table 12. Class Code register (address 09h) bit description

Bit	Symbol	Description
23 to 16	BCC[7:0]	**Base Class Code**: 0Ch is the base class code assigned to this byte. It implies a serial bus controller.
15 to 8	SCC[7:0]	**Sub-Class Code**: 03h is the sub-class code assigned to this byte. It implies the USB Host Controller.
7 to 0	RLPI[7:0]	**Register-Level Programming Interface**: 10h is the programming interface code assigned to OHCI, which is USB 1.1 specification compliant. 20h is the programming interface code assigned to EHCI, which is USB 2.0 specification compliant.

8.2.1.7 Cache Line Size register

The Cache Line Size register is a read and write single-byte register that specifies the system Cache Line size in units of double word. This register must be implemented by master devices that can generate the Memory Write and Invalidate command. The value in this register is also used by master devices to determine whether to use Read, Read Line or Read Multiple command to access the memory.

Slave devices that want to allow memory bursting using a Cache Line-wrap addressing mode must implement this register to know when a burst sequence wraps to the beginning of the Cache Line.

This field must be initialized to logic 0 on activation of RST#. Table 13 shows the bit description of the Cache Line Size register.

Table 13. CLS - Cache Line Size register (address 0Ch) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	CLS[7:0]	R/W	00h*	**Cache Line Size**: This byte identifies the system Cache Line size.

8.2.1.8 Latency Timer register

This register specifies—in units of PCI bus clocks—the value of the Latency Timer for the PCI bus master. Table 14 shows the bit description of the Latency Timer register.

Table 14. LT - Latency Timer register (address 0Dh) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	LT[7:0]	R/W	00h*	**Latency Timer**: This byte identifies the latency timer.

Remark: It is recommended to set the value of the Latency Timer register to 20h.

8.2.1.9 Header Type register

The Header Type register identifies the layout of the second part of the predefined header, beginning at byte 10h in configuration space. It also identifies whether the device contains multiple functions. For bit allocation, see Table 15.

Table 15. Header Type register (address 0Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MFD	HT[6:0]						
Reset	1	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 16. Header Type register (address 0Eh) bit description

Bit	Symbol	Description
7	MFD	**Multi-Function Device**: This bit identifies a multifunction device. **0 —** The device has single function **1 —** The device has multiple functions
6 to 0	HT[6:0]	**Header Type**: These bits identify the layout of the part of the predefined header, beginning at byte 10h in configuration space.

8.2.1.10 Base Address register 0

Power-up software must build a consistent address map before booting the machine to an operating system. This means it must determine how much memory is in the system, and how much address space the I/O controllers in the system require. After determining this information, power-up software can map the I/O controllers into reasonable locations and proceed with system boot. To do this mapping in a device-independent manner, the base registers for this mapping are placed in the predefined header portion of configuration space.

Bit 0 in all Base Address registers is read-only and used to determine whether the register maps into memory or I/O space. Base Address registers that map to memory space must return logic 0 in bit 0. Base Address registers that map to I/O space must return logic 1 in bit 0.

The bit description of the BAR 0 register is given in Table 17.

Table 17. BAR 0 - Base Address register 0 (address 10h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	BAR 0[31:0]	R/W	0000 0000h*	**Base Address to Memory-Mapped Host Controller Register Space**: The memory size required by OHCI and EHCI are 4 kB and 256 B, respectively. Therefore, BAR 0[31:12] is assigned to the two OHCI ports, and BAR 0[31:8] is assigned to the EHCI port.

8.2.1.11 Subsystem Vendor ID register

The Subsystem Vendor ID register is used to uniquely identify the expansion board or subsystem where the PCI device resides. This register allows expansion board vendors to distinguish their boards, even though the boards may have the same Vendor ID and Device ID.

Subsystem Vendor IDs are assigned by PCI-SIG to maintain uniqueness. The bit description of the Subsystem Vendor ID register is given in Table 18.

Table 18. SVID - Subsystem Vendor ID register (address 2Ch) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	SVID[15:0]	R	1131h*	**Subsystem Vendor ID**: 1131h is the subsystem Vendor ID assigned to NXP Semiconductors.

8.2.1.12 Subsystem ID register

Subsystem ID values are vendor specific. The bit description of the Subsystem ID register is given in Table 19.

Table 19. SID - Subsystem ID register (address 2Eh) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	SID[15:0]	R	156Xh*[1]	**Subsystem ID**: For the SAF1562HL, NXP Semiconductors has defined OHCI functions as 1561h, and the EHCI function as 1562h.

[1] X is 1h for OHCI1 and OHCI2; X is 2h for EHCI.

8.2.1.13 Capabilities Pointer register

This register is used to point to a linked list of new capabilities implemented by the device. This register is only valid if CL (bit 4 in the Status register) is set. If implemented, bit 1 and bit 0 are reserved and should be set to 00b. Software should mask these bits off before using this register as a pointer in configuration space to the first entry of a linked list of new capabilities. The bit description of the register is given in Table 20.

Table 20. CP - Capabilities Pointer register (address 34h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	CP[7:0]	R	DCh*	**Capabilities Pointer**: EHCI efficiently manages power using this register. This Power Management register is allocated at offset DCh. Only one Host Controller is needed to manage power in the SAF1562HL.

8.2.1.14 Interrupt Line register

This is a 1 B register used to communicate interrupt line routing information. This register must be implemented by any device or device function that uses an interrupt pin. The interrupt allocation is done by the BIOS. The POST software needs to write the routing information to this register because it initializes and configures the system.

The value in this register specifies which input of the system interrupt controller(s) the interrupt pin of the device is connected. This value is used by device drivers and operating systems to determine priority and vector information. Values in this register are system architecture specific. The bit description of the register is given in Table 21.

Table 21. IL - Interrupt Line register (address 3Ch) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	IL[7:0]	R/W	00h*	**Interrupt Line**: Indicates which IRQ is used to report interrupt from the SAF1562HL.

8.2.1.15 Interrupt Pin register

This 1 B register is use to specify which interrupt pin the device or device function uses.

A value of 1h corresponds to INTA#, 2h corresponds to INTB#, 3h corresponds to INTC#, and 4h corresponds to INTD#. Devices or functions that do not use interrupt pin must set this register to logic 0. The bit description is given in Table 22.

Table 22. IP - Interrupt Pin register (address 3Dh) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	IP[7:0]	R	01h*	**Interrupt Pin**: INTA# is the default interrupt pin used by the SAF1562HL.

8.2.1.16 Min_Gnt and Max_Lat registers

The Minimum Grant (Min_Gnt) and Maximum Latency (Max_Lat) registers are used to specify the desired settings of the device for latency timer values. For both registers, the value specifies a period of time in units of 250 ns. Logic 0 indicates that the device has no major requirements for setting latency timers.

The Min_Gnt register bit description is given in Table 23.

Table 23. Min_Gnt - Minimum Grant register (address 3Eh) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	MIN_GNT [7:0]	R	0Xh*[1]	**Min_Gnt**: It is used to specify how long a burst period the device needs, assuming a clock rate of 33 MHz.

[1] X is 1h for OHCI1 and OHCI2; X is 2h for EHCI.

The Max_Lat register bit description is given in Table 24.

Table 24. Max_Lat - Maximum Latency register (address 3Fh) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	MAX_LAT [7:0]	R	XXh*[1]	**Max_Lat**: It is used to specify how often the device needs to gain access to the PCI bus.

[1] XX is 2Ah for OHCI1 and OHCI2; XX is 10h for EHCI.

8.2.1.17 TRDY time-out register

This is a read and write register at address 40h. The default and recommended value is 00h—TRDY time-out disabled. This value can, however, be modified. It is an implementation-specific register, and not a standard PCI configuration register.

The TRDY timer is 13 bits—the lower 5 bits are fixed as logic 0, and the upper 8 bits are determined by the TRDY time-out register value. The time-out is calculated by multiplying the 13-bit timer with the PCI CLK cycle time.

This register determines the maximum TRDY delay without asserting the Unrecoverable Error (UE) bit. If TRDY is longer than the delay determined by this register value, then the UE bit will be set.

8.2.1.18 Retry time-out register

The default value of this read and write register is 80h, and is located at address 41h. This value can, however, be modified. Programming this register as 00h means that retry time-out is disabled. This is an implementation-specific register, and not a standard PCI configuration register.

The time-out is determined by multiplying the register value with the PCI CLK cycle time. This register determines the maximum number of PCI retires before the UE bit is set. If the number of retries is longer than the delay determined by this register value, then the UE bit will be set.

Remark: It is recommended to set the value of the Retry time-out register to 00h.

8.2.2 Enhanced Host Controller-specific PCI registers

In addition to the PCI configuration header registers, EHCI needs some additional PCI configuration space registers to indicate the serial bus release number, downstream port wake-up event capability, and adjust the USB bus frame length for Start-of-Frame (SOF). The EHCI-specific PCI registers are given in Table 25.

Table 25. EHCI-specific PCI registers

Offset	Register
60h	Serial Bus Release Number (SBRN)
61h	Frame Length Adjustment (FLADJ)
62h and 63h	Port Wake Capability (PORTWAKECAP)

8.2.2.1 SBRN register

The Serial Bus Release Number (SBRN) register is a 1 B register, and the bit description is given in Table 26. This register contains the release number of the USB specification with which this USB Host Controller module is compliant.

Table 26. SBRN - Serial Bus Release Number register (address 60h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	SBRN[7:0]	R	20h*	**Serial Bus Specification Release Number**: This register value is to identify Serial Bus Specification Rev. 2.0. All other combinations are reserved.

8.2.2.2 FLADJ register

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written to these six bits, the length of the frame is adjusted. The bit allocation of the Frame Length Adjustment (FLADJ) register is given in Table 27.

Table 27. FLADJ - Frame Length Adjustment register (address 61h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]		FLADJ[5:0]					
Reset	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 28. FLADJ - Frame Length Adjustment register (address 61h) bit description

Bit	Symbol	Description
7 and 6	reserved	-
5 to 0	FLADJ[5:0]	**Frame Length Timing Value**: Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time—number of SOF counter clock periods to generate a SOF micro frame length—is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000.

FLADJ value	SOF cycle time (480 MHz)
0 (00h)	59488
1 (01h)	59504
2 (02h)	59520
:	:
31 (1Fh)	59984
32 (20h)	60000
:	:
62 (3Eh)	60480
63 (3Fh)	60496

8.2.2.3 PORTWAKECAP register

Port Wake Capability (PORTWAKECAP) is a 2 B register used to establish a policy about which ports are for wake events; see Table 29. Bit positions 15 to 1 in the mask correspond to a physical port implemented on the current EHCI controller. Logic 1 in a bit position indicates that a device connected below the port can be enabled as a wake-up device and the port may be enabled for disconnect or connect, or overcurrent events as wake-up events. This is an information only mask register. The bits in this register do not affect the actual operation of the EHCI Host Controller. The system-specific policy can be established by BIOS initializing this register to a system-specific value. The system software uses the information in this register when enabling devices and ports for remote wake-up.

Table 29. PORTWAKECAP - Port Wake Capability register (address 62h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	PORTWAKECAP [15:0]	R/W	0007h*	**Port Wake-Up Capability Mask**: EHCI does not implement this feature.

8.2.3 Power management registers

Table 30. Power Management registers

Offset	Register
Value read from address 34h + 0h	Capability Identifier (Cap_ID)
Value read from address 34h + 1h	Next Item Pointer (Next_Item_Ptr)
Value read from address 34h + 2h	Power Management Capabilities (PMC)
Value read from address 34h + 4h	Power Management Control/Status (PMCSR)
Value read from address 34h + 6h	Power Management Control/Status PCI-to-PCI Bridge Support Extensions (PMCSR_BSE)
Value read from address 34h + 7h	Data

8.2.3.1 Cap_ID register

The Capability Identifier (Cap_ID) register when read by the system software as 01h indicates that the data structure currently being pointed to is the PCI Power Management data structure. Each function of a PCI device may have only one item in its capability list with Cap_ID set to 01h. The bit description of the register is given in Table 31.

Table 31. Cap_ID - Capability Identifier register bit description
Address: Value read from address 34h + 0h
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	CAP_ID[7:0]	R	01h*	**ID**: This field when 01h identifies the linked list item as being PCI Power Management registers.

8.2.3.2 Next_Item_Ptr register

The Next Item Pointer (Next_Item_Ptr) register describes the location of the next item in the function's capability list. The value given is an offset into the function's PCI configuration space. If the function does not implement any other capabilities defined by the PCI-SIG for inclusion in the capabilities list, or if power management is the last item in the list, then this register must be set to 00h. See Table 32.

Table 32. Next_Item_Ptr - Next Item Pointer register bit description

Address: Value read from address 34h + 1h

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	NEXT_ITEM_PTR[7:0]	R	00h*	**Next Item Pointer**: This field provides an offset into the function's PCI configuration space, pointing to the location of the next item in the function's capability list. If there are no additional items in the capabilities list, this register is set to 00h.

8.2.3.3 PMC register

The Power Management Capabilities (PMC) register is a 2 B register, and the bit allocation is given in Table 33. This register provides information on the capabilities of the function related to power management.

Table 33. PMC - Power Management Capabilities register bit allocation

Address: Value read from address 34h + 2h

Bit	15	14	13	12	11	10	9	8
Symbol	PME_S[4:0]					D2_S	D1_S	AUX_C
Reset	1	1	X[1]	1	X[1]	X[1]	1	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	AUX_C[1:0]		DSI	reserved	PMI	VER[2:0]		
Reset	1	0	0	0	0	0	1	0
Access	R	R	R	R	R	R	R	R

[1] X = logic 0 for OHCI1 and OHCI2; X = logic 1 for EHCI.

Table 34. PMC - Power Management Capabilities register bit description

Address: Value read from address 34h + 2h

Bit	Symbol	Description
15 to 11	PME_S[4:0]	**PME_Support**: These bits indicate the power states in which the function may assert PME#. Logic 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. **PME_S[0] —** PME# can be asserted from D0 **PME_S[1] —** PME# can be asserted from D1 **PME_S[2] —** PME# can be asserted from D2 **PME_S[3] —** PME# can be asserted from $D3_{hot}$ **PME_S[4] —** PME# can be asserted from $D3_{cold}$
10	D2_S	**D2_Support**: If this bit is logic 1, this function supports the D2 Power Management State. Functions that do not support D2 must always return logic 0 for this bit.
9	D1_S	**D1_Support**: If this bit is logic 1, this function supports the D1 Power Management State. Functions that do not support D1 must always return logic 0 for this bit.

Table 34. PMC - Power Management Capabilities register bit description *...continued*

Address: Value read from address 34h + 2h

Bit	Symbol	Description
8 to 6	AUX_C [2:0]	**Aux_Current**: This three-bit field reports the $V_{aux(3V3)}$ auxiliary current requirements for the PCI function. If the Data register is implemented by this function: • A read from this field needs to return a value of 000b • The Data register takes precedence over this field for $V_{aux(3V3)}$ current requirement reporting If the PME# generation from $D3_{cold}$ is not supported by the function (PMC[15] = logic 0), this field must return a value of 000b when read. For functions that support PME# from $D3_{cold}$ and do not implement the Data register, the bit assignments corresponding to the maximum current required for $V_{aux(3V3)}$ are: **111b —** 375 mA **110b —** 320 mA **101b —** 270 mA **100b —** 220 mA **011b —** 160 mA **010b —** 100 mA **001b —** 55 mA **000b —** 0 (self powered)
5	DSI	**Device Specific Initialization**: This bit indicates whether special initialization of this function is required, beyond the standard PCI configuration header, before the generic class device driver is able to use it. This bit is not used by some operating systems. For example, Microsoft Windows and Windows NT do not use this bit to determine whether to use D3. Instead, it is determined using the capabilities of the driver. Logic 1 indicates that the function requires a device-specific initialization sequence, following transition to D0 un-initialized state.
4	reserved	-
3	PMI	**PME Clock**: **0 —** Indicates that no PCI clock is required for the function to generate PME# **1 —** Indicates that the function relies on the presence of the PCI clock for the PME# operation Functions that do not support the PME# generation in any state must return logic 0 for this field.
2 to 0	VER[2:0]	**Version**: A value of 010b indicates that this function complies with *PCI Bus Power Management Interface Specification Rev. 1.1*.

8.2.3.4 PMCSR register

The Power Management Control/Status Register (PMCSR) is a 2 B register used to manage the power management state of the PCI function, as well as to allow and monitor Power Management Events (PMEs). The bit allocation of the register is given in Table 35.

Table 35. PMCSR - Power Management Control/Status register bit allocation

Address: Value read from address 34h + 4h

Bit	15	14	13	12	11	10	9	8
Symbol	PMES	DS[1:0]		D_S[3:0]				PMEE
Reset	X[1]	0	0	0	0	0	0	X[1]
Access	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[2]						PS[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] Sticky bit, if the function supports PME# from $D3_{cold}$, then X is indeterminate at the time of initial operating system boot; X is 0 if the function does not support PME# from $D3_{cold}$.

[2] The reserved bits should always be written with the reset value.

Table 36. PMCSR - Power Management Control/Status register bit description

Address: Value read from address 34h + 4h

Bit	Symbol	Description
15	PMES	**PME Status**: This bit is set when the function normally asserts the PME# signal independent of the state of the PMEE bit. Writing logic 1 to this bit clears it and causes the function to stop asserting PME#, if enabled. Writing logic 0 has no effect. This bit defaults to logic 0, if the function does not support the PME# generation from $D3_{cold}$. If the function supports the PME# generation from $D3_{cold}$, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
14 and 13	DS[1:0]	**Data Scale**: This two-bit read-only field indicates the scaling factor when interpreting the value of the Data register. The value and meaning of this field vary, depending on which data value is selected by the D_S field. This field is a required component of the Data register (offset 7) and must be implemented, if the Data register is implemented. If the Data register is not implemented, this field must return 00b when PMCSR is read.
12 to 9	D_S[3:0]	**Data_Select**: This four-bit field selects the data that is reported through the Data register and the D_S field. This field is a required component of the Data register (offset 7) and must be implemented, if the Data register is implemented. If the Data register is not implemented, this field must return 00b when PMCSR is read.

Table 36. PMCSR - Power Management Control/Status register bit description *…continued*

Address: Value read from address 34h + 4h

Bit	Symbol	Description
8	PMEE	**PME Enabled**: Logic 1 allows the function to assert PME#. When it is logic 0, PME# assertion is disabled. This bit defaults to logic 0, if the function does not support the PME# generation from $D3_{cold}$. If the function supports PME# from $D3_{cold}$, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
7 to 2	reserved	-
1 and 0	PS[1:0]	**Power State**: This two-bit field is used to determine the current power state of the EHCI function and to set the function into a new power state. The definition of the field values is given as: **00b —** D0 **01b —** D1 **10b —** D2 **11b —** $D3_{hot}$ If the software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no status change occurs.

8.2.3.5 PMCSR_BSE register

The PMCSR PCI-to-PCI Bridge Support Extensions (PMCSR_BSE) register supports PCI bridge-specific functionality and is required for all PCI-to-PCI bridges. The bit allocation of this register is given in Table 37.

Table 37. PMCSR_BSE - PMCSR PCI-to-PCI Bridge Support Extensions register bit allocation

Address: Value read from address 34h + 6h

Bit	7	6	5	4	3	2	1	0
Symbol	BPCC_EN	B2_B3#	reserved					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 38. PMCSR_BSE - PMCSR PCI-to-PCI Bridge Support Extensions register bit description

Address: Value read from address 34h + 6h

Bit	Symbol	Description
7	BPCC_EN	**Bus Power/Clock Control Enable**: **1 —** Indicates that the bus power or clock control mechanism as defined in Table 39 is enabled **0 —** Indicates that the bus or power control policies as defined in Table 39 are disabled When the Bus Power or Clock Control mechanism is disabled, the bridge's PMCSR Power State (PS) field cannot be used by the system software to control the power or clock of the bridge's secondary bus.
6	B2_B3#	**B2/B3 support for $D3_{hot}$**: The state of this bit determines the action that is to occur as a direct result of programming the function to $D3_{hot}$. **1 —** Indicates that when the bridge function is programmed to $D3_{hot}$, its secondary bus's PCI clock will be stopped (B2) **0 —** Indicates that when the bridge function is programmed to $D3_{hot}$, its secondary bus will have its power removed (B3) This bit is only meaningful if bit 7 (BPCC_EN) is logic 1.
5 to 0	reserved	-

Table 39. PCI bus power and clock control

Originating device's bridge PM state	Secondary bus PM state	Resultant actions by bridge (either direct or indirect)
D0	B0	none
D1	B1	none
D2	B2	clock stopped on secondary bus
$D3_{hot}$	B2, B3	clock stopped and PCI V_{CC} removed from secondary bus (B3 only); for definition of B2_B3#, see Table 38
$D3_{cold}$	B3	none

8.2.3.6 Data register

The Data register is an optional, 1 B register that provides a mechanism for the function to report state dependent operating data, such as power consumed or heat dissipated. Table 40 shows the bit description of the register.

Table 40. Data register bit description

Address: Value read from address 34h + 7h

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	DATA[7:0]	R	00h*	**DATA**: This register is used to report the state dependent data requested by the D_S field of the PMCSR register. The value of this register is scaled by the value reported by the DS field of the PMCSR register.

9. I²C-bus interface

A simple I²C-bus interface is provided in the SAF1562HL to read customized vendor ID, product ID and some other configuration bits from an external EEPROM.

The I²C-bus interface is for bidirectional communication between ICs using two serial bus wires: SDA (data) and SCL (clock). Both lines are driven by open-drain circuits and must be connected to the positive supply voltage through pull-up resistors when in use; otherwise, they must be connected to ground.

9.1 Protocol

The I²C-bus protocol defines the following conditions:

- **Bus free**: both SDA and SCL are HIGH
- **START**: a HIGH-to-LOW transition on SDA, while SCL is HIGH
- **STOP**: a LOW-to-HIGH transition on SDA, while SCL is HIGH
- **Data valid**: after a START condition, data on SDA is stable during the HIGH period of SCL; data on SDA may only change while SCL is LOW

Each device on the I²C-bus has a unique slave address, which the master uses to select a device for access.

The master starts a data transfer using a START condition and ends it by generating a STOP condition. Transfers can only be initiated when the bus is free. The receiver must acknowledge each byte by using a LOW level on SDA during the ninth clock pulse on SCL.

For detailed information, refer to *The I²C-bus Specification, Version 2.1*.

9.2 Hardware connections

The SAF1562HL can be connected to an external EEPROM through the I²C-bus interface. The hardware connections are shown in Figure 6.

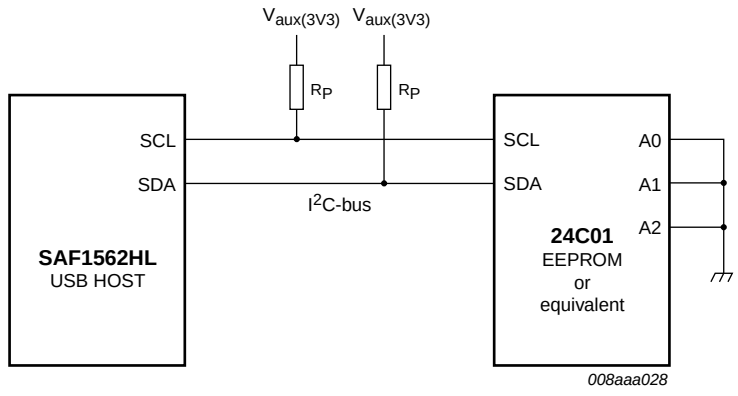
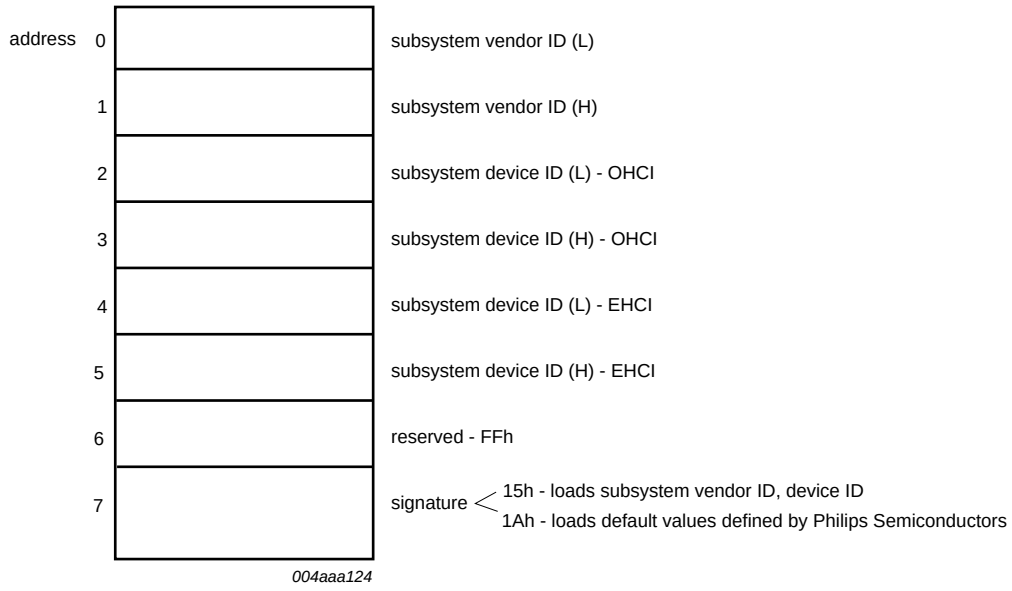


Fig 6. EEPROM connection diagram

The slave address that the SAF1562HL uses to access the EEPROM is 1010 000b. Page mode addressing is not supported. Therefore, pins A0, A1 and A2 of the EEPROM must be connected to ground (logic 0).

9.3 Information loading from EEPROM

Figure 7 shows the content of the EEPROM memory. If the EEPROM is not present, the default values of Device ID, Vendor ID, subsystem VID and subsystem DID assigned to NXP Semiconductors by PCI-SIG will be loaded. For default values, see Table 3.



L = LOW; H = HIGH.

Fig 7. Information loading from EEPROM

10. Power management

10.1 PCI bus power states

The PCI bus can be characterized by one of the four power management states: B0, B1, B2 and B3.

B0 state (PCI clock = 33 MHz, PCI bus power = on) — This corresponds to the bus being fully operational.

B1 state (PCI clock = intermittent clock operation mode, PCI bus power = on) — When a PCI bus is in B1, PCI V_{CC} is still applied to all devices on the bus. No bus transactions, however, are allowed to take place on the bus. The B1 state indicates a perpetual idle state on the PCI bus.

B2 state (PCI clock = stop, PCI bus power = on) — PCI V_{CC} is still applied on the bus, but the clock is stopped and held in the LOW state.

B3 state (PCI clock = stop, PCI bus power = off) — PCI V_{CC} is removed from all devices on the PCI bus segment.

10.2 USB bus states

Reset state — When the USB bus is in the reset state, the USB system is stopped.

Operational state — When the USB bus is in the active state, the USB system is operating normally.

Suspend state — When the USB bus is in the suspend state, the USB system is stopped.

Resume state — When the USB bus is in the resume state, the USB system is operating normally.

11. USB Host Controller registers

Each Host Controller contains a set of on-chip operational registers that are mapped to un-cached memory of the system addressable space. This memory space must begin on a double word (32-bit) boundary. The size of the allocated space is defined by the initial value in the Base Address register 0. HCDs must interact with these registers to implement USB functionality.

After the PCI enumeration driver finishes the PCI device configuration, the new base address of these memory-mapped operational registers is defined in BAR 0. The HCD can access these registers by using the address of base address value + offset.

Table 41 contains a list of Host Controller registers.

Table 41. USB Host Controller registers

Address	OHCI register	Reset value[1]		EHCI register	Reset value[1]
		Func0 OHCI1	Func1 OHCI2		Func2 EHCI
00h	HcRevision	0000 0**010**h	0000 0**010**h	CAPLENGTH/HCIVERSION[2]	**0100 0020**h
04h	HcControl	0000 0000h	0000 0000h	HCSPARAMS	**0000 2192**h
08h	HcCommandStatus	0000 0000h	0000 0000h	HCCPARAMS	**0000 0012**h
0Ch	HcInterruptStatus	0000 0000h	0000 0000h	HCSP-PORTROUTE1[31:0]	**0000 0010**h
10h	HcInterruptEnable	0000 0000h	0000 0000h	HCSP-PORTROUTE2[59:32]	**0000 0000**h
14h	HcInterruptDisable	0000 0000h	0000 0000h	reserved	-
18h	HcHCCA	0000 0000h	0000 0000h	reserved	-
1Ch	HcPeriodCurrentED	0000 0000h	0000 0000h	reserved	-
20h	HcControlHeadED	0000 0000h	0000 0000h	USBCMD	0008 0000h
24h	HcControlCurrentED	0000 0000h	0000 0000h	USBSTS	0000 1000h
28h	HcBulkHeadED	0000 0000h	0000 0000h	USBINTR	0000 0000h
2Ch	HcBulkCurrentED	0000 0000h	0000 0000h	FRINDEX	0000 0000h
30h	HcDoneHead	0000 0000h	0000 0000h	reserved	-
34h	HcFmInterval	0000 2EDFh	0000 2EDFh	PERIODICLISTBASE	0000 0000h
38h	HcFmRemaining	0000 0000h	0000 0000h	ASYNCLISTADDR	0000 0000h
3Ch	HcFmNumber	0000 0000h	0000 0000h	reserved	-
40h	HcPeriodicStart	0000 0000h	0000 0000h	reserved	-
44h	HcLSThreshold	0000 0628h	0000 0628h	reserved	-
48h	HcRhDescriptorA	**FF00 0901**h	**FF00 0901**h	reserved	-

Table 41. USB Host Controller registers *...continued*

Address	OHCI register	Reset value[1]		EHCI register	Reset value[1]
		Func0 OHCI1	Func1 OHCI2		Func2 EHCI
4Ch	HcRhDescriptorB	0002 0000h	0002 0000h	reserved	-
50h	HcRhStatus	0000 0000h	0000 0000h	reserved	-
54h	HcRhPortStatus[1]	0000 0000h	0000 0000h	reserved	-
58h	HcRhPortStatus[2]	-	-	reserved	-
5Ch	reserved	-	-	reserved	-
60h	reserved	-	-	CONFIGFLAG	0000 0000h
64h	reserved	-	-	PORTSC1	0000 0000h
68h	reserved	-	-	PORTSC2	0000 0000h
6Ch	reserved	-	-	reserved	-
70h	reserved	-	-	reserved	-

[1] Reset values that are highlighted—for example, **0**—are the SAF1562HL implementation-specific reset values; and reset values that are not highlighted—for example, 0—are compliant with OHCI and EHCI specifications.

[2] HCIVERSION is 0100h when subsystem ID and subsystem vendor ID are configured through the external EEPROM or when SCL is pulled down. Otherwise, it is 0095h.

For the OHCI Host Controller, there are only operational registers for the USB operation.

For the Enhanced Host Controller, there are two types of registers: one set of read-only capability registers and one set of read and write operational registers.

11.1 OHCI USB Host Controller operational registers

OHCI HCDs need to communicate with these registers to implement USB data transfers. Based on their functions, these registers are classified into four partitions:

- Control and Status
- Memory Pointer
- Frame Counter
- Root Hub

11.1.1 HcRevision register

Table 42. HcRevision - Host Controller Revision register bit allocation

Address: Content of the base address register + 00h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	REV[7:0]							
Reset	0	0	0	1	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 43. HcRevision - Host Controller Revision register bit description

Address: Content of the base address register + 00h

Bit	Symbol	Description
31 to 8	reserved	-
7 to 0	REV[7:0]	**Revision**: This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this Host Controller. For example, a value of 11h corresponds to version 1.1. All of the Host Controller implementations that are compliant with this specification need to have a value of 10h.

11.1.2 HcControl register

This register defines the operating modes for the Host Controller. All the fields in this register, except for HCFS and RWC, are modified only by the HCD. The bit allocation is given in Table 44.

Table 44. HcControl - Host Controller Control register bit allocation

Address: Content of the base address register + 04h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]					RWE	RWC	IR
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	HCFS[1:0]		BLE	CLE	IE	PLE	CBSR[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 45. HcControl - Host Controller Control register bit description

Address: Content of the base address register + 04h

Bit	Symbol	Description
31 to 11	reserved	-
10	RWE	**Remote Wakeup Enable**: This bit is used by the HCD to enable or disable the remote wake-up feature on detecting upstream resume signaling. When this bit and RD (bit 3) in the HcInterruptStatus register are set, a remote wake-up is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	RWC	**Remote Wakeup Connected**: This bit indicates whether the Host Controller supports remote wake-up signaling. If remote wake-up is supported and used by the system, it is the responsibility of the system firmware to set this bit during POST. The Host Controller clears the bit on a hardware reset but does not alter it on a software reset. Remote wake-up signaling of the host system is host-bus-specific and is not described in this specification.
8	IR	**Interrupt Routing**: This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. The HCD clears this bit on a hardware reset, but it does not alter this bit on a software reset. The HCD uses this bit as a tag to indicate the ownership of the Host Controller.
7 and 6	HCFS [1:0]	**Host Controller Functional State** for USB: **00b —** USBRESET **01b —** USBRESUME **10b —** USBOPERATIONAL **11b —** USBSUSPEND A transition to USBOPERATIONAL from another state causes SOF generation to begin 1 ms later. The HCD may determine whether the Host Controller has begun sending SOFs by reading SF (bit 2) in HcInterruptStatus. This field may be changed by the Host Controller only when in the USBSUSPEND state. The Host Controller may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. The Host Controller enters USBSUSPEND after a software reset; it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
5	BLE	**Bulk List Enable**: This bit is set to enable the processing of the bulk list in the next frame. If cleared by the HCD, processing of the bulk list does not occur after the next SOF. The Host Controller checks this bit whenever it wants to process the list. When disabled, the HCD may modify the list. If HcBulkCurrentED is pointing to an Endpoint Descriptor (ED) to be removed, the HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.

Table 45. HcControl - Host Controller Control register bit description *...continued*

Address: Content of the base address register + 04h

Bit	Symbol	Description
4	CLE	**Control List Enable**: This bit is set to enable the processing of the control list in the next frame. If cleared by the HCD, processing of the control list does not occur after the next SOF. The Host Controller must check this bit whenever it wants to process the list. When disabled, the HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, the HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.
3	IE	**Isochronous Enable**: This bit is used by the HCD to enable or disable processing of isochronous EDs. While processing the periodic list in a frame, the Host Controller checks the status of this bit when it finds an isochronous ED (F = logic 1). If set (enabled), the Host Controller continues processing the EDs. If cleared (disabled), the Host Controller halts processing of the periodic list—which now contains only isochronous EDs—and begins processing the bulk or control lists. Setting this bit is guaranteed to take effect in the next frame and not the current frame.
2	PLE	**Periodic List Enable**: This bit is set to enable the processing of the periodic list in the next frame. If cleared by the HCD, processing of the periodic list does not occur after the next SOF. The Host Controller must check this bit before it starts processing the list.
1 and 0	CBSR [1:0]	**Control Bulk Service Ratio**: This specifies the service ratio of control EDs over bulk EDs. Before processing any of the nonperiodic lists, the Host Controller must compare the ratio specified with its internal count on how many nonempty control EDs are processed, in determining whether to continue serving another control ED or switching to bulk EDs. The internal count must be retained when crossing the frame boundary. After a reset, the HCD is responsible to restore this value. **00b —** 1 : 1 **01b —** 2 : 1 **10b —** 3 : 1 **11b —** 4 : 1

11.1.3 HcCommandStatus register

The HcCommandStatus register is used by the Host Controller to receive commands issued by the HCD. It also reflects the current status of the Host Controller. To the HCD, it appears as a 'write to set' register. The Host Controller must ensure that bits written as logic 1 become set in the register while bits written as logic 0 remain unchanged in the register. The HCD may issue multiple distinct commands to the Host Controller without concern for corrupting previously issued commands. The HCD has normal read access to all bits.

The SOC[1:0] field (bit 17 and bit 16 in the HcCommandStatus register) indicates the number of frames with which the Host Controller has detected the scheduling overrun error. This occurs when the periodic list does not complete before EOF. When a scheduling overrun error is detected, the Host Controller increments the counter and sets SO (bit 0 in the HcInterruptStatus register).

Table 46 shows the bit allocation of the HcCommandStatus register.

Table 46. HcCommandStatus - Host Controller Command Status register bit allocation

Address: Content of the base address register + 08h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]						SOC[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]				OCR	BLF	CLF	HCR
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 47. HcCommandStatus - Host Controller Command Status register bit description

Address: Content of the base address register + 08h

Bit	Symbol	Description
31 to 18	reserved	-
17 and 16	SOC[1:0]	**Scheduling Overrun Count**: The bit is incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. It must be incremented when a scheduling overrun is detected, even if SO (bit 0 in HcInterruptStatus) is already set. This is used by the HCD to monitor any persistent scheduling problems.
15 to 4	reserved	-
3	OCR	**Ownership Change Request**: This bit is set by an OS HCD to request a change of control of the Host Controller. When set, the Host Controller must set OC (bit 30 in HcInterruptStatus). After the changeover, this bit is cleared and remains so until the next request from the OS HCD.

Table 47. HcCommandStatus - Host Controller Command Status register bit description
…continued

Bit	Symbol	Description
2	BLF	**Bulk List Filled**: This bit is used to indicate whether there are any Transfer Descriptors (TDs) on the bulk list. It is set by the HCD whenever it adds a TD to an ED in the bulk list. When the Host Controller begins to process the head of the bulk list, it checks Bulk-Filled (BF). If BLF is logic 0, the Host Controller does not need to process the bulk list. If BLF is logic 1, the Host Controller needs to start processing the bulk list and set BF to logic 0. If the Host Controller finds a TD on the list, then the Host Controller needs to set BLF to logic 1, causing the bulk list processing to continue. If no TD is found on the bulk list, and if the HCD does not set BLF, then BLF is still logic 0 when the Host Controller completes processing the bulk list and the bulk list processing stops.
1	CLF	**Control List Filled**: This bit is used to indicate whether there are any TDs on the control list. It is set by the HCD whenever it adds a TD to an ED in the control list. When the Host Controller begins to process the head of the control list, it checks CLF. If CLF is logic 0, the Host Controller does not need to process the control list. If Control-Filled (CF) is logic 1, the Host Controller needs to start processing the control list and set CLF to logic 0. If the Host Controller finds a TD on the list, then the Host Controller needs to set CLF to logic 1, causing the control list processing to continue. If no TD is found on the control list, and if the HCD does not set CLF, then CLF is still logic 0 when the Host Controller completes processing the control list and the control list processing stops.
0	HCR	**Host Controller Reset**: This bit is set by the HCD to initiate a software reset of the Host Controller. Regardless of the functional state of the Host Controller, it moves to the USBSUSPEND state in which most of the operational registers are reset, except those stated otherwise; for example, IR (bit 8) in the HcControl register, and no host bus accesses are allowed. This bit is cleared by the Host Controller on completing the reset operation. The reset operation must be completed within 10 µs. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

11.1.4 HcInterruptStatus register

This is a 4 B register that provides the status of the events that cause hardware interrupts. The bit allocation of the register is given in Table 48. When an event occurs, the Host Controller sets the corresponding bit in this register. When a bit becomes set, a hardware interrupt is generated, if the interrupt is enabled in the HcInterruptEnable register (see Table 50) and the MIE (MasterInterruptEnable) bit is set. The HCD may clear specific bits in this register by writing logic 1 to the bit positions to be cleared. The HCD may not set any of these bits. The Host Controller does not clear the bit.

Table 48. HcInterruptStatus - Host Controller Interrupt Status register bit allocation
Address: Content of the base address register + 0Ch

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]	OC	reserved[1]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]	RHSC	FNO	UE	RD	SF	WDH	SO
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 49. HcInterruptStatus - Host Controller Interrupt Status register bit description

Address: Content of the base address register + 0Ch

Bit	Symbol	Description
31	reserved	-
30	OC	**Ownership Change**: This bit is set by the Host Controller when HCD sets OCR (bit 3) in the HcCommandStatus register. This event, when unmasked, will always immediately generate a System Management Interrupt (SMI). This bit is forced to logic 0 when the SMI# pin is not implemented.
29 to 7	reserved	-
6	RHSC	**Root Hub Status Change**: This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	FNO	**Frame Number Overflow**: This bit is set when the MSB of HcFmNumber (bit 15) changes value, or after the HccaFrameNumber is updated.
4	UE	**Unrecoverable Error**: This bit is set when the Host Controller detects a system error not related to USB. The Host Controller should not proceed with any processing nor signaling before the system error is corrected. The HCD clears this bit after the Host Controller is reset.
3	RD	**Resume Detected**: This bit is set when the Host Controller detects that a device on the USB is asserting resume signaling. This bit is set by the transition from no resume signaling to resume signaling. This bit is not set when the HCD sets the USBRESUME state.
2	SF	**Start-of-Frame**: At the start of each frame, this bit is set by the Host Controller and an SOF token is generated at the same time.
1	WDH	**Writeback Done Head**: This bit is immediately set after the Host Controller has written HcDoneHead to HccaDoneHead. Further, updates of HccaDoneHead occur only after this bit is cleared. The HCD should only clear this bit after it has saved the content of HccaDoneHead.
0	SO	**Scheduling Overrun**: This bit is set when USB schedules for current frame overruns and after the update of HccaFrameNumber. A scheduling overrun increments the SOC[1:0] field (bit 17 and bit 16 of HcCommandStatus).

11.1.5 HcInterruptEnable register

Each enable bit in the HcInterruptEnable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptEnable register is used to control which events generate a hardware interrupt. A hardware interrupt is requested on the host bus if the following conditions occur:

- A bit is set in the HcInterruptStatus register
- The corresponding bit in the HcInterruptEnable register is set
- The MIE (MasterInterruptEnable) bit is set

Writing logic 1 to a bit in this register sets the corresponding bit, whereas writing logic 0 to a bit in this register leaves the corresponding bit unchanged. On a read, the current value of this register is returned. The bit allocation is given in Table 50.

Table 50. HcInterruptEnable - Host Controller Interrupt Enable register bit allocation
Address: Content of the base address register + 10h

Bit	31	30	29	28	27	26	25	24
Symbol	MIE	OC	reserved[1]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]	RHSC	FNO	UE	RD	SF	WDH	SO
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 51. HcInterruptEnable - Host Controller Interrupt Enable register bit description
Address: Content of the base address register + 10h

Bit	Symbol	Description
31	MIE	**Master Interrupt Enable**: **0 —** Ignore **1 —** Enables interrupt generation by events specified in other bits of this register
30	OC	**Ownership Change**: **0 —** Ignore **1 —** Enables interrupt generation because of Ownership Change
29 to 7	reserved	-

Table 51. HcInterruptEnable - Host Controller Interrupt Enable register bit description
…continued

Bit	Symbol	Description
6	RHSC	**Root Hub Status Change**: **0 —** Ignore **1 —** Enables interrupt generation because of Root Hub Status Change
5	FNO	**Frame Number Overflow**: **0 —** Ignore **1 —** Enables interrupt generation because of Frame Number Overflow
4	UE	**Unrecoverable Error**: **0 —** Ignore **1 —** Enables interrupt generation because of Unrecoverable Error
3	RD	**Resume Detect**: **0 —** Ignore **1 —** Enables interrupt generation because of Resume Detect
2	SF	**Start-of-Frame**: **0 —** Ignore **1 —** Enables interrupt generation because of Start-of-Frame
1	WDH	**HcDoneHead Writeback**: **0 —** Ignore **1 —** Enables interrupt generation because of HcDoneHead Writeback
0	SO	**Scheduling Overrun**: **0 —** Ignore **1 —** Enables interrupt generation because of Scheduling Overrun

11.1.6 HcInterruptDisable register

Each disable bit in the HcInterruptDisable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptDisable register is coupled with the HcInterruptEnable register. Therefore, writing logic 1 to a bit in this register clears the corresponding bit in the HcInterruptEnable register, whereas writing logic 0 to a bit in this register leaves the corresponding bit in the HcInterruptEnable register unchanged. On a read, the current value of the HcInterruptEnable register is returned.

The register contains 4 B, and the bit allocation is given in Table 52.

Table 52. HcInterruptDisable - Host Controller Interrupt Disable register bit allocation
Address: Content of the base address register + 14h

Bit	31	30	29	28	27	26	25	24
Symbol	MIE	OC	reserved[1]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]	RHSC	FNO	UE	RD	SF	WDH	SO
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 53. HcInterruptDisable - Host Controller Interrupt Disable register bit description

Address: Content of the base address register + 14h

Bit	Symbol	Description
31	MIE	**Master Interrupt Enable**: **0 —** Ignore **1 —** Disables interrupt generation because of events specified in other bits of this register This field is set after a hardware or software reset. Interrupts are disabled.
30	OC	**Ownership Change**: **0 —** Ignore **1 —** Disables interrupt generation because of Ownership Change
29 to 7	reserved	-
6	RHSC	**Root Hub Status Change**: **0 —** Ignore **1 —** Disables interrupt generation because of Root Hub Status Change
5	FNO	**Frame Number Overflow**: **0 —** Ignore **1 —** Disables interrupt generation because of Frame Number Overflow
4	UE	**Unrecoverable Error**: **0 —** Ignore **1 —** Disables interrupt generation because of Unrecoverable Error
3	RD	**Resume Detect**: **0 —** Ignore **1 —** Disables interrupt generation because of Resume Detect
2	SF	**Start-of-Frame**: **0 —** Ignore **1 —** Disables interrupt generation because of Start-of-Frame
1	WDH	**HcDoneHead Writeback**: **0 —** Ignore **1 —** Disables interrupt generation because of HcDoneHead Writeback
0	SO	**Scheduling Overrun**: **0 —** Ignore **1 —** Disables interrupt generation because of Scheduling Overrun

11.1.7 HcHCCA register

The HcHCCA register contains the physical address of the Host Controller Communication Area (HCCA). The bit allocation is given in Table 54. The HCD determines the alignment restrictions by writing all ones to HcHCCA and reading the content of HcHCCA. The alignment is evaluated by examining the number of zeroes in the lower order bits. The minimum alignment is 256 B; therefore, bits 0 through 7 will always return logic 0 when read. This area is used to hold the control structures and the interrupt table that are accessed by both the Host Controller and the HCD.

Table 54. HcHCCA - Host Controller Communication Area register bit allocation

Address: Content of the base address register + 18h

Bit	31	30	29	28	27	26	25	24
Symbol	HCCA[23:16]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	HCCA[15:8]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	HCCA[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 55. HcHCCA - Host Controller Communication Area register bit description

Address: Content of the base address register + 18h

Bit	Symbol	Description
31 to 8	HCCA[23:0]	**Host Controller Communication Area Base Address**: This is the base address of the HCCA.
7 to 0	reserved	-

11.1.8 HcPeriodCurrentED register

The HcPeriodCurrentED register contains the physical address of the current isochronous or interrupt ED. Table 56 shows the bit allocation of the register.

Table 56. HcPeriodCurrentED - Host Controller Period Current Endpoint Descriptor register bit allocation

Address: Content of the base address register + 1Ch

Bit	31	30	29	28	27	26	25	24
Symbol	PCED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	PCED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	PCED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PCED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 57. HcPeriodCurrentED - Host Controller Period Current Endpoint Descriptor register bit description

Address: Content of the base address register + 1Ch

Bit	Symbol	Description
31 to 4	PCED[27:0]	**Period Current ED**: This is used by the Host Controller to point to the head of one of the periodic lists that must be processed in the current frame. The content of this register is updated by the Host Controller after a periodic ED is processed. The HCD may read the content in determining which ED is being processed at the time of reading.
3 to 0	reserved	-

11.1.9 HcControlHeadED register

The HcControlHeadED register contains the physical address of the first ED of the control list. The bit allocation is given in Table 58.

Table 58. HcControlHeadED - Host Controller Control Head Endpoint Descriptor register bit allocation

Address: Content of the base address register + 20h

Bit	31	30	29	28	27	26	25	24
Symbol	CHED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	CHED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8
Symbol	CHED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CHED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 59. HcControlHeadED - Host Controller Control Head Endpoint Descriptor register bit description

Address: Content of the base address register + 20h

Bit	Symbol	Description
31 to 4	CHED[27:0]	**Control Head ED**: The Host Controller traverses the control list, starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of the Host Controller.
3 to 0	reserved	-

11.1.10 HcControlCurrentED register

The HcControlCurrentED register contains the physical address of the current ED of the control list. The bit allocation is given in Table 60.

Table 60. HcControlCurrentED - Host Controller Control Current Endpoint Descriptor register bit allocation

Address: Content of the base address register + 24h

Bit	31	30	29	28	27	26	25	24
Symbol	CCED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	CCED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	CCED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CCED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 61. HcControlCurrentED - Host Controller Control Current Endpoint Descriptor register bit description

Address: Content of the base address register + 24h

Bit	Symbol	Description
31 to 4	CCED[27:0]	**Control Current ED**: This pointer is advanced to the next ED after serving the present. The Host Controller must continue processing the list from where it left off in the last frame. When it reaches the end of the control list, the Host Controller checks CLF (bit 1 of HcCommandStatus). If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. The HCD is allowed to modify this register only when CLE (bit 4 in the HcControl register) is cleared. When set, the HCD only reads the instantaneous value of this register. Initially, this is set to logic 0 to indicate the end of the control list.
3 to 0	reserved	-

11.1.11 HcBulkHeadED register

This register (see Table 62) contains the physical address of the first ED of the bulk list.

Table 62. HcBulkHeadED - Host Controller Bulk Head Endpoint Descriptor register bit allocation

Address: Content of the base address register + 28h

Bit	31	30	29	28	27	26	25	24
Symbol	BHED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	BHED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	BHED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BHED[3:0]				reserved[1]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 63. HcBulkHeadED - Host Controller Bulk Head Endpoint Descriptor register bit description

Address: Content of the base address register + 28h

Bit	Symbol	Description
31 to 4	BHED[27:0]	**Bulk Head ED**: The Host Controller traverses the bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of the Host Controller.
3 to 0	reserved	-

11.1.12 HcBulkCurrentED register

This register contains the physical address of the current endpoint of the bulk list. The endpoints are ordered according to their insertion to the list because the bulk list must be served in a round-robin fashion. The bit allocation is given in Table 64.

Table 64. HcBulkCurrentED - Host Controller Bulk Current Endpoint Descriptor register bit allocation

Address: Content of the base address register + 2Ch

Bit	31	30	29	28	27	26	25	24
Symbol	BCED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	BCED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	BCED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BCED[3:0]				reserved[1]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 65. HcBulkCurrentED - Host Controller Bulk Current Endpoint Descriptor register bit description

Address: Content of the base address register + 2Ch

Bit	Symbol	Description
31 to 4	BCED[27:0]	**Bulk Current ED**: This is advanced to the next ED after the Host Controller has served the current ED. The Host Controller continues processing the list from where it left off in the last frame. When it reaches the end of the bulk list, the Host Controller checks CLF (bit 1 of HcCommandStatus). If the CLF bit is not set, nothing is done. If the CLF bit is set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the CLF bit. The HCD can modify this register only when BLE (bit 5 in the HcControl register) is cleared. When HcControl is set, the HCD reads the instantaneous value of this register. This is initially set to logic 0 to indicate the end of the bulk list.
3 to 0	reserved	-

11.1.13 HcDoneHead register

The HcDoneHead register contains the physical address of the last completed TD that was added to the Done queue. In normal operation, the HCD need not read this register because its content is periodically written to the HCCA. Table 66 contains the bit allocation of the register.

Table 66. HcDoneHead - Host Controller Done Head register bit allocation

Address: Content of the base address register + 30h

Bit	31	30	29	28	27	26	25	24
Symbol	DH[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	DH[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	DH[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DH[3:0]				reserved[1]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 67. HcDoneHead - Host Controller Done Head register bit description

Address: Content of the base address register + 30h

Bit	Symbol	Description
31 to 4	DH[27:0]	**Done Head**: When a TD is completed, the Host Controller writes the content of HcDoneHead to the NextTD field of the TD. The Host Controller then overwrites the content of HcDoneHead with the address of this TD. This is set to logic 0 whenever the Host Controller writes the content of this register to HCCA.
3 to 0	reserved	-

11.1.14 HcFmInterval register

This register contains a 14-bit value that indicates the bit time interval in a frame—that is, between two consecutive SOFs—and a 15-bit value indicating the full-speed maximum packet size that the Host Controller may transmit or receive, without causing a scheduling overrun. The HCD may carry out minor adjustment on FI (Frame Interval) by writing a new value over the present at each SOF. This provides the possibility for the Host Controller to synchronize with an external clocking resource and to adjust any unknown local clock offset. The bit allocation of the register is given in Table 68.

Table 68. HcFmInterval - Host Controller Frame Interval register bit allocation

Address: Content of the base address register + 34h

Bit	31	30	29	28	27	26	25	24
Symbol	FIT	FSMPS[14:8]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Symbol	FSMPS[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]		FI[13:8]					
Reset	0	0	1	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FI[7:0]							
Reset	1	1	0	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 69. HcFmInterval - Host Controller Frame Interval register bit description

Address: Content of the base address register + 34h

Bit	Symbol	Description
31	FIT	**Frame Interval Toggle**: The HCD toggles this bit whenever it loads a new value to Frame Interval.
30 to 16	FSMPS[14:0]	**FS Largest Data Packet**: This field specifies the value that is loaded into the largest data packet counter at the beginning of each frame. The counter value represents the largest amount of data in bits that can be sent or received by the Host Controller in a single transaction at any given time, without causing a scheduling overrun. The field value is calculated by the HCD.
15 and 14	reserved	-
13 to 0	FI[13:0]	**Frame Interval**: This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to 11,999. The HCD should store the current value of this field before resetting the Host Controller to reset this field to its nominal value. The HCD can then restore the stored value on completing the reset sequence.

11.1.15 HcFmRemaining register

This register is a 14-bit down counter showing the bit time remaining in the current frame. Table 70 contains the bit allocation of this register.

Table 70. HcFmRemaining - Host Controller Frame Remaining register bit allocation

Address: Content of the base address register + 38h

Bit	31	30	29	28	27	26	25	24
Symbol	FRT	reserved[1]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8
Symbol	reserved[1]				FR[13:8]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FR[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 71. HcFmRemaining - Host Controller Frame Remaining register bit description

Address: Content of the base address register + 38h

Bit	Symbol	Description
31	FRT	**Frame Remaining Toggle**: This bit is loaded from FIT (bit 31 of HcFmInterval) whenever FR[13:0] reaches 0. This bit is used by the HCD for the synchronization between FI[13:0] (bit 13 to bit 0 of HcFmInterval) and FR[13:0].
30 to 14	reserved	-
13 to 0	FR[13:0]	**Frame Remaining**: This counter is decremented at each bit time. When it reaches 0, it is reset by loading the FI[13:0] value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, the Host Controller reloads the content with FI[13:0] of HcFmInterval and uses the updated value from the next SOF.

11.1.16 HcFmNumber register

This register is a 16-bit counter, and the bit allocation is given in Table 72. It provides a timing reference among events happening in the Host Controller and the HCD. The HCD may use the 16-bit value specified in this register and generate a 32-bit frame number, without requiring frequent access to the register.

Table 72. HcFmNumber - Host Controller Frame Number register bit allocation

Address: Content of the base address register + 3Ch

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]				FN[13:8]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Symbol	FN[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 73. HcFmNumber - Host Controller Frame Number register bit description

Address: Content of the base address register + 3Ch

Bit	Symbol	Description
31 to 14	reserved	-
13 to 0	FN[13:0]	**Frame Number**: Incremented when HcFmRemaining is reloaded. It must be rolled over to 0h after FFFFh. Automatically incremented when entering the USBOPERATIONAL state. The content is written to HCCA after the Host Controller has incremented Frame Number at each frame boundary and sent an SOF but before the Host Controller reads the first ED in that frame. After writing to HCCA, the Host Controller sets SF (bit 2 in HcInterruptStatus).

11.1.17 HcPeriodicStart register

This register has a 14-bit programmable value that determines when is the earliest time for the Host Controller to start processing the periodic list. For bit allocation, see Table 74.

Table 74. HcPeriodicStart - Host Controller Periodic Start register bit allocation

Address: Content of the base address register + 40h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]		P_S[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	P_S[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 75. HcPeriodicStart - Host Controller Periodic Start register bit description

Address: Content of the base address register + 40h

Bit	Symbol	Description
31 to 14	reserved	-
13 to 0	P_S[13:0]	**Periodic Start**: After a hardware reset, this field is cleared. It is then set by the HCD during the Host Controller initialization. The value is roughly calculated as 10 % of HcFmInterval. A typical value is 3E67h. When HcFmRemaining reaches the value specified, processing of the periodic lists have priority over control or bulk processing. The Host Controller, therefore, starts processing the interrupt list after completing the current control or bulk transaction that is in progress.

11.1.18 HcLSThreshold register

This register contains an 11-bit value used by the Host Controller to determine whether to commit to the transfer of a maximum of 8 B low-speed packet before EOF. Neither the Host Controller nor the HCD can change this value. For bit allocation, see Table 76.

Table 76. HcLSThreshold - Host Controller LS Threshold register bit allocation

Address: Content of the base address register + 44h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]				LST[11:8]			
Reset	0	0	0	0	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	LST[7:0]							
Reset	0	0	1	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 77. HcLSThreshold - Host Controller LS Threshold register bit description

Address: Content of the base address register + 44h

Bit	Symbol	Description
31 to 12	reserved	-
11 to 0	LST[11:0]	**LS Threshold**: This field contains a value that is compared to the FR[13:0] field, before initiating a low-speed transaction. The transaction is started only if FR ≥ this field. The value is calculated by the HCD, considering the transmission and setup overhead.

11.1.19 HcRhDescriptorA register

This register is the first of two registers describing the characteristics of the Root Hub. Reset values are implementation-specific.

Table 78 contains the bit allocation of the HcRhDescriptorA register.

Table 78. HcRhDescriptorA - Host Controller Root Hub Descriptor A register bit allocation

Address: Content of the base address register + 48h

Bit	31	30	29	28	27	26	25	24
Symbol	POTPGT[7:0]							
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]			NOCP	OCPM	DT	NPS	PSM
Reset	0	0	0	0	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	NDP[7:0]							
Reset	0	0	0	0	0	0	0	1
Access	R	R	R	R	R	R	R	R

[1] The reserved bits should always be written with the reset value.

Table 79. HcRhDescriptorA - Host Controller Root Hub Descriptor A register bit description

Address: Content of the base address register + 48h

Bit	Symbol	Description
31 to 24	POTPGT [7:0]	**Power On To Power Good Time**: This byte specifies the duration the HCD must wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT × 2 ms.
23 to 13	reserved	-
12	NOCP	**No Over Current Protection**: This bit describes how the overcurrent status for Root Hub ports are reported. When this bit is cleared, the OCPM bit specifies global or per-port reporting. **0 —** Overcurrent status is collectively reported for all downstream ports **1 —** No overcurrent protection supported
11	OCPM	**Over Current Protection Mode**: This bit describes how the overcurrent status for Root Hub ports are reported. At reset, this fields reflects the same mode as Power Switching Mode. This field is valid only if the NOCP bit is cleared. **0 —** Overcurrent status is collectively reported for all downstream ports **1 —** Overcurrent status is reported on a per-port basis

Table 79. HcRhDescriptorA - Host Controller Root Hub Descriptor A register bit description
…continued

Address: Content of the base address register + 48h

Bit	Symbol	Description
10	DT	**Device Type**: This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read logic 0.
9	NPS	**No Power Switching**: This bit is used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PSM bit specifies global or per-port switching. **0 —** Ports are power switched **1 —** Ports are always powered on when the Host Controller is powered on
8	PSM	**Power Switching Mode**: This bit is used to specify how the power switching of Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NPS field is cleared. **0 —** All ports are powered at the same time **1 —** Each port is individually powered. This mode allows port power to be controlled by either the global switch or per-port switching. If the PPCM (Port Power Control Mask) bit is set, the port responds only to port power commands (Set/Clear Port Power). If the port mask is cleared, then the port is controlled only by the global power switch (Set/Clear Global Power).
7 to 0	NDP[7:0]	**Number Downstream Ports**: These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OHCI is 15.

11.1.20 HcRhDescriptorB register

The HcRhDescriptorB register is the second of two registers describing the characteristics of the Root Hub. The bit allocation is given in Table 80. These fields are written during initialization to correspond to the system implementation. Reset values are implementation-specific.

Table 80. HcRhDescriptorB - Host Controller Root Hub Descriptor B register bit allocation
Address: Content of the base address register + 4Ch

Bit	31	30	29	28	27	26	25	24
Symbol	PPCM[15:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	PPCM[7:0]							
Reset	0	0	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	DR[15:8]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Symbol	DR[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 81. HcRhDescriptorB - Host Controller Root Hub Descriptor B register bit description

Address: Content of the base address register + 4Ch

Bit	Symbol	Description
31 to 16	PPCM [15:0]	**Port Power Control Mask**: Each bit indicates whether a port is affected by a global power control command when Power Switching Mode is set. When set, only the power state of the port is affected by per-port power control (Set/Clear Port Power). When cleared, the port is controlled by the global power switch (Set/Clear Global Power). If the device is configured to global switching mode (Power Switching Mode = logic 0), this field is not valid. **Bit 0 —** Reserved **Bit 1 —** Ganged-power mask on port 1 **Bit 2 —** Ganged-power mask on port 2
15 to 0	DR [15:0]	**Device Removable**: Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. **Bit 0 —** Reserved **Bit 1 —** Device attached to port 1 **Bit 2 —** Device attached to port 2

11.1.21 HcRhStatus register

This register is divided into two parts. The lower word of a double word represents the Hub Status field, and the upper word represents the Hub Status Change field. Reserved bits should always be written as logic 0. Table 82 shows the bit allocation of the register.

Table 82. HcRhStatus - Host Controller Root Hub Status register bit allocation

Address: Content of the base address register + 50h

Bit	31	30	29	28	27	26	25	24
Symbol	CRWE	reserved[1]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]						CCIC	LPSC
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	DRWE	reserved[1]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]						OCI	LPS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	RW

[1] The reserved bits should always be written with the reset value.

Table 83. HcRhStatus - Host Controller Root Hub Status register bit description

Address: Content of the base address register + 50h

Bit	Symbol	Description
31	CRWE	On write—**Clear Remote Wakeup Enable**: **0 —** No effect **1 —** Clears DRWE (Device Remote Wakeup Enable)
30 to 18	reserved	-
17	CCIC	**Over Current Indicator Change**: This bit is set by hardware when a change has occurred to the OCI bit of this register. **0 —** No effect **1 —** The HCD clears this bit
16	LPSC	On read—**Local Power Status Change**: The Root Hub does not support the local power status feature. Therefore, this bit is always logic 0. On write—**Set Global Power**: In global power mode (Power Switching Mode = logic 0), logic 1 is written to this bit to turn on power to all ports (clear Port Power Status). In per-port power mode, it sets Port Power Status only on ports whose Port Power Control Mask bit is not set. Writing logic 0 has no effect.
15	DRWE	On read—**Device Remote Wakeup Enable**: This bit enables bit Connect Status Change (CSC) as a resume event, causing a state transition from USBSUSPEND to USBRESUME and setting the Resume Detected interrupt. **0 —** CSC is not a remote wake-up event **1 —** CSC is a remote wake-up event On write—**Set Remote Wakeup Enable**: Writing logic 1 sets DRWE (Device Remote Wakeup Enable). Writing logic 0 has no effect.
14 to 2	reserved	-
1	OCI	**Over Current Indicator**: This bit reports overcurrent conditions when global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If the per-port overcurrent protection is implemented, this bit is always logic 0.
0	LPS	On read—**Local Power Status**: The Root Hub does not support the local power status feature. Therefore, this bit is always read as logic 0. On write—**Clear Global Power**: In global power mode (Power Switching Mode = logic 0), logic 1 is written to this bit to turn off power to all ports (clear Port Power Status). In per-port power mode, it clears Port Power Status only on ports whose Port Power Control Mask bit is not set. Writing logic 0 has no effect.

11.1.22 HcRhPortStatus[4:1] register

The HcRhPortStatus[4:1] register is used to control and report port events on a per-port basis. Number Downstream Ports represents the number of HcRhPortStatus registers that are implemented in hardware. The lower word reflects the port status. The upper word reflects the status change bits. Some status bits are implemented with special write behavior. If a transaction—token through handshake—is in progress when a write to change port status occurs, the resulting port status change is postponed until the transaction completes. Always write logic 0 to the reserved bits. The bit allocation of the register is given in Table 84.

Table 84. HcRhPortStatus[4:1] - Host Controller Root Hub Port Status[4:1] register bit allocation

Address: Content of the base address register + 54h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]			PRSC	OCIC	PSSC	PESC	CSC
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]						LSDA	PPS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]			PRS	POCI	PSS	PES	CCS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 85. HcRhPortStatus[4:1] - Host Controller Root Hub Port Status[4:1] register bit description

Address: Content of the base address register + 54h

Bit	Symbol	Description
31 to 21	reserved	-
20	PRSC	**Port Reset Status Change**: This bit is set at the end of the 10 ms port reset signal. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. **0 —** Port reset is not complete **1 —** Port reset is complete
19	OCIC	**Port Over Current Indicator Change**: This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when the Root Hub changes the POCI (Port Over Current Indicator) bit. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. **0 —** No change in POCI **1 —** POCI has changed

Table 85. HcRhPortStatus[4:1] - Host Controller Root Hub Port Status[4:1] register bit description *...continued*

Address: Content of the base address register + 54h

Bit	Symbol	Description
18	PSSC	**Port Suspend Status Change**: This bit is set when the resume sequence is completed. This sequence includes the 20 ms resume pulse, LS EOP and 3 ms resynchronization delay. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. This bit is also cleared when ResetStatusChange is set. **0 —** Resume is not completed **1 —** Resume is completed
17	PESC	**Port Enable Status Change**: This bit is set when hardware events cause the PES (Port Enable Status) bit to be cleared. Changes from the HCD writes do not set this bit. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. **0 —** No change in PES **1 —** Change in PES
16	CSC	**Connect Status Change**: This bit is set whenever a connect or disconnect event occurs. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. If CCS (Current Connect Status) is cleared when a Set Port Reset, Set Port Enable or Set Port Suspend write occurs, this bit is set to force the driver to re-evaluate the connection status because these writes should not occur if the port is disconnected. **0 —** No change in CCS **1 —** Change in CCS **Remark:** If the Device Removable [NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
15 to 10	reserved	-
9	LSDA	On read—**Low Speed Device Attached**: This bit indicates the speed of the device attached to this port. When set, a low-speed device is attached to this port. When cleared, a full-speed device is attached to this port. This field is valid only when CCS is set. **0 —** Port is not suspended **1 —** Port is suspended On write—**Clear Port Power**: The HCD can clear the PPS (Por Power Status) bit by writing logic 1 to this bit. Writing logic 0 has no effect.

Table 85. HcRhPortStatus[4:1] - Host Controller Root Hub Port Status[4:1] register bit description *...continued*

Address: Content of the base address register + 54h

Bit	Symbol	Description
8	PPS	On read—**Port Power Status**: This bit reflects the port power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. The HCD can set this bit by writing Set Port Power or Set Global Power. The HCD can clear this bit by writing Clear Port Power or Clear Global Power. Power Switching Mode and Port Power Control Mask [NDP] determine which power control switches are enabled. In global switching mode (Power Switching Mode = logic 0), only Set/Clear Global Power controls this bit. In the per-port power switching (Power Switching Mode = logic 1), if the Port Power Control Mask [NDP] bit for the port is set, only Set/Clear Port Power commands are enabled. If the mask is not set, only Set/Clear Global Power commands are enabled. When port power is disabled, bits CCS (Current Connect Status), PES (Port Enable Status), PSS (Port Suspend Status) and PRS (Port Reset Status) should be reset. **0 —** Port power is off **1 —** Port power is on On write—**Set Port Power**: The HCD can write logic 1 to set the PPS (Port Power Status) bit. Writing logic 0 has no effect. **Remark:** This bit always reads logic 1 if power switching is not supported.
7 to 5	reserved	-
4	PRS	On read—**Port Reset Status**: When this bit is set by a write to Set Port Reset, port reset signaling is asserted. When reset is completed and PRSC is set, this bit is cleared. **0 —** Port reset signal is inactive **1 —** Port reset signal is active On write—**Set Port Reset**: The HCD can set the port reset signaling by writing logic 1 to this bit. Writing logic 0 has no effect. If CCS is cleared, this write does not set PRS (Port Reset Status) but instead sets CCS. This informs the driver that it attempted to reset a disconnected port.
3	POCI	On read—**Port Over Current Indicator**: This bit is valid only when the Root Hub is configured to show overcurrent conditions are reported on a per-port basis. If the per-port overcurrent reporting is not supported, this bit is set to logic 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. **0 —** No overcurrent condition **1 —** Overcurrent condition detected On write—**Clear Suspend Status**: The HCD can write logic 1 to initiate a resume. Writing logic 0 has no effect. A resume is initiated only if PSS (Port Suspend Status) is set.

Table 85. HcRhPortStatus[4:1] - Host Controller Root Hub Port Status[4:1] register bit description *...continued*

Address: Content of the base address register + 54h

Bit	Symbol	Description
2	PSS	On read—**Port Suspend Status**: This bit indicates whether the port is suspended or is in the resume sequence. It is set by a Set Suspend State write and cleared when PSSC (Port Suspend Status Change) is set at the end of the resume interval. This bit is not set if CCS (Current Connect Status) is cleared. This bit is also cleared when PRSC is set at the end of the port reset or when the Host Controller is placed in the USBRESUME state. If an upstream resume is in progress, it will propagate to the Host Controller. **0 —** Port is not suspended **1 —** Port is suspended On write—**Set Port Suspend**: The HCD can set the PSS (Port Suspend Status) bit by writing logic 1 to this bit. Writing logic 0 has no effect. If CCS is cleared, this write does not set PSS; instead it sets CSS. This informs the driver that it attempted to suspend a disconnected port.
1	PES	On read—**Port Enable Status**: This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power or operational bus error is detected. This change also causes Port Enabled Status Change to be set. The HCD can set this bit by writing Set Port Enable and clear it by writing Clear Port Enable. This bit cannot be set when CCS (Current Connect Status) is cleared. This bit is also set on completing a port reset when Reset Status Change is set or on completing a port suspend when Suspend Status Change is set. **0 —** Port is disabled **1 —** Port is enabled On write—**Set Port Enable**: The HCD can set PES (Port Enable Status) by writing logic 1. Writing logic 0 has no effect. If CCS is cleared, this write does not set PES, but instead sets CSC (Connect Status Change). This informs the driver that it attempted to enable a disconnected port.
0	CCS	On read—**Current Connect Status**: This bit reflects the current state of the downstream port. **0 —** No device connected **1 —** Device connected On write—**Clear Port Enable**: The HCD can write logic 1 to this bit to clear the PES (Port Enable Status) bit. Writing logic 0 has no effect. The CCS bit is not affected by any write. **Remark:** This bit always reads logic 1 when the attached device is nonremovable (Device Removable [NDP]).

11.2 EHCI controller capability registers

Other than the OHCI Host Controller, there are some registers in EHCI that define the capability of EHCI. The address range of these registers is located before the operational registers.

11.2.1 CAPLENGTH/HCIVERSION register

The bit allocation of this 4 B register is given in Table 86.

Table 86. CAPLENGTH/HCIVERSION - Capability Registers Length/Host Controller Interface Version Number register bit allocation

Address: Content of the base address register + 00h

Bit	31	30	29	28	27	26	25	24
Symbol	HCIVERSION[15:8]							
Reset	0	0	0	0	0	0	0	1
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	HCIVERSION[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CAPLENGTH[7:0]							
Reset	0	0	1	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 87. CAPLENGTH/HCIVERSION - Capability Registers Length/Host Controller Interface Version Number register bit description

Address: Content of the base address register + 00h

Bit	Symbol	Description
31 to 16	HCIVERSION [15:0]	**Host Controller Interface Version Number**: This field contains a BCD encoded version number of the interface to which the Host Controller interface conforms.
15 to 8	reserved	-
7 to 0	CAPLENGTH [7:0]	**Capability Register Length**: This is used as an offset. It is added to the register base to find the beginning of the operational register space.

11.2.2 HCSPARAMS register

The Host Controller Structural Parameters (HCSPARAMS) register is a set of fields that are structural parameters. The bit allocation is given in Table 88.

Table 88. HCSPARAMS - Host Controller Structural Parameters register bit allocation

Address: Content of the base address register + 04h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8
Symbol	N_CC[3:0]				N_PCC[3:0]			
Reset	0	0	1	0	0	0	0	1
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PRR	reserved		PPC	N_PORTS[3:0]			
Reset	1	0	0	1	0	0	1	0
Access	R	R	R	R	R	R	R	R

Table 89. HCSPARAMS - Host Controller Structural Parameters register bit description

Address: Content of the base address register + 04h

Bit	Symbol	Description
31 to 16	reserved	-
15 to 12	N_CC[3:0]	**Number of Companion Controller**: This field indicates the number of companion controllers associated with this Hi-Speed USB Host Controller. A value of zero in this field indicates there are no companion Host Controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the Host Controller root ports. A value larger than zero in this field indicates there are companion Original USB Host Controller(s). Port-ownership hand-offs are supported.
11 to 8	N_PCC [3:0]	**Number of Ports per Companion Controller**: This field indicates the number of ports supported per companion Host Controller. It is used to indicate the port routing configuration to the system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC can have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, and so on. In the previous example, N_PCC could have been 4, in which case the first four are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC.
7	PRR	**Port Routing Rules**: This field indicates the method used to map ports to companion controllers. **0 —** The first N_PCC ports are routed to the lowest numbered function companion Host Controller, the next N_PCC ports are routed to the next lowest function companion controller, and so on **1 —** The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTROUTE array
6 and 5	reserved	-
4	PPC	**Port Power Control**: This field indicates whether the Host Controller implementation includes port power control. Logic 1 indicates the port has port power switches. Logic 0 indicates the port does not have port power switches. The value of this field affects the functionality of the Port Power field in each port status and control register.
3 to 0	N_PORTS [3:0]	**N_Ports**: This field specifies the number of physical downstream ports implemented on this Host Controller. The value in this field determines how many port registers are addressable in the operational register space. Logic 0 in this field is undefined.

11.2.3 HCCPARAMS register

The Host Controller Capability Parameters (HCCPARAMS) register is a 4 B register, and the bit allocation is given in Table 90.

Table 90. HCCPARAMS - Host Controller Capability Parameters register bit allocation

Address: Content of the base address register + 08h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	IST[3:0]				reserved		PFLF	64AC
Reset	0	0	0	1	0	0	1	0
Access	R	R	R	R	R	R	R	R

Table 91. HCCPARAMS - Host Controller Capability Parameters register bit description

Address: Content of the base address register + 08h

Bit	Symbol	Description
31 to 8	reserved	-
7 to 4	IST[3:0]	**Isochronous Scheduling Threshold**: Default = implementation dependent. This field indicates—relative to the current position of the executing Host Controller—where software can reliably update the isochronous schedule. When IST[3] is logic 0, the value of the least significant three bits indicates the number of micro frames a Host Controller can hold a set of isochronous data structures—one or more—before flushing the state. When IST[3] is logic 1, the host software assumes the Host Controller may cache an isochronous data structure for an entire frame.
3 and 2	reserved	-
1	PFLF	**Programmable Frame List Flag**: Default = implementation dependent. If this bit is cleared, the system software must use a frame list length of 1024 elements with the Host Controller. The USBCMD register FLS[1:0] (bit 3 and bit 2) is read-only and should be cleared. If PFLF is set, the system software can specify and use a smaller frame list and configure the host through the FLS bit. The frame list must always be aligned on a 4 kB page boundary to ensure that the frame list is always physically contiguous.
0	64AC	**64-bit Addressing Capability**: This field contains the addressing range capability. **0 —** Data structures using 32-bit address memory pointers **1 —** Data structures using 64-bit address memory pointers

11.2.4 HCSP-PORTROUTE register

The HCSP-PORTROUTE (Companion Port Route Description) register is an optional read-only field that is valid only if PRR (bit 7 in the HCSPARAMS register) is logic 1. Its address is the value read from content of the base address register + 0Ch.

This field is a 15-element nibble array—each 4 bits is one array element. Each array location corresponds one-to-one with a physical port provided by the Host Controller. For example, PORTROUTE[0] corresponds to the first PORTSC port, PORTROUTE[1] to the second PORTSC port, and so on. The value of each element indicates to which of the companion Host Controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion Host Controller. A value of one indicates that the port is routed to the next lowest numbered function companion Host Controller, and so on.

11.3 Operational registers of Enhanced USB Host Controller

11.3.1 USBCMD register

The USB Command (USBCMD) register indicates the command to be executed by the serial Host Controller. Writing to this register causes a command to be executed. Table 92 shows the bit allocation.

Table 92. USBCMD - USB Command register bit allocation

Address: Content of the base address register + 20h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	ITC[7:0]							
Reset	0	0	0	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	LHCR	IAAD	ASE	PSE	FLS[1:0]		HC RESET	RS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 93. USBCMD - USB Command register bit description

Address: Content of the base address register + 20h

Bit	Symbol	Description
31 to 24	reserved	-
23 to 16	ITC[7:0]	**Interrupt Threshold Control**: Default = 08h. This field is used by the system software to select the maximum rate at which the Host Controller will issue interrupts. If software writes an invalid value to this register, the results are undefined. Valid values are: **00h —** reserved **01h —** 1 micro frame **02h —** 2 micro frames **04h —** 4 micro frames **08h —** 8 micro frames (equals 1 ms) **10h —** 16 micro frames (equals 2 ms) **20h —** 32 micro frames (equals 4 ms) **40h —** 64 micro frames (equals 8 ms) Software modifications to this field while HCH (bit 12) in the USBSTS register is zero results in undefined behavior.
15 to 8	reserved	-
7	LHCR	**Light Host Controller Reset**: This control bit is not required. It allows the driver software to reset the EHCI controller, without affecting the state of the ports or the relationship to the companion Host Controllers. If not implemented, a read of this field will always return zero. If implemented, on read: **0 —** Indicates that the Light Host Controller Reset has completed and it is ready for the host software to reinitialize the Host Controller **1 —** Indicates that the Light Host Controller Reset has not yet completed
6	IAAD	**Interrupt on Asynchronous Advance Doorbell**: This bit is used as a doorbell by software to notify the Host Controller to issue an interrupt the next time it advances the asynchronous schedule. Software must write logic 1 to this bit to ring the doorbell. When the Host Controller has evicted all appropriate cached schedule states, it sets IAA (bit 5 in the USBSTS register). If IAAE (bit 5 in the USBINTR register) is logic 1, then the Host Controller will assert an interrupt at the next interrupt threshold. The Host Controller sets this bit to logic 0 after it sets IAA. Software should not set this bit when the asynchronous schedule is inactive because this results in an undefined value.

Table 93. USBCMD - USB Command register bit description *...continued*

Address: Content of the base address register + 20h

Bit	Symbol	Description
5	ASE	**Asynchronous Schedule Enable**: Default = logic 0. This bit controls whether the Host Controller skips processing the asynchronous schedule. **0 —** Do not process the asynchronous schedule **1 —** Use the ASYNCLISTADDR register to access the asynchronous schedule
4	PSE	**Periodic Schedule Enable**: Default = logic 0. This bit controls whether the Host Controller skips processing the periodic schedule. **0 —** Do not process the periodic schedule **1 —** Use the PERIODICLISTBASE register to access the periodic schedule
3 and 2	FLS[1:0]	**Frame List Size**: Default = 00b. This field is read and write only if PFLF (bit 1) in the HCCPARAMS register is set to logic 1. This field specifies the size of the frame list. The size the frame list controls which bits in the Frame Index register should be used for the frame list current index. **00b —** 1024 elements (4096 B) **01b —** 512 elements (2048 B) **10b —** 256 elements (1024 B) for small environments **11b —** reserved
1	HCRESET	**Host Controller Reset**: This control bit is used by the software to reset the Host Controller. The effects of this on Root Hub registers are similar to a chip hardware reset. Setting this bit causes the Host Controller to reset its internal pipelines, timers, counters, state machines, and so on, to their initial values. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. This reset does not affect the PCI Configuration registers. All operational registers, including port registers and port state machines, are set to their initial values. Port ownership reverts to the companion Host Controller(s). The software must reinitialize the Host Controller to return it to an operational state. This bit is cleared by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing logic 0 to this register. Software should check that bit HCH is logic 0 before setting this bit. Attempting to reset an actively running Host Controller results in undefined behavior.
0	RS	**Run/Stop**: logic 1 = Run. logic 0 = Stop. When set, the Host Controller executes the schedule. The Host Controller continues execution as long as this bit is set. When this bit is cleared, the Host Controller completes the current and active transactions in the USB pipeline, and then halts. Bit HCH indicates when the Host Controller has finished the transaction and has entered the stopped state. Software should check that the HCH bit is logic 1, before setting this bit.

11.3.2 USBSTS register

The USB Status (USBSTS) register indicates pending interrupts and various states of the Host Controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software clears the register bits by writing ones to them. The bit allocation is given in Table 94.

Table 94. USBSTS - USB Status register bit allocation

Address: Content of the base address register + 24h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	ASS	PSSTAT	RECL	HCH	reserved[1]			
Reset	0	0	0	1	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]		IAA	HSE	FLR	PCD	USB ERRINT	USBINT
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 95. USBSTS - USB Status register bit description

Address: Content of the base address register + 24h

Bit	Symbol	Description
31 to 16	reserved	-
15	ASS	**Asynchronous Schedule Status**: Default = logic 0. The bit reports the current real status of the asynchronous schedule. If this bit is logic 0, the status of the asynchronous schedule is disabled. If this bit is logic 1, the status of the asynchronous schedule is enabled. The Host Controller is not required to immediately disable or enable the asynchronous schedule when software changes ASE (bit 5 in the USBCMD register). When this bit and the ASE bit have the same value, the asynchronous schedule is either enabled (1) or disabled (0).
14	PSSTAT	**Periodic Schedule Status**: Default = logic 0. This bit reports the current status of the periodic schedule. If this bit is logic 0, the status of the periodic schedule is disabled. If this bit is logic 1, the status of the periodic schedule is enabled. The Host Controller is not required to immediately disable or enable the periodic schedule when software changes PSE (bit 4) in the USBCMD register. When this bit and the PSE bit have the same value, the periodic schedule is either enabled (1) or disabled (0).
13	RECL	**Reclamation**: Default = logic 0. This is a read-only status bit that is used to detect an empty asynchronous schedule.
12	HCH	**HCHalted**: Default = logic 1. This bit is logic 0 when RS (bit 0) in the USBCMD register is logic 1. The Host Controller sets this bit to logic 1 after it has stopped executing because the RS bit is set to logic 0, either by software or by the Host Controller hardware. For example, on an internal error.

Table 95. USBSTS - USB Status register bit description *...continued*

Address: Content of the base address register + 24h

Bit	Symbol	Description
11 to 6	reserved	-
5	IAA	**Interrupt on Asynchronous Advance**: Default = logic 0. The system software can force the Host Controller to issue an interrupt the next time the Host Controller advances the asynchronous schedule by writing logic 1 to IAAD (bit 6) in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	HSE	**Host System Error**: The Host Controller sets this bit when a serious error occurs during a host system access, involving the Host Controller module. In a PCI system, conditions that set this bit include PCI parity error, PCI master abort and PCI target abort. When this error occurs, the Host Controller clears RS (bit 0 in the USBCMD register) to prevent further execution of the scheduled TDs.
3	FLR	**Frame List Rollover**: The Host Controller sets this bit to logic 1 when the frame list index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size—as programmed in FLS (bit 3 and bit 2) of the USBCMD register—is 1024, the Frame Index register rolls over every time bit 13 of the FRINDEX register toggles. Similarly, if the size is 512, the Host Controller sets this bit to logic 1 every time bit 12 of the FRINDEX register toggles.
2	PCD	**Port Change Detect**: The Host Controller sets this bit to logic 1 when any port— where PO (bit 13 of PORTSC) is cleared—changes to logic 1, or FPR (bit 6 of PORTSC) changes to logic 1 as a result of a J-to-K transition detected on a suspended port. This bit is allowed to be maintained in the auxiliary power well. Alternatively, it is also acceptable that—on a D3-to-D0 transition of the EHCI Host Controller device—this bit is loaded with the logical OR of all the PORTSC change bits, including force port resume, overcurrent change, enable or disable change, and connect status change.
1	USB ERRINT	**USB Error Interrupt**: The Host Controller sets this bit when an error condition occurs because of completing a USB transaction. For example, error counter underflow. If the Transfer Descriptor (TD) on which the error interrupt occurred also had its IOC bit set, both this bit and the USBINT bit are set. For details, refer to the *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*.
0	USBINT	**USB Interrupt**: The Host Controller sets this bit on completing a USB transaction, which results in the retirement of a TD that had its IOC bit set. The Host Controller also sets this bit when a short packet is detected, that is, the actual number of bytes received was less than the expected number of bytes. For details, refer to the *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*.

11.3.3 USBINTR register

The USB Interrupt Enable (USBINTR) register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in USBSTS to allow the software to poll for events. The USBSTS register bit allocation is given in Table 96.

Table 96. USBINTR - USB Interrupt Enable register bit allocation

Address: Content of the base address register + 28h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]		IAAE	HSEE	FLRE	PCIE	USB ERRINTE	USBINTE
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 97. USBINTR - USB Interrupt Enable register bit description

Address: Content of the base address register + 28h

Bit	Symbol	Description
31 to 6	reserved	-
5	IAAE	**Interrupt on Asynchronous Advance Enable**: When this bit and IAA (bit 5 in the USBSTS register) are set, the Host Controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing bit IAA.
4	HSEE	**Host System Error Enable**: When this bit and HSE (bit 4 in the USBSTS register) are set, the Host Controller issues an interrupt. The interrupt is acknowledged by software clearing bit HSE.
3	FLRE	**Frame List Rollover Enable**: When this bit and FLR (bit 3 in the USBSTS register) are set, the Host Controller issues an interrupt. The interrupt is acknowledged by software clearing bit FLR.
2	PCIE	**Port Change Interrupt Enable**: When this bit and PCD (bit 2 in the USBSTS register) are set, the Host Controller issues an interrupt. The interrupt is acknowledged by software clearing bit PCD.
1	USB ERRINTE	**USB Error Interrupt Enable**: When this bit and USBERRINT (bit 1 in the USBSTS register) are set, the Host Controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing bit USBERRINT.
0	USBINTE	**USB Interrupt Enable**: When this bit and USBINT (bit 0 in the USBSTS register) are set, the Host Controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing bit USBINT.

11.3.4 FRINDEX register

The Frame Index (FRINDEX) register is used by the Host Controller to index into the periodic frame list. The register updates every 125 µs—once each micro frame.
Bits N to 3 are used to select a particular entry in the periodic frame list during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by the system software in FLS[1:0] (bit 3 and bit 2) of the USBCMD register. This register must be written as a double word. Byte writes produce undefined results. This register cannot be written unless the Host Controller is in the halted state, as indicated by HCH (bit 12 in the USBSTS register). A write to this register while RS (bit 0 in the USBCMD register) is set produces undefined results. Writes to this register also affect the SOF value.

The bit allocation is given in Table 98.

Table 98. FRINDEX - Frame Index register bit allocation
Address: Content of the base address register + 2Ch

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]		FRINDEX[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FRINDEX[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 99. FRINDEX - Frame Index register bit description

Address: Content of the base address register + 2Ch

Bit	Symbol	Description
31 to 14	reserved	-
13 to 0	FRINDEX [13:0]	**Frame Index**: Bits in this register are used for the frame number in the SOF packet and as the index into the frame list. The value in this register increments at the end of each time frame. For example, micro frame. The bits used for the frame number in the SOF token are taken from bits 13 to 3 of this register. Bits N to 3 are used for the frame list current index. This means that each location of the frame list is accessed eight times—frames or micro frames—before moving to the next index. The following illustrates values of N based on the value of FLS[1:0] (bit 3 and bit 2 in the USBCMD register).

FLS[1:0]	Number elements	N
00b	1024	12
01b	512	11
10b	256	10
11b	reserved	-

11.3.5 PERIODICLISTBASE register

The Periodic Frame List Base Address (PERIODLISTBASE) register contains the beginning address of the periodic frame list in the system memory. If the Host Controller is in 64-bit mode—as indicated by logic 1 in 64AC (bit 0 of the HCCSPARAMS register)—the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register. The system software loads this register before starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed as 4 kB aligned. The contents of this register are combined with the FRINDEX register to enable the Host Controller to step through the periodic frame list in sequence.

The bit allocation is given in Table 100.

Table 100. PERIODICLISTBASE - Periodic Frame List Base Address register bit allocation

Address: Content of the base address register + 34h

Bit	31	30	29	28	27	26	25	24
Symbol	BA[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	BA[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	BA[3:0]				reserved[1]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 101. PERIODICLISTBASE - Periodic Frame List Base Address register bit description
Address: Content of the base address register + 34h

Bit	Symbol	Description
31 to 12	BA[19:0]	**Base Address**: These bits correspond to memory address signals 31 to 12, respectively.
11 to 0	reserved	-

11.3.6 ASYNCLISTADDR register

This 32-bit register contains the address of the next asynchronous queue head to be executed. If the Host Controller is in 64-bit mode—as indicated by logic 1 in 64AC (bit 0 of the HCCPARAMS register)—the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register. Bits 4 to 0 of this register always return zeros when read. The memory structure referenced by the physical memory pointer is assumed as 32 B (cache aligned). For bit allocation, see Table 102.

Table 102. ASYNCLISTADDR - Current Asynchronous List Address register bit allocation
Address: Content of the base address register + 38h

Bit	31	30	29	28	27	26	25	24
Symbol	LPL[26:19]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	LPL[18:11]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	LPL[10:3]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	LPL[2:0]			reserved[1]				
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 103. ASYNCLISTADDR - Current Asynchronous List Address register bit description
Address: Content of the base address register + 38h

Bit	Symbol	Description
31 to 5	LPL[26:0]	**Link Pointer List**: These bits correspond to memory address signals 31 to 5, respectively. This field may only reference a Queue Head (QH).
4 to 0	reserved	-

11.3.7 CONFIGFLAG register

The bit allocation of the Configure Flag (CONFIGFLAG) register is given in Table 104.

Table 104. CONFIGFLAG - Configure Flag register bit allocation
Address: Value read from func2 of address 10h + 60h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]							CF
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits should always be written with the reset value.

Table 105. CONFIGFLAG - Configure Flag register bit description
Address: Value read from func2 of address 10h + 60h

Bit	Symbol	Description
31 to 1	reserved	-
0	CF	**Configure Flag**: The host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic. **0 —** Port-routing control logic default-routes each port to an implementation dependent classic Host Controller **1 —** Port-routing control logic default-routes all ports to this Host Controller

11.3.8 PORTSC registers 1, 2

The Port Status and Control (PORTSC) register is in the auxiliary power well. It is only reset by hardware when the auxiliary power is initially applied or in response to a Host Controller reset. The initial conditions of a port are:

- No device connected
- Port disabled

If the port has power control, software cannot change the state of the port until it sets the port power bits. Software must not attempt to change the state of the port until power is stable on the port; maximum delay is 20 ms from the transition. For bit allocation, see Table 106.

Table 106. PORTSC 1, 2 - Port Status and Control 1, 2 register bit allocation

Address: Content of the base address register + 64h + (4 × Port Number − 1) where Port Number is 1, 2

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved	WKOC_E	WKDS CNNT_E	WKCNNT _E	PTC[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]		PO	PP	LS[1:0]		reserved[1]	PR
Reset	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SUSP	FPR	OCC	OCA	PEDC	PED	ECSC	ECCS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R/W	R/W	R/W	R

[1] The reserved bits should always be written with the reset value.

Table 107. PORTSC 1, 2 - Port Status and Control 1, 2 register bit description

Address: Content of the base address register + 64h + (4 × Port Number − 1) where Port Number is 1, 2

Bit	Symbol	Description
31 to 23	reserved	-
22	WKOC_E	**Wake on Overcurrent Enable**: Default = logic 0. Setting this bit enables the port to be sensitive to overcurrent conditions as wake-up events.[1]
21	WKDS CNNT_E	**Wake on Disconnect Enable**: Default = logic 0. Setting this bit enables the port to be sensitive to device disconnects as wake-up events.[1]
20	WKCNNT _E	**Wake on Connect Enable**: Default = logic 0. Setting this bit enables the port to be sensitive to device connects as wake-up events.[1]

Table 107. PORTSC 1, 2 - Port Status and Control 1, 2 register bit description *...continued*

Address: Content of the base address register + 64h + (4 × Port Number − 1) where Port Number is 1, 2

Bit	Symbol	Description
19 to 16	PTC[3:0]	**Port Test Control**: Default = 0000b. When this field is logic 0, the port is not operating in test mode. A nonzero value indicates that it is operating in test mode and test mode is indicated by the value. The encoding of the test mode bits are: **0000b —** Test mode disabled **0001b —** Test J_STATE **0010b —** Test K_STATE **0011b —** Test SE0_NAK **0100b —** Test packet **0101b —** Test FORCE_ENABLE **0110b to 1111b —** reserved
15 and 14	reserved	-
13	PO	**Port Owner**: Default = logic 1. This bit unconditionally goes to logic 0 when CF (bit 0) in the CONFIGFLAG register makes logic 0 to logic 1 transition. This bit unconditionally goes to logic 1 when the CF bit is logic 0. The system software uses this field to release ownership of the port to a selected Host Controller, if the attached device is not a high-speed device. Software writes logic 1 to this bit, if the attached device is not a high-speed device. Logic 1 in this bit means that a companion Host Controller owns and controls the port.
12	PP	**Port Power**: The function of this bit depends on the value of PPC (bit 4) in the HCSPARAMS register. **If PPC = logic 0 and PP = logic 1 —** The Host Controller does not have port power control switches. Always powered **If PPC = logic 1 and PP = logic 1 or logic 0 —** The Host Controller has port power control switches. This bit represents the current setting of the switch: logic 0 = off, logic 1 = on. When PP is logic 0, the port is nonfunctional and will not report any status When an overcurrent condition is detected on a powered port and PPC is logic 1, the PP bit in each affected port may be changed by the Host Controller from logic 1 to logic 0, removing power from the port.
11 and 10	LS[1:0]	**Line Status**: This field reflects the current logical levels of the DP (bit 11) and DM (bit 10) signal lines. These bits are used to detect low-speed USB devices before the port reset and enable sequence. This field is valid only when the Port Enable bit is logic 0, and the Current Connect Status bit is set to logic 1. **00b —** SE0: Not a low-speed device, perform EHCI reset **01b —** K-state: Low-speed device, release ownership of port **10b —** J-state: Not a low-speed device, perform EHCI reset **11b —** Undefined: Not a low-speed device, perform EHCI reset If the PP bit is logic 0, this field is undefined
9	reserved	-

Table 107. PORTSC 1, 2 - Port Status and Control 1, 2 register bit description *...continued*

Address: Content of the base address register + 64h + (4 × Port Number − 1) where Port Number is 1, 2

Bit	Symbol	Description
8	PR	**Port Reset**: Logic 1 means the port is in reset. Logic 0 means the port is not in reset. Default = logic 0. When software sets this bit from logic 0, the bus reset sequence as defined in *Universal Serial Bus Specification Rev. 2.0* is started. Software clears this bit to terminate the bus reset sequence. Software must hold this bit at logic 1 until the reset sequence, as specified in *Universal Serial Bus Specification Rev. 2.0*, is completed. **Remark:** When software sets this bit, it must also clear the Port Enable bit. **Remark:** When software clears this bit, there may be a delay before the bit status changes to logic 0 because it will not read logic 0 until the reset is completed. If the port is in high-speed mode after reset is completed, the Host Controller will automatically enable this port; it can set the Port Enable bit. A Host Controller must terminate the reset and stabilize the state of the port within 2 ms of software changing this bit from logic 1 to logic 0. For example, if the port detects that the attached device is high-speed during a reset, then the Host Controller must enable the port within 2 ms of software clearing this bit. HCH (bit 12) in the USBSTS register must be logic 0 before software attempts to use this bit. The Host Controller may hold Port Reset asserted when the HCH bit is set.[1]
7	SUSP	**Suspend**: Default = logic 0. Logic 1 means the port is in the suspend state. Logic 0 means the port is not suspended. The PED (Port Enabled) bit and this bit define the port states as follows: **PED = logic 0 and SUSP = X —** Port is disabled **PED = logic 1 and SUSP = logic 0 —** Port is enabled **PED = logic 1 and SUSP = logic 1 —** Port is suspended When in the suspend state, downstream propagation of data is blocked on this port, except for the port reset. If a transaction was in progress when this bit was set, blocking occurs at the end of the current transaction. In the suspend state, the port is sensitive to resume detection. The bit status does not change until the port is suspended and there may be a delay in suspending a port, if there is a transaction currently in progress on the USB. Attempts to clear this bit are ignored by the Host Controller. The Host Controller will unconditionally set this bit to logic 0 when: • Software changes the FPR (Force Port Resume) bit to logic 0 • Software changes the PR (Port Reset) bit to logic 1 If the host software sets this bit when the Port Enabled bit is logic 0, the results are undefined.[1]

Table 107. PORTSC 1, 2 - Port Status and Control 1, 2 register bit description *...continued*

Address: Content of the base address register + 64h + (4 × Port Number − 1) where Port Number is 1, 2

Bit	Symbol	Description
6	FPR	**Force Port Resume**: Logic 1 means resume detected or driven on the port. Logic 0 means no resume (K-state) detected or driven on the port. Default = logic 0. Software sets this bit to drive the resume signaling. The Host Controller sets this bit if a J-to-K transition is detected, while the port is in the suspend state. When this bit changes to logic 1 because a J-to-K transition is detected, PCD (bit 2) in the USBSTS register is also set to logic 1. If software sets this bit to logic 1, the Host Controller must not set the PCD bit. When the EHCI controller owns the port, the resume sequence follows the sequence specified in *Universal Serial Bus Specification Rev. 2.0*. The resume signaling (full-speed 'K') is driven on the port as long as this bit remains set. Software must time the resume and clear this bit after the correct amount of time has elapsed. Clearing this bit causes the port to return to high-speed mode, forcing the bus below the port into a high-speed idle. This bit will remain at logic 1, until the port has switched to the high-speed idle. The Host Controller must complete this transition within 2 ms of software clearing this bit.[1]
5	OCC	**Overcurrent Change**: Default = logic 0. This bit is set to logic 1 when there is a change in overcurrent active. Software clears this bit by setting it to logic 1.
4	OCA	**Overcurrent Active**: Default = logic 0. If set to logic 1, this port has an overcurrent condition. If set to logic 0, this port does not have an overcurrent condition. This bit will automatically change from logic 1 to logic 0 when the overcurrent condition is removed.
3	PEDC	**Port Enable/Disable Change**: Logic 1 means the port enabled or disabled status has changed. Logic 0 means no change. Default = logic 0. For the root hub, this bit is set only when a port is disabled because of the appropriate conditions existing at the EOF2 point. For definition of port error, refer to Chapter 11 of *Universal Serial Bus Specification Rev. 2.0*. Software clears this bit by setting it.[1]
2	PED	**Port Enabled/Disabled**: Logic 1 means enable. Logic 0 means disable. Default = logic 0. Ports can only be enabled by the Host Controller as a part of the reset and enable sequence. Software cannot enable a port by writing logic 1 to this field. The Host Controller will only set this bit when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition or by host software. The bit status does not change until the port state has changed. There may be a delay in disabling or enabling a port because of other Host Controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port, except for reset.[1]
1	ECSC	**Connect Status Change**: Logic 1 means change in ECCS. Logic 0 means no change. Default = logic 0. This bit indicates a change has occurred in the ECCS of the port. The Host Controller sets this bit for all changes to the port device connect status, even if the system software has not cleared an existing connect status change. For example, the insertion status changes two times before the system software has cleared the changed condition, hub hardware will be setting an already-set bit, that is, the bit will remain set. Software clears this bit by writing logic 1 to it.[1]
0	ECCS	**Current Connect Status**: Logic 1 indicates a device is present on the port. Logic 0 indicates no device is present. Default = logic 0. This value reflects the current state of the port and may not directly correspond to the event that caused the ECSC bit to be set.[1]

[1] These fields read logic 0, if the PP bit is logic 0.

12. Power consumption

Table 108 shows the power consumption.

Table 108. Power consumption

Power pins group	Conditions	Typ	Unit
Total power $V_{CC(I/O)\_AUX} + V_{I(VAUX3V3)} + V_{DDA\_AUX} + V_{CC(I/O)} + V_{I(VREG3V3)}$	no device connected to the SAF1562HL[1]	39	mA
	one high-speed device connected to the SAF1562HL	58	mA
	two high-speed devices connected to the SAF1562HL	76	mA
Auxiliary power $V_{CC(I/O)\_AUX} + V_{I(VAUX3V3)} + V_{DDA\_AUX}$	no device connected to the SAF1562HL[1]	26	mA
	one high-speed device connected to the SAF1562HL	44	mA
	two high-speed devices connected to the SAF1562HL	62	mA
$V_{CC(I/O)} + V_{I(VREG3V3)}$	no device connected to the SAF1562HL[1]	13	mA
	one high-speed device connected to the SAF1562HL	14	mA
	two high-speed devices connected to the SAF1562HL	14	mA

[1] When one or two full-speed or low-speed power devices are connected, the power consumption is comparable to the power consumption when no high-speed devices are connected. There is a difference of approximately 1 mA.

Table 109 shows the power consumption in S1 and S3 suspend modes.

Table 109. Power consumption: S1 and S3

Power state	Typ	Unit
S1[1]	20	mA
S3[2]	12[3]	mA

[1] S1 represents the system state that will determine the B1 and D1 states. For details refer to the *PCI Bus Power Management Interface Specification Rev.1.1.*

[2] S3 represents the system state that will determine the B3 and D3 states. For details refer to the *PCI Bus Power Management Interface Specification Rev.1.1.*

[3] When I^2C-bus is present.

13. Limiting values

Table 110. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(I/O)}$	supply voltage to I/O pins			–0.5	+4.6	V
$V_{I(VREG3V3)}$	supply voltage to internal regulator			–0.5	+4.6	V
$V_{CC(I/O)\_AUX}$	auxiliary supply voltage to I/O pins			–0.5	+4.6	V
$V_{I(VAUX3V3)}$	auxiliary input voltage to internal regulator			–0.5	+4.6	V
V_{DDA_AUX}	auxiliary supply voltage for analog block			–0.5	+4.6	V
$V_{I(3V3)}$	input voltage on 3.3 V buffers			0	$V_{CC(I/O)}$ + 0.5 V	V
I_{lu}	latch-up current	$V_I < 0$ V or $V_I > V_{CC(I/O)}$		-	100	mA
V_{esd}	electrostatic discharge voltage	machine model	[1]	–200	+200	V
		human body model	[2]	–2000	+2000	V
T_{amb}	ambient temperature			–40	+85	°C
T_{stg}	storage temperature			–55	+150	°C

[1] Class B according to EIA/JESD22-A115-A.

[2] Class 2 according to JESD22-A114C.01.

14. Thermal characteristics

Table 111. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		12	K/W

15. Static characteristics

Table 112. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(I/O)}$	supply voltage to I/O pins		3.0	3.3	3.6	V
$V_{I(VREG3V3)}$	supply voltage to internal regulator		3.0	3.3	3.6	V
$V_{CC(I/O)\_AUX}$	auxiliary supply voltage to I/O pins		3.0	3.3	3.6	V
$V_{I(VAUX3V3)}$	auxiliary input voltage to internal regulator		3.0	3.3	3.6	V
V_{DDA_AUX}	auxiliary supply voltage for analog block		3.0	3.3	3.6	V

Table 113. Static characteristics: I²C-bus interface (SDA and SCL)

$V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.1	-	3.6	V
V_{IL}	LOW-level input voltage		0	-	0.9	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V

Table 114. Static characteristics: digital pins

$V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.0	-	3.6	V
V_{IL}	LOW-level input voltage		0	-	0.8	V
I_{LI}	input leakage current	0 V < V_I < $V_{CC(I/O)}$	–10	-	+10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	2.4	-	-	V

Table 115. Static characteristics: PCI interface block

$V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		0.66$V_{CC(I/O)}$	-	$V_{CC(I/O)}$	V
V_{IL}	LOW-level input voltage		0	-	0.9	V
V_{IPU}	input pull-up voltage		2.1	-	-	V
I_{LI}	input leakage current	0 V < V_I < $V_{CC(I/O)}$	–10	-	+10	µA
V_{OH}	HIGH-level output voltage	I_O = –500 µA	2.7	-	-	V
V_{OL}	LOW-level output voltage	I_O = 1500 µA	-	-	0.3	V
C_{IN}	input pin capacitance		-	-	10	pF
C_{clk}	clock capacitance		5	-	12	pF
C_{IDSEL}	IDSEL pin capacitance		-	-	8	pF

Table 116. Static characteristics: USB interface block (pins DM1 to DM2 and DP1 to DP2)

V_{DDA_AUX} = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified. Abstract of the USB specification rev. 2.0.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels for high-speed						
V_{HSSQ}	squelch detection threshold (differential signal amplitude)	squelch detected	-	-	100	mV
		no squelch detected	150	-	-	mV
V_{HSDSC}	disconnect detection threshold (differential signal amplitude)	disconnect detected	625	-	-	mV
		disconnect not detected	-	-	525	mV
V_{HSCM}	data signaling common mode voltage range		–50	-	+500	mV
Output levels for high-speed						
V_{HSOI}	idle state		–10	-	+10	mV
V_{HSOH}	data signaling HIGH		360	-	440	mV
V_{HSOL}	data signaling LOW		–10	-	+10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	[1]	700	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	[1]	–900	-	–500	mV
Input levels for full-speed and low-speed						
V_{IH}	HIGH-level input voltage (drive)		2.0	-	-	V
V_{IHZ}	HIGH-level input voltage (floating)		2.7	-	3.6	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{DI}	differential input sensitivity	$\|V_{DP} - V_{DM}\|$	0.2	-	-	V
V_{CM}	differential common mode range		0.8	-	0.6V_{DDA_AUX}	V

Table 116. Static characteristics: USB interface block (pins DM1 to DM2 and DP1 to DP2) *…continued*

V_{DDA_AUX} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. Abstract of the USB specification rev. 2.0.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output levels for full-speed and low-speed						
V_{OH}	HIGH-level output voltage		V_{DDA_AUX} − 1.1	-	V_{DDA_AUX}	V
V_{OL}	LOW-level output voltage		0	-	0.3	V
V_{OSE1}	SE1		0.8	-	-	V
V_{CRS}	output signal crossover point voltage		1.3	-	2.0	V

[1] Minimum value: High-speed termination resistor disabled, pull-up resistor connected. Only during reset, when both the hub and device are capable of high-speed operation.

Table 117. Static characteristics: POR

T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{trip(H)}$	HIGH-level trip voltage		1.0	1.2	1.4	V
$V_{trip(L)}$	LOW-level trip voltage		0.95	1.1	1.3	V

16. Dynamic characteristics

Table 118. Dynamic characteristics: system clock timing

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Crystal oscillator							
f_{clk}	PCI clock			31	-	33	MHz
	external clock input	crystal	[1][2]	-	12	-	MHz
R_S	series resistance			-	-	100	Ω
C_L	load capacitance			-	18	-	pF
External clock input							
V_{IH}	HIGH-level input voltage			$0.8V_{AUX1V8}$	-	V_{AUX1V8}	V
V_{IL}	LOW-level input voltage			-	-	$0.2V_{AUX1V8}$	V
J	external clock jitter			-	-	50	ppm
t_{CR}, t_{CF}	rise time and fall time			-	-	3	ns
δ	clock duty cycle			-	50	-	%

[1] Recommended accuracy of the clock frequency is 50 ppm for the crystal and oscillator.

[2] Suggested values for external capacitors when using a crystal are 22 pF to 27 pF.

Table 119. Dynamic characteristics: I^2C-bus interface (SDA and SCL)

$V_{CC(I/O)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. Abstract of the I^2C-bus specification rev. 2.1.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{CF}	output fall time V_{IH} to V_{IL}	$10 < C_b < 400$	[1]	-	0	250	ns

[1] The capacitive load for each bus line (C_b) is specified in pF. To meet the specification for V_{OL} and the maximum rise time (300 ns), use an external pull-up resistor with $R_{UP(max)} = 850 / C_b$ kΩ and $R_{UP(min)} = (V_{CC(I/O)} − 0.4) / 3$ kΩ.

Table 120. Dynamic characteristics: high-speed source electrical characteristics

V_{DDA_AUX} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. Abstract of the USB specification rev. 2.0.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{HSR}	high-speed differential rise time	10 % to 90 %	500	-	-	ps
t_{HSF}	high-speed differential fall time	90 % to 10 %	500	-	-	ps
Z_{HSDRV}	drive output resistance; also serves as a high-speed termination	includes the R_S resistor	40.5	45	49.5	Ω
Clock timing						
t_{HSDRAT}	data rate		479.76	-	480.24	Mbit/s
t_{HSFRAM}	micro frame interval		124.9375	-	125.0625	µs
t_{HSRFI}	consecutive micro frame interval difference	[1]	1	-	-	ns

[1] Maximum value: four high-speed bit times.

Table 121. Dynamic characteristics: full-speed source electrical characteristics

V_{DDA_AUX} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. Abstract of the USB specification rev. 2.0.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{FR}	rise time	C_L = 50 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRFM}	differential rise and fall time matching		90	-	111.1	%
Data timing: see Figure 11						
t_{FDEOP}	source jitter for differential transition to SEO transition	full-speed timing	−2	-	+5	ns
t_{FEOPT}	source SE0 interval of EOP		160	-	175	ns
t_{FEOPR}	receiver SE0 interval of EOP		82	-	-	ns
t_{LDEOP}	source jitter for differential transition to SEO transition	low-speed timing	−40	-	+100	ns
t_{LEOPT}	source SE0 interval of EOP		1.25	-	1.5	µs
t_{LEOPR}	receiver SE0 interval of EOP		670	-	-	ns
t_{FST}	width of SE0 interval during the differential transaction		-	-	14	ns

Table 122. Dynamic characteristics: full-speed source electrical characteristics

V_{DDA_AUX} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. Abstract of the USB specification rev. 2.0.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{LR}	rise time		75	-	300	ns
t_{LF}	fall time		75	-	300	ns
t_{LRFM}	differential rise and fall time matching		90	-	125	%

16.1 Timing

Table 123. PCI clock and IO timing
Abstract of the USB specification rev. 2.0.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PCI clock timing; see Figure 8						
$T_{cyc(PCICLK)}$	PCICLK cycle time		30	-	32	ns
$t_{HIGH(PCICLK)}$	PCICLK HIGH time		11	-	-	ns
$t_{LOW(PCICLK)}$	PCICLK LOW time		11	-	-	ns
SR_{PCICLK}	PCICLK slew rate		1	-	4	V/ns
$SR_{RST\#}$	RST# slew rate		50	-	-	mV/ns
PCI input timing; see Figure 9						
$t_{su(PCICLK)bs}$	setup time to PCICLK (bus signal)		7	-	-	ns
$t_{su(PCICLK)ptp}$	setup time to PCICLK (point-to-point)	[1]	10	-	-	ns
$t_{h(PCICLK)}$	input hold time from PCICLK		0	-	-	ns
PCI output timing; see Figure 10						
$t_{val(PCICLK)bs}$	PCICLK to signal valid delay (bus signal)		2	-	11	ns
$t_{val(PCICLK)ptp}$	PCICLK to signal valid delay (point-to-point)	[1]	2	-	12	ns
$t_{dZ(act)}$	float to active delay		2	-	-	ns
$t_{d(act)Z}$	active to float delay		-	-	28	ns
PCI reset timing						
t_{rst}	reset active time after CLK stable		1	-	-	ms

[1] REQ# and GNT# are point-to-point signals. GNT# has a setup of 10 ns; REQ# has a setup of 12 ns. All others are bus signals.

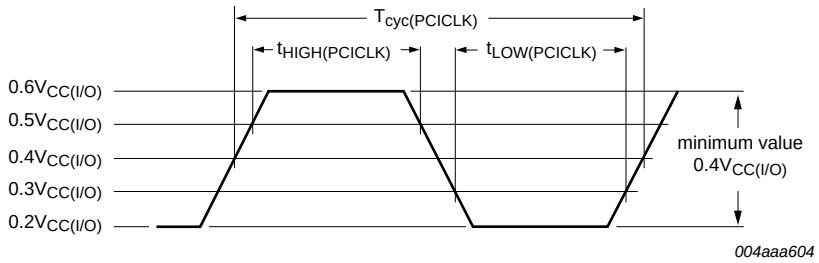


Fig 8. PCI clock

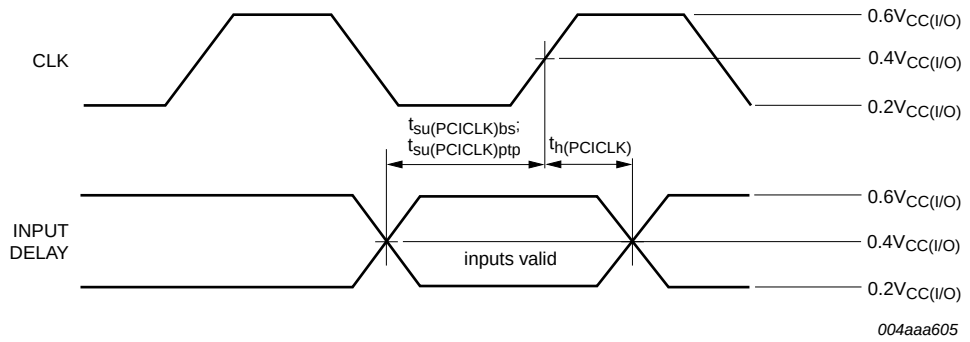


Fig 9. PCI input timing

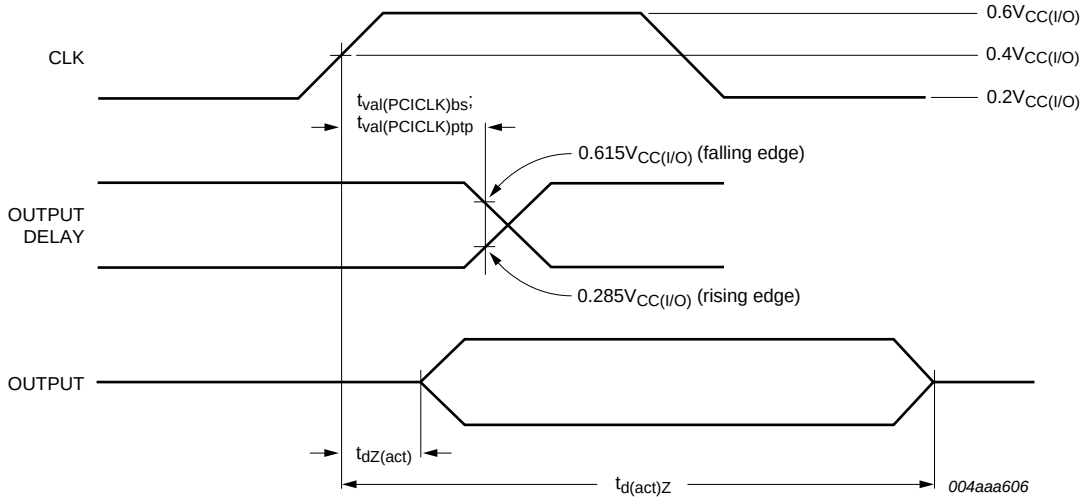
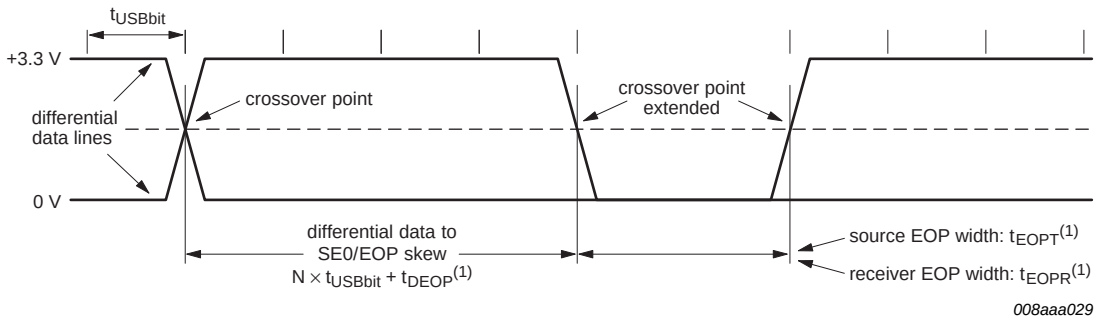


Fig 10. PCI output timing



t$_{USBbit}$ is the bit duration (USB data).

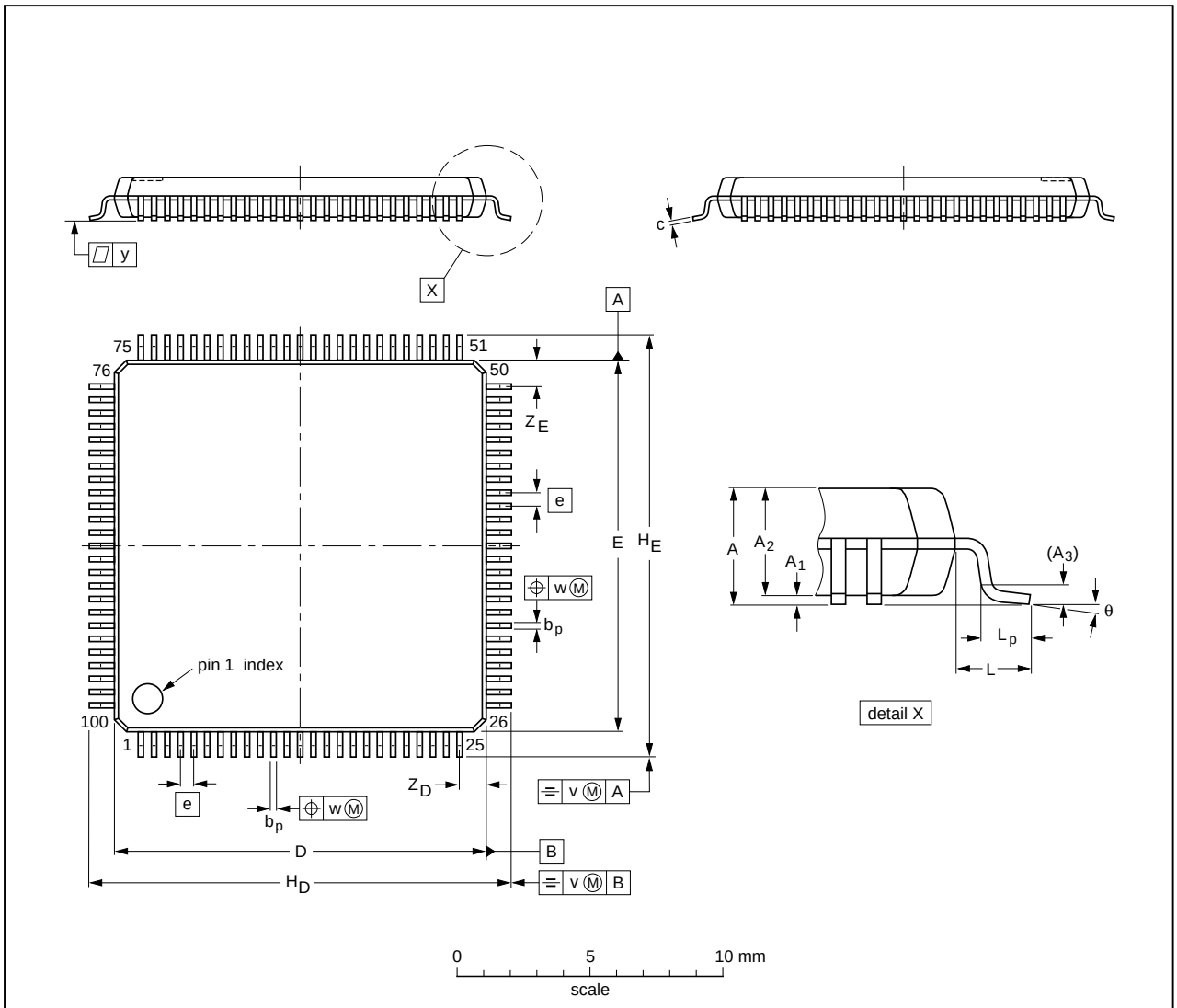
t$_{DEOP}$[1] is the source jitter for differential transition to SEO transition.

(1) Full-speed and low-speed timing symbols have a subscript prefix 'F' and 'L', respectively.

Fig 11. USB source differential data-to-EOP transition skew and EOP width

17. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 12. Package outline SOT407-1 (LQFP100)

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 124 and 125

Table 124. SnPb eutectic process (from J-STD-020C)

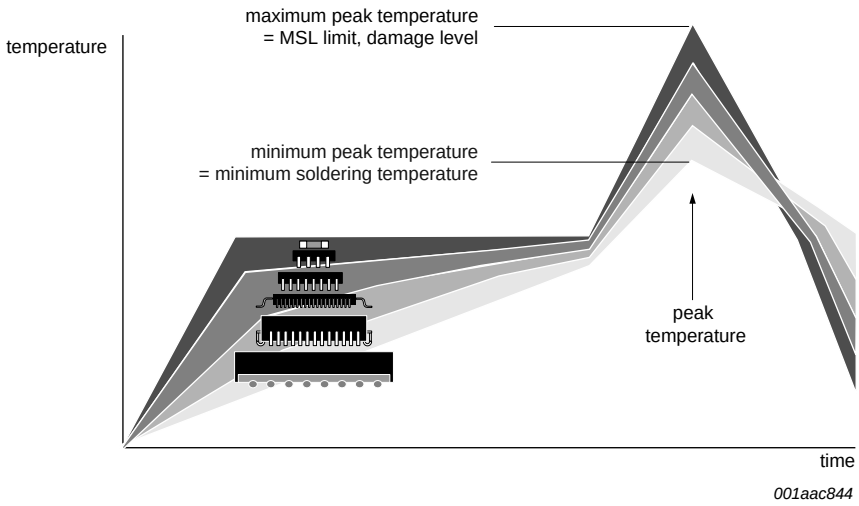
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 125. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Appendix

19.1 Erratum 1

A higher than expected suspend current is measured in $D3_{cold}$ suspend.

19.1.1 Problem description

The $D3_{cold}$ suspend current is approximately 12 mA which is higher than expected. The higher suspend current is due to internal leakage. In $D3_{cold}$ suspend only $V_{I(VAUX3V3)}$ is supplied. The remaining supply voltages are cut off to save power.

19.1.2 Implication

The implication is moderate. This issue occurs only in $D3_{cold}$ suspend which is generally seen in the system that implements PCI power management such as a desktop PC.

This issue is not applicable to common embedded system where $V_{I(VREG3V3)}$, $V_{I(VAUX3V3)}$, $V_{CC(I/O)}$, $V_{CC(I/O)\_AUX}$ and V_{DDA_AUX} are connected together to a single power source.

19.1.3 Status

This erratum is no longer valid. The suspend current value has been updated in Table 109.

19.2 Erratum 2

A hub disconnection occurs on the SAF1562 downstream port when the hub generates a remote wake-up from system $D3_{cold}$ suspend.

19.2.1 Problem description

After the USB device resume signaling is completed, incorrect resume signaling is observed on the SAF1562 port which triggers the remote wake-up. As a result, the hub will be disconnected. This requires new enumeration of the hub and all USB peripherals connected to its downstream ports.

The problem is intermittent failure and it depends on the hub solution used.

This does not affect another port of the HC which does not trigger the $D3_{cold}$ resume.

19.2.2 Implication

The implication is moderate.

19.2.3 Workaround

When the hub disconnection is detected after $D3_{cold}$ resume, the USB host should perform new enumeration of the hub and all connected USB peripherals. In an embedded system which does not implement power management modes, this erratum is not applicable because the supply voltages to the various pins are always present.

19.3 Erratum 3

When a Hi-Speed USB device is repeatedly plugged and unplugged from the downstream port, sometimes the device enumerates as full-speed.

19.3.1 Problem description

When a Hi-Speed USB device is repeatedly plugged and unplugged from the downstream port, sometimes the port owner bit (PO) in the PORTSC register (bit 13) is set to logic 1 after device disconnection. As a result, the device is enumerated as full-speed during the next Hi-Speed USB device connection.

19.3.2 Implication

The implication is moderate.

19.3.3 Workaround

Whenever a device disconnection is detected, write logic 0 to the port owner bit in the PORTSC register. Device connection and disconnection status is determined based on the value of both bits ECSC and ECCS.

Repeated unplugging and plugging of device for less than a second can affect both bits ECSC and ECCS. For example, the device has just been disconnected but bit ECSC is still logic 0 (a change is not detected) and bit ECCS is logic 1 (indicating that the device is still connected although it has been disconnected). If this condition occurs, perform a device disconnection and connection cycle to determine the correct device connection status.

19.4 Erratum 4

A Cyclic Redundancy Check (CRC) error is generated on the USB packet when either a single transaction occurs on the PCI bus or the CPU allocates a low PCI bandwidth for the SAF1562.

19.4.1 Problem description

To enhance data throughput performance for large data packets, the SAF1562 implements a watermark level. This is the level at which data transfer on the USB is triggered when the CPU fills up data on the PCI bus. The watermark level is 191 bytes, 255 bytes, 383 bytes, 511 bytes, 639 bytes, 767 bytes and so on.

The CRC error will not occur if the data packet transferred is 512 bytes because the watermark level is 511 bytes. The data packet will appear on the USB once the CPU finishes writing above 511 bytes on the PCI bus.

Several scenarios are described as follows.

It is assumed that the PCI data burst is in 16 double words. This means that the data will be transferred in 64 bytes. The CPU takes approximately 3.3 µs to write from 64 bytes to the next 64 bytes on the PCI bus.

- Scenario 1: The CPU will write a total of 380 bytes data to the PCI bus in the following manner. It writes 5 bursts (320 bytes) followed by 60 bytes. After the CPU finishes writing 5 bursts (320 bytes) the USB packet will appear on the USB. The SAF1562 will take approximately 5.81 µs to transfer these 320 bytes on the USB. At the same time, the CPU will write the remaining packet of 60 bytes to the PCI bus in less than 3.3 µs. As a result, the USB data can be transferred smoothly and the CRC error does not occur because the USB packet can be transferred as a complete data.
- Scenario 2: The CPU will write a total of 380 bytes data to the PCI bus in the following manner. It writes the data into 3 steps: 4 bursts (256 bytes), 4 bytes and 120 bytes.

  After the CPU finishes writing 4 bursts and 4 bytes (total of 260 bytes) the USB packet will appear on the USB. The SAF1562 will take approximately 4.7 µs to transfer these 260 bytes on the USB. At the same time, the CPU will write the remaining packet of 120 bytes to the PCI bus which takes approximately 6.6 µs.

  The SAF1562 will transfer the 260 bytes data on the USB faster than the CPU writes the 120 bytes data on the PCI bus. Therefore, the SAF1562 buffer is already empty when the CPU finishes writing 120 bytes. As a result, the SAF1562 cannot transfer the remaining 120 bytes since it has not crossed over the watermark level which is at 191 bytes. This condition will cause CRC error because the USB packet transferred is not complete (380 bytes).

The CRC error also can occur during USB data transfer when the PCI bandwidth is not high enough to transfer data with the defined packet size. If the PCI bus is dedicated to other transfers, this can cause repetitive CRC error generation for a number of subsequent transfers.

19.4.2 Implication

The implication is moderate.

19.4.3 Workaround

The EHCI data buffer has 4 kB alignment:

[Page 0] X bytes

[Page 1] 4096 bytes

[Page 2] 4096 bytes

[Page 3] 4096 bytes

[Page 4] 4096 bytes

If a short packet data is located on this boundary, a single transaction can occur on the PCI bus, causing the CRC error.

The software must be modified so that a short packet does not exist at a page boundary. This software modification must be made on the application and driver side to ensure that data requests sent are properly aligned.

In another scenario, allocating a higher priority on PCI for the SAF1562 data transfer will prevent this problem. The issue is not normally noticed in tests carried out on PC systems. The problem is only seen in heavily loaded embedded systems with a very low PCI bandwidth and memory bus allocation.

19.5 Erratum 5

Bulk data is written to a wrong address when a 2 bytes transfer and a 16-bit aligned memory access occurs almost at the same time.

19.5.1 Problem description

The problem may occur when two full-speed peripherals are simultaneously running for several hours, involving bulk, control and interrupt data transfers.

When the problem occurs, the data written to the wrong memory address will be lost.

The problem does not occur in the case of a double word aligned transfer. Also, this issue is not normally observed on a PC system.

This problem often arises when a bulk INput (IN) with 64 bytes of data is immediately followed by an interrupt IN which a Not AcKnowledge (NAK) has been performed.

The problem occurs if the second transaction (interrupt IN) is finished before the first transaction (bulk IN) can write back all data to the system memory.

19.5.2 Implication

The implication is moderate.

19.5.3 Workaround

It is recommended to always program the SAF1562 for 32-bit memory access.

If it is necessary to have a 16-bit aligned memory access, the HcPeriodicStart register can be programmed as 2EA7h. This will ensure that the periodic transfers are started at the beginning of the SOF.

19.6 Erratum 6

The PC unexpectedly starting up may be observed when the SAF1562 PCI evaluation (eval) board is plugged into a PCI slot, when the PC is initially powered off.

19.6.1 Problem description

The PME# voltage level will drop to an intermediate level when the SAF1562 PCI board is inserted into the PCI slot because of internal leakage from PME# to V_{CC}. This will affect the normal voltage level of the PME# signal because V_{CC} is initially absent and PME# is pulled up by a resistor on the system board.

19.6.2 Implication

The implication is moderate. The generated PME# pulse will produce the system wake-up. This issue does not affect the normal SAF1562 PME# functionality when the system enters $D3_{cold}$ suspend and V_{CC} is cut off, with the SAF1562 eval board present in a PCI slot.

19.6.3 Workaround

System wake-up by PCI PME# can be normally disabled in the BIOS.

19.7 Erratum 7

OHCI activity may suddenly stop in a certain configuration after continuously running for several hours. This configuration has at least two full-speed devices, for example, USB wireless device and USB printer, simultaneously running.

19.7.1 Problem description

This issue occurs when the OHCI interrupt disable or enable is done by setting the individual interrupt enable and disable bits in the OHCI HcInterruptEnable and HcInterruptDisable registers, instead of using the MasterInterruptEnable (MIE) bit.

19.7.2 Implication

The implication is moderate. The problem described will sometimes cause a failure in enabling of the SAF1562 interrupts, which will subsequently prevent normal functionality of the respective OHCI.

The other OHCI will continue with normal functionality.

19.7.3 Workaround

The MIE bit, in general, must be used to enable and disable the interrupts inside the Interrupt Service Routine (ISR); instead of using the individual interrupt source bits, as described in *Open Host Controller Interface Specification for USB Rev. 1.0a*, Section 5.3.

19.8 Erratum 8

Various problems may be encountered on the VIA KM400 chip set because of its specific design, causing repeated PCI retries. Some examples: full-speed device enumeration failure and high-speed data transfer stoppage.

19.8.1 Problem description

The SAF1562 implementation of the retry time-out will set the UE bit of the HcInterruptStatus register (OHCI) and the HSE bit in the USBSTS register (EHCI) when the number of SAF1562 PCI retries is greater than the value defined in the Retry time-out register (default = 80h).

19.8.2 Implication

The implication is moderate. Device drivers will disable normal OHCI or EHCI functionality when an interrupt is generated because of the setting of the UE or HSE bit. The MIE bit will be disabled.

19.8.3 Workaround

The retry time-out is an SAF1562-specific feature and not a standard PCI feature. The retry time-out must normally be disabled at the time of initializing the SAF1562, by writing 00h to the Retry time-out register.

The Retry time-out register will be reset to its default value when resuming from the $D3_{cold}$ suspend because of the PCI reset (RST#) assertion. Therefore, it must be re-initialized with 00h.

Keeping the retry time-out disabled will prevent these issues.

19.9 Erratum 9

Correct functionality of the SAF1562 is guaranteed only when PCI clock (pin PCICLK) frequency is 31 MHz to 33 MHz.

19.9.1 Problem description

The correct functionality of the SAF1562 is not guaranteed if the PCI clock (pin PCICLK) has a frequency lower than 31 MHz. The host system will be slower or may stop responding (hang-up).

19.9.2 Implication

The implication is low. It is recommended to use the SAF1562 on systems with a PCI clock frequency of 31 MHz to 33 MHz. Normal functionality is not guaranteed at other frequencies.

19.9.3 Workaround

Use PCI clock frequency at 31 MHz to 33 MHz.

19.10 Erratum 10

The write operation to the SAF1562 registers fails when the PCI burst timing is too fast.

19.10.1 Problem description

If the PCI burst timing during write operation is too fast, the SAF1562 registers may not capture this data. As a result, the write operation fails. The timing between two consecutive writes must not be less than 84 ns.

19.10.2 Implication

The implication is serious.

19.10.3 Workaround

Introduce a delay time between burst writes, for example by reading a dummy register, so that the timing between two consecutive writes is greater than or equal to 84 ns.

19.11 Erratum 11

Interrupt devices cannot work under the SAF1562 in a Microsoft Windows CE system with default OHCI drivers. This is applicable for Windows CE 4.2 as well as Windows CE 5.0.

19.11.1 Problem description

When an interrupt device, such as keyboard or mouse, is connected to the SAF1562 in a Windows CE system using the native Microsoft driver, this device does not function. This is because the SAF1562 does not send any interrupt transactions to the device after the device enumeration is successful. However, the device can function properly if it is connected to a high-speed hub. This would mean that the issue occurs only on the OHCI of the SAF1562.

To ensure that the interrupt transactions are scheduled by the SAF1562, both Periodic List Enable bit (PLE - bit 2 of OHCI HcControl register) and Isochronous Enable bit (IE - bit 3 of OHCI HcControl register) must be set to logic 1.

This issue occurs in the default OHCI driver of Microsoft Windows CE Ver. 4.2 and 5.0 because during interrupt transactions the bit IE is not set to logic 1.

19.11.2 Implication

The implication is serious.

19.11.3 Workaround

Set both bit PLE and bit IE to logic 1 in the OHCI HcControl register for interrupt transactions.

19.12 Erratum 12

In a full-speed IN data endpoint, after receiving a long series of NAK handshakes from a device, the SAF1562 may generate Packet IDentifier (PID) check failure (condition code 06h) or device not responding (condition code 05h).

19.12.1 Problem description

When a full-speed USB device is connected to the SAF1562 host, enumeration completes successfully. An IN data endpoint (bulk) is established to allow the device to transfer data to the host. The SAF1562 will schedule a continuous stream of IN token to be sent to the bulk endpoint of the device. When the device has no data to send, it will return an NAK handshake to the host. After receiving a continuous series of NAKs, ranging from 150 ms to 500 ms, the SAF1562 will return a condition code 06h (PID check failure) or 05h (device not responding) in the general Transfer Descriptor (TD). This error causes the software to stall the endpoint.

Table 126. Field definitions for a general TD

Symbol	Host controller access	Description
T	R/W	**DataToggle**: This two-bit field is used to generate or compare the data PID value (DATA0 or DATA1). It is updated after each successful transmission or reception of a data packet. The Most Significant Bit (MSB) of this field is logic 0 when the data toggle value is acquired from the toggleCarry field in the ED and logic 1 when the data toggle value is taken from the Least Significant Bit (LSB) of this field.
EC	R/W	**ErrorCount**: This value is incremented for each transmission error. If ErrorCount is 2 and another error occurs, the error type is recorded in the ConditionCode field and placed in the done queue. When a transaction completes without error, ErrorCount is reset to 0.
CC	R/W	**ConditionCode**: This field contains the status of the last attempted transaction.
CBP	R/W	**CurrentBufferPointer**: Contains the physical address of the next memory location that will be accessed for transfer to or from the endpoint. A value of zero indicates a zero-length data packet or that all bytes have been transferred.
NextTD	R/W	**NextTD**: This entry points to the next TD on the list of TDs linked to this endpoint.
BE	R	**BufferEnd**: Contains the physical address of the last byte in the buffer for this TD.

19.12.2 Implication

The implication depends on the application and the device because the problem appears only in certain applications with a series of NAKs from the device with a certain signal quality (e.g. a mass storage device connected to a full-speed hub with 4 m to 5 m cable in both downstream and upstream port).

19.12.3 Workaround

Whenever a PID check failure or device not responding occurs, ensure that the HCD retries the error transaction by resending the corresponding TD. If the retries keep failing for 5 times, the HCD should inform the client driver to take the appropriate action, for example: perform a USB class driver reset or power cycle the V_{BUS}.

19.13 Erratum 13

The SAF1562 EHCI cannot work properly if the CPU allocates a lower priority of PCI bandwidth to the SAF1562.

19.13.1 Problem description

The SAF1562 EHCI stops accessing the PCI bus if its request for the PCI bus access is not granted within approximately 125 µs. SOFs, however, are still seen on the USB. This only affects the request of the SAF1562 EHCI to write data from IN packets to the system memory.

The root cause issue is described as follows. The SAF1562 has internal mechanism which will clear any buffer that is locked for 2 successive SOFs. If the SAF1562 cannot finish writing the buffer to the system memory during this time, the buffer will be cleared. This condition will lock the SAF1562 state machine out of the idle state. As a result, the EHCI stops accessing the PCI bus.

19.13.2 Implication

This is hardware and system dependent and usually seen on systems which allocate less PCI bandwidth to the SAF1562.

19.13.3 Workaround

Allocate a higher priority of PCI bandwidth to the SAF1562.

19.14 Erratum 14

Setting the multiplier field in the QH for the asynchronous list to a value other than 1 (for example 2 or 3) will cause the HC to stop responding.

19.14.1 Problem description

According to the *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*, the multiplier bits (bits 30 and 31 of Queue Head DWord 2) apply only to the periodic list. The EHCI core can stop functioning when this field in asynchronous QH is set to a value other than 1.

19.14.2 Implication

The implication is serious.

19.14.3 Workaround

The EHCI HCD must keep this field at 1. This is applicable only to the asynchronous list.

19.15 Erratum 15

In the OHCI, sometimes the HcDoneHead register is not properly updated.

19.15.1 Problem description

In the OHCI, the interrupt and the WDH bit are set but the HC does not immediately update the HccaDoneHead register (in the system memory) through the PCI. Therefore, while reading the HccaDoneHead register, you will get the old data, which is incorrect.

19.15.2 Implication

The implication is serious.

19.15.3 Workaround

When a WDH interrupt occurs, do not check the HccaDoneHead value. Instead check the condition code for all scheduled TDs to determine whether TD has been completed.

19.16 Erratum 16

The OHCI returns the same TD to the HCD in 2 consecutive USB frames. As a result, memory pointer faulty could occur.

19.16.1 Problem description

The TD and ED are updated consecutively upon completing each USB transfer. Meanwhile, the HccaFrameNumber and HccaDoneHead are updated in the next SOF if the ongoing transfers are completed.

If a write back of HccaDoneHead occurs during the time between the HC updates TD and the HC updates ED, the corresponding HccaDoneHead will be listed in the done list of the next USB frame. As a result, the same TD which is already transferred to the HCD in the current USB frame will be transferred again in the next USB frame. If the same TD is processed by the HCD for the second time, memory pointer faulty could occur because the NextTD pointer is no longer valid after the TD is processed in the current transfer.

19.16.2 Implication

The implication is serious.

19.16.3 Workaround

Ensure that TDs on the done list are valid before processing them. The TDs validity checking can be implemented in the HCD done list process. It will check whether the TD has already been used to schedule a new transfer or not. The pseudo code is shown as follows.

```
1    if (!TD.InUse)
2         TDCompleteStatus = !valid;
3    else if (TD == PrevHccaDoneHead)
4    {
5    /*To limit increase in CPU utilization TDInEDTransferList function is only called
     if TD is equal PrevHccaDoneHead.
6    */
7         if (TDInEDTransferList(TD))
8              TDCompleteStatus = !valid;
9    }
10   else
11        TDCompleteStatus = valid;
```

TD.InUse: This is a software flag that notifies whether TD has been used for scheduling the transfer or not.

TDCompleteStatus: Notifies whether TD is a valid completed TD or incorrectly placed on the done list.

PrevHccaDoneHead: HccaDoneHead of the previous USB frame.

TDInEDTransferList: This is a function to check whether TD is still in EDs transfer list. An example of the function is listed as follows.

```
12   /* This function will check if the TD passed in is still in the transfer list of
     the ED. It will return TRUE when TD is still in the transfer list and FALSE
     otherwise.
```

```
13   */
14   boolean TDInEDTransferList (TDStruct TD)
15   {
16        TDStruct CurrTransferListTD = ED.HeadP;
17        while (CurrTransferListTD != ED.TailP)
18        {
19             if (TD == CurrTransferListTD) {
20                  return TRUE;
21   }
22             CurrTransferListTD = CurrTransferListTD.NextTD
23        }
24
25        /*Needed to check TailP as it will not be check by while loop. */
26        if (TD == CurrTransferListTD)
27             {
28                  return TRUE;
29             }
30        return FALSE;
31   }
```

Remark: Windows XP has implemented the improvement in the OHCI driver to handle this limitation.

19.17 Erratum 17

A data toggle error occurs when an IN transfer sent by a full-speed device is completed with either a short packet or a zero-length packet. As a result, the OHCI driver could not get the complete data. For example, full-speed Wireless Local Area Network (WLAN) or LAN devices could not function properly in Windows CE Ver. 5.0 system with default driver.

19.17.1 Problem description

This problem occurs on full-speed devices with short packet or a zero-length packet for data transfer termination. It is common for WLAN or LAN devices to terminate the data transfer with either a short packet or a zero-length packet.

The issue is further described as follows: When a full-speed LAN device terminates the data transfer with a zero-length byte, the SAF1562 will set the halted bit to logic 1 in the ED, sets bit CC in TD to DATAUNDERRUN and does not toggle the bit toggleCarry in the ED. Therefore, when there is a new data transfer scheduled in the same IN endpoint, the OHCI driver will drop the first packet because it assumes that data toggle error occurs since the bit toggleCarry is not toggled. As a result, the OHCI driver will pass an incomplete data to the LAN device driver. If this condition occurs continuously, the full-speed LAN device may not function properly.

19.17.2 Implication

The implication is moderate because the problem occurs only on the full-speed device with a short packet or a zero-length packet for data transfer termination.

19.17.3 Workaround

Whenever receiving IN transfer completed with a halted bit in the ED and the bit CC is set to DATAUNDERRUN, the HCD must toggle the bit toggleCarry and clear the halted bit in the ED.

19.18 Erratum 18

There is a register access issue when IRDY# (pin 37) is asserted later than the third clock cycle.

19.18.1 Problem description

The SAF1562 has a limitation when being written to as a PCI target. If IRDY# is asserted later than the third clock cycle of the data phase of a write to the SAF1562 operational registers, the accessed register will be corrupted.

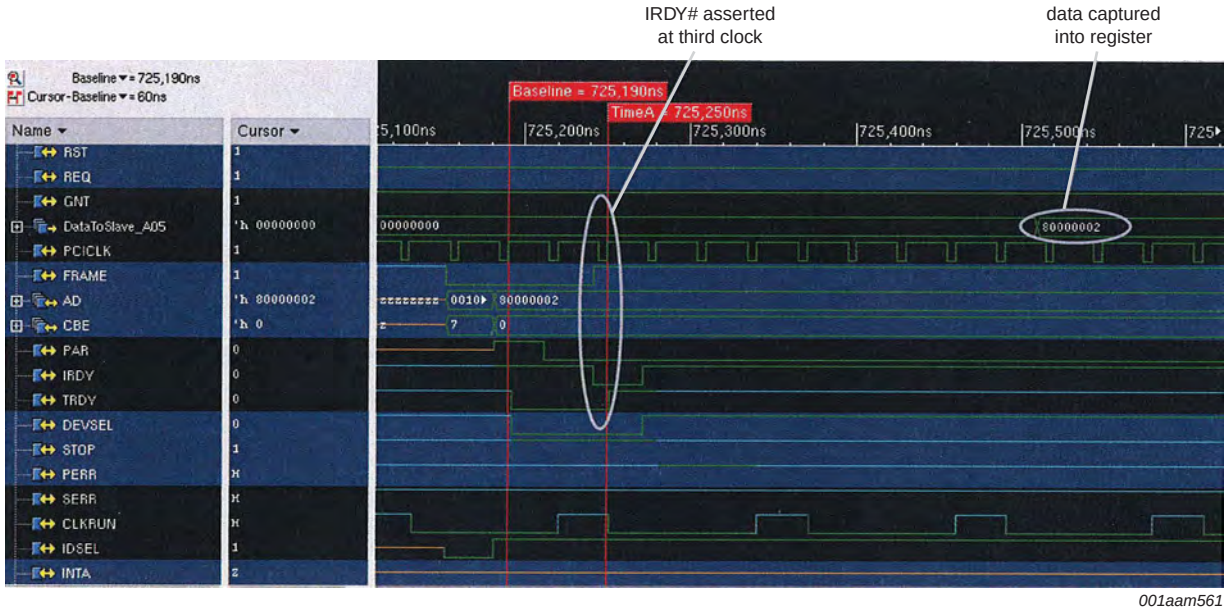


Fig 14. IRDY# asserted at the third clock

In Figure 14, the third clock asserts IRDY# and data is correctly captured in the register to which it is written.

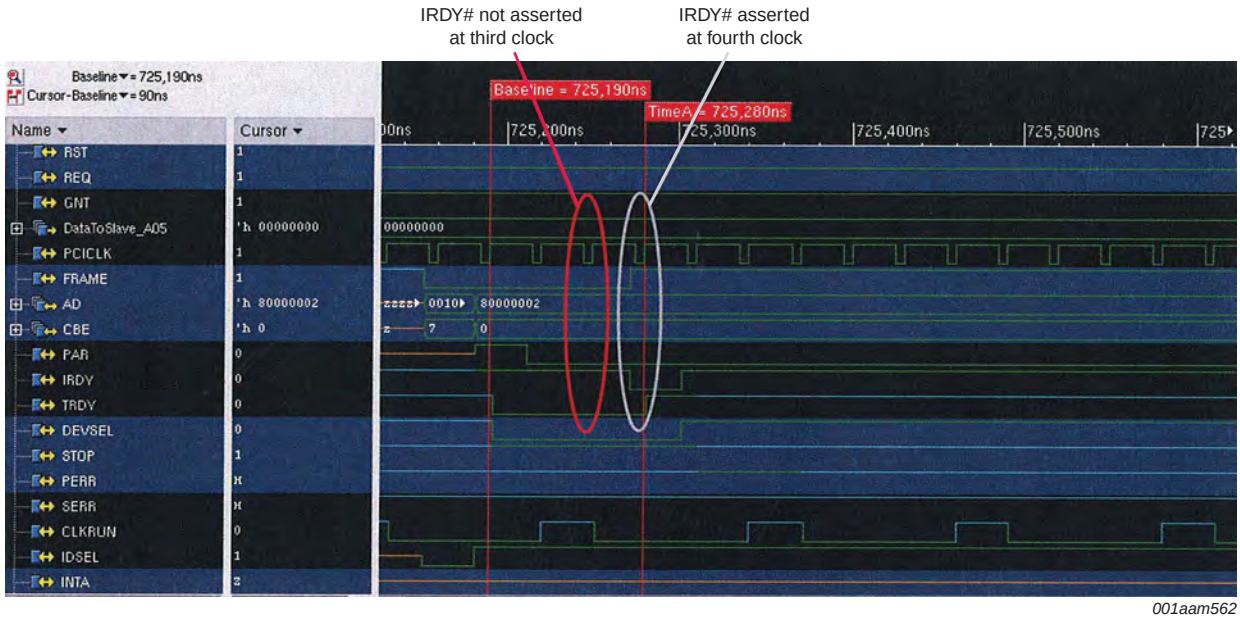


Fig 15. IRDY# asserted at the fourth clock

In Figure 15, the fourth clock asserts IRDY# and data is incorrectly captured in the register to which it is written.

19.18.2 Implication

This limitation is very rarely seen because most of the processor platforms do not exhibit such behavior.

19.18.3 Workaround

In the system implementation, ensure that IRDY# is asserted within three clock cycles.

19.19 Erratum 19

Repeated PCI reset assertion, PCI reset assertion during cold start-up and unexpected power supply behavior during cold start-up could cause high-speed intermittent issue.

19.19.1 Problem description

There are 3 observed conditions that could cause high-speed intermittent issue: repeated PCI reset assertion, PCI reset assertion during cold start-up and unexpected power supply behavior during cold start-up.

19.19.1.1 Repeated PCI reset assertion

While repeatedly rebooting the system, sometimes high-speed devices could not be enumerated due to data corruption. Full-speed and low-speed devices still work.

The SAF1562 has several internal test modes for factory testing that can be entered during PCI reset with certain combination of key signals. These key signals are pins OC1_N, PWE1_N and PWE2_N.

If noise or spike occurs on the key signals during PCI reset assertion, it could accidentally turn on the enable signal of test modes. As a result, the EHCI does not get a proper reset. This improper reset will cause the high-speed intermittent issue (for example, high-speed device cannot get enumerated due to data corruption).

19.19.1.2 PCI reset assertion during cold start-up

When PCI reset is LOW during cold start-up, it could cause misaligned high-speed clock between port 1 and port 2. As a result, data corruption (CRC16 error) could occur during bulk OUTput (OUT) transfer if both ports are communicating to Hi-Speed USB devices. The issue does not occur if only one high-speed device is connected. Full-speed device and low-speed device are not affected.

19.19.1.3 Unexpected power supply behavior during cold start-up

There are 3 possible scenario as follows:

1. During start-up, the SAF1562 power supply ramps up from an offset (e.g. 0.65 V) to 3.3 V within 6 ms. This 0.65 V offset voltage can cause the SAF1562 bandgap to fail to start. As a result, both ports cannot detect high-speed device.
2. The SAF1562 power supply ramps up from 0 V to 3.3 V with a rise time less than 5 ms (e.g. 1 ms). This condition could cause port 2 of the SAF1562 to fail to detect high-speed device.
3. The SAF1562 power supply ramps up from 0 V to 3.3 V with a rise time greater than 11 ms (e.g. 30 ms). This ramp-up time can cause the SAF1562 bandgap to fail to start. As a result, both ports cannot detect high-speed device.

19.19.2 Implication

The implication is serious if the required application can only run in high-speed mode.

19.19.3 Workaround

Figure 16 shows the timing diagram which resolves the problems described in Section 19.19.1.

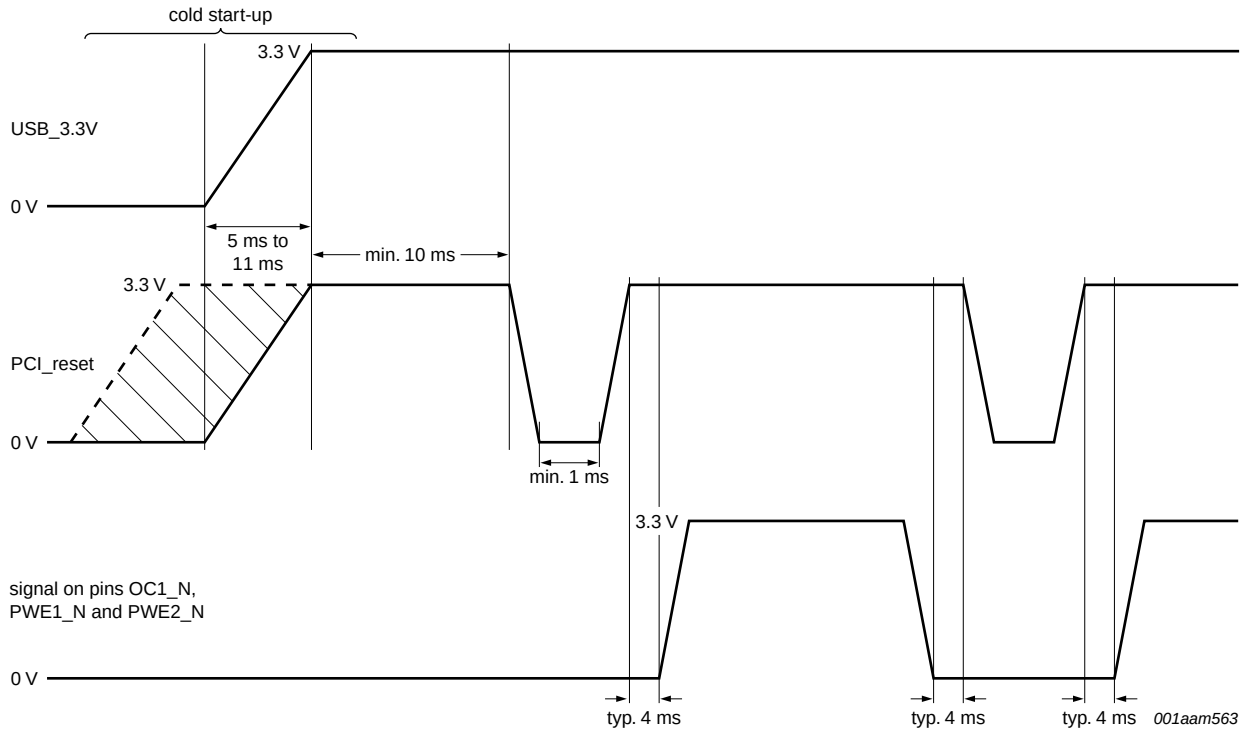


Fig 16. SAF1562 signals during cold start-up and PCI reset assertion

19.19.3.1 Workaround for repeated PCI reset assertion

Ensure that the signal on pins OC1_N, PWE1_N and PWE2_N is not HIGH or toggling during the PCI reset assertion as shown in Figure 16.

Remarks:

- If only one port is needed then it is recommended to use port 2. As port 1 is not used, the pins OC1_N and PWE1_N can be connected directly to ground. Please note that the software should ignore the overcurrent status on the port 1 since OC1_N is connected permanently to ground.
- If port 1 and port 2 are needed then Figure 17 is one application example. To achieve the timing requirement as shown in Figure 16 use General Purpose Input Output (GPIO) ports from the microcontroller to control the key signals assertion.
  The OC1_N, PWE1_N and PWE2_N signals must be asserted before the PCI reset assertion and must be deasserted after the PCI reset deassertion. The recommended safety margin for the timing assertion and deassertion between the key signals and PCI reset is approximately 4 ms.

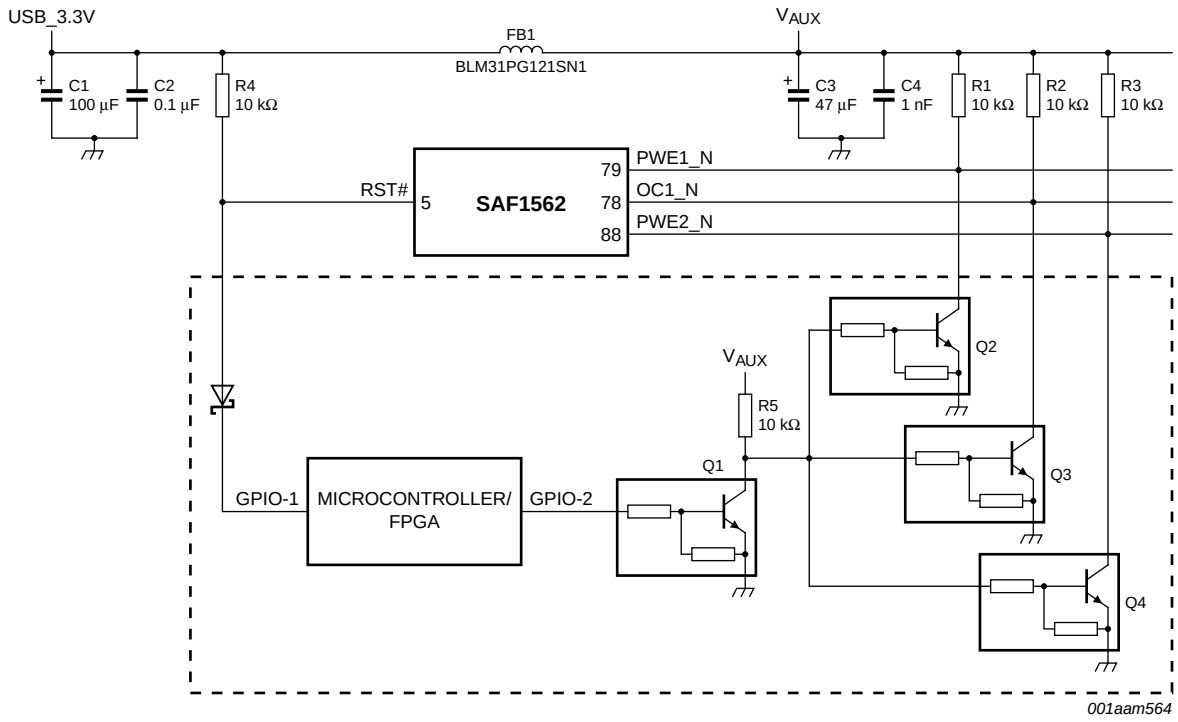


Fig 17. Workaround when all ports are needed in an implementation

19.19.3.2 Workaround for PCI reset assertion during cold start-up

Ensure that the PCI reset is HIGH during cold start-up (refer to Figure 16 for the timing diagram).

19.19.3.3 Workaround for the unexpected power supply behavior during cold start-up

Ensure that the power supply during cold start-up ramps up linearly from 0 V to 3.3 V within 5 ms to 11 ms (refer to Figure 16 for the timing diagram).

19.20 Erratum 20

In a CardBus application on a Windows OS notebook, the system may momentarily freeze and EHCIs root hub does not function when EHCI is disabled and enabled again. The system crashes if the SAF1562 based CardBus is removed and then inserted again.

19.20.1 Problem description

When the EHCI is enabled again, Windows performs the following sequence:

1. Disable the OHCI
2. Enable the EHCI
3. Enable the OHCI

When the OHCI is disabled, the Memory Space (MS) bit, bit 1 in the PCI Configuration Command register is cleared; see Table 7. If the MS bit is cleared, the HCD must not accept any memory space accesses.

The problem occurs whenever the new EHCI base address is a subregion of the previous OHCI base address. When this happens, the EHCI will return an incorrect value while it is being read during the EHCI enable process.

The EHCI driver typically uses the value of Capability Length (CAPLENGTH) register to determine the offset where EHCI registers begin. If the EHCI returns the incorrect value of CAPLENGTH, the EHCI driver will not get the correct offset value. As a result, all accesses to the EHCI registers will go to the wrong address.

19.20.2 Implication

The implication is moderate because it occurs only in the scenario as described in Section 19.20.1.

19.20.3 Workaround

Do not allocate the host controllers in any overlapping memory region irrespective of the MS bit value.

19.21 Erratum 21

When using the SAF1562 USB host controller for CardBus applications with Apple MAC PowerBook G4, the USB device enumerates correctly, but occasionally, subsequent data transfers fail.

19.21.1 Problem description

According to the *Open Host Controller Interface Specification for USB Rev. 1.0a*, the control or bulk list is considered empty when all EDs on the list have no transfer, that is, skip = 1, halt = 1 or TD queue tail pointer (TailP) = TD queue head pointer (HeadP).

The detection scheme in the SAF1562, however, must satisfy the following requirements for an ED to be considered as not having pending transfer(s).

- If skip = 1, the TailP of the used ED must be the same as the HeadP of the unused ED
- If halt = 1, the TailP of the used ED must be the same as the HeadP of the unused ED

For example, there are 3 EDs on the control list with 1 of them being used for enumeration of the device under test and the other 2 EDs have their skip = 1.

In case of no failure, MAC will set the TailP of the used ED to the same value as the HeadP of the unused EDs.

In case of failure, MAC will set the TailP to a different value from the HeadP. As a result, the SAF1562 assumes that there are transfers to be processed on the control list because the TailP of the used ED has a different value from the HeadP of the 2 unused EDs. This will cause the OHCI driver to indefinitely traverse the control list, resulting in ControlBulkServiceRatio (see Table 45 HcControl CBSR[1:0]) is not met. Therefore, the bulk transfer will never be serviced because the OHCI will never traverse the bulk list.

19.21.2 Implication

The implication is moderate because it occurs only in certain specific HCD implementations.

19.21.3 Workaround

Ensure that whenever an ED is allocated, its entire data structure is initialized to zero. This will set the TailP of the used ED to the HeadP of the unused ED.

19.22 Erratum 22

Cumulative USB errors cause the TD to retire prematurely.

19.22.1 Problem description

The SAF1562 implements the ErrorCount of OHCI TD as a cumulative error counter rather than as a consecutive error counter. This implies that a scheduled TD will be retired if three transmission errors occur, even when these errors are not consecutive.

In the noisy environment, the larger amount of data scheduled in TD, the higher the occurrence of TD is retired prematurely. If this happens, the application must reschedule the TD.

19.22.2 Implication

The implication is moderate because it depends on the amount of data transferred and how noisy the physical environment is.

19.22.3 Workaround

Split the large data transfer of TD into multiple TDs. For example, instead of transferring 64 kB data in 1 TD, split it into 8 TDs of 8 kB data.

19.23 Erratum 23

Repeated PCI retry occurs when EHCI and OHCI operational registers are read with Memory Read Line or Memory Read Multiple PCI commands.

19.23.1 Problem description

The SAF1562 does not support Memory Read Line and Memory Read Multiple PCI commands. Therefore, the host controller driver cannot read the content of operational registers when using either of these commands.

19.23.2 Implication

The implication is moderate.

19.23.3 Workaround

Use only Memory Read PCI command when reading the operational registers of the SAF1562.

19.24 Erratum 24

With the updated gold tree setup from USB-IF interoperability testing, the SAF1562 does not work properly with some of the devices.

19.24.1 Problem description

In Figure 18, the mouse and video camera which are connected to the Hub HS5 do not work properly.

Normally in Windows environment, interoperability testing is done with a gold tree setup. It is observed that the SAF1562 cannot properly perform an isochronous transfer through a web camera (e.g. Logitech QuickCam Ultravision) and simultaneously an interrupt transfer through a mouse (e.g. Microsoft basic optical mouse or Dell mouse) connected to the high-speed hub. Sometimes the mouse cannot move freely and the left click does not work properly.

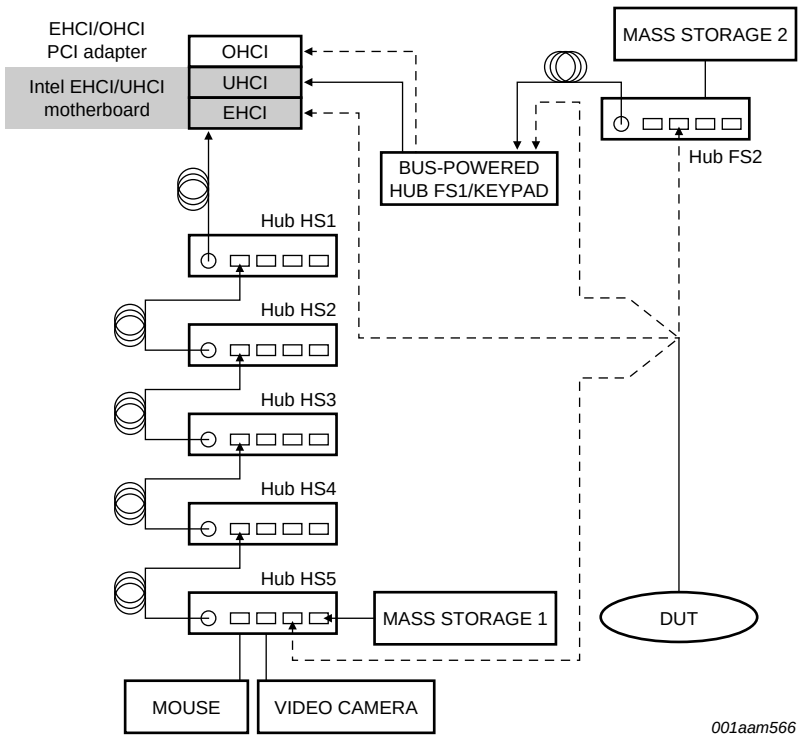


Fig 18. Gold tree setup

19.24.2 Implication

The implication is moderate for non-embedded application.

19.24.3 Workaround

For embedded system applications, the supported devices and the test setup are defined by the product manufacturer. The supported devices are defined in the Targeted Peripheral List (TPL) while the test setup is defined in the user guide. Therefore, the issue is not critical.

19.25 Erratum 25

The SAF1562 OHCI or EHCI bus master cannot be disabled if either OHCI bit BM or EHCI bit BM is still set to logic 1.

19.25.1 Problem description

In the SAF1562, if the OHCI bit BM is set to logic 0 and the EHCI bit BM is set to logic 1, the OHCI bus master still occurs. The same condition also applies to the SAF1562 EHCI. When the EHCI bit BM is set to logic 0 and the OHCI bit BM is set to logic 1, the EHCI bus mastering still occurs. To disable bus mastering in the SAF1562, OHCI bit BM and EHCI bit BM must be set to logic 0.

19.25.2 Implication

The implication is low. It is very rarely to disable the bus mastering. Generally, the bus mastering is disabled when the PCI bus has some errors.

19.25.3 Workaround

To disable PCI bus master, set the EHCI bit BM and OHCI bit BM to logic 0.

19.26 Erratum 26

The SAF1562 Parity Error Response bit (see Table 7 address 04h bit PER) and the SERR# Enable bit (see Table 7 address 04h bit SERRE) cannot be disabled.

19.26.1 Problem description

In the SAF1562, if bit PER of the OHCI is enabled and bit PER of the EHCI is disabled, pin PERR# can still get asserted when data parity error occurs in EHCI transaction. The same behavior also applies to bit SERRE which triggers pin SERR#.

19.26.2 Implication

The implication is low because these bits are only used for error reporting and are only useful for debugging. It does not affect the normal operation of the device.

19.26.3 Workaround

The PERR# and SERR# assertion cannot be disabled. Ignore the pins assertion when they are not needed.

19.27 Erratum 27

The PCI configuration space data might be wrong during bus mastering.

19.27.1 Problem description

If configuration read occurs during the time when the SAF1562 Direct Memory Access (DMA) is requesting data, the data returned to the configuration read might be wrong. This condition can never happen in a normal scenario.

19.27.2 Implication

The implication is low because the SAF1562 host controller is not supposed to behave as target and master of the PCI transaction at the same time.

19.27.3 Workaround

Configuration read must be avoided during bus mastering.

19.28 Erratum 28

When using certain EEPROM ICs for programming, data downloading could fail if the data line (SDA) is stuck at LOW after PCI reset.

19.28.1 Problem description

If system reset occurs during the scanning process of the I^2C-bus device, the SDA might get stuck at LOW. When this happens, the SAF1562 cannot download data from the EEPROM because it cannot detect the slave address or the START condition of the I^2C-bus. As a result, the SAF1562 will assume that there is no EEPROM attached.

This issue occurs only at certain EEPROMs that need nine clocks to detect the START condition of the I^2C-bus.

19.28.2 Implication

The implication is low because this problem is applicable only to certain EEPROMs that need nine clocks to detect the START condition of the I^2C-bus.

19.28.3 Workaround

Avoid using EEPROMs that require nine clocks to detect the START condition of the I^2C-bus.

19.29 Erratum 29

Although data parity error occurs, the data can still be written into the PCI configuration space or SAF1562 host registers.

19.29.1 Problem description

During PCI configuration write or register write, the data can still be written into the PCI configuration space or SAF1562 host registers although data parity error occurs. This data should be discarded because the host controller might process the corrupted data.

19.29.2 Implication

The implication is low. Parity error will not occur during normal operation. This can happen only during debugging.

19.29.3 Workaround

During debugging, if pin PERR# is asserted, ignore the data written to the PCI configuration space or SAF1562 host registers.

20. Abbreviations

Table 127. Abbreviations

Acronym	Description
BIOS	Built-In Operating System
CC	Condition Code
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit

Table 127. Abbreviations *...continued*

Acronym	Description
CRC	Cyclic Redundancy Check
DID	Device ID
DMA	Direct Memory Access
ED	Endpoint Descriptor
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMI	Electro-Magnetic Interference
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
GPIO	General Purpose Input Output
HC	Host Controller
HCCA	Host Controller Communication Area
HCD	Host Controller Driver
IN	INput
ISR	Interrupt Service Routine
LAN	Local Area Network
LSB	Least Significant Bit
MSB	Most Significant Bit
NAK	Not AcKnowledged
OHCI	Open Host Controller Interface
OS	Operating System
OUT	OUTput
PCI	Peripheral Component Interconnect
PCI-SIG	PCI-Special Interest Group
PID	Packet IDentifier
PLL	Phase-Locked Loop
PMC	Power Management Capabilities
PME	Power Management Event
PMCSR	Power Management Control/Status Register
POR	Power-On Reset
QH	Queue Head
SDA	Serial DAta
SOF	Start-Of-Frame
STB	Set-Top Box
TD	Transfer Descriptor
TPL	Targeted Peripheral List
USB	Universal Serial Bus
VID	Vendor ID
WLAN	Wireless Local Area Network

21. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0

[3] Open Host Controller Interface Specification for USB Rev. 1.0a

[4] PCI Local Bus Specification Rev. 2.2

[5] PCI Bus Power Management Interface Specification Rev. 1.1

[6] The I^2C-bus Specification, Version 2.1

22. Revision history

Table 128. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAF1562 v.3	20120619	Product data sheet	-	SAF1562 v.2
Modifications:	• Limit application to automotive use			
SAF1562 v.2	20101124	Product data sheet	-	SAF1562 v.1
SAF1562 v.1	20070207	Product data sheet	-	-

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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25. Tables

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