



PRELIMINARY

CY37192

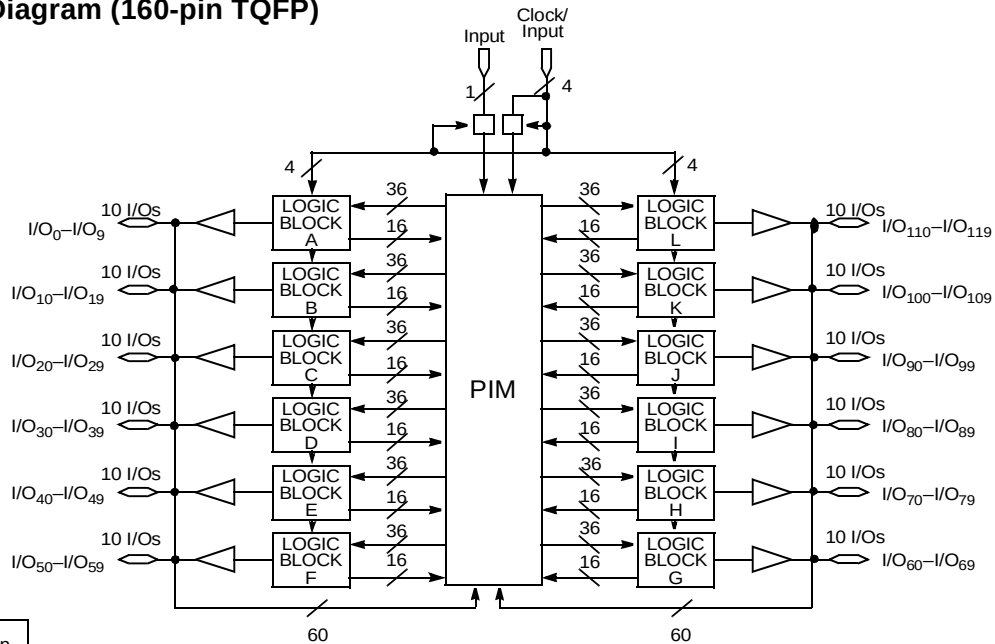
UltraLogic™ 192-Macrocell ISR™ CPLD

Features

- 192 macrocells in twelve logic blocks
- In-System Reprogrammable™ (ISR™)
 - JTAG-compliant on-board programming
 - Design changes don't cause pinout changes
 - Design changes don't cause timing changes
- 120 I/Os
 - plus 5 dedicated inputs including 4 clock inputs
- High speed
 - $f_{MAX} = 154$ MHz
 - $t_{PD} = 7.5$ ns
 - $t_S = 5$ ns

- $t_{CO} = 4.5$ ns
- Product-term clocking
- IEEE 1149.1 JTAG boundary scan
- Programmable slew rate control on individual I/Os
- Low power option on individual logic block basis
- 5V and 3.3V I/O capability
- User-Programmable Bus Hold capabilities on all I/Os
- Simple Timing Model
- PCI compliant
- Available in 160-pin TQFP
- Pinout compatible with CY37192V, CY37128/37128V, CY37256/37256V, CY7C375i

Logic Block Diagram (160-pin TQFP)



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Selection Guide

	CY37192-154	CY37192-125	CY37192-83
Maximum Propagation Delay, t_{PD} (ns)	7.5	10	15
Minimum Set-Up, t_S (ns)	5	5.5	8
Maximum Clock to Output, t_{CO} (ns)	4.5	6.5	8
Typical Supply Current, I_{CC} (mA) in Low Power Mode	90	90	90

Functional Description

The CY37192 is an In-System Reprogrammable (ISR) Complex Programmable Logic Device (CPLD) and is part of the Ultra37000™ family of high-density, high-speed CPLDs. Like all members of the Ultra37000 family, the CY37192 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs. The CY37192P160 features 72 Buried and 120 I/O Macrocells.

For a more detailed description of the architecture and features of the CY37192 see the Ultra37000 family data sheet.

Fully Routable with 100% Logic Utilization

The CY37192 is designed with a robust routing architecture which allows utilization of the entire device with a fixed pinout. This makes Ultra37000 optimal for implementing on-board design changes using ISR without changing pinouts.

Simple Timing Model

The CY37192 features a very simple timing model with predictable delays. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. The timing model allows for design changes with ISR without causing changes to system performance.

Low-Power Operation

Each Logic Block of the CY37192 can be configured as either High-Speed (default) or Low-Power. In the Low-Power mode, the logic block consumes approximately 50% less power and slows down by t_{LP} .

Output Slew Rate Control

Each output can be configured with either a fast edge rate (default) for high performance, or a slow edge rate for added noise reduction. In the fast edge rate mode, outputs switch at 3V/ns max. and in the slow edge rate mode, outputs switch at

1V/ns max. There is a nominal delay for I/Os using the slow edge rate mode.

3.3V or 5V I/O Operation

The CY37192 operates with a 5V supply, and can support 5V or 3.3V I/O levels. V_{CCO} connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the V_{CCO} pins to 5V the user insures 5V TTL levels on the outputs. If V_{CCO} is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. A nominal timing delay is incurred on output buffers when V_{CCO} is set to 3.3V. This device requires 5V ISR programming.

In System Reprogramming

The CY37192 can be programmed in system using IEEE 1149.1 compliant JTAG programming protocol. The CY37192 can also be programmed on a number of traditional parallel programmers including Cypress's *Impulse3™* programmer and industry standard third-party programmers. For an overview of ISR programming, refer to the Ultra37000 Family data sheet and for UltraISR cable and software specifications, refer to InSRkit: ISR Programming data sheet (CY3600i).

User-Programmable Bus Hold

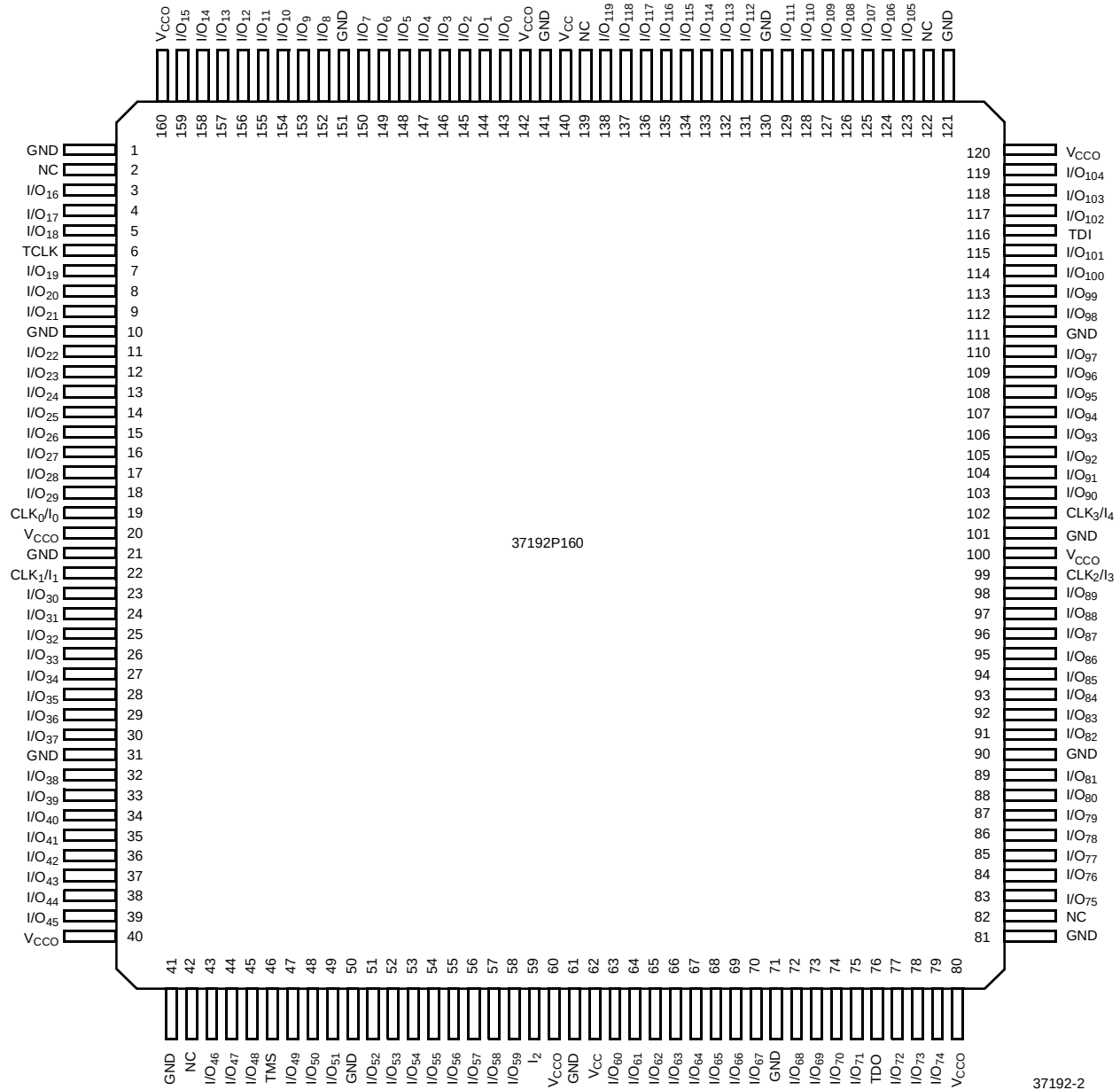
All outputs of the CY37192 can either be configured into bus hold mode or left floating. When in bus hold mode, the undriven outputs retain their last value with a weak latch. This feature allows the designer the flexibility of either eliminating or including external pull-up/pull-down resistors. Enabling this feature affects all I/Os simultaneously.

Design Tools

Development software for the CY37192 is available from Cypress's *Warp™* or third-party bolt-in software packages as well as a number of third-party development packages. Please refer to the *Warp* or third-party tool support data sheets for further information.

Pin Configurations

**160-pin TQFP
Top View**



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State -0.5V to +7.0V

DC Input Voltage -0.5V to +7.0V

DC Program Voltage 4.5 to 5.5V

Current into Outputs 16 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range^[1]

Range	Ambient Temperature ^[1]	Junction Temperature	Output Condition	V _{CC}	V _{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	-40°C to +85°C	-40°C to +125°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -3.2 mA ^[2]	2.4			V
V _{OHZ}	Output HIGH Voltage with Output Disabled ^[6]	V _{CC} = Max.	I _{OH} = 0 μA (Com'I/Ind) ^[3]			4.0	V
			I _{OH} = -50 μA (Com'I/Ind) ^[3]			3.6	V
V _{OL}	Output LOW Voltage	V _{CC} = Min.	I _{OL} = 16 mA ^[2]			0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs ^[4]		2.0		V _{CCmax}	V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs ^[4]		-0.5		0.8	V
I _{IX}	Input Load Current	V _I = GND or V _{CC}		-10		10	μA
I _{OZ}	Output Leakage Current	V _O = GND or V _{CC} , Output Disabled		-50		50	μA
		V _{CC} = Max., V _O = 3.3V, Output Disabled ^[3]		0	-70	-125	μA
I _{OS}	Output Short Circuit Current ^[5, 6]	V _{CC} = Max., V _{OUT} = 0.5V		-30		-160	mA
I _{BHL}	Input Bus Hold LOW Sustaining Current	V _{CC} = Min., V _{IL} = 0.8V		+75			μA
I _{BHH}	Input Bus Hold HIGH Sustaining Current	V _{CC} = Min., V _{IH} = 2.0V		-75			μA
I _{BHLO}	Input Bus Hold LOW Overdrive Current	V _{CC} = Max.				+500	μA
I _{BHHO}	Input Bus Hold HIGH Overdrive Current	V _{CC} = Max.				-500	μA

Inductance^[6]

Parameter	Description	Test Conditions	160-lead TQFP	Unit
L	Maximum Pin Inductance	V _{IN} = 5.0V at f = 1 MHz	9	nH

Notes:

1. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 family devices see the Ultra37000 family data sheet.
2. I_{OH} = -2 mA, I_{OL} = 2 mA for TDO.
3. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information.
4. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
5. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Tested initially and after any design or process changes that may affect these parameters.

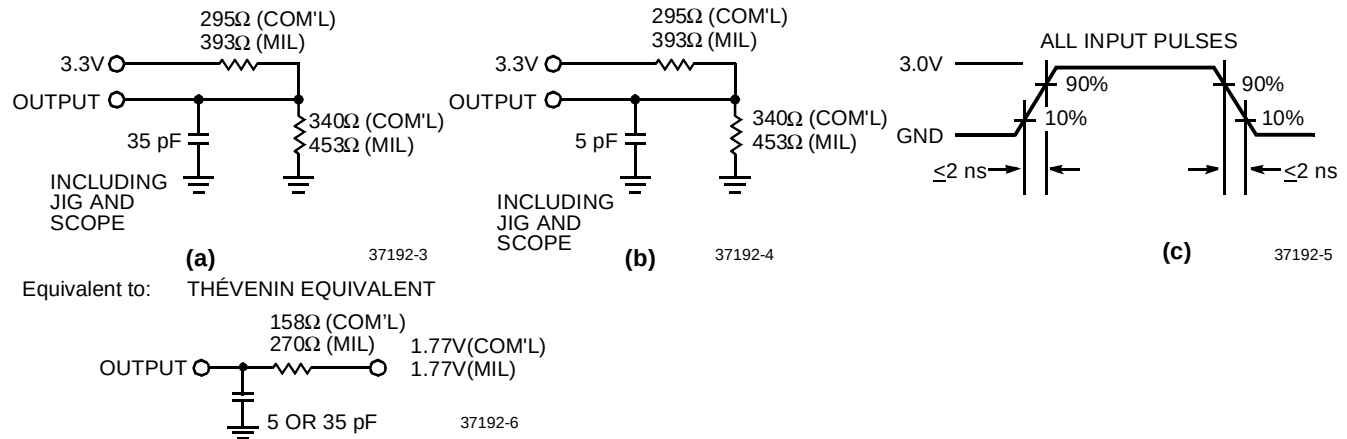
Capacitance^[6]

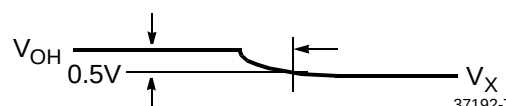
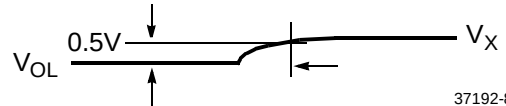
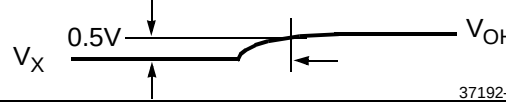
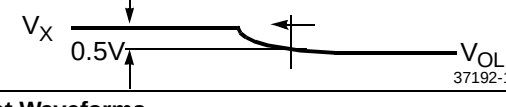
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	8	pF
C_{CLK}	Clock Signal Capacitance	$V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	12	pF

Endurance Characteristics^[6]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions ^[1]	1,000	10,000	Cycles

AC Test Loads and Waveforms



Parameter ^[7]	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	 37192-7
$t_{ER(+)}$	2.6V	 37192-8
$t_{EA(+)}$	1.5V	 37192-9
$t_{EA(-)}$	V_{the}	 37192-10

(d) Test Waveforms

Note:

7. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range^[8]

Parameter	Description	37192-154		37192-125		37192-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t _{PD} ^[9, 10, 11]	Input to Combinatorial Output		7.5		10		15	ns
t _{PDL} ^[9, 10, 11]	Input to Output Through Transparent Input or Output Latch		12		13		18	ns
t _{PDLL} ^[9, 10, 11]	Input to Output Through Transparent Input and Output Latches		13		15		19	ns
t _{EA} ^[9, 10, 11]	Input to Output Enable		11		14		19	ns
t _{ER} ^[9]	Input to Output Disable		11		14		19	ns
Input Register Parameters								
t _{WL}	Clock or Latch Enable Input LOW Time ^[6]	2.5		3		4		ns
t _{WH}	Clock or Latch Enable Input HIGH Time ^[6]	2.5		3		4		ns
t _{IS}	Input Register or Latch Set-Up Time	2		2		3		ns
t _{IH}	Input Register or Latch Hold Time	2		2		3		ns
t _{ICO} ^[9, 10, 11]	Input Register Clock or Latch Enable to Combinatorial Output		11		12.5		19	ns
t _{ICOL} ^[9, 10, 11]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		12		16		21	ns
Synchronous Clocking Parameters								
t _{CO} ^[10, 11]	Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Output		4.5		6.5		8	ns
t _S ^[9]	Set-Up Time from Input to Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	5		5.5		8		ns
t _H	Register or Latch Data Hold Time	0		0		0		ns
t _{CO2} ^[9, 10, 11]	Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Combinatorial Output Delay (Through Logic Array)		11		14		19	ns
t _{SCS} ^[9]	Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable (Through Logic Array)	6.5		8		12		ns
t _{SL} ^[9]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	8.5		10		15		ns
t _{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	0		0		0		ns
Product Term Clocking Parameters								
t _{COPT} ^[9, 10, 11]	Product Term Clock or Latch Enable (PTCLK) to Output		10		13		15	ns
t _{SPT}	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	2.5		3		4.5		ns
t _{HPT}	Register or Latch Data Hold Time	2.5		3		4.5		ns

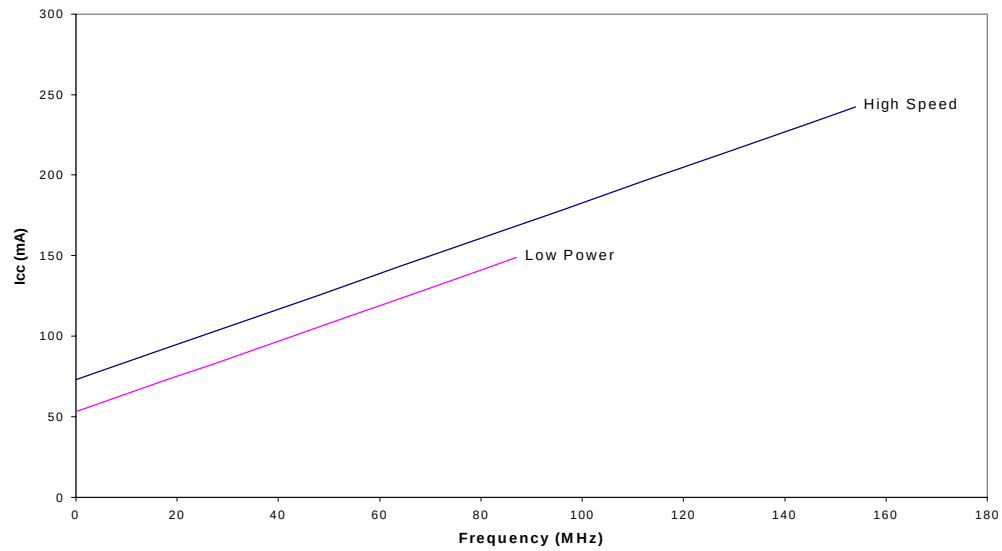
Notes:

8. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
9. Logic Blocks operating in low power mode, add t_{LP} to this spec.
10. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
11. When $V_{CC0} = 3.3V$, add $t_{3.3IO}$ to this spec.

Switching Characteristics Over the Operating Range^[8] (continued)

Parameter	Description	37192-154		37192-125		37192-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{ISPT}^{[9]}$	Set-Up Time for Buried Register Used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)		-2		-2		-2	ns
t_{IHPT}	Buried Register Used as an Input Register or Latch Data Hold Time		6.5		9		14	ns
$t_{CO2PT}^{[9, 10, 11]}$	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)		15		19		24	ns
Pipelined Mode Parameters								
$t_{ICS}^{[9]}$	Input Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) to Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃)	6		8		12		ns
Operating Frequency Parameters								
f_{MAX1}	Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$) ^[6]	154		125		83		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	200		158		125		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$)	105		83		67		MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_S)$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	143		125		67		MHz
Reset/Preset Parameters								
t_{RW}	Asynchronous Reset Width ^[6]	8		10		15		ns
$t_{RR}^{[9]}$	Asynchronous Reset Recovery Time ^[6]	10		12		17		ns
$t_{RO}^{[9, 10, 11]}$	Asynchronous Reset to Output		13		15		21	ns
t_{PW}	Asynchronous Preset Width ^[6]	8		10		15		ns
$t_{PR}^{[9]}$	Asynchronous Preset Recovery Time ^[6]	10		12		17		ns
$t_{PO}^{[9, 10, 11]}$	Asynchronous Preset to Output		13		15		21	ns
User Option Parameters								
t_{LP}	Low Power Adder		4		4		4	ns
t_{SLEW}	Slow Output Slew Rate Adder		2		2		2	ns
$t_{3.3IO}$	3.3V I/O Mode Timing Adder		0.1		0.1		0.1	ns
JTAG Timing Parameters								
$t_{S JTAG}$	Set-Up Time from TDI and TMS to TCK	0		0		0		ns
$t_{H JTAG}$	Hold Time on TDI and TMS	20		20		20		ns
$t_{CO JTAG}$	Falling Edge of TCK to TDO		20		20		20	ns
f_{JTAG}	Maximum JTAG Tap Controller Frequency		20		20		20	MHz

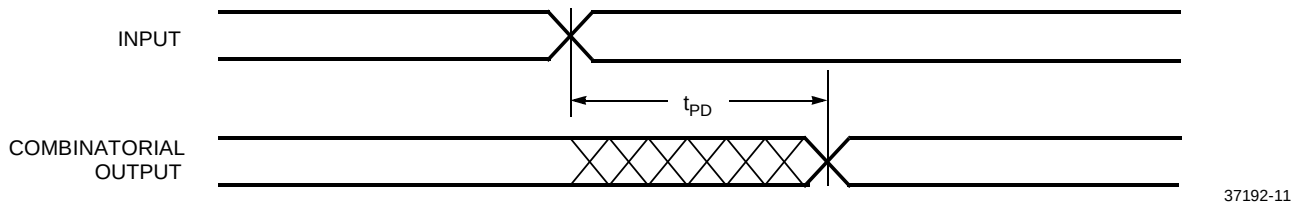
Typical I_{CC} Characteristics



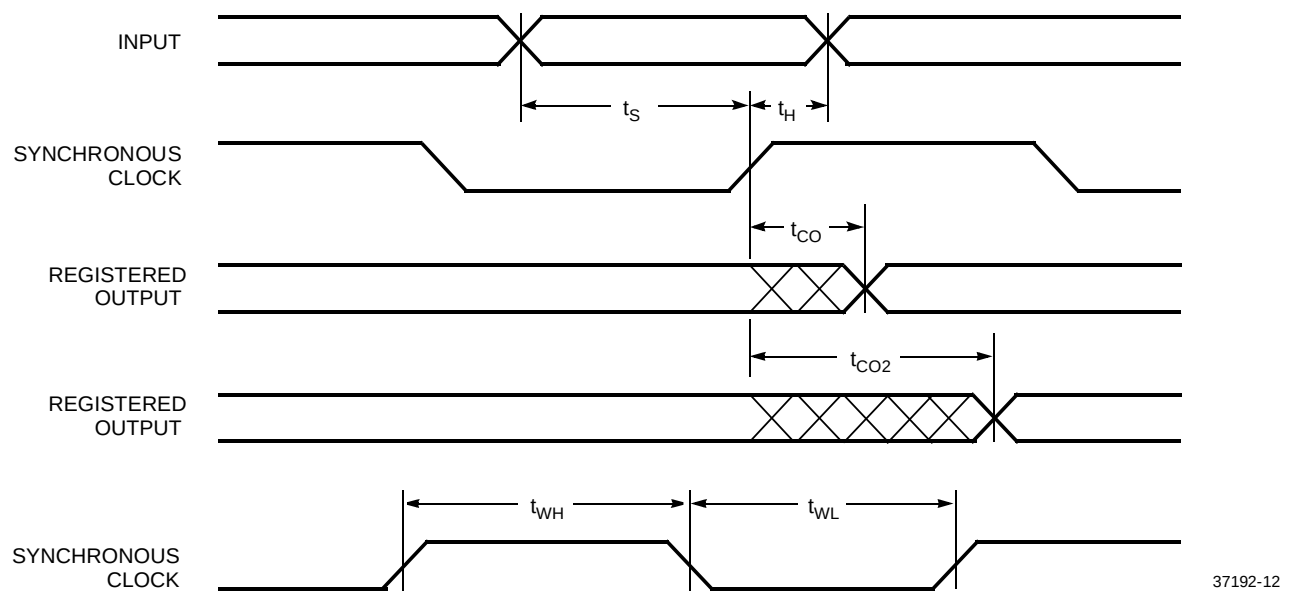
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

Switching Waveforms

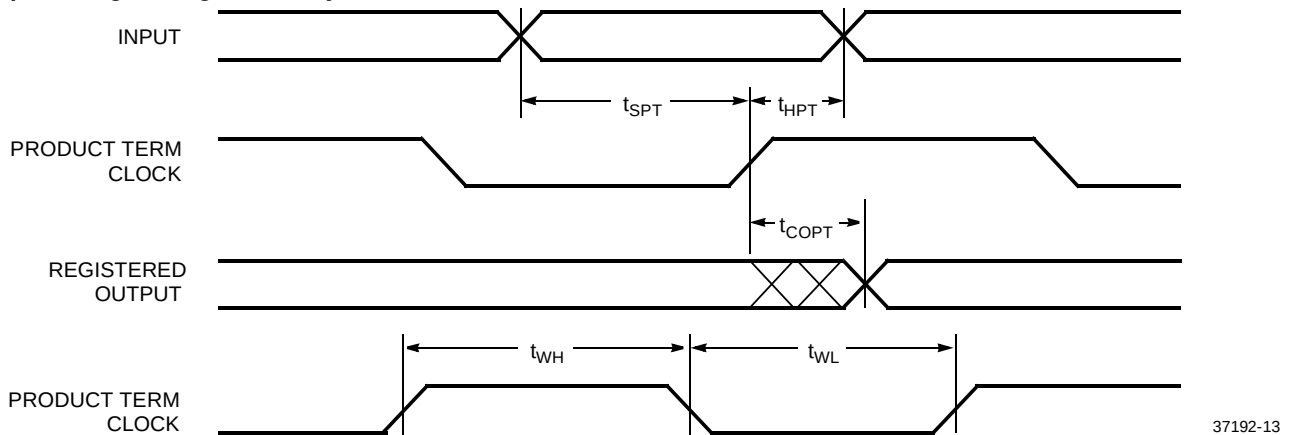
Combinatorial Output



Registered Output with Synchronous Clocking

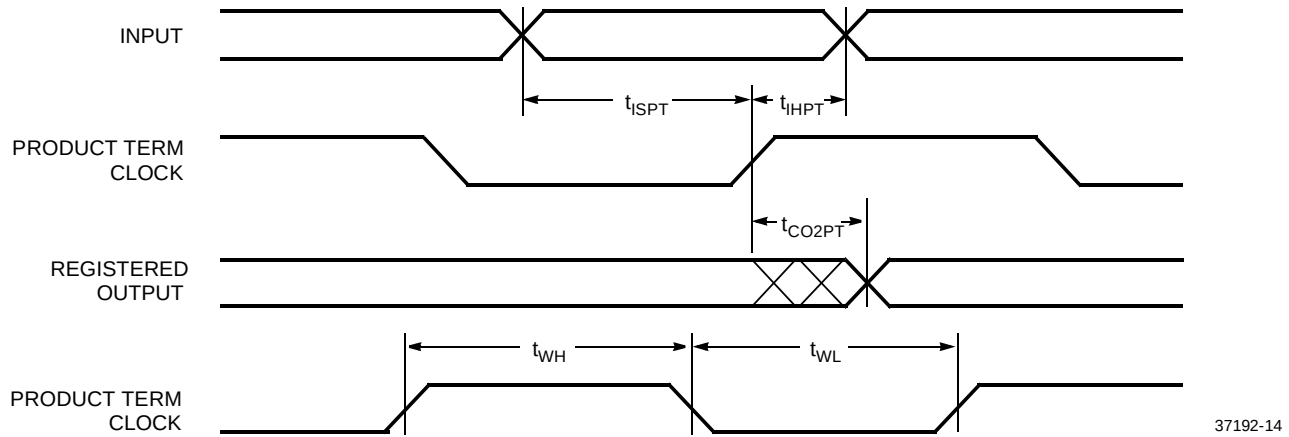


Registered Output with Product Term Clocking Input Going Through the Array

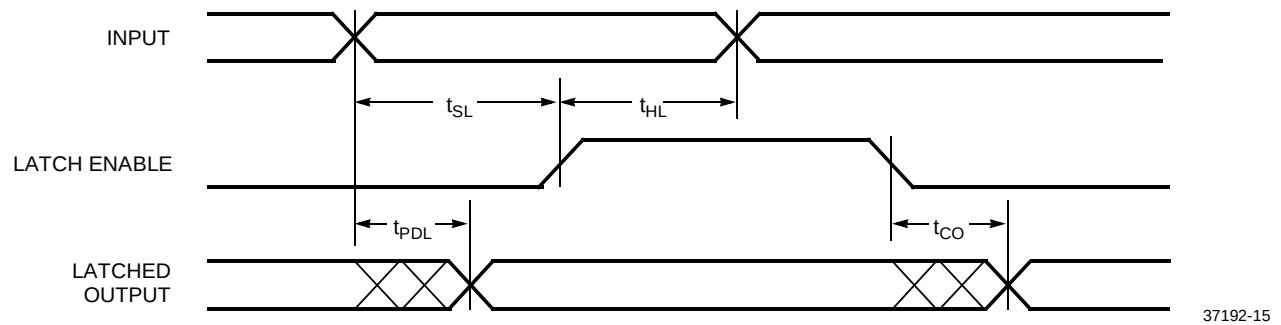


Switching Waveforms (continued)

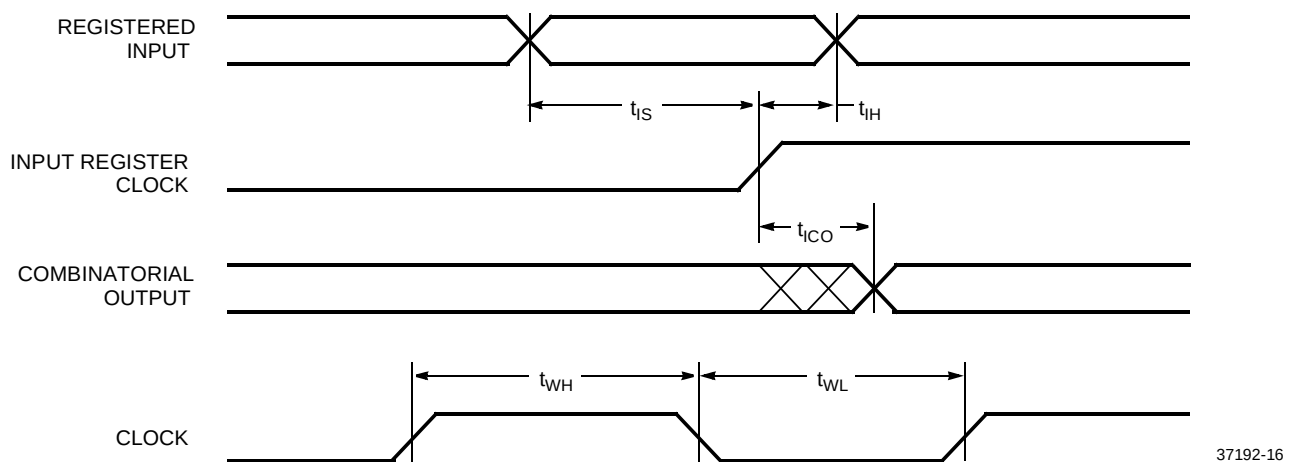
Registered Output with Product Term Clocking Input Coming from Adjacent Buried Register



Latched Output

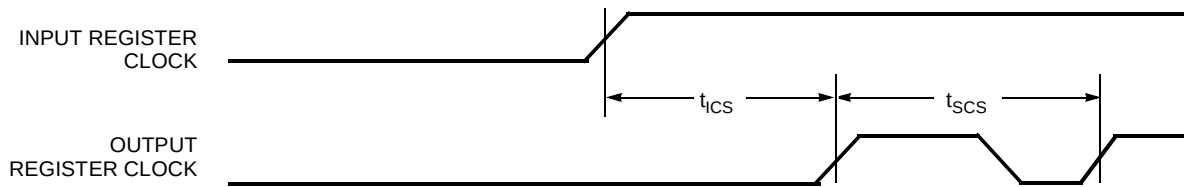


Registered Input



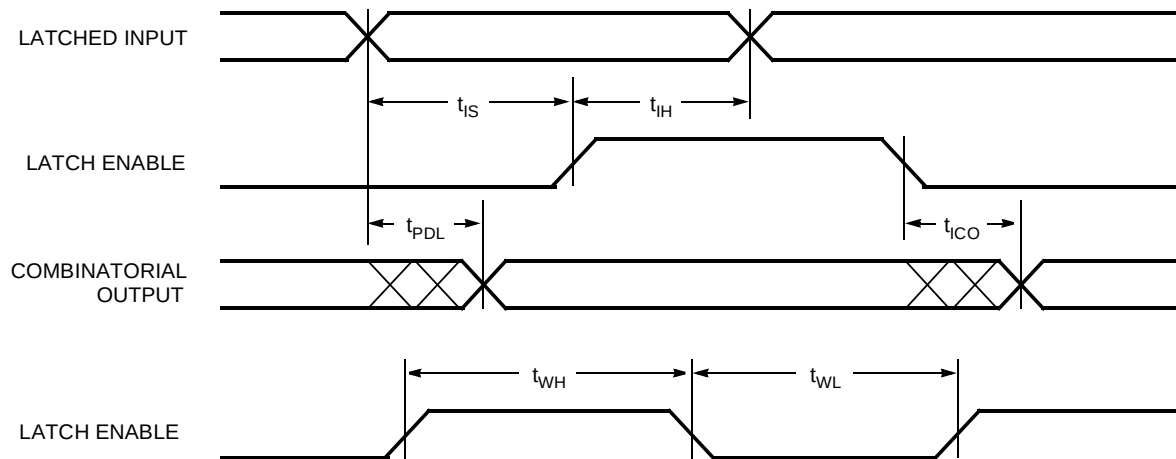
Switching Waveforms (continued)

Clock to Clock



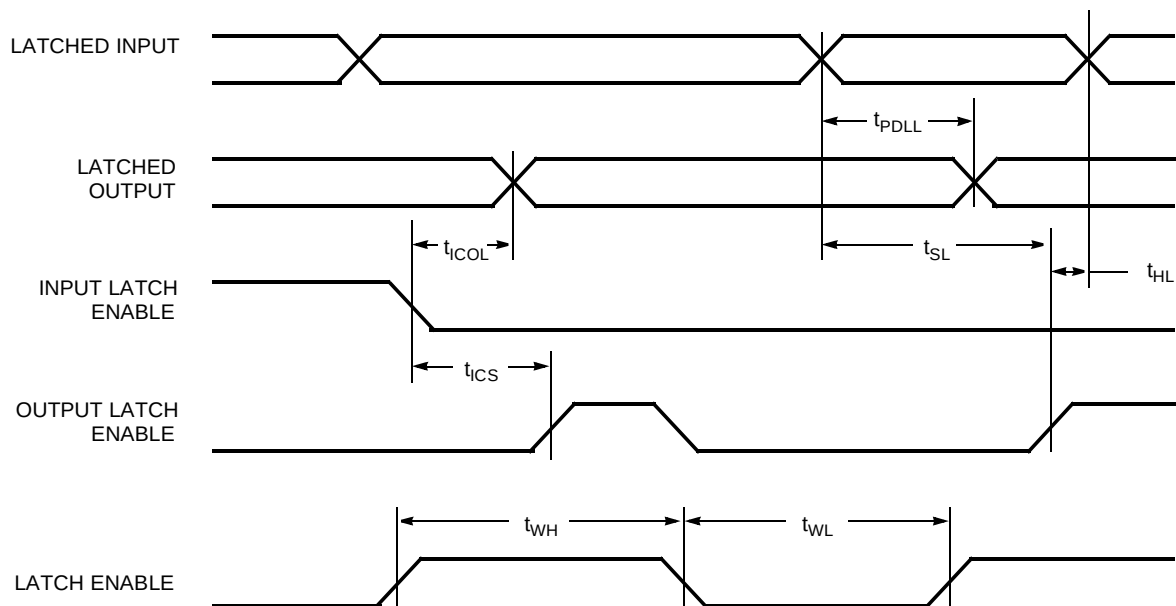
37192-17

Latched Input



37192-18

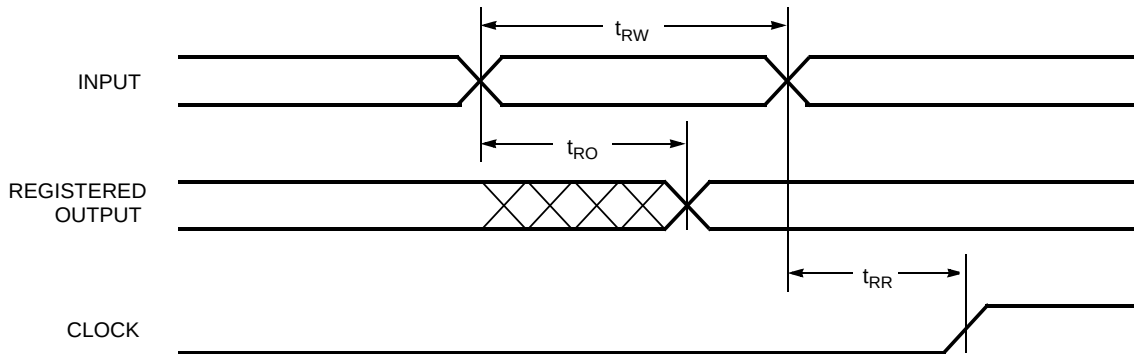
Latched Input and Output



37192-19

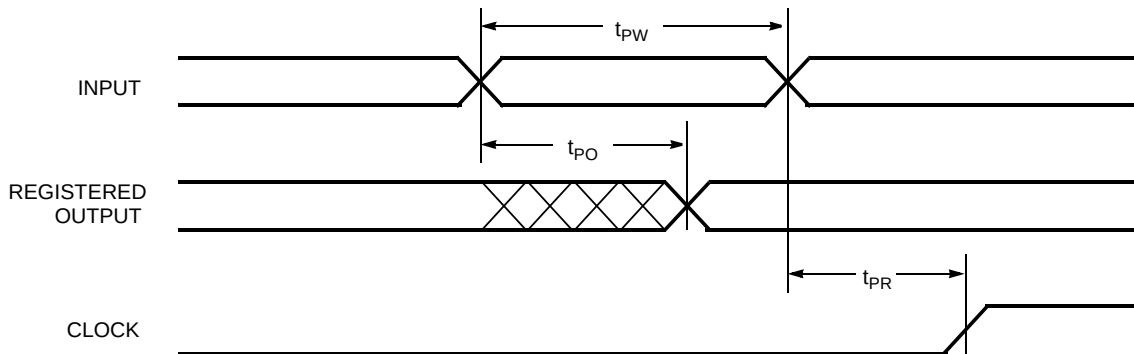
Switching Waveforms (continued)

Asynchronous Reset



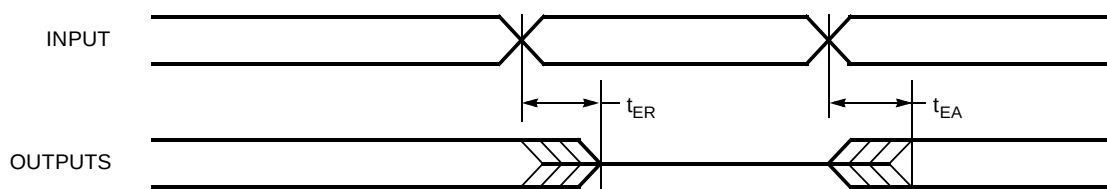
37192-20

Asynchronous Preset



37192-21

Output Enable/Disable



37192-22

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
154	CY37192P160-154AC	A160	160-Pin Thin Quad Flatpack	Commercial
125	CY37192P160-125AC	A160	160-Pin Thin Quad Flatpack	Commercial
	CY37192P160-125AI	A160	160-Pin Thin Quad Flatpack	Industrial
83	CY37192P160-83AC	A160	160-Pin Thin Quad Flatpack	Commercial
	CY37192P160-83AI	A160	160-Pin Thin Quad Flatpack	Industrial

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Document #: 38-00649-B

Package Diagram

160-Pin Thin Plastic Quad Flat Pack (TQFP) A160

DIMENSIONS ARE IN MILLIMETERS.

