

HD74LS195A • 4-bit Parallel-Access Shift Registers

This 4-bit register features parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

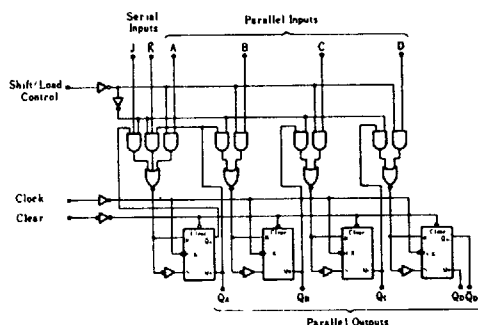
Parallel (broadside) load

Shift (in the direction Q_A toward Q_D)

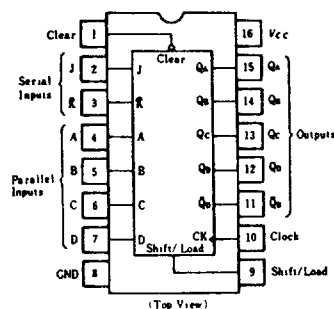
Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data

is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Clock frequency		f_{clock}	0	—	30	MHz
Clock pulse width		$t_w(CK)$	16	—	—	ns
Clear pulse width		$t_w(CLR)$	12	—	—	ns
Setup time	Shift/load	t_m	25	—	—	ns
	Serial and parallel data		15	—	—	
	Clear inactive-state		25	—	—	
Release time		$t_{release}$	—	—	5	ns
Hold time		t_h	0	—	—	ns

■ FUNCTION TABLE

Inputs									Outputs				
Clear	Shift/Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\bar{Q}_D$
			J	K	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\bar{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\bar{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\bar{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$

Notes) 1. H, high level, L, low level, X; irrelevant

2. ↑; transition from low to high level

3. ↓; transition from high to low level

4. a~d; the level of steady-state input at inputs A, B, C, or D, respectively

5. Q_{A0} ~ Q_{D0} ; the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established.

6. Q_{An} ~ Q_{Dn} ; the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most-recent ↑ transition of the clock.



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HD74LS195A

■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0	—	—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75\text{V}$, $V_{IH}=2\text{V}$, $V_{IL}=0.8\text{V}$, $I_{OH}=-400\mu\text{A}$	2.7	—	—	V
	V_{OL}	$V_{CC}=4.75\text{V}$, $V_{IH}=2\text{V}$, $I_{OL}=4\text{mA}$	—	—	0.4	V
		$V_{IL}=0.8\text{V}$, $I_{OL}=8\text{mA}$	—	—	0.5	
Input current	I_{IH}	$V_{CC}=5.25\text{V}$, $V_i=2.7\text{V}$	—	—	20	μA
	I_{IL}	$V_{CC}=5.25\text{V}$, $V_i=0.4\text{V}$	—	—	-0.4	mA
	I_i	$V_{CC}=5.25\text{V}$, $V_i=7\text{V}$	—	—	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25\text{V}$	-20	—	-100	mA
Supply current**	I_{CC}	$V_{CC}=5.25\text{V}$	—	14	21	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75\text{V}$, $I_{IK}=-18\text{mA}$	—	—	-1.5	V

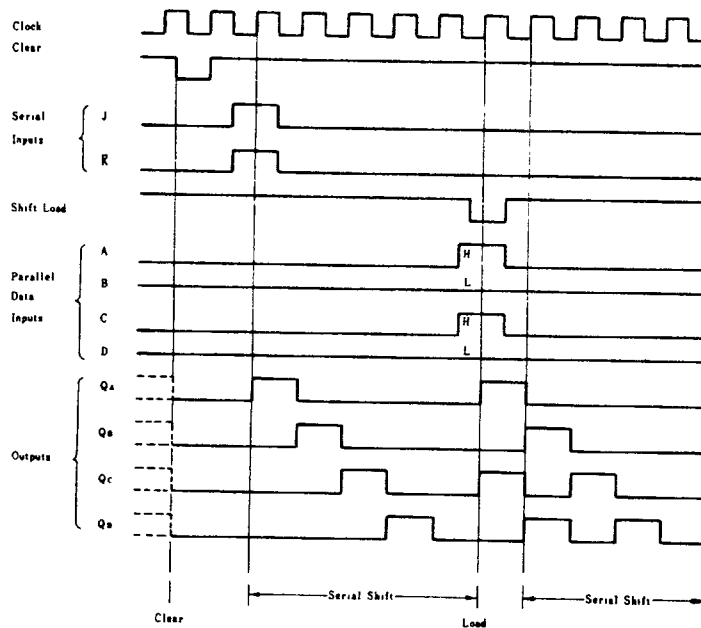
* $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$

** With all outputs open, shift/load grounded, and 4.5V applied to the J, $\bar{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V, to clear and then applying a momentary ground, followed by 4.5V, to clock.

■ SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$)

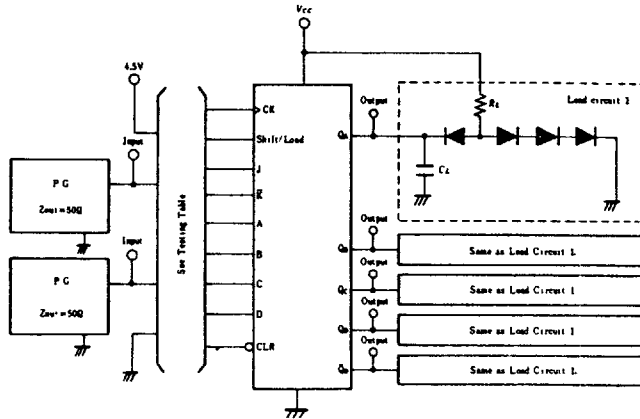
Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}	Clock	$Q_A \sim Q_D$	$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$	30	39	—	MHz
Propagation delay time	t_{PHL}	Clear	$Q_A \sim Q_D$		—	19	30	ns
	t_{PLH}	Clock	$Q_A \sim Q_D, \overline{Q_D}$		—	14	22	ns
	t_{PHL}				—	17	26	ns

■ COUNT SEQUENCE



TESTING METHOD

1) Test Circuit

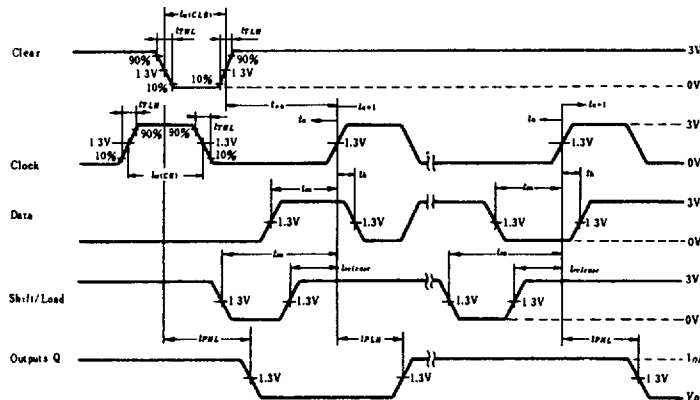


- Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 (H).

2) Testing Table

Item	From input to output	Inputs									Outputs				
		CLR	Shift/Load	J	K	CK	A	B	C	D	Q _A	Q _B	Q _C	Q _D	Q _D ⁻
f_{max}		4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	OUT
t_{PHL}	Clear → Q _A ~ Q _D	IN	GND	4.5V	4.5V	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	—
t_{PLH}	Clock → Q _A ~ Q _D , Q _D ⁻	4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	OUT
t_{PHL}		4.5V	GND	4.5V	4.5V	IN	IN	IN	IN	IN	OUT	OUT	OUT	OUT	OUT

Waveform



- Notes) 1. Input pulse; $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$, $PRR = 1\text{MHz}$, duty cycle 50%.
2. A clear pulse is applied prior to each test.
3. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+4} . Proper shifting of data is verified at t_{n+4} with a functional test.
4. J and K inputs are tested the same as data A, B, C, and D

- inputs except that shift/load input remains high.
5. t_n ; bit time before clocking transition.
6. t_{n+1} ; bit time after one clocking transition.
7. t_{n+4} ; bit time after four clocking transition.



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PACKAGING INFORMATION

T-90-20

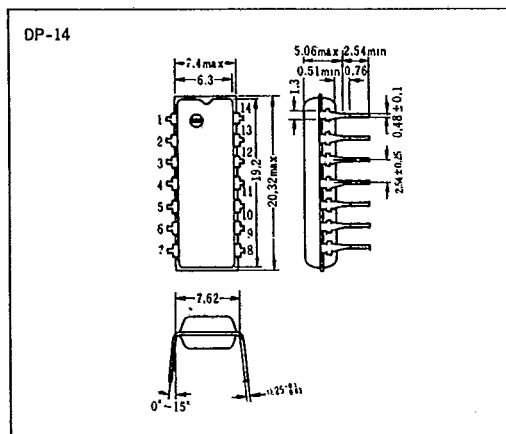
Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

HD 74LS00 P

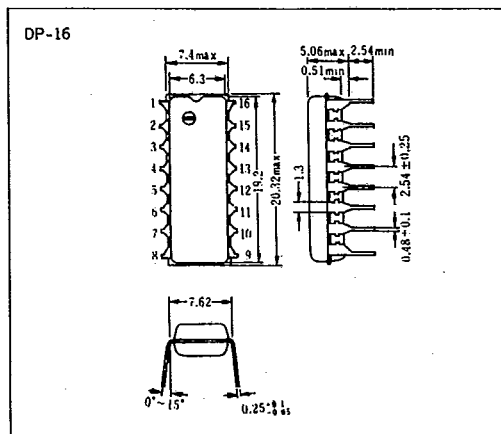
Package ; Plastic DIP ; letters P
Cerdip ; non-letters
Circuit description
Prefix : HD ; Hitachi Digital IC

■ Plastic DIP

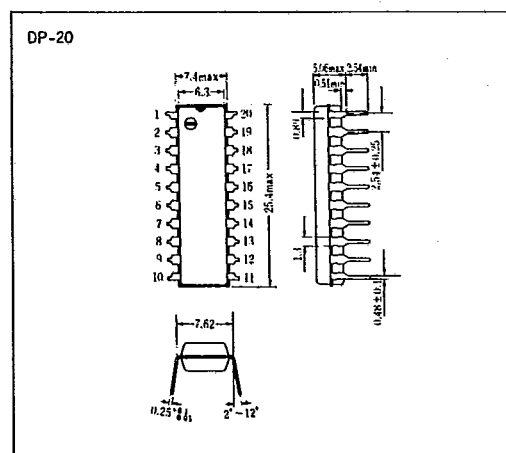
● 14 Pin



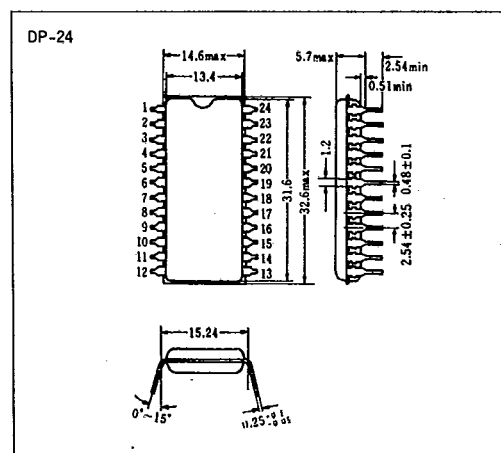
● 16 Pin



● 20 Pin



● 24 Pin



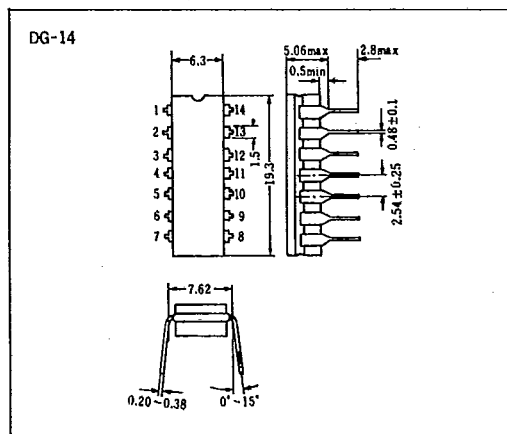
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T-90-20

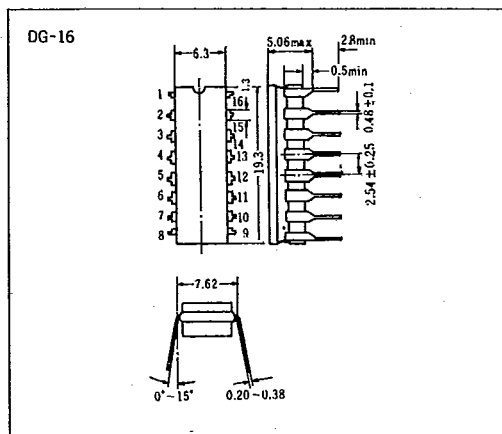
PACKAGING INFORMATION

■Cerdip

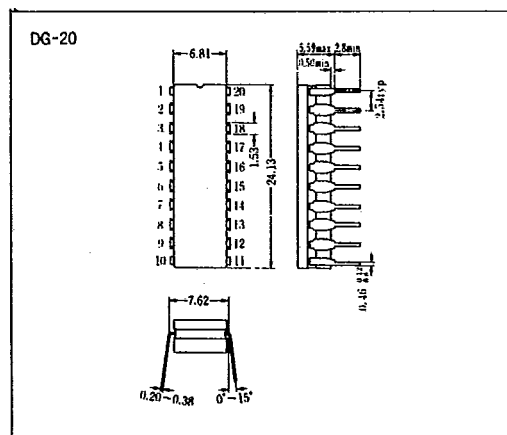
●14 Pin



●16 Pin



●20 Pin



●24 Pin

