*Preliminary Information*

AMD

# AMD-768™

# Peripheral Bus Controller

# Data Sheet

| Publication | Revision | Date |
|---|---|---|
| **24467** | **B** | **October 2001** |

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# Revision History

| Date | Revision | Description |
|---|---|---|
| October 2001 | B | Initial public release |

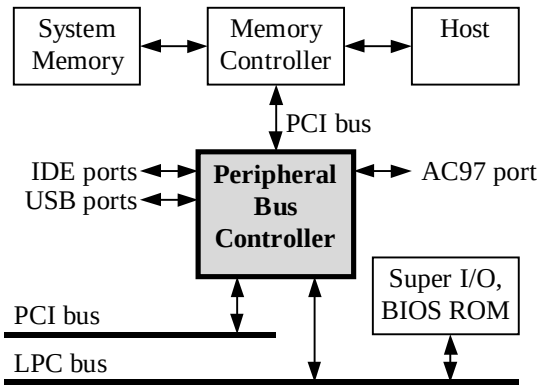
# 1 Overview

The AMD-768™ peripheral bus controller is an integrated circuit (IC) that serves as the *I/O hub*, *interface module*, or *Southbridge* component of personal computer chipsets. The AMD-768 device (*the IC*) connects to a host memory controller through the PCI bus and provides a secondary PCI-bus bridge.

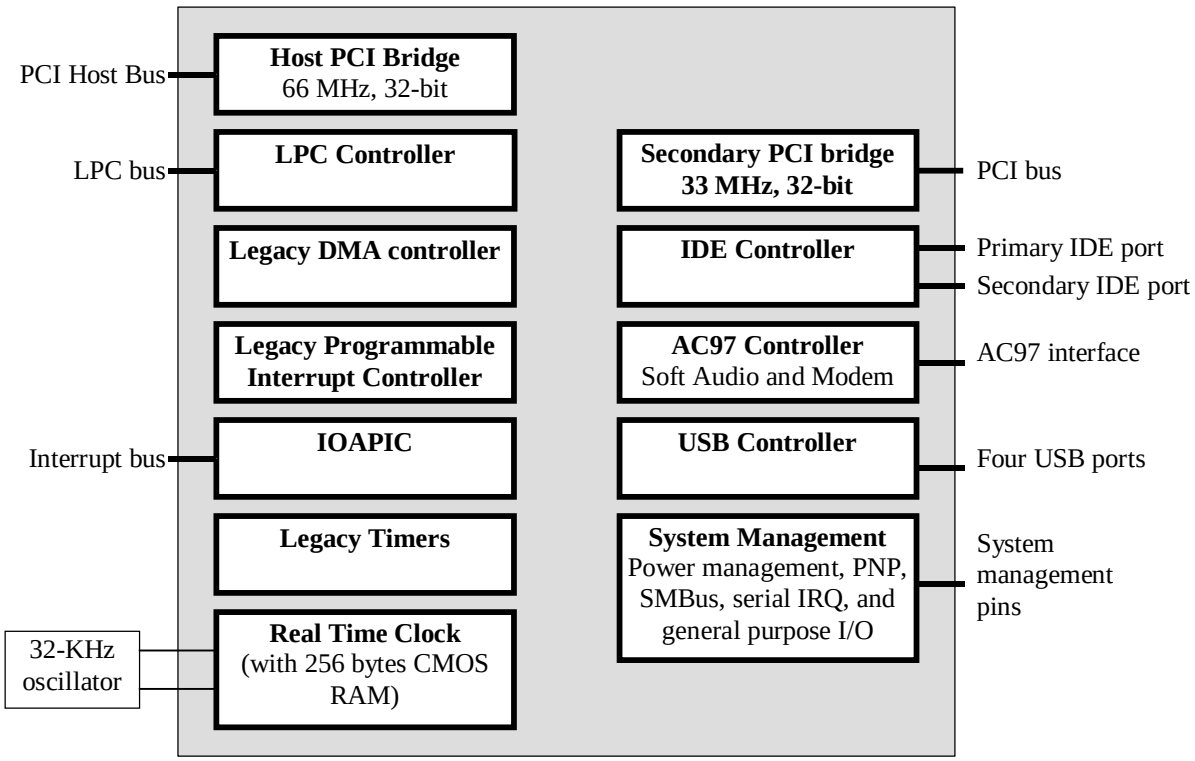
## 1.1 Features

- Host (primary) PCI bus utilizes a 66-MHz, 32-bit interface.
- Secondary PCI bridge utilizes a 33-MHz, 32-bit interface. PCI version 2.2 compliant. Includes PCI bus arbiter with support for up to eight external devices.
- AC97 soft modem and soft audio controller.
- Enhanced IDE controller. Support for a primary and a secondary dual-drive ports, PIO modes 0-4, multiword DMA, UDMA (through to ATA-100), ATAPI, 2 separate FIFOs for DMA accesses.
- OHCI-based USB host. Supports specification version 1.1. Includes a root hub and support for four ports.
- LPC bus to connect peripherals such as super IO and BIOS.
- Serial IRQ protocol.
- Extensive ACPI-compliant power management logic including: programmable C2, C3, power-on-suspend, suspend to RAM, suspend to disk, and soft off states; throttling; device monitors; hardware traps; system inactivity timers.
- 32 general-purpose IO (GPIO) pins. Many are multiplexed with other hard-wired functions.
- Privacy/security logic. ROM access control.
- Legacy AT-compatible logic: programmable interrupt controller; programmable interval timer; DMA controller (for LPC bus); legacy ports.
- IO APIC controller.
- Real-time clock. Includes 256 bytes of CMOS battery-powered RAM and ACPI-compliant extensions.
- SMBus controller with one SMBus port.
- Random number generator.
- 492-pin BGA package; 26-by-26 BGA grid; 35x35 millimeters square.
- 2.5-volt core; 3.3-volt output drivers; 5-volt tolerant input buffers.

The IC is intended to fit into the IO hub position on platforms that include a 66-MHz PCI bus. It interfaces with the host processor through the PCI bus.

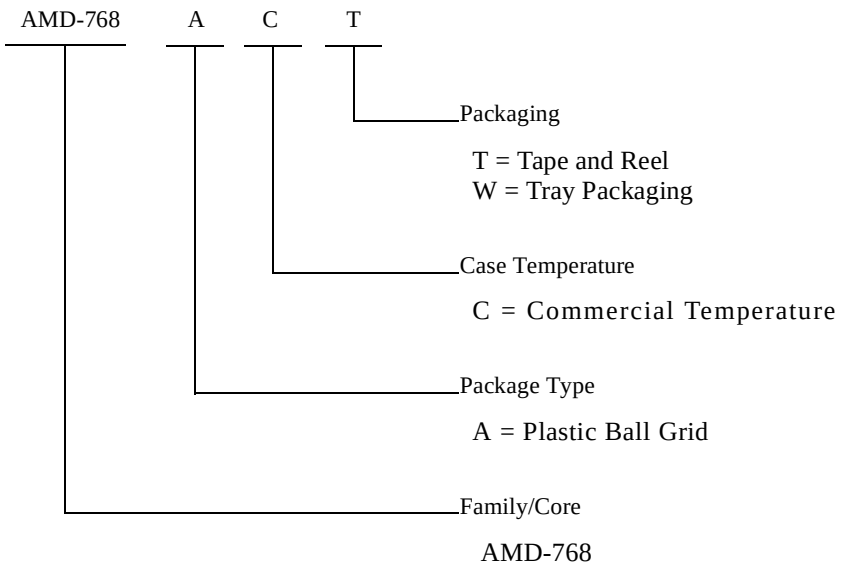



Block Diagram of the IC:



# 2 Ordering Information

The order number is formed by a combination of the elements shown below. Contact your AMD representative for detailed ordering information.



# 3 Signal Descriptions

## 3.1 Terminology

See Section 5.1.2 for a description of the register naming conventions used in this document. See Section 4.7.1.5 for a description of the system power states: MOFF, SOFF, STD, STR, POS, C3, C2, and FON. See Section 3.11 for a description of the power planes. See Section 4.1.1 for a description of the types of resets.

Signals with a # suffix are active Low.

Signals described in this chapter utilize the following IO cell types:

| Name | Notes |
|---|---|
| Input | Input signal only. |
| Output | Output signal only. This includes outputs that are capable of being in the high-impedance state. |
| OD | Open drain output. These pins are driven Low and expected to be pulled High by external circuitry. |
| IO | Input or output signal. |
| IOD | Input or open-drain output. |
| Analog | Analog signal. |

The following tables provide definitions and reference data about each of the IC's pins.

- The *During Reset* column provides the state of the pin while the pin's power plane is being reset (while RESET# is Low for the main power plane; while the internal RST_SOFT signal is asserted for the VDD_AUX power plane).
- The *After Reset* column provides the state of the pin immediately after the pin's power plane reset.
- The *During POS* column provides the state of the pin while in the power on suspend system sleep states.
- The *During S3:S5* column provides the state of the pin while in the suspend to disk, suspend to RAM, or soft off system sleep states.
- The abbreviation "Func." means the signal is functional and operating per its defined function.
- The "Main" power plane is VDD3 and VDD_CORE.

# 3.2 Host PCI Interface

| Pin Name and Description | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **A_AD[31:0].** Address-data bus. | IO | Main | 3-State | 3-State | 3-State | |
| **A_CBE_L[3:0].** Command-byte enable bus. | IO | Main | 3-State | 3-State | 3-State | |
| **A_DEVSEL#.** Device select signal. | IO | Main | 3-State | 3-State | 3-State | |
| **A_FRAME#.** Frame signal. | IO | Main | 3-State | 3-State | 3-State | |
| **A_GNT#.** Grant signal. | Input | Main | | | | |
| **A_IDSELA.** PCI-defined IDSEL pin for device A, the PCI bridge. See Section 5.1.1 for more details on this configuration space. | Input | Main | | | | |
| **A_IDSELB.** PCI-defined IDSEL pin for device B, the LPC bridge along with other functions. See Section 5.1.1 for more details on this configuration space. | Input | Main | | | | |
| **A_IRDY#.** Master ready signal. | IO | Main | 3-State | 3-State | 3-State | |
| **A_ISAREQ#.** Obsolete. | Output | Main | High | High | High | |
| **A_M66EN.** PCI-defined select for the operation of PCLK66. 0=Up to 33 MHz operation. 1=Up to 66 MHz operation. | Input | Main | | | | |
| **A_PAR.** Parity signal. | IO | Main | 3-State | 3-State | 3-State | |
| **A_REQ#.** Request signal. | Output | Main | High | High | High | |
| **A_SERR#.** system error signal. | Input | Main | | | | |
| **A_STOP#.** Target abort signal. | IO | Main | 3-State | 3-State | 3-State | |
| **A_TRDY#.** Target ready signal. | IO | Main | 3-State | 3-State | 3-State | |
| **PCLK66.** 66-MHz PCI clock. This may be 33 or 66 MHz, depending on the state of A_M66EN. If it is 33 MHz, it is allowed to be aligned with or inverted from PCLK. | Input | Main | | | | |

# 3.3 Secondary PCI Interface

| Pin Name and Description | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **AD[31:0].** PCI address-data bus. Some of these pins require pull-up and pull-down resistors for strapping options. See DevB:3x48. | IO | Main | 3-State | Parked | Parked | |
| **CBE_L[3:0].** PCI command-byte enable bus. | IO | Main | 3-State | Parked | Parked | |
| **DEVSEL#.** PCI device select signal. | IO | Main | 3-State | 3-State | 3-State | |
| **FRAME#.** PCI frame signal. | IO | Main | 3-State | 3-State | 3-State | |
| **GNT[6:0]#.** PCI master grant signals. | Output | Main | High | High | High | |
| **IRDY#.** PCI master ready signal. | IO | Main | 3-State | 3-State | 3-State | |
| **PAR.** PCI parity signal. | IO | Main | 3-State | Func. | Func. | |
| **PCLK.** 33-MHz PCI clock. | Input | Main | | | | |
| **PERR#.** PCI parity error. This signal is only applicable to parity errors on the secondary PCI bus interface. This signal is enabled by DevA:0x3C[PEREN]. | IO | Main | 3-State | 3-State | 3-State | |
| **PGNT#.** Priority PCI master grant. See PREQ#. | Output | Main | High | High | High | |
| **PIRQ[A, B, C, D]#.** PCI interrupt requests. | IOD | Main | 3-State | 3-State | Func. | |
| **PREQ#.** Priority PCI master request. PREQ#/PGNT# have no functional differences from REQ[6:0]#/GNT[6:0]#. | Input | Main | | | | |
| **REQ[6:0]#.** PCI master request signals. | Input | Main | | | | |
| **SERR#.** PCI system error signal. This may be asserted by the system to indicate a system error condition. If enabled by RTC70[7], an NMI interrupt may be generated. | Input | Main | | | | |
| **STOP#.** PCI target abort signal. | IO | Main | 3-State | 3-State | 3-State | |
| **TRDY#.** PCI target ready signal. | IO | Main | 3-State | 3-State | 3-State | |

# 3.4 Processor Interface

| Pin Name and Description | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **A20M#.** Address bit[20] mask to the processor. This output is a logical OR of the KA20G pin from the external keyboard controller and PORT92[A20EN]. | OD | Main | 3-State | 3-State | Func. | |
| **CPURST#.** Reset to the processor. This is the reset to processor(s). It is identical to RESET# in timing (but open drain, not push-pull). | OD | VDD_AUX | Low | Func. | Func. | |
| **FERR#.** Floating-point error from the processor. The processor asserts this signal to indicate a floating-point error has occurred. This is used to create IRQ13 to the PIC and IOAPIC. | Input | Main | | | | |
| **IGNNE#.** Ignore numeric error to the processor. | OD | Main | 3-State | 3-State | Func. | |
| **INIT#.** Initialization interrupt to the processor. The power-up timing of INIT# is the same as RESET#. | OD | Main | 3-State | 3-State | Func. | |
| **INTR.** Interrupt request to the processor. | OD | Main | Low | Low | Func. | |
| **NMI.** Non-maskable interrupt request to the processor. | OD | Main | Low | Low | Func. | |
| **PICD[1:0]#.** Interrupt message bus data bits 1 and 0 for the IOAPIC. | IOD | Main | 3-State | 3-State | Func. | |
| **PICCLK.** Interrupt message bus clock for the IOAPIC. This is controlled through DevB:0x4B[APICCKS]. | IOD | Main | Func. | Func. | Func. | |
| **SMI#.** System management interrupt to the processor. | OD | Main | 3-State | 3-State | Func. | |
| **STPCLK#.** Processor Stop Grant request. | OD | Main | 3-State | 3-State | Func. | |
| **WSC#.** Write snoop complete. This signal is used to ensure that the most recent PCI bus writes from the IC to system memory are visible to the host. WSC# is described in Section 4.4.2.2. This signal requires an external pull-up resistor with a value between 10K and 200K ohms. | IO | Main | 3-State | 3-State | Func. | |

# 3.5 LPC Bus and Legacy Support Pins

| Pin Name and Description | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **LAD[3:0].** LPC address-data bus. | IO | Main | 3-State | 3-State | 3-State | |
| **LDRQ0# and LDRQ1#.** LPC DMA request signals. | Input | Main | | | | |
| **LFRAME#.** LPC frame signal. | Output | Main | High | High | High | |
| **OSC.** 14.31818-MHz clock. This is used for the programmable interval timer and various power management timers. | Input | Main | | | | |
| **SPKR.** Speaker driver from programmable interval timer. This pin is an input only while PWROK is Low; it is used to select the default state of DevB:3x48[12]. | IO | Main | Input | Low | Last state | |

# 3.6 Ultra DMA Enhanced IDE Interface

| Pin Name and Description | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **DADDR[P,S][2:0].** IDE controller [primary, secondary] port address. | Output | Main | Low | Low | Low | |
| **DCS1P#.** IDE controller primary port chip select 1. This is active during accesses to the IO address space 1F7h–1F0h. | Output | Main | High | High | High | |
| **DCS1S#.** IDE controller secondary port chip select 1. This is active during accesses to the IO address space 177h–170h. | Output | Main | High | High | High | |
| **DCS3P#.** IDE controller primary port chip select 3. This is active during accesses to the IO address space 3F7h–3F4h. | Output | Main | High | High | High | |
| **DCS3S#.** IDE controller secondary port chip select 3. This is active during accesses to the IO address space 377h–374h. | Output | Main | High | High | High | |
| **DDACK[P,S]#.** IDE controller [primary, secondary] port DMA acknowledge signal. | Output | Main | High | High | High | |
| **DDATA[P,S][15:0].** IDE controller [primary, secondary] port data bus. | IO | Main | 3-State | 3-State | 3-State | |
| **DDRQ[P,S].** IDE controller [primary, secondary] port DMA request signal. | Input | Main | | | | |
| **DIOR[P,S]#.** IDE controller [primary, secondary] port IO read command. | Output | Main | High | High | High | |
| **DIOW[P,S]#.** IDE controller [primary, secondary] port IO write command. | Output | Main | High | High | High | |
| **DRDY[P,S].** IDE controller [primary, secondary] port ready strobe. | Input | Main | | | | |
| **DRST[P,S]#.** IDE controller [primary IDE port reset signal. This is asserted when RESET# is asserted. However, it may be separately asserted via DevB:1x54. | Output | Main | Low | High | Func. | |

# 3.7 System Management Pins

This group includes all the GPIO pins, most of which are multiplexed with other functions. The default function of GPIO pins after reset is specified by PM[DF:C0]. When programmed as GPIOs, these pins are capable of being programmed to be inputs or push-pull outputs. GPIO pins that are programmed as outputs, remain functional during sleep states (if they are powered).

| System Management Pin Name and Description | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **ACAV.** AC available input. This may be used to detect changes to the state of system AC power. It controls PM20[ACAV_STS]. This pin may be configured as GPIO0 by PMC0. | Input, IO | VDD_AUX | Input | Input | Func. | Func. |
| **AGPSTOP#.** AGP clock stop output. This may be used to control the system clock chip to control the AGP bus clock signal. It is controlled by DevB:3x50[ASTP]. This pin may be configured as GPIO1 by PMC1. | Output, IO | Main | High | High | Func. | |
| **BATLOW#.** Battery low input. This may be used to prevent system resumes from sleep states if the battery power is low and AC power is not available. This pin may be configured as GPIO2 by PMC2. | Input, IO | VDD_AUX | Input | Input | Func. | Func. |
| **C32KHZ.** 32.768-KHz clock output. This signal is active in all states except the MOFF state. This pin may be configured as GPIO3 by PMC3. | Output, IO | VDD_AUX | Func. | Func. | Func. | Func. |
| **CACHE_ZZ.** Level 2 cache sleep mode output. This may be connected to the power-control input of a processor's second level cache to place it into low-power mode. This function is controlled by DevB:3x4F[ZZ_C3EN]. This pin may be configured as GPIO4 by PMC4. | Output, IO | Main | Low | Low | Func. | |
| **CPUSLEEP#.** Processor non-snoop sleep mode open drain output. This may be connected to the sleep pin of the processor to place it into a non-snoop-capable low-power state. This function is controlled by DevB:3x4F[CSLP_C3EN] and DevB:3x50[CSLP]. This pin may be configured as GPIO6 by PMC6. | OD, IO | Main | High | High | Func. | |
| **CPUSTOP#.** Processor clock stop output. This may be connected to the system clock chip to control the host clock signals. It is controlled by DevB:3x4F[CSTP_C3EN] and DevB:3x50[CSTP]. This pin may be configured as GPIO7 by PMC7. | Output, IO | Main | High | High | Func. | |
| **DCSTOP#.** DRAM controller stop. This may be connected to the system memory controller to indicate that the its clock is going to stop. It is controlled by DevB:3x50[DCSTP]. | Output | VDD_AUX | Func. | Func. | Func. | Func. |
| **EXTSMI#.** External SMI. This pin may be used to generate SMI or SCI interrupts and resume events. It controls PM20[EXTSMI_STS]. | Input | VDD_AUX | | | | |
| **FANCON[1:0].** Fan control outputs. These may be used to control system fans. The frequency and duty cycle are specified by PMF8. FANCON1 may be configured as GPIO9 by PMC9. | Output, IO | Main | Low | Func. | Func. | |

| System Management Pin Name and Description (Continued) | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **FANRPM.** Fan revolutions per minute input. This may come from the system power supply. It is expected to produce 2 pulses per fan revolution. PM1F, which is a counter that is clocked by this signal, can be used to determine the speed of the fan. This pin may be configured as GPIO10 by PMCA. | Input, IO | Main | | | | |
| **GPIO[14].** General purpose IO 14. This is controlled by PMCE. See PM[DF:C0] for the power up defaults of all GPIO pins. | IO | VDD_ AUX | See left | See left | Func. | Func. |
| **GPIO[31:26, 17, 16, 8, 5].** General purpose IO. These are controlled by PM[DF:C0]. See PM[DF:C0] for the power up defaults of all GPIO pins. | IO | Main | See left | See left | Func. | |
| **INTIRQ8#.** Real-time clock interrupt output. This is real-time clock interrupt. This pin may be configured as GPIO11 by PMCB. | Output, IO | Main | High | High | Func. | |
| **INTRUDER#.** Intruder detection. This controls PM46[INTRDR_STS]. | Input | VDD_ AL | | | | |
| **IRQ1.** Keyboard interrupt request input. This pin may be configured as GPIO12 by PMCC. | Input, IO | Main | | | | |
| **IRQ6.** Floppy disk controller interrupt request input. This pin may be configured as GPIO13 by PMCD. | Input, IO | Main | | | | |
| **IRQ12.** Mouse interrupt request input. This pin may be configured as GPIO15 by PMCF. | Input, IO | Main | | | | |
| **IRQ14.** IDE primary port interrupt request. | Input | Main | | | | |
| **IRQ15.** IDE secondary port interrupt request. | Input | Main | | | | |
| **KA20G.** Keyboard A20 gate. This is expected to be the gate A20 signal from the system keyboard controller. It affects A20M#. | Input | Main | | | | |
| **KBRC#.** Keyboard reset command. This is expected to be the processor reset signal from the system keyboard controller. When asserted, it will generate an INIT interrupt to the processor. | Input | Main | | | | |
| **LID.** Lid change-state detect input. This may be used to detect state changes in notebook shell lids. The logic for this pin includes a 16 millisecond debounce circuit; the signal must be stable for about 16 milliseconds (going High or going Low) before it is detected by the rest of the internal logic. This pin may be configured as GPIO18 by PMD2. | Input, IO | VDD_ AUX | | | | |
| **PCISTOP#.** PCI bus clock stop. This may be used to control the system clock chip to control the PCI bus clock signals. It is controlled by DevB:3x50[PSTP]. | Output | Main | High | High | Func. | |
| **PME#.** Power management interrupt. This pin may be used to generate SMI or SCI interrupts and resume events. It controls PM20[PME_STS]. | Input | VDD_ AUX | | | | |
| **PNPIRQ[2:0].** Plug and play interrupt request inputs. These may be assigned to control any of 12 of the internal IRQ signals by DevB:3x44. PNPIRQ0 may be configured as GPIO19 by PMD3; PNPIRQ1 may be configured as GPIO20 by PMD4; PNPIRQ2 may be configured as GPIO21 by PMD5. | Input, IO, | Main | Input | Input | Input | |

| System Management Pin Name and Description (Continued) | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **PRDY.** Processor ready. When this is asserted, the IC freezes the timers specified by DevB:3x4C. | Input | Main | | | | |
| **PWRBTN#.** Power button. This may be used to control the automatic transition from a sleep state to FON. It controls PM00[PWRBTN_STS]. Also, if it is asserted for four seconds from any state other than SOFF, then a power button override event is generated. A power button override event causes the PWRON# pin to be driven High and PM00[PBOR_STS] to be set High. The logic for this pin includes a 16 millisecond debounce circuit; the signal must be stable for about 16 milliseconds before it is detected by the rest of the internal logic. | Input | VDD_ AUX | | | | |
| **PWROK.** Power OK. This is required to be Low while the main power planes are not valid, stay Low for at least 50 milliseconds after they become valid, and then go High. It is the reset source for the main power supplies of the IC, VDD_CORE and VDD3. The rising edge of this pin is debounced for one to two 32-KHz (RTC) clocks before it is internally detected as being High. | Input | VDD_ AUX | | | | |
| **PWRON#.** Main power on. This is expected to control the main power supplies to the system board. It is asserted during the FON, C2, C3, and POS states; it is deasserted during the STR, STD and SOFF states. When power is applied to the VDD_AUX plane, this signal is forced inactive until RST_SOFT is deasserted. See Section 4.7.1.5.2 for more details. | OD | VDD_ AUX | 3-State | Low | Low | 3-State |
| **RESET#.** System reset. This is the system reset signal for logic that is powered by the main power supplies. See Sections 4.1.1 and 4.7.1.5.2 for more details. | Output | VDD_ AUX | Func. | Func. | High | Low |
| **RI#.** Ring indicate. This is intended to cause the system to resume to the FON states and generate SCI or SMI interrupts. It controls PM20[RI_STS]. | Input | VDD_ AUX | | | | |
| **RPWRON.** RAM power on. This is intended to control power to the system memory power plane. When High, it is expected that power to system memory is enabled. When Low, it is expected that power to system memory is disabled. This pin is Low during STD and SOFF and High in all other states. See Section 4.7.1.5.2 for more details. | OD | VDD_ AUX | Func. | 3-State | 3-State | Func. |
| **RTCX_IN.** Real-time clock 32.768-KHz crystal input. This pin is expected to be connected through a crystal oscillator to RTCX_OUT. | Analog | VDD_ AL | Func. | Func. | Func. | Func. |
| **RTCX_OUT.** Real-time clock 32.768-KHz crystal output. | Analog | VDD_ AL | Func. | Func. | Func. | Func. |
| **SERIRQ.** Serial IRQ signal. This pin supports the serial IRQ protocol. Control for this is in DevB:3x4A. | IO | Main | 3-State | 3-State | Func. | |

| System Management Pin Name and Description (Continued) | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **SLPBTN#.** Sleep button input. This may be used to control the automatic transition from a sleep state to FON. It controls PM00[SLPBTN_STS]. Also, if it is asserted for four seconds from any state other than SOFF, then a power button override event is generated. A power button override event causes the PWRON# pin to be driven High and PM00[PBOR_STS] to be set High. The logic for this pin includes a 16 millisecond debounce circuit; the signal must be stable for about 16 milliseconds before it is detected by the rest of the internal logic. This pin may be configured as GPIO23 by PMD7. | Input, IO | VDD_AUX | | | | |
| **SMBALERT#.** SMBus alert input. This may be used to generate an SMI or SCI interrupt or a resume event associated with the SMBus logic. This pin may be configured as GPIO22 by PMD6. Note: although this pin resides on the VDD_AUX power plane, it can only be used for the SMBus alert function while the main power supply is valid. | Input, IO | VDD_AUX | | | | |
| **SMBUSC.** System management bus (SMBus) clock. | IOD | VDD_AUX | 3-State | 3-State | Func. | Func. |
| **SMBUSD.** System management bus (SMBus) data. | IOD | VDD_AUX | 3-State | 3-State | Func. | Func. |
| **SQWAVE.** Square wave clock output. This is a square wave output, the frequency for which is specified by DevB:3x4E. This pin may be configured as GPIO24 by PMD8. | Output, IO | Main | Low | Low | Func. | |
| **SUSPEND#.** Suspend output. This may be used during the POS state to control an external power planes. It is controlled by DevB:3x50[SUSP]. This pin may be configured as GPIO25 by PMD9. | Output, IO | Main | High | High | Func. | |
| **THERM#.** Thermal warning detect. This may be used to automatically enable processor throttling as specified by DevB:3x4D[TTH_RATIO, TTH_EN]. This pin is also controlled by DevB:3x40[TH2SD, TTPER, and THMINEN]. See Section 4.7.1.4 for more details. | Input | Main | | | | |

# 3.8 Universal Serial Bus Interface

| Pin Name and Description | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **USBCLK.** 48-MHz USB clock. | Input | Main | | | | |
| **USBP[3:0], USBN[3:0].** USB ports. These are the four pairs of differential USB signals. USBP[3:0] are the positive signals and USBN[3:0] are the negative signals. | IO | VDD_AUX | Low | Low | 3-State; can detect resume | 3-State; can detect resume |
| **USBOC0#.** USB over current. This goes to the USB logic to report the occurrence of an over-current condition on the voltage supplied to the USB ports. | Input | Main | | | | |
| **USBOC1#.** USB over current detect 1. When enabled to do so, this can be routed to the USB block to be a second source of USB port over-current detection. | Input | Main | | | | |

# 3.9 AC97 Interface

| Pin Name and Description | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **ACCLK.** AC97 bit clock. 12.288-MHz fixed frequency from primary codec. An external 10Kohm pull-down is required on this pin in support of powering down the AC-link codec. | Input | Main | | | | |
| **ACRST#.** AC97 asynchronous reset. | Output | VDD_AUX | Low | Low | Low | Low |
| **ACSDI0.** AC97 primary codec serial data in (slot 0 codec ID field = 00b) from first codec in system. An external 10Kohm pull-down is required on this pin in support of powering down the AC-link codec. | Input | VDD_AUX | | | Can detect resume | Can detect resume |
| **ACSDI1.** AC97 secondary codec serial data in (slot 0 codec ID field = 01b) from second codec in system. An external 10Kohm pull-down is required on this pin in support of powering down the AC-link codec. | Input | VDD_AUX | | | Can detect resume | Can detect resume |
| **ACSDO.** AC97 serial data out. | Output | Main | Low | Low | Low | |
| **ACSYNC.** AC97 frame synchronization pulse. | Output | Main | Low | Low | Low | |

# 3.10 Test and Miscellaneous

| Pin Name and Description | IO Cell Type | Power Plane | During Reset | After Reset | During POS | During S3:S5 |
|---|---|---|---|---|---|---|
| **NC[32:0].** No connection. These pins should not be tied to any nodes. | | | | | | |
| **STRAPL[25:0].** Strapping option to be tied Low. These pins should be tied to ground. | Input | Main | | | | |
| **STRAPH[3:0].** Strapping option to be tied High. These pins should be tied through a pull up resistor to VDD3. | Input | Main | | | | |
| **TEST#.** Scan, NAND tree, and high-impedance mode enable. See Chapter 9 for more details. | Input | Main | | | | |
| **SPARE[4:0].** Spare pins. These outputs are all driven as zeros. | Output | VDD_ AUX | | | | |
| **SPARE[19:5].** Spare pins. These outputs are all driven as zeros. | Output | Main | | | | |

# 3.11 Power and Ground

See Section 4.7.1.5 for a description of the system power states. The following power and ground planes are connected to the IC through BGA pins.

**VDD3.** 3.3 volt supply. This plane is required to be valid in the FON and POS power states. It is part of the *main* power supply.

**VDD_AUX2** and **VDD_AUX3.** VDD_AUX2 is a 2.5 volt plane and VDD_AUX3 is a 3.3 volt plane. Both of these planes are required to be valid at the same times. They are valid in all system power states except MOFF. *VDD_AUX* refers both of these planes. The pins powered by these planes are: PWRBTN#, PWRON#, PME#, SMBUS[C,D], EXTSMI#, SLPBTN#, RI#, PWROK, SMBALERT#, RESET#, RPWRON, DCSTOP#, ACAV, LID, BATLOW#, C32KHZ, ACSDI[1,0], ACRST#, CPURST#, GPIO14, SPARE[4:0], USBP[3:0], USBN[3:0]. Register bits that are on the VDD_AUX plane are reset by the internal RST_SOFT pulse that is generated for about 30 milliseconds after VDD_AUX becomes valid.

**VDD_CORE.** 2.5 volt supply. This plane is required to be valid in the FON and POS power states. It is part of the *main* power supply.

**VDD_REF.** 5.0 volt reference supply. This plane is required to be valid in all power states except MOFF.

**VDD_RTC.** 3.3 volt supply. This plane is required to be valid in all power states. It is typically powered by a battery. It supplies power for the internal VDD_AL power plane when VDD_AUX is not valid.

**VDD_USB.** 3.3 volt supply filtered for the USB transceivers. This plane is required to be valid in all power states except MOFF.

**VSS.** Main ground plane.

**VSS_USB.** Ground plane filtered for the USB transceivers.

The IC also includes the following internal power plane.

**VDD_AL.** VDD always. This is an internal plane. It is supplied by VDD_AUX when that plane is valid or by VDD_RTC when VDD_AUX is not valid. VDD_AL powers the real-time clock and some system management circuitry. The pins powered by VDD_AL are: RTCX_IN, RTCX_OUT, INTRUDER#.

General requirements:
- The voltage level of VDD_CORE is required to be less than VDD3 at all times.
- The voltage level of VDD_AUX2 is required to be less than VDD_AUX3 at all times.
- VDD_AUX2 and VDD_AUX3 are both required to be powered before VDD3 and VDD_CORE may be powered.

# 4 Functional Operation

The IC connects to the host memory controller through a 66-MHz, 32-bit PCI bus as described in Section 1.1.

The IC supports processor accesses to BIOS on either the secondary PCI bus or the LPC bus. At boot the BIOS is specified to reside on one of these busses as described in the strapping option located at DevB:3x48[PCI-BIOS].

See Section 5.1 for details about the software view of the IC. See Section 5.1.2 for a description of the register naming convention.

## 4.1 Overview

### 4.1.1 Resets

The IC generates an internal reset for the VDD_AUX power planes called RST_SOFT. RST_SOFT lasts for about 30 milliseconds after the VDD_AUX plane becomes valid. See Section 4.7.1.5.2 for more details.

PWROK is the source of reset for some of the IC's VDD3 and VDD_CORE logic. From this signal, RESET#, INIT#, and CPURST# are derived. See Section 4.7.1.5.2 for more details.

It is possible to generate system resets via DevB:0x47[SWRST]. These cause RESET# and CPURST# to be asserted for greater than 1.5 milliseconds.

Various system resets may be initiated through PORTCF9.

It is also possible to reset the processor (without clearing the cache) with an INIT interrupt through the external keyboard controller via KBRC#, the PORT92 register, or from a shutdown special cycle from the host.

## 4.1.2 Error Reporting and Handling

The following is a summary of the errors that are reported and how they are handled in the IC; “secondary” refers to the secondary PCI bridge, which includes an external PCI bus and internal devices on the secondary PCI bus.

| Error Type | Status bit | Handler enable | Handler action | Notes |
|---|---|---|---|---|
| Received target abort on host | DevA:0x04[RTA] | DevB:0x40[NMIONERR] | Generate NMI | 1 |
| Received master abort on host | DevA:0x04[RMA] | DevB:0x40[NMIONERR] | Generate NMI | 1 |
| Received A_SERR# from host | DevB:0x40[RSEA] | DevB:0x40[NMIONERR] | Generate NMI | 1 |
| Detected parity error on the host | DevA:0x04[DPE] | DevB:0x40[NMIONERR] | Generate NMI | 1 |
| Signaled target abort on secondary | DevA:0x1C[STA] | DevB:0x40[NMIONERR] | Generate NMI | |
| Received target abort on secondary | DevA:0x1C[RTA] | DevB:0x40[NMIONERR] | Generate NMI | |
| Received master abort on secondary | DevA:0x1C[RMA] | DevB:0x40[NMIONERR] | Generate NMI | |
| SERR# assertion detected | DevA:0x1C[RSE] | DevB:0x40[NMIONERR] | Generate NMI | |
| | PORT61[SERR] | PORT61[CLRSERR] | Generate NMI | |
| Detected parity error on secondary | DEV:0x1C[DPE] | DevB:0x40[NMIONERR] | Generate NMI; assert PERR# | 2 |
| PERR# assertion detected | DevA:0x1C[MDPE] | DevA:0x3C[PEREN] | Generate NMI | |
| Master detect parity error on secondary | DevA:0x1C[MDPE] | DevB:0x3C[PEREN] | Generate NMI; assert PERR# | 2 |
| LPC protocol error | DevB:0x40[LPCERR], PORT61[IOCHK] | PORT61[CLRIOCHK] | Generate NMI | |

Note 1: The host refers to the host PCI bus.
Note 2: PERR# is only asserted if it is enabled by DevA:0x3C[PEREN].

See Section 4.4.2.3 for more details about NMI.

# 4.2 Host Interface

The 32-bit, 66-MHz primary PCI interface provides the host connection.

# 4.3 Secondary PCI Bridge

The secondary PCI bridge interfaces to the internal USB controller and the external PCI bus. Peer to peer transactions are supported between devices on the external PCI bus. However, all other transactions pass through the host interface; peer to peer transactions between internal and external devices are not supported. This means internal devices cannot be accessed from the secondary bus.

# 4.4 LPC Bridge and Legacy Logic

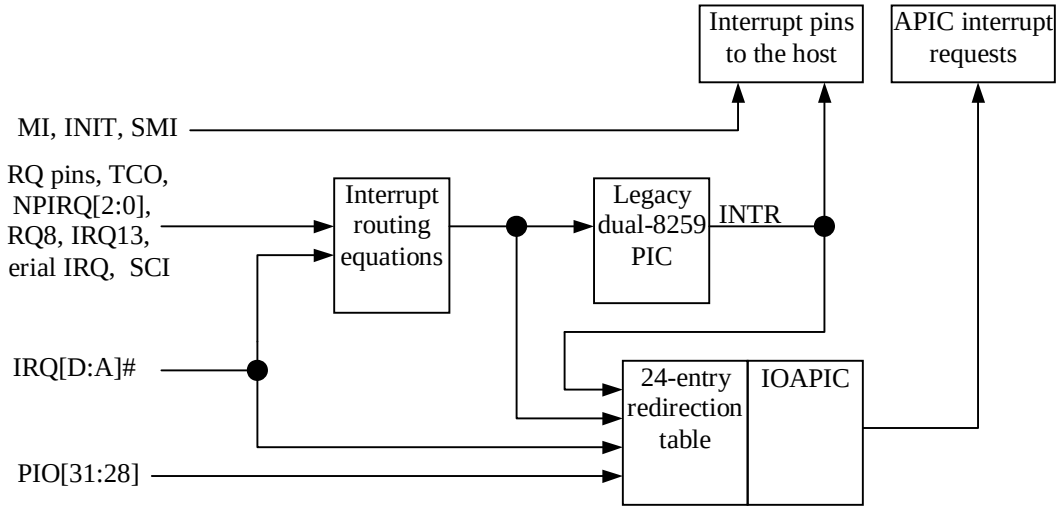
The LPC bridge supports external peripherals and BIOS devices through the LPC bus. It also includes legacy devices and logic required for compatibility with existing software.

## 4.4.1 Legacy and Miscellaneous Support Logic

The IC includes the following legacy support logic:
- PORT61 and PORT92 legacy registers.
- FERR# and IGNNE interrupt logic.
- PORT4D0 legacy interrupt edge-level select logic.
- PORTCF9 reset logic.
- Legacy dual-8237 DMA controller.
- Legacy 8254 PIT.

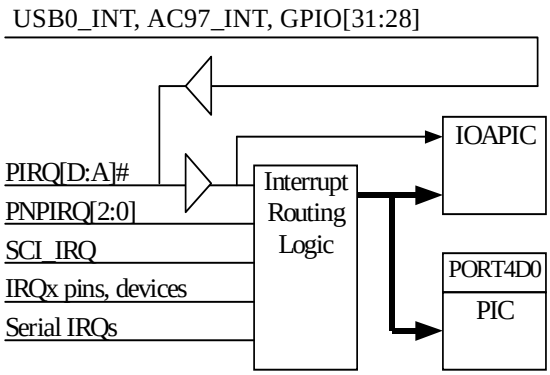
## 4.4.2 Interrupt Controllers

Interrupt types include vectored interrupts--INTR, ExtINT, fixed, and lowest priority--and non-vectored interrupts NMI, SMI, and INIT. These are sent through routing equations, the legacy PIC, and the IOAPIC to be transmitted to the host via the APIC interrupt message bus or processor interrupt pins.




### 4.4.2.1 Interrupt Control and Routing

Vectored interrupt requests are routed to the legacy PIC and APIC as shown. The interrupt signals to the PIC can be either rising-edge triggered or active-Low level triggered. It is expected that edge-triggered interrupts such as IRQ14 from the IDE controller rise into the PIC to indicate the presence of an interrupt. Conversely, level-sensitive interrupts are Low into the PIC to indicate the presence of an interrupt. Edge and level sensitivity for each IRQ are programmed into the PIC through PORT4D0.




Several internal interrupts are shared with the PCI interrupts pins. These internal interrupts signals drive the PIRQ[D:A]# pins Low as outputs; when the internal interrupts are deasserted, the pins are left in the high impedance state. These pins are wire-ORed into the active state with external interrupts. The result enters the IC and goes to the interrupt routing logic. The internal interrupts are mapped to the PIRQ[D:A]# pins as follows:

- GPIO[31:28] can be specified by DevB:0x4B[MPIRQ] to drive onto PIRQ[D:A]#, respectively.
- The AC97 interrupt—AC97_INT—drives onto the PIRQB# pin.
- The USB interrupt—USB0_INT—drives onto the PIRQD# pin.

Alternatively, these interrupts may all be mapped to PIRQD#, as specified by DevB:0x47[ALLTOD].

Here are the interrupt routing logic equations:

```
PIRQ_POLA = ~PIRQA# | SERINTA | DevB:1x08[8] & IRQ14 | DevB:1x08[10] & IRQ15;
PIRQ_POLB = ~PIRQB# | SERINTB;
PIRQ_POLC = ~PIRQC# | SERINTC;
PIRQ_POLD = ~PIRQD# | SERINTD;
PCI_IRQx  = PIRQ_POLA & (DevB:3x56[3:0]  == 4'hx) | PIRQ_POLB & (DevB:3x56[7:4]   == 4'hx)
          | PIRQ_POLC & (DevB:3x56[11:8] == 4'hx) | PIRQ_POLD & (DevB:3x56[15:12] == 4'hx);

PNP_IRQx  = PNPIRQ2 & (DevB:3x44[11:8] == 4'hx) | PNPIRQ1 & (DevB:3x44[7:4] == 4'hx)
          | PNPIRQ0 & (DevB:3x44[3:0] == 4'hx);

SCI_IRQx  = SCI_IRQ & (DevB:3x42[3:0] == 4'hx);

ISA_IRQx  = ~(IRQx  & SERIRQx ) &
            ~( (DevB:3x56[3:0]   == 4'hx) | (DevB:3x56[7:4]  == 4'hx) | (DevB:3x56[11:8] == 4'hx)
             | (DevB:3x56[15:12] == 4'hx) | (DevB:3x44[11:8] == 4'hx) | (DevB:3x44[7:4]  == 4'hx)
             | (DevB:3x44[3:0]   == 4'hx) | (DevB:3x42[3:0]  == 4'hx) );

KIRQ1     = IRQ1  & SERIRQ1;  // to the USB keyboard emulation logic
KIRQ12    = IRQ12 & SERIRQ12; // to the USB keyboard emulation logic

USB0_IRQ1  = ~ExternalIRQEn & KIRQ1                 // signal names from USB OHCI spec
           |  EmulationEnable & IRQEn & OutputFull & ~AuxOutputFull;
USB0_IRQ12 = ~ExternalIRQEn & KIRQ12                // signal names from USB OHCI spec
           |  EmulationEnable & IRQEn & OutputFull &  AuxOutputFull;

ISA_IRQ1  = ~(USB0_IRQ1) &
            ~( (DevB:3x56[3:0]   == 4'h1) | (DevB:3x56[7:4]  == 4'h1) | (DevB:3x56[11:8] == 4'h1)
             | (DevB:3x56[15:12] == 4'h1) | (DevB:3x44[11:8] == 4'h1) | (DevB:3x44[7:4]  == 4'h1)
             | (DevB:3x44[3:0]   == 4'h1) | (DevB:3x42[3:0]  == 4'h1);

ISA_IRQ12 = ~(USB0_IRQ12) &
            ~( (DevB:3x56[3:0]   == 4'hC) | (DevB:3x56[7:4]  == 4'hC) | (DevB:3x56[11:8] == 4'hC)
             | (DevB:3x56[15:12] == 4'hC) | (DevB:3x44[11:8] == 4'hC) | (DevB:3x44[7:4]  == 4'hC)
             | (DevB:3x44[3:0]   == 4'hC) | (DevB:3x42[3:0]  == 4'hC);

ISA_IRQ14 = ~(IRQ14  & SERIRQE ) &
            ~( (DevB:3x56[3:0]   == 4'hE) | (DevB:3x56[7:4]  == 4'hE) | (DevB:3x56[11:8] == 4'hE)
             | (DevB:3x56[15:12] == 4'hE) | (DevB:3x44[11:8] == 4'hE) | (DevB:3x44[7:4]  == 4'hE)
             | (DevB:3x44[3:0]   == 4'hE) | (DevB:3x42[3:0]  == 4'hE) | DevB:1x08[8]);

ISA_IRQ15 = ~(IRQ15  & SERIRQF ) &
            ~( (DevB:3x56[3:0]   == 4'hF) | (DevB:3x56[7:4]  == 4'hF) | (DevB:3x56[11:8] == 4'hF)
             | (DevB:3x56[15:12] == 4'hF) | (DevB:3x44[11:8] == 4'hF) | (DevB:3x44[7:4]  == 4'hF)
             | (DevB:3x44[3:0]   == 4'hF) | (DevB:3x42[3:0]  == 4'hF) | DevB:1x08[10]);

PIC_IRQx  = ~(ISA_IRQx | PCI_IRQx  | PNP_IRQx  | SCI_IRQx );
```

Where:

| | |
|---|---|
| x | The PIC IRQ number, 1, 3 through 7, 9 through 12, 14, and 15. |
| PIRQ[A,B,C,D]# | The input PCI interrupts (with the polarity of the external signals). |
| SERINT[y] | The PCI interrupts captured from the SERIRQ pin (with the same polarity as the SERIRQ pin). |
| SERIRQ[x] | The ISA interrupts captured from the SERIRQ pin (with the same polarity as the SERIRQ pin). |

| | |
|---|---|
| USB0_IRQ[12,1] | Outputs of the keyboard emulation logic from the USB controller. |
| EKIRQ[12,1] | External keyboard controller's interrupts from IRQ1 and IRQ12 when the interrupt function is selected by GPIO12 and GPIO15. |
| PNPIRQ[2:0] | PNP IRQ pins (with the polarity specified by the associated GPIO control register). |
| SCI_IRQ | Active-High SCI interrupt. |
| IRQx | External interrupt. |
| PIC_IRQx | The interrupt signals that go to the PIC. |

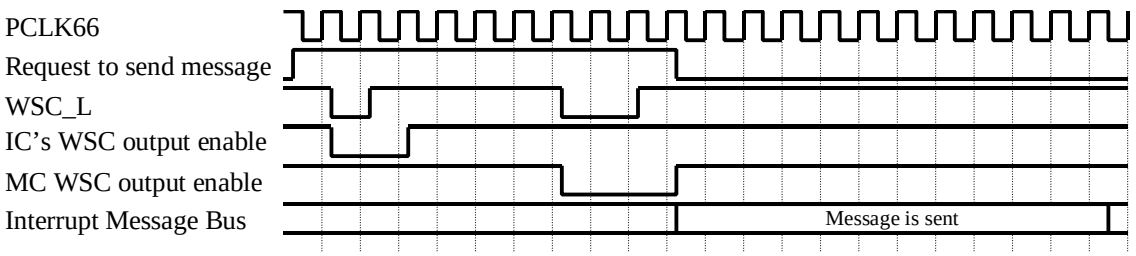
Notes from the interrupt routing equations:
- When a PCI, PNP, or SCI interrupt is enabled onto a PIC_IRQ, then the external and serial IRQ capability for the IRQ is disabled.
- External IRQs and serial IRQs are expected to be edge triggered.
- PCI pin and SCI interrupts are intended to be level triggered.
- PNP interrupts can be level or edge triggered. The inverter available in the GPIO control register must be used to preserve the polarity from the external signal to the PIC; if this inverter is not selected, then there will be an inversion from the external signal to the PIC.
- IRQ14 and IRQ15 change from external interrupts to native mode interrupts driven by the IDE drives if DevB:1x08[8 and 10] are set respectively. As native mode interrupts, they are still expected to be active High (externally); they are combined with PIRQA# logic to become level-triggered, active-Low signals into the PIC.
- The keyboard and mouse interrupt pins, IRQ1 and IRQ12, are ANDed with the serial IRQ versions to go to the USB keyboard emulation logic. The outputs of this logic enter the routing equations.
- In order for the USB keyboard and mouse emulation interrupts to function properly, either the IRQ1 and IRQ12 pins must both be strapped Low or an external keyboard controller must keep the serial IRQ slots for IRQ1 and IRQ12 Low.

#### 4.4.2.2 IOAPIC

The IOAPIC supports 24 interrupt signals that come from the interrupt routing logic, the PCI interrupts, GPIOs, and internal signals. When enabled, it sends interrupt messages through the 3-wire interrupt message bus (IMB).

##### 4.4.2.2.1 WSC#

The WSC# signal is used to insure that upstream posted writes are visible to the host prior to interrupt message transmission over the IMB. It connects between the IC and the system memory controller. It is enabled when the IOAPIC is enabled (DevB:0x4B[APICEN]). The IC requests that the memory controller guarantee that the upstream posted write transactions in its data buffers are visible to the host by placing a single-PCLK66 pulse on WSC#. When all the posted writes that were in the memory controller when the first pulse was detected are visible to the host, then the memory controller responds with a two-PCLK66 pulse back to the IC. After this is received, the IC transmits the interrupt message over the IMB.




The IC enables WSC# during the PCLK66 cycle in which it drives WSC# Low and the following cycle in which WSC# is driven High. It is expected that the memory controller enables the line for three PCLK66 cycles. WSC# is required to be driven High for at least one clock before it is allowed to be driven Low again.

#### 4.4.2.2.2 IOAPIC Redirection Registers

The IOAPIC supports 24 interrupt request signals. Each interrupt request input is combined with its corresponding redirection register to specify the behavior of the interrupt. These interrupt request signals are connected to redirection registers (APIC IRQs) as shown in the following table.

| APIC IRQ | Connection | APIC IRQ | Connection |
|---|---|---|---|
| 0 | PIC INTR output | 12 | PIC IRQ12 |
| 1 | PIC IRQ1 | 13 | PIC IRQ13 (floating-point error) |
| 2 | PIC IRQ0 (PIT) | 14 | PIC IRQ14 |
| 3 | PIC IRQ3 | 15 | PIC IRQ15 |
| 4 | PIC IRQ4 | 16 | PIRQA# |
| 5 | PIC IRQ5 | 17 | PIRQB# |
| 6 | PIC IRQ6 | 18 | PIRQC# |
| 7 | PIC IRQ7 | 19 | PIRQD# |
| 8 | PIC INT8 (RTC) | 20 | GPIO28 |
| 9 | PIC IRQ9 | 21 | GPIO29 |
| 10 | PIC IRQ10 | 22 | GPIO30 |
| 11 | PIC IRQ11 | 23 | GPIO31 |

See Section 4.4.2.1 for the definition of the "PIC IRQ" signals. See DevB:0x4B[MPIRQ] for a description of how the mask bits from redirection table entries 20 to 23 can affect the routing of GPIO[31:28] onto PIRQ[D:A]#. See DevB:3x44[TCO_INT_SEL] for a description of how other interrupts may be directed to the IOAPIC.

#### 4.4.2.3 NMI

NMI is controlled as described in the following equation:

```
NMI      = ~PORT70[NMIDIS] &
           (  PM48[NMI_NOW]
           | ~PM48[NMI2SMI_EN] &
             (  PORT61[SERR] &         ~PORT61[CLRSERR]
             |  PORT61[IOCHK] &        ~PORT61[CLRIOCHK]
             |  DevB:0x40[NMIONERR] &  [status bits described in Section 4.1.2]
             |  DevA:0x1C[MDPE] &       DevA:0x3C[PEREN] ) );
```

### 4.4.3 Real-Time Clock (Logic Powered by VDD_AL)

The real-time clock logic requires an external 32-KHz oscillator. It includes a clock and calendar timer, an alarm (which generates an interrupt), and 256 bytes of non-volatile RAM. It is register compatible with the legacy PC real-time clocks. It meets ACPI real-time clock requirements. The real-time clock resides on the VDD_AL power plane.

## 4.5 Enhanced IDE Controller

The enhanced IDE controller support independent primary and secondary ports. Each port supports two drives. Supported protocols include PIO modes 0-4, multi-word DMA, ultra DMA modes through to ATA-100.

The IDE ports can be individually controlled via DevB:1x54 such that the drives can be powered down.

## 4.6 USB Controller

The USB Controller is an implementation of the *Open Host Controller Interface Specification Version 1.1* containing a host controller core, a 4-port root hub, and hardware traps for legacy keyboard and mouse emulation.

### 4.6.1 USB Interrupts

The USB interrupt signal normally drives the PCI interrupt PIRQD# Low. However, it can be diverted to SMIs by the OHCI-defined register HcControl_InterruptRouting. See Section 4.4.2.1 for data on routing of keyboard and mouse emulation interrupts. SMI interrupts are also generated in response to accesses to IO ports 60h and 64h and to IRQ1 and IRQ12 in support of the emulation logic.

# 4.7 System Management Logic

System management includes logic for most of the multiplexed-function pins—such as general-purpose IO (GPIO) pins, the power management (PM) pins, system management bus (SMBus) pins, the processor interface pins, and the plug and play (PNP) interrupt pins—as well as the logic required for ACPI-compliant power management for desktop and mobile systems. Programmable register access to most of this logic is contained in the DevB:3xXX configuration space and the PMxx IO space. Here are the major functions:

- ACPI interrupt (SCI or SMI based on the state of PM04[SCI_EN] status bits and enables
- SMI status bits and enables
- System power state machine (SPSM)
- Resume event logic (to place the SPSM into the full-on state)
- SMBus
- System power state control pins and general purpose pins
- Device monitors (hardware traps; interrupt traps; DMA request traps; re-trigger timers)
- System inactivity timer
- Serial IRQ logic

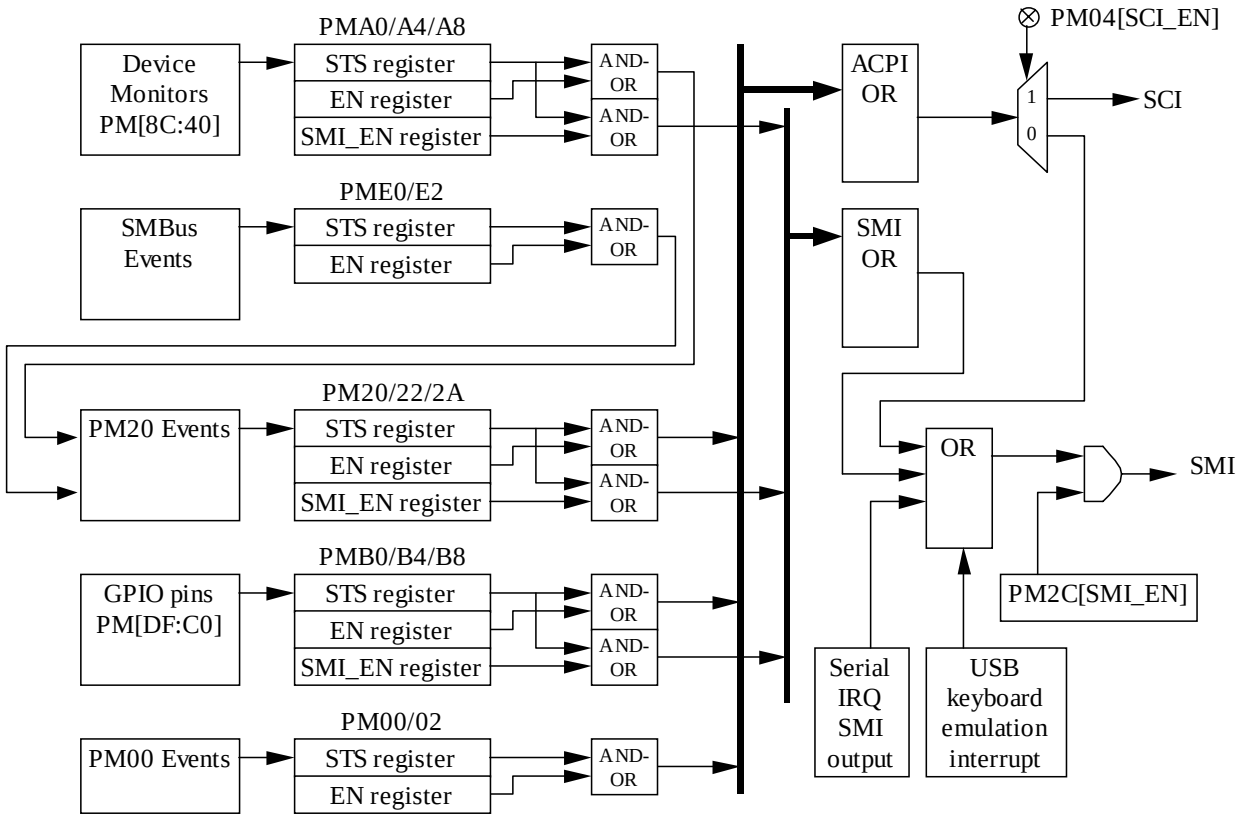
## 4.7.1 Power Management

The following table summarizes all the system management events that can be detected by the system management logic and the hardware response enable registers. The columns are: SCI/SMI Parent STS/EN, where the status and enable bits for ACPI interrupts are accessible; and SMI-only STS/EN, where the status and enable bits for SMI interrupts are accessible.

| Events | SCI/SMI Parent STS/EN | SMI-Only STS/EN | Notes; Other Functions |
|---|---|---|---|
| OS release (PM04[GBL_RLS]) | | PM28/2A | SMI only |
| BIOS release (PM2C[BIOS_RLS]) | PM00/02 | | SCI only |
| Software SMI via PM1E, PM2F | | PM28/2A | SMI only |
| Device monitors; GP timer time out | PM20/22 | PMA0/A8 | See PM[8C:50] for definitions; child STS/EN bits in PMA0/A4 |
| System inactivity timer time out | PM20/22 | PM20/2A | See PM98 for SIT; reload registers in PM[8C:50] and PMAC |
| ACPI timer overflow | PM00/02 | | SCI only |
| SMBus events | PM20/22 | PM28/2A | Child STS/EN bits in PME0/E2 |
| USB bus resume event | PM20/22 | PM20/2A | |
| Power button override | PM00 | | No SCI; PM26 control only used to go to SOFF |
| TCO events | PM20/22 | PM28/2A | |
| Miscellaneous SMI events | | PM30/32 | |
| PIC INTR signal (unmasked IRQs) | | | Reload SIT via PMAC; also causes C2/C3 resume; POS resume via PM28/2A |
| Real-time clock IRQ | PM00/02 | | SCI only |
| NMI to processor | | | Reload SIT via PMAC; also causes C2/C3/POS resume |
| INIT to processor | | | Reload SIT via PMAC; also causes C2/C3/POS resume |
| SMI to processor | | | Also causes C2/C3/POS resume |
| PCI bus masters | PM00 | | Resumes from C3 with no SCI; reload SIT via PMAC; re-trigger timer via PM54 |
| 32 GPIO inputs | PMB0/B4 | PMB0/B8 | |
| PWRBTN# pin | PM00/02 | PM00/2A | |
| EXTSMI# pin | PM20/22 | PM002A | |
| PME# pin | PM20/22 | PM20/2A | |
| RI# pin | PM20/22 | PM20/2A | |
| SLPBTN# pin | PM00/02 | PM00/2A | |
| THERM# pin | PM20/22 | PM20/2A | |
| LID pin | PM20/22 | PM20/2A | |
| ACAV pin | PM20/22 | PM20/2A | |

### 4.7.1.1 SCI and SMI Control

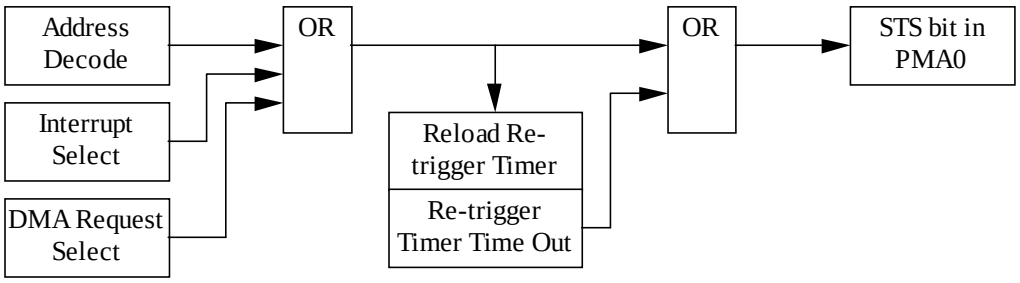
System management events cause corresponding STS registers to be set. STS registers can be enabled to generate SCI and SMI interrupts. The following diagram shows how the STS registers are routed to the interrupts.




The “AND-OR” boxes in the middle of the diagram specify the logical AND of the STS and EN registers (or STS and SMI_EN registers, as the case may be) the results of which are logically ORed together; for example: (STS1 & EN1) | (STS2 & EN2)... All enabled ACPI interrupts may be routed to either SCI or SMI interrupts by PM04[SCI_EN]. Or these STS registers may be routed directly to SMI through the SMI_EN registers, regardless of the state of PM04[SCI_EN]. The USB controller and serial IRQ logic also provide sources of SMI that is ORed into the logic. SMI and SCI are inputs to the interrupt routing logic; see Section 4.4.2.

### 4.7.1.2 Device Monitors and Re-Trigger Timers

Device monitors consist of a set of registers that may be used to enable traps on transactions, interrupts, DMA activity, and device inactivity. Each monitor circuit includes transaction decode logic, optional interrupt and DMA channel enables, a re-trigger timer that gets reloaded every time the monitored event occurs, and enable bits for passing events to SCI or SMI interrupts. Interrupt device monitor events occur whenever the monitored interrupt signal changes state (High to Low or Low to High). DMA device monitor events occur whenever the monitored DMA request signal (to the legacy 8237 DMA controller from the LPC interface logic) is asserted.




#### 4.7.1.2.1 Traps

Configuration registers DevB:3x[D8:B4] specify several traps for memory, IO, and configuration space address ranges. These traps are generated for the specified transactions that (1) are targeted at the IC or any device on or behind the secondary PCI bus or any devices on the LPC bus, (2) are not targeted to the configuration space or IO space of the IDE controller, and (3) are not targeted at any of the DevA:0x[FF:C0] configuration registers.

### 4.7.1.3 System Inactivity Timer

Any of the hardware traps, IRQ lines, or PCI bus master activity can be enabled to reload the system inactivity timer (SIT). If the SIT decrements to zero, then an interrupt is generated, if enabled.

### 4.7.1.4 Throttling Logic

When throttling, the IC repetitively places the processor into the Stop Grant state for a specified percentage of time in order to reduce the power being consumed by the processor. STPCLK# is used to control the processor Stop Grant state with a period specified by DevB:3x40[NTPER, TTPER] and a duty cycle specified by DevB:3x40[THMINEN], DevB:3x4D and PM10.

Two types of throttling are possible: normal and thermal. Normal throttling is controlled by software. Thermal throttling is controlled by the THERM# pin (see also DevB:3x40[TH2SD]). If both are enabled simultaneously, then the duty cycle specified for thermal throttling is used. Throttling is only possible when in the FON state. If throttling is enabled when entering other states, then it will stop; after exiting the state, throttling will resume.

#### 4.7.1.5 System Power State Controller (SPSC)

The system power state controller (SPSC) supports the following system power states:

| System Power State | VDD3, VDD_CORE | VDD_AUX | VDD_RTC, VDD_AL |
|---|---|---|---|
| Full on (FON) | On | On | On |
| C2 | On | On | On |
| C3 | On | On | On |
| Power on suspend (POS; S1) | On | On | On |
| Suspend to RAM (STR; S3) | Off | On | On |
| Soft off (SOFF; S5); suspend to disk (STD; S4) | Off | On | On |
| Mechanical off (MOFF; G3) | Off | Off | On |

**Mechanical off (MOFF or ACPI G3 state).** MOFF is the state when only VDD_AL is powered. This can happen at any time, from any state, due to the loss of power to the VDD_AUX planes (e.g., a power outage, the power supply is unplugged, or the power supply's mechanical switch is thrown). When power is applied to VDD_AUX, then the system transitions to either FON or SOFF.

**Soft off (SOFF or ACPI G2/S5 states).** In the SOFF state, the system appears to the user to be off. The IC's VDD_AUX planes are powered, but the main supplies are not; RPWRON is Low to disable power system DRAM. The system normally uses PWRBTN# to transition from SOFF to FON. The IC also allows SMBus activity, USB resume events, the real-time clock alarm, the EXTSMI# pin, the SLPBTN# pin, the PME# pin, the LID pin, and the ACAV pin to be enabled to cause this transition.

**Suspend to disk (STD or ACPI S4 state).** The IC's behavior in this state equivalent to SOFF.

**Suspend to RAM (STR or ACPI S3 state).** In the STR state, the system's context is stored in system memory (which remains powered; RPWRON is High) and the main power supplies are shut off (PWRON# High). The IC's behavior in the STR state is similar to SOFF; the main difference is that RPWRON is asserted in STR.

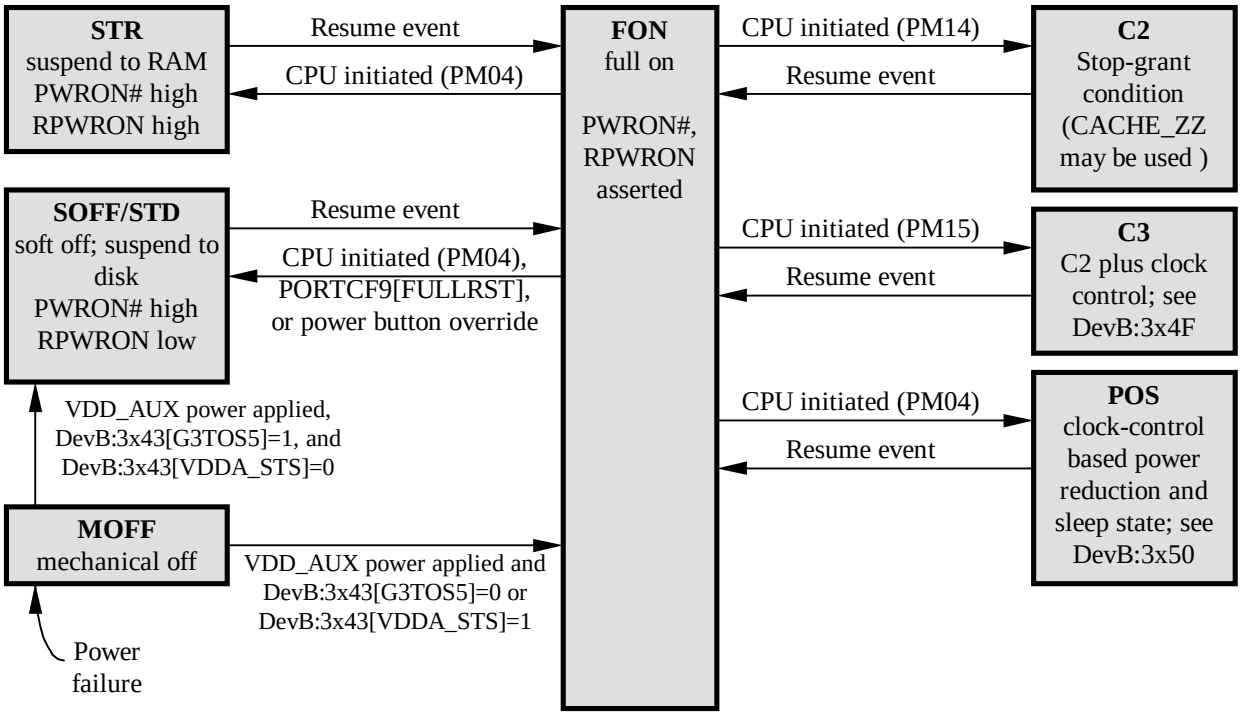
**Power on suspend (POS or ACPI S1 state).** All power planes to the IC are valid in POS. Signal control during POS is specified by DevB:3x50.

**Snoop-capable clock control (C2).** In C2, the processor is placed into the Stop Grant state. Signal control during C2 is specified by DevB:3x4F. It is expected that the processor's cache may be snooped while in this state.

**Snoop-disabled clock control (C3).** In C3, the processor is placed into the Stop Grant state such that the processor's cache cannot be snooped; requests that result in snoops are resume events (see PM04[BM_RLD]). Signal control during C3 is specified by DevB:3x4F.

**Full on (FON).** In FON, all the power planes are powered and the processor is not in the Stop Grant state.

The following figure shows the system power state transitions.




#### 4.7.1.5.1 Summary of Resume Events

In general, resume events occur when there is an event that sets a status bit while the ACPI interrupt enable for that status bit is active.

**MOFF:** no resume events.

**SOFF/STR/STD:** resume events are those enabled by registers PM22[RI_EN, PME_EN, ACAV_EN, LID_EN, SMBUS_EN, USBRSM_EN, EXTSMI_EN, AC97_EN], PM02[PWRBTN_EN, SLPBTN_EN, RTC_EN]. Also, PM26[BATLOW_CTL] can be used to inhibit the resume.

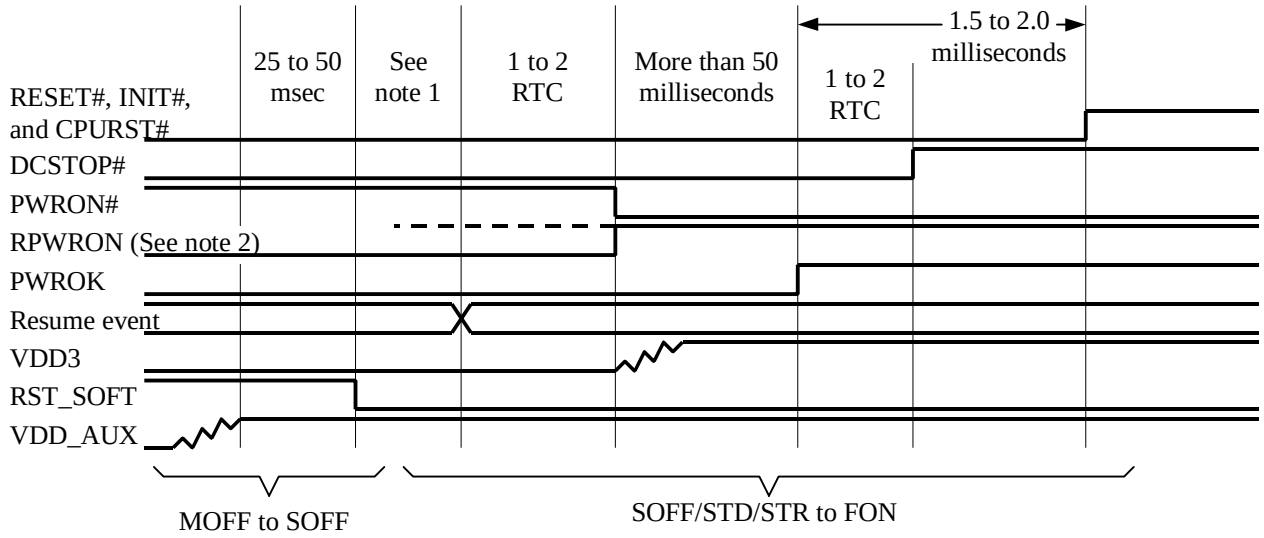
**POS:** resume events are those enabled by registers PM02, PM22, PMA4 or PMB4. Also, PM2A[IRQ_RSM] enables an additional resume event. Also, PM26[BATLOW_CTL] can be used to inhibit the resume.

**C2:** resume events are the same as for POS, except PM2A[IRQ_RSM] is not included and PM26[BATLOW_CTL] does not inhibit the resume. In addition, any unmasked interrupts (INTR, the output of the PIC), an NMI interrupt, an INIT interrupt, or an SMI interrupt will cause a resume event.

**C3:** resume events are the same as for C2. In addition, PM04[BM_RLD] enables a resume event.

#### 4.7.1.5.2 Transitions between MOFF/SOFF/STD/STR and FON

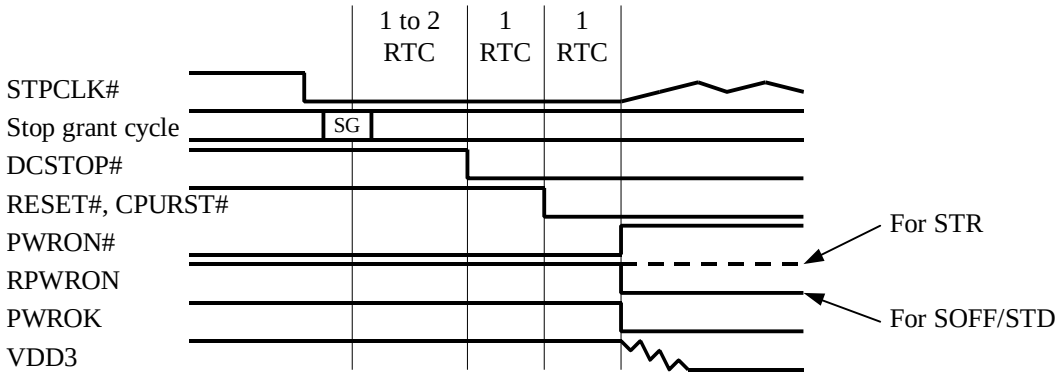
In the following timing diagrams, RTC refers to 32-KHz clocks cycles.




**MOFF to SOFF/STD/STR to FON**

Note 1: If DevB:3x43[G3TOS5] = 0, then the time from the end of RST_SOFT to PWRON# assertion is 1 to 2 RTC clocks. If DevB:3x43[G3TOS5] = 1, then the resume event must occur before PWRON# is asserted.

Note 2: RPWRON# is High during STR and Low during STD and SOFF.




**FON to SOFF/STD/STR**

For transitions to SOFF that are initiated by a power/sleep button override event or by a PORTCF9[FULL-RST], the STPCLK# assertion and Stop Grant cycles are skipped; the sequence starts with the assertion of DCSTOP#.

#### 4.7.1.5.3 Transitions From FON to C2/C3

DevB:3x4F specifies the enabled functions for transitions to C2 and C3. Here are the steps to enter C2/C3:

- **Processor initiation.** Software initiates the transition to C2 by reading PM14 or to C3 by reading PM15.
- **Stop Grant.** The IC asserts STPCLK# and then waits for the Stop Grant cycle from the host to be completed. This completes the transition to C2; the remaining steps only apply to the transition to C3. .
- **CACHE_ZZ.** At least four PCLK cycles after Stop Grant, CACHE_ZZ is asserted, if it is enabled for C3.
- **CPUSLEEP#.** At least 64 PCLK cycles after Stop Grant, CPUSLEEP# is asserted, if it is enabled for C3.
- **CPUSTOP#.** At least 96 PCLK cycles after Stop Grant, CPUSTOP# is asserted, if it is enabled for C3.

#### 4.7.1.5.4 Transitions From C2/C3 to FON

The following is the resume sequence from C2/C3, once an enabled resume event occurs. Note: if CPUSTOP# and CPUSLEEP# are not enabled to be asserted in C3 by DevB:3x4F, then the C3 resume sequence starts from "CACHE_ZZ" below; if either of these are set, then the sequence starts from "CPUSTOP#" below:

- **CPUSTOP#.** CPUSTOP# is deasserted immediately after the resume event (C3 only).
- **CPUSLEEP#.** Up to one millisecond after the resume event (as specified by DevB:3x54), CPUSLEEP# is deasserted.
- **CACHE_ZZ.** At least 4 PCLK cycles after CPUSLEEP#, CACHE_ZZ is deasserted. Note: if CPUSTOP# and CPUSLEEP# are not enabled to be asserted in C3 by DevB:3x4F, then the C3 resume sequence starts from this step.
- **STPCLK#.** At least 4 PCLK cycles after CACHE_ZZ, STPCLK# is deasserted.

#### 4.7.1.5.5 Transitions From FON to POS

DevB:3x50 specifies the enabled functions for transitions to POS. The transition to POS occurs as follows, for each of the enabled pin controls:

- **Processor initiation.** Software initiates the transition to POS by writing the appropriate value to PM04[SLP_TYP, SLP_EN].
- **Stop Grant.** The IC asserts STPCLK# and then waits for the Stop Grant cycle from the host to be completed.
- **DCSTOP#.** Eight PCLK cycles after Stop Grant, DCSTOP# is asserted.
- **CPUSLEEP#.** At least 64 PCLK cycles after Stop Grant, CPUSLEEP# is asserted.
- **AGPSTOP#, CPUSTOP# and PCISTOP#.** At least 96 PCLK cycles after Stop Grant, AGPSTOP#, CPUSTOP# and PCISTOP# are asserted.
- **SUSPEND#.** At least 128 PCLK cycles after Stop Grant, the SUSPEND# pin is asserted.

#### 4.7.1.5.6 Transitions From POS to FON

The following is the resume sequence, once an enabled resume event occurs, if the SUSPEND# pin is utilized:

- **SUSPEND#.** Immediately after the resume event, the SUSPEND# pin is deasserted along with CPUSLEEP#. Enabled reset signals are asserted at this time as well.
- **AGPSTOP#, CPUSTOP# and PCISTOP#.** 17 to 18 milliseconds after SUSPEND#, AGPSTOP#, CPUSTOP# and PCISTOP# are deasserted.
- **DCSTOP#.** Up to 1 millisecond after AGPSTOP#, CPUSTOP# and PCISTOP (as specified by DevB:3x54), DCSTOP# is deasserted.
- **STPCLK#.** One C32KHZ cycle after DCSTOP#, STPCLK# is deasserted.

The following is the resume sequence, once an enabled resume event occurs, if the SUSPEND# pin is not utilized, but DCSTOP#, AGPSTOP#, PCISTOP#, CPUSLEEP, or CPUSTOP# is utilized:

- **AGPSTOP#, CPUSTOP# and PCISTOP#.** AGPSTOP#, CPUSTOP# and PCISTOP# are de-asserted immediately after the resume event.
- **DCSTOP#.** Up to 1 millisecond after the resume event (as specified by DevB:3x54), DCSTOP# and CPUSLEEP# are de-asserted.
- **STPCLK#.** One C32KHZ cycle after DCSTOP#, the STPCLK# is deasserted.

The resume sequence, once an enabled resume event occurs, if the SUSPEND#, AGPSTOP#, PCISTOP#, CPUSTOP#, CPUSLEEP, and DCSTOP# pins are not utilized consists only of the transition out of Stop Grant.

## 4.7.2 Serial IRQ Protocol

The IC supports the serial IRQ protocol. This logic controls the SERIRQ pin and outputs IRQs to the PIC and IOAPIC blocks. This logic runs off of PCLK. It is specified by DevB:3x4A. The serial IRQ logic does not provide support for generating IRQ0, IRQ2, IRQ8, or IRQ13. In order to use IRQ[15, 14, 12, 6, or 1], the corresponding external IRQ pin must be pulled High. The PCI IRQs from the serial IRQ logic are routed to the interrupts specified by DevB:3x56; they are not routed to the IOAPIC.

## 4.7.3 SMBus

The IC includes a system management bus (SMBus) interface. SMBus is a two-wire serial interface typically used to communicate with system devices such as temperature sensors, clock chips, and batteries. The control registers for this bus are PME0 through PMEF.

The SMBus interface includes a host controller and a host-as-slave controller.

**Host controller.** The host controller is used to generate cycles over the SMBus as a master. Software accomplishes this by setting up PME2[CYCTYPE] to specify the type of SMBus cycle desired and then (or concurrently) writing a 1 to PME2[HOSTST]. This triggers an SMBus cycle with the address, command, and data fields as specified by the registers called out in PME2[CYCTYPE].

Writes to the host controller registers PME2[3:0], PME4, PME8, and PME9 are illegal while the host is busy with a cycle. If a write occurs to PME2 while PME0[HST_BSY] is active, then the four LSBs be ignored. Writes to PME4, PME8, and PME9 while PME0[HST_BSY] is active are ignored (the transaction is completed, but no data is transferred to the SMBus controller).

If an SMBus-defined time out occurs while the host is master of the SMBus, then the host logic will attempt to generate a SMBus stop event to clear the cycle and PME0[TO_STS] will be set.

The host controller is only available in the FON state.

**Host-as-slave controller.** The host-as-slave controller responds to word-write accesses to either the host address specified by PMEE or the snoop address specified by PMEF. In either case, if the address matches, then the subsequent data is placed in PMEC and PMEA. In the case of snoop address accesses, the command information is stored in PMEC[7:0] and the data is stored in PMEA[15:0]. In the case of host address accesses, the device's address is stored in PMEC[7:1] if the transaction includes a 7-bit address, or PMEC[15:1] if the device has a 10-bit address. After the address match is detected, the logic waits for the subsequent stop command before setting the appropriate status bits in PME0[HSLV_STS, SNP_STS]; however, if a time out occurs during the cycle, after the address match is detected, then the appropriate bit in PME0 (HSLV_STS or SNP_STS) is set.

If one of the slave status bits, PME0[HSLV_STS, SNP_STS], is already set and then another access to the host-as-slave controller is initiated, then the later access will not be acknowledged (via the first SMBus acknowledge cycle) until the status bit is cleared.

The host-as-slave controller operates in all system power states except MOFF; it can be used to generate interrupts and resume events.

**SMBALERT.** The host controller includes support for the SMBALERT# signal. If this signal is asserted in the FON state, an interrupt will result, and it is expected that software determines the source of the alert by generating a host read cycle to the alert response address, 0001100b. If the SMBus host controller detects this address for a read cycle with PME2[CYCTYPE] set to receive byte (001b), then it will store the address returned by the SMBALERT# slave in PME6[7:0]. If bits[7:1] of this address are 1111_0xxb, indicating a 10-bit address, then it will store the next byte from the slave in PME6[15:8].

## 4.7.4 Plug and Play IRQs

The IC supports three PNP IRQs. The register that specifies these is DevB:3x44. The PNPIRQ[2:0] pins are multiplexed with GPIO functions; the control registers that specify the functions (PMD3, PMD4, and PMD5) must be set up appropriately for the PNP functions to operate.

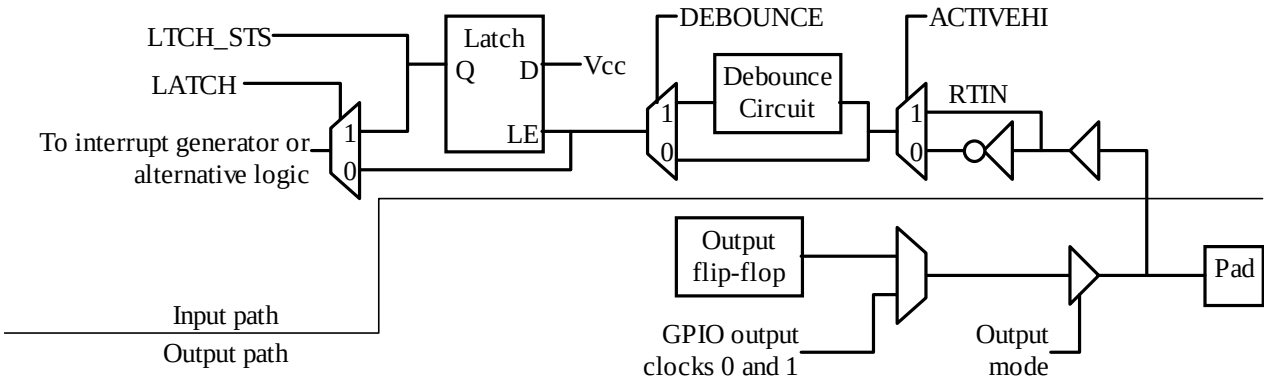
## 4.7.5 General Purpose IO

The general-purpose IO pins, GPIO[31:0], can be assigned to be inputs, outputs, interrupt generators, or bus controls. These pins can be programmed to be general-purpose IO or to serve alternate functions; see the PM[DF:C0] register definitions. Most of these pins are named after their alternate functions. There is one control register for each pin, PM[DF:C0]. IRQ status and enables are available for each pin in registers PMB0 and PMB4; SMI enables are available in PMB8.

**General-purpose IO functions.** When programmed as a GPIO pin, the following functions are available:

- Outputs.
  - Can be set High or Low.
  - Can be controlled by GPIO output clocks 0 or 1 (see PMBC).
- Inputs.
  - Active High or active Low programmable.
  - SCI or SMI IRQ capable.
  - Can be latched or not latched.
  - Inputs can be debounce protected.

The following diagram shows the format for all GPIO pins. The input path is not disabled when the output path is enabled or when the pin is used for an alternate function.




**Debounce.** The input signal must be active and stable for 12 to 16 milliseconds before the output signal will be asserted.

**GPIO output clocks.** There are two GPIO output clocks numbered 0 and 1. Their behavior is specified by PMBC. Each output clock includes a 7-bit programmable High time, a 7-bit programmable Low time, and the counter can be clocked by one of four frequencies. Here are the options:

| PMBC[CLK[1,0]BASE] | Base Clock Period | Output High Time Range | Output Low Time Range |
|---|---|---|---|
| 00b | 250 microseconds | 250 µs to 32 ms | 250 us to 32 ms |
| 01b | 2 milliseconds | 2 ms to 256 ms | 2 ms to 256 ms |
| 10b | 16 milliseconds | 16 ms to 2 seconds | 16 ms to 2 seconds |
| 11b | 128 milliseconds | 128 ms to 16.4 seconds | 128 ms to 16.4 seconds |

The output of the two GPIO output clocks can be selected to drive the output of any of the GPIO pins. They may be used to blink LEDs or for other functions.

# 4.8 AC ’97 Controller

## 4.8.1 Introduction

The AC’97 host controller supports the following features:

- Independent PCI functions for audio (function 5, address space DevB:5xXX) and modem (function 6, address space DevB:6xXX).
- Independent channels for PCM In, PCM Out, Microphone In, Modem In, Modem Out.
- 2-channel stereo for PCM Audio In; 2-channel stereo for PCM Audio Out.
- Left and right audio channels.
- 16 bit sample resolution.
- Multiple sampling rates.
- Up to two codecs.

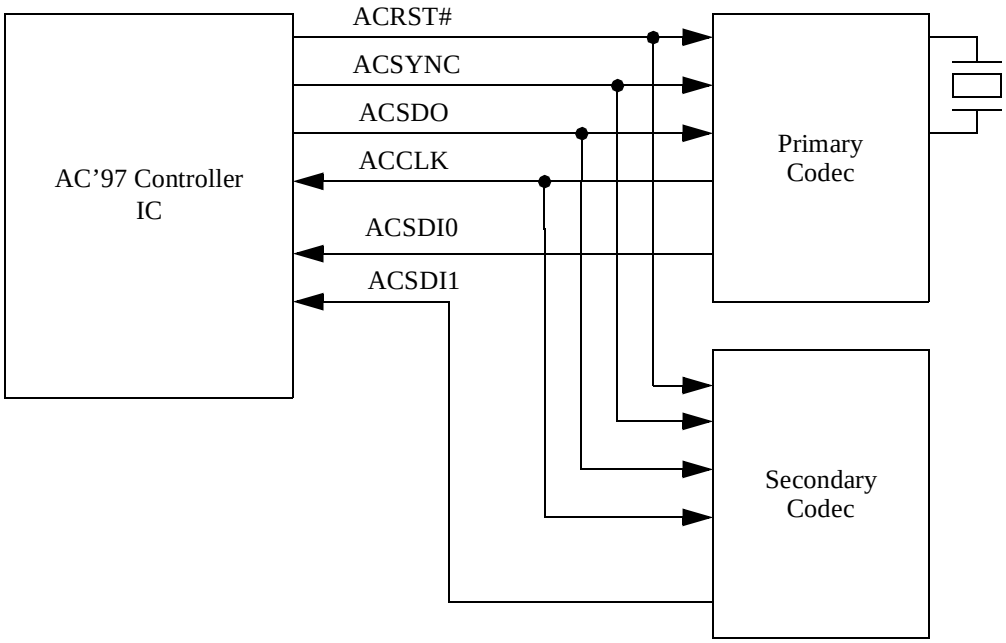
The AC '97 sub-system includes the digital controller that resides within the IC and a set of up to two external codecs: the audio codec (AC) and the modem codec (MC).

The AC’97 controller does not distinguish between primary and secondary codec. Since registers are specific to ACSDIN0 and ACSDIN1 for reporting wake events, codec status etc., however, the documentation is written with the presumption that the primary codec is attached to ACSDIN0 and the secondary codec is attached to ACSDIN1.

Supported codec configurations are:
- AC as primary.
- MC as primary.
- AC as primary and MC as secondary.
- AMC as primary.

The IC does not support optional test modes outlined in the AC’97 specification.

AC’97 Codec Connections:




## 4.8.2 AC’97 Serial Link Interface

The AC’97 serial link interface is AC '97 revision 2.1 compliant. It consists of six interface signals between the controller and the codec.

When mono audio sample streams are output from the IC, it is required that both left and right sample stream slots are filled with the same data; i.e., both slots are transmitted to the codec in the same output frame. For input frames, the appropriate request bits for both slots are required to be set and cleared in tandem.

The IC supports up to two ACSDIN signals for use with a primary and secondary codec. Depending on which codec (AC, MC, AMC) is attached, various input slots will be valid or invalid. With the exception of the input tag slot 0, these input slots must be mutually exclusive; i.e., no two data slots at the same location may be valid on both input signals. This precludes the ability to implement two similar codecs (e.g. two ACs or MCs) that use the same data slots.

The codec ready bit, bit 15 of input slot 0, indicates whether the codec on the AC-link is ready for normal operation. The codec ready bits from input slots 0 at ACSDIN0 and ACSDIN1 are visible through the Global Status controller register, AC30.

Output slot 1 provides a command port to control features and monitor status of the AC’97 codec. The controller supports read-write access to a maximum of 64 16-bit codec registers, addressable on even byte boundaries. Only even register addresses are valid.

The input slot 1 tag bit in input slot 0 only pertains to the Control Register Index data from a previous read. Slot request bits are always valid and therefore must be checked independent of the slot 1 tag bit.

The IC supports transmission of GPIO values to the codec in output slot 12. The values of the bits in this slot are the values written to the GPIO Pin Status modem mixer register at offsets 54h and D4h. The following rules govern the usage of slot 12.

- Slot 12 is marked invalid by default out of reset and remains invalid until a GPIO Pin Status modem mixer register write.
- GPIO Pin Status modem mixer register writes cause the write data to be transmitted in slot 12 in the next possible frame with slot 12 marked valid and the address/data information transmitted in slots 1 and 2 of the same frame.
- After the first GPIO Pin Status modem mixer register write, slot 12 remains valid for all subsequent frames. The data transmitted in slot 12 is the data last written to the GPIO Pin Status modem mixer register. Any subsequent write to the register will cause the new data to be transmitted in the next frame.
- Slot 12 is invalidated again after any of the following events: AC'97 cold reset; AC'97 warm reset; any RESET# assertion.

The contents of the GPIO Pin Status modem mixer register is expected to be returned in slot 12 of every input frame. Reads from the GPIO Pin Status modem mixer register at offset 54h/D4h are not transmitted across the link. The data from the most recent slot 12 is stored in a controller shadow register and is returned instead. This data is also accessible in MC48.

When accessing codec mixer registers, only one IO cycle may be pending across the AC-link at any time. The IC provides arbitration logic to ensure this. The CAS bit in the Codec Access Semaphore register, AC34, is provided to allow software to determine if a codec access is in progress. However, the GPIO Pin Status codec register may be read at any time. Accesses of the GPIO Pin Status register do not reset the affect the CAS bit.

The controller does not issue back to back reads. It must respond to the first read before it will accept a second.

### 4.8.3 AC '97 PCI Interface and Bus Master Controller

The AC'97 controller is a host bus master with scatter/gather support. The bus master interface has the following characteristics:

- In response to host reads of a codec, the controller presumes the codec will respond within the next frame; after which, if no response is received, it will complete the transaction to the processor with data of FFFFh and also set the Read Completion Status bit in the Global Status Register, AC30. If ACCLK is detected to be invalid, the same response occurs immediately (with data of FFFFh and AC30[RCSTAT] set). In response to host writes to a codec, the controller returns a write completion to the processor after the write data is inserted into a frame to the codec. If ACCLK is detected to be invalid, the transaction is completed immediately.

- Audio and modem interrupts generated by the AC '97 controller are connected to one PCI interrupt request. See Section 4.4.2.1 for a description of interrupt routing. The following table shows all AC'97 interrupt sources.

| Interrupt Register Bit | Enable Register Bit | Interrupt |
|---|---|---|
| ACx6/MCx6[BCIS] | ACxB/MCxB[IOCE] | Scatter/gather host memory buffer completion interrupt Status |
| ACx6/MCx6[FIFOERR] | ACxB/MCxB[FEIE] | FIFO over-run or under-run error |
| ACx6/MCx6[LVBCI] | ACxB/MCxB[LVBCIEN] | Last valid buffer completion interrupt |
| AC30/MC40[SRINT] | AC2C/MC3C[SRIEN] | Secondary resume interrupt |
| AC30/MC40[PRINT] | AC2C/MC3C[PRIEN] | Primary resume interrupt |
| AC30/MC40[GPIINT] | AC2C/MC3C[GPIIEN] | GPI interrupt |

The principal function of the scatter/gather bus master unit is to assist the operating system in managing memory fragmentation. One logically contiguous buffer is split among multiple physical blocks or pages of host memory. A logical buffer is mapped to physical host memory pages using the descriptor table that is pointed to by the Buffer Descriptor List Base Address register. Each descriptor table entry contains the physical memory address of the host memory page, the length of the page, and other information. Descriptor tables have up to 32 entries. Host memory page sizes of up to 65536 samples are supported. The descriptor format is provided in the following table.

| Bit | Description |
|---|---|
| 63 | **IOC: Interrupt on Completion.** When set, indicates that an interrupt should be generated upon completion of data transfer to/from the host memory page buffer. |
| 62 | **BUP: buffer under-run Policy.** When set, the controller transmits zeros in the case that this buffer is completed and the last valid buffer has been processed. Otherwise the controller transmits the last valid sample. This bit typically is only set for the last buffer in the stream. |
| 61:48 | Reserved. |
| 47:32 | **Length.** Length of host memory page buffer in 16-bit words. |
| 31:1 | **BASE_ADDR.** Bits[31:1] of the base address of the host memory page buffer. |
| 0 | Reserved. |

The Current Index Value (CIV) provides the current descriptor being processed. This value is one greater than the value provided in the Last Valid Index (LVI) register. It will roll over from index 31 to index 0. To allow a roll-over, the descriptor table must utilize 32 valid entries. No roll-over from an index less than 31 is possible. Other than a roll-over, the CIV value may only be set to a value of 0 by applying reset to the AC'97 controller.

After reset, the first descriptor at index 0 is prefetched, as specified by the Prefetched Index Value register (PIV). After passing the prefetched descriptor index to CIV, the next descriptor in the descriptor table is prefetched at an index incremented by one (and rolling over after index 31). When CIV equals LVI, the next descriptor will be prefetched, but only processed after LVI is incremented by software, thus providing that descriptor to the controller.

Modem subsystem bus master requests are prioritized above audio subsystem bus master requests.

The bus master logic, once set up by software, automatically fetches descriptors, transfers data to and from host memory, and generates interrupts, as part of its implemented control mechanism. This scatter/gather control mechanism is implemented for each data stream.

## 4.8.4 AC'97 Data Streams

The AC'97 digital controller buffers the following independent streams:
- Audio PCM out: left and right
- Audio PCM in: left and right
- Audio microphone in
- Modem in
- Modem out

The two samples of the Audio PCM out stream are controlled by a single scatter/gather bus master controller. The same is true for the two-sample Audio PCM in stream. The Audio PCM out samples are transferred from host memory in the following order:

| Audio Channel | AC97 Timeslot | Sample Order |
|---|---|---|
| Left | 3 | 1 |
| Right | 4 | 2 |

For a given 2-channel audio stream, it is required that each sample group start with the left sample in the least significant 16-bit address followed by the subsequent samples.
The order of the sample pairs can be swapped via DevB:5x4C.

Transfers to/from the AC-link utilize one sample per frame. The 16-bit samples are transferred as the 16 most significant bits of each 20-bit slot. The four low-order bits of input data are discarded. The four low-order bits of output data are padded with zeros.

When mono audio sample streams are transferred, it is required that both left and right samples are transferred with the same data. So two identical samples are transferred for each mono sample.

## 4.8.5 AC '97 Power Management Logic

AC30/MC40[PRINT] or AC30/MC40[SRINT] is set when an AC'97-defined wake-up event occurs on the AC-link and the system is not in a sleep state. AC2C/MC3C[PRIEN] and AC2C/MC3C[SRIEN] enable AC-link wake-up events to initiate interrupts.

PM20[AC97_STS] is set when a wake-up event occurs on the AC-link while the system is in a sleep state. PM22[AC97_EN] enables an AC-link wake-up event to initiate an interrupt and wake the system. PM2C[AC97SMI_EN] enables an AC-link wake-up event to initiate an SMI.

AC2C/MC3C[SHUTOFF] may be used to disable the AC-link IO signals. When the AC-link is disabled, all outputs, including ACRST_L, are forced Low and all inputs are ignored, except for wake-up event detection.

Once the codec is instructed to halt ACCLK, the wake-up protocol must be used to bring the AC-link to the active mode. Three methods for waking up the AC-link are supported:

- External wake-up
- Warm reset
- Cold reset

A transition from Low to High at ACSDIN0 or ACSDIN1 causes the AC'97 controller to sequence through a wake-up event detection and set the appropriate status bits. A subsequent warm or cold reset to the codec is required (by setting the appropriate bit in the Global Control register, AC2C) to finish the wake-up sequence.

During a cold reset, ACRST_L is asserted for a minimum of 1 microsecond. This is expected to initialize all codec registers to their default power-on-reset values. Internal AC-link control registers and FIFOs in the AC'97 are initialized as well. The bus AC'97 controller bus master registers are not affected.

A warm reset re-activates the AC-link without altering the current codec register values. It is signaled by driving ACSYNC High for a minimum of 1 microsecond in the absence of ACCLK. The AC'97 controller is not reset, but potentially remaining slot requests from the last frame before the warm reset are discarded.

Once powered down, activation of the AC-link via re-assertion of the ACSYNC signal must not occur for a minimum of 4 frame times following the frame in which the power down was triggered. The AC'97 controller samples ACSDIN[1:0] immediately, but delay any wake-up event reporting until after this period has expired.

When the AC-link powers up, readiness is indicated via the codec ready bits in the Global Status controller register, AC30. These bits must be checked before accessing the codec.

The IC never deasserts ACRST_L automatically. After reset, AC2C/MC3C[CRST_L] defaults to zero and software is required to deassert this bit.

# 5 Registers

## 5.1 Register Overview

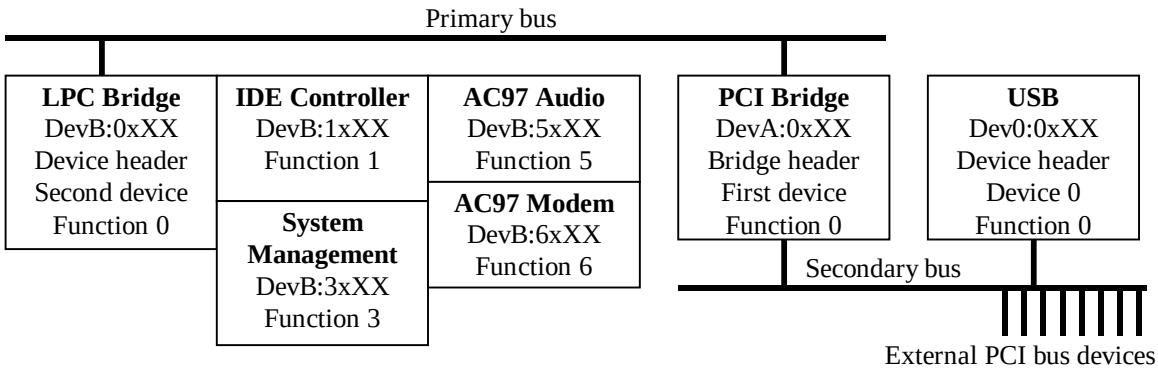
The IC includes several sets of registers accessed through a variety of address spaces. IO address space refers to register addresses that are accessed via x86 IO instructions such as IN and OUT. PCI configuration space is typically accessed via PCI-defined IO cycles to CF8h and CFCh in the host. There is also memory space and indexed address space in the IC.

### 5.1.1 Configuration Space

The address space for PCI configuration registers is broken up into *busses*, *devices*, *functions*, and, *offsets*, as defined by the PCI specification. The IC includes configuration space on two busses, the primary and secondary. The configuration space on the primary (host) bus is accessed by type 0 configuration cycles (as defined by the PCI specifications). The function number is mapped into bits[10:8] of the configuration address. The offset is mapped to bits[7:2] of the configuration address. Type 1 configuration cycles on the host bus that are targeted to internal or external devices on the secondary PCI bus are converted to type 0 configuration cycles.

The following diagram shows where all the functions reside in configuration space. The IC is viewed by software as two PCI bus devices that sit on the primary bus, typically bus 0. Device numbers are assigned via A_IDSEL[A,B] pins. Since USB resides on the secondary PCI bus, its device number is hard wired to 0 on that bus. The remaining device numbers through 15 are available on the external bus, per the PCI-to-PCI bridge specification. Configuration cycles to device numbers 16 through 31 on the secondary PCI bus are generated with address bits[31:11] all zero so no IDSEL lines are set.

Devices and functions in the IC:




Configuration accesses to non-existant functions, or functions disabled by DevB:0x48[PRIENS], within devices A and B are not claimed by the IC. Configuration writes to non-existent registers within each enabled function are ignored and reads return all zeros.

## 5.1.2 Register Naming and Description Conventions

Each register location has an assigned mnemonic that specifies the address space and offset. These mnemonics start with two or three characters that identify the space followed by characters that identify the offset within the space. Register fields within register locations are also identified with a name or bit group in brackets following the register location mnemonic. For example, the ACPI sleep type register field, which is located at offset 04h of PMxx space, bits 10, 11, and 12, is referenced as PM04[SLP_TYP] or PM04[12:10].

PCI configuration spaces are referenced with mnemonics that takes the form of Dev[A|B|0]:[7:0]x[FF:0], where the first bracket contains the device number, the second bracket contains the function number, and the last bracket contains the offset. Devices "A" and "B" are on the primary bus and their values are assigned by the platform designer.

| Bus | Device | Function | Mnemonic | Function |
|---|---|---|---|---|
| Primary | "A" | 0 | DevA:0xXX | PCI bridge |
| Primary | "B" | 0 | DevB:0xXX | LPC bridge, legacy circuitry |
| Primary | | 1 | DevB:1xXX | Enhanced IDE controller |
| Primary | | 3 | DevB:3xXX | System management registers |
| Primary | | 5 | DevB:5xXX | AC97 soft audio controller |
| Primary | | 6 | DevB:6xXX | AC97 soft modem controller |
| Secondary | 0 | 0 | Dev0:0xXX | OHCI-based USB controller 0 |

Fixed address spaces.

| Port(s) | Mnemonic | Type | Function |
|---|---|---|---|
| 00-0F | PORTxx | IO mapped | Slave DMA controller |
| 20-21 | PORTxx | IO mapped | Master interrupt controller |
| 40-43 | PORTxx | IO mapped | Programmable interval timer |
| 60 | PORT60 | IO mapped | USB keyboard emulation address |
| 61 | PORT61 | IO mapped | AT compatibility Register |
| 64 | PORT64 | IO mapped | USB keyboard emulation address |
| 70-73 | RTCxx | IO mapped | Real-time clock and CMOS RAM |
| 80-8F | PORTxx | IO mapped | DMA page registers |
| 92 | PORT92 | IO mapped | System control register |
| A0-A1 | PORTxx | IO mapped | Slave interrupt controller |
| C0-DF | PORTxx | IO mapped | Master DMA controller |
| F0-F1 | PORTxx | IO mapped | Floating-point error control |
| 170-177, 376 | PORTxx | IO mapped | Secondary IDE drives (not used when in native mode) |
| 1F0-1F7, 3F6 | PORTxx | IO mapped | Primary IDE drives (not used when in native mode) |
| 4D0-4D1 | PORT4D0 | IO mapped | EISA-defined level-triggered interrupt control registers |
| CF9 | PORTCF9 | IO mapped | Reset register |
| FEC0_0000, FEC0_0010-13 | IOAxx | Memory mapped | IOAPIC register set |

Relocatable address spaces.

| Address Specified By Configuration Register | Size (bytes) | Type | Mnemonic | Function |
|---|---|---|---|---|
| DevB:1x10 | 8 | IO mapped | None | Pointer to primary port IDE command space |
| DevB:1x14 | 4 | IO mapped | None | Pointer to primary port IDE control space |
| DevB:1x18 | 8 | IO mapped | None | Pointer to secondary port IDE command space |
| DevB:1x1C | 4 | IO mapped | None | Pointer to secondary port IDE control space |
| DevB:1x20 | 16 | IO mapped | IBMx | IDE controller bus-master control registers |
| DevB:3x58 | 256 | IO mapped | PMxx | System management IO register space |
| DevB:5x10 | 256 | IO mapped | None | Pointer to AC97 audio mixer space |
| DevB:5x14 | 64 | IO mapped | ACxx | AC97 audio bus master control registers |
| DevB:6x10 | 256 | IO mapped | None | Pointer to AC97 modem mixer space |
| DevB:6x14 | 64 | IO mapped | MCxx | AC97 modem bus master control registers |
| Dev0:0x10 | 4K | Memory mapped | USBxxx | USB IO register space |

Note: DevB:1x10, DevB:1x14, DevB:1x18, and DevB:1x1C are only used when the IDE controller is in native mode as specified by DevB:1x08.

The following are register behaviors found in the register descriptions.

| Type | Description |
|---|---|
| Read or read-only | Capable of being read by software. Read-only implies that the register cannot be written to by software. |
| Write | Capable of being written by software. |
| Set by hardware | Register bit is set High hardware. |
| Write 1 to clear | Software must write a 1 to the bit in order to clear it. Writing a 0 to these bits has no effect. |
| Write 1 only | Software can set the bit High by writing a 1 to it. However subsequent writes of 0 will have no effect. RESET# must be asserted in order to clear the bit. |
| Write once | After RESET#, these registers may be written to once. After they are written, they become read-only until the next RESET# assertion. |

### 5.1.3 Positively- and Subtractively-Decoded Spaces

The IC positively decodes all address ranges described above as well as address windows for the secondary PCI bus, specified by the PCI bridge header. All transactions received that are not positively decoded are passed either directly to the LPC bridge or provided onto the secondary PCI bus before being sent to the LPC bus (see DevB:0x40[SUBDEC]). Thus, the LPC bridge is the subtractive path for all unclaimed cycles.

The IC claims all unclaimed memory and IO cycles on the host bus during the subtractive DEVSEL window.

### 5.1.4 Subsystem Vendor and Device Identification

System firmware is required to write the correct values of Subsystem Vendor and Subsystem Device ID to each function in the IC after every reset. For the LPC Bridge (DevB:0x), EIDE Controller (DevB:1x), and USB Host Controller (Dev0:0x), this is accomplished with a write to offset 70 in configuration space. For the System Management configuration space (DevB:3x) it is a write to offset 7C. For the AC97 Audio and Modem configuration spaces (DevB:5x and DevB:6x), the Vendor/Device ID registers may be written once (and only once) after reset. The PCI Bridge (DevA:0x) does not have a Subsystem Vendor/Device ID registers because the *PCI-PCI Bridge Specification* does not define a location for them.

## 5.2 PCI Bridge Configuration Registers (DevA:0xXX)

These registers are located in PCI configuration space on the primary PCI interface, in the first device (device A), function 0. See Section 5.1.2 for a description of the register naming convention.

**PCI Bridge Vendor and Device ID Register** **DevA:0x00**

Default: 7448 1022h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:16 | **PCI Bridge device ID.** |
| 15:0 | **Vendor ID.** |

**PCI Bridge Status and Command Register** **DevA:0x04**

Default: 0220 0003h. Attribute: See below.

| Bits | Description |
|---|---|
| 31 | **DPE: detected parity error.** Read capable; set by hardware; write 1 to clear. 1=A parity error was detected on the host interface. |
| 30 | **SSE: signaled system error.** Read only. This bit is fixed in the Low state. |
| 29 | **RMA: received master abort.** Read; set by hardware; write 1 to clear. 1=A request sent to the host bus received a master abort. Note: this bit is cleared by PWROK reset but not by RESET#. |
| 28 | **RTA: received target abort.** Read; set by hardware; write 1 to clear. 1=A request sent to the host bus received a target abort. Note: this bit is cleared by PWROK reset but not by RESET#. |
| 27 | **Signaled target abort.** Read only. This bit is fixed in the Low state. |
| 26:25 | **DEVSEL Timing.** Read only. These bits are fixed at STATUS[10:9] = 01b. This specifies “medium” timing as defined by the PCI specification. |
| 24 | **Data parity detected.** Read only. This bit is fixed in the Low state. |
| 23 | **Fast back to back enable.** Read only. This bit is fixed in the Low state. |
| 22 | **User definable features.** Read only. This bit is fixed in the Low state. |
| 21 | **66 MHz capable.** Read only. This bit is fixed in the High state. |
| 20 | **Capabilities pointer.** Read only. This bit is fixed in the Low state. |
| 19:9 | Reserved |
| 8 | **SERREN: SERR# enable.** Read-write. This bit controls no hardware. |
| 7 | Reserved. |
| 6 | **PERSP: Parity error response.** Read-write. This bit controls no hardware. |
| 5 | Reserved. |
| 4 | **MWIEN: Memory write and invalidate enable.** Read-write. This bit does not control any internal hardware. |
| 3 | **Special cycle enable.** Read only. This bit is hardwired Low. |
| 2 | **MASEN: PCI master enable.** Read-write. 1=Enables internal and external PCI secondary bus masters to initiate cycles. When this bit is 0, peer-to-peer cycles on the secondary bus are not allowed. |
| 1 | **MEMEN: memory enable.** Read-write. 1=Enables access to the secondary PCI bus memory space. |
| 0 | **IOEN: IO enable.** Read-write. 1=Enables access to the secondary PCI bus IO space. |

**PCI Bridge Revision and Class Code Register** **DevA:0x08**

Default: 0604 0004h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:8 | **CLASSCODE.** Provides the bridge class code as defined in the PCI specification. |
| 7:0 | **REVISION.** PCI bridge silicon revision. |

**PCI Bridge BIST-Header-Latency-Cache Register** **DevA:0x0C**

Default: 0001 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:24 | **BIST.** Read only. These bits fixed at their default values. |
| 23:16 | **HEADER.** Read only. These bits fixed at their default values. |
| 15:8 | **LATENCY.** Read-write. These bits control no hardware. |
| 7:0 | **CACHE.** Read only. These bits fixed at their default values. |

**PCI Bridge Bus Numbers and Secondary Latency Register** **DevA:0x18**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:24 | **SECLAT.** Secondary latency timer. |
| 23:16 | **SUBBUS.** Subordinate bus number. |
| 15:8 | **SECBUS.** Secondary bus number. |
| 7:0 | **PRIBUS.** Primary bus number. |

**PCI Bridge Memory Base-Limit Registers** **DevA:0x1C, DevA:0x20 and DevA:0x24**

These registers specify the IO-space (DevA:0x1C), non-prefetchable memory-space (DevA:0x20), and prefetchable memory-space (DevA:0x24) address windows for transactions that are mapped to the secondary PCI bus as follows:

```
PCI IO window =
     {16'h0000,DevA:0x1C_IOLIM,12'hFFF} >= address >= {16'h0000,DevA:0x1C_IOBASE,12'h000};
PCI non-prefetchable memory window =
     {DevA:0x20_MEMLIM,20'hF_FFFF}      >= address >= {DevA:0x20_MEMBASE,20'h0_0000};
PCI prefetchable memory window =
     {DevA:0x24_PMEMLIM,20'hF_FFFF}     >= address >= {DevA:0x24_PMEMBASE,20'h0_0000};
```

These windows may also be altered by DevA:0x3C[VGAEN, ISAEN]. When the address (from either the host or from a secondary PCI bus master) is inside one of the windows, then the transaction is assumed to be intended for a target that sits on the secondary PCI bus. Therefore, the following transactions are possible:

- Host-initiated transactions inside the windows are sent to the PCI bus.
- Secondary PCI-initiated transactions inside the windows are not claimed by the IC, even when DevA:0x04[MEMEN or IOEN] are 0.
- Host initiated transactions outside the windows that are not claimed by any other functions within the IC are passed to the LPC bus.
- Secondary PCI initiated transactions outside the windows are claimed by the IC using medium decoding and passed to the host.
- If IOBASE > IOLIM, MEMBASE > MEMLIM, and PMEMBASE > PMEMLIM, then *no* host-initiated transactions will be forwarded by the secondary PCI bus and *all* secondary-PCI-bus-initiated memory and IO (not configuration) transactions will be forwarded to the host.

**DevA:0x1C.** Default:0200 00F0h. Attribute: See below.

| Bits | Description |
|---|---|
| 31 | **DPE: detected parity error.** Read; set by hardware; write 1 to clear. 1=The IC detected an address parity error as the target of a secondary PCI bus cycle or a data parity error as the target of a secondary PCI bus write cycle or a data parity error as the master of a secondary PCI bus read cycle. |
| 30 | **RSE: received system error.** Read; set by hardware; write 1 to clear. 1=The IC detected assertion of SERR#. Note: this bit is cleared by PWROK reset but not by RESET#. |
| 29 | **RMA: received master abort.** Read; set by hardware; write 1 to clear. 1=The IC received a master abort as a master on the secondary PCI bus. Note: this bit is cleared by PWROK reset but not by RESET#. |
| 28 | **RTA: received target abort.** Read; set by hardware; write 1 to clear. 1=The IC received a target abort as a master on the secondary PCI bus. Note: this bit is cleared by PWROK reset but not by RESET#. |
| 27 | **STA: signaled target abort.** Read; set by hardware; write 1 to clear. 1=The IC generated a target abort as a target on the secondary PCI bus. The IC will generate a target abort if it receives a target abort (a non-NXA error) response from the host to a secondary PCI master transaction request. Note: this bit is cleared by PWROK reset but not by RESET#. |
| 26:25 | **Device select timing.** Read only. These bits are hard wired to indicate medium decoding. |

| Bits | Description (Continued) |
|---|---|
| 24 | **MDPE: master data parity error.** Read; set by hardware; write 1 to clear. 1=The IC detected a parity error during a data phase of a read or detected PERR# asserted during a write as a master on the secondary PCI bus and DevA:0x3C[PEREN] is set. When this bit is set, an NMI is generated; see PM48[NMI2SMI_EN] for information on how NMI interrupts may be controlled. |
| 23:16 | Reserved. |
| 15:12 | **IOLIM.** IO limit address bits[15:12]. See DevA:0x[24:1C] above. |
| 11:8 | Reserved. |
| 7:4 | **IOBASE.** IO base address bits[15:12]. See DevA:0x[24:1C] above. |
| 3:0 | Reserved. |

**DevA:0x20.** Default:0000 FFF0h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:20 | **MEMLIM.** Non-prefetchable memory limit address bits[31:20]. See DevA:0x[24:1C] above. |
| 19:16 | Reserved. |
| 15:4 | **MEMBASE.** Non-prefetchable memory base address bits[31:20]. See DevA:0x[24:1C] above. |
| 3:0 | Reserved. |

**DevA:0x24.** Default:0000 FFF0h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:20 | **PMEMLIM.** Prefetchable memory limit address bits[31:20]. See DevA:0x[24:1C] above. |
| 19:16 | Reserved. |
| 15:4 | **PMEMBASE.** Prefetchable memory base address bits[31:20]. See DevA:0x[24:1C] above. |
| 3:0 | Reserved. |

**PCI Bridge Interrupt and Bridge Control Register** **DevA:0x3C**

Default: 0000 00FFh. Attribute: See below.

| Bits | Description |
|---|---|
| 31:22 | Reserved. |
| 21 | **MARSP: master abort response.** Read-write. 1=The response to non-posted requests that come from the host bus or secondary PCI bus that results in a master aborts will indicate a target abort. 0=Master aborts result in normal responses; read responses are sent with the appropriate amount of data, which are all 1's and writes are ignored. |
| 20 | Reserved. |
| 19 | **VGAEN: VGA decoding enable.** Read-write. 1=Route host-initiated commands targeting VGA-compatible address ranges to the secondary PCI bus. These include memory accesses from A0000h to BFFFFh, IO accesses in which address bits[9:0] range from 3B0h to 3BBh or 3C0h to 3DFh (address bits[15:10] are not decoded, regardless of bit[18], ISA enable). 0=PCI does not decode VGA-compatible address ranges. |
| 18 | **ISAEN: ISA decoding enable.** Read-write. 1=The IO address window specified by DevA:0x1C[15:0] is limited to the first 256 bytes of each 1K byte block specified. 0=The PCI IO window is the whole range specified by DevA:0x1C[15:0]. |
| 17 | **SERREN: system error enable.** Read-write. This bit controls no hardware. |
| 16 | **PEREN: parity error response enable.** Read-write. 1=Enable parity error detection on secondary PCI interface (see DevA:0x1C[MDPE]); PERR# signal enabled to set status bit or be driven. 0=DevA:0x1C[MDPE] cannot be set; PERR# signal is ignored and it is not driven by the IC. |
| 15:8 | **INTERRUPT_PIN.** Read only. These bits fixed in their default state. |
| 7:0 | **INTERRUPT_LINE.** Read-write. These bits control no internal logic. |

**Read-Write Register** **DevA:0xE8**

Default: 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:0 | **RW.** Read-write. These bits are read-write accessible through software; they control no hardware. |

# 5.3 LPC Bridge Configuration Registers (DevB:0xXX)

These registers are located in PCI configuration space on the primary PCI interface, in the second device (device B), function 0. See Section 5.1.2 for a description of the register naming convention.

**LPC Bridge Vendor and Device ID Register** **DevB:0x00**

Default: 7440 1022h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:16 | **LPC bridge device ID.** |
| 15:0 | **Vendor ID.** |

**LPC Bridge Status and Command Register** **DevB:0x04**

Default: 0220 000Fh. Attribute: See below.

| Bits | Description |
|---|---|
| 31:4 | These bits are fixed at their default values. |
| 3 | **SPCYCEN: special cycle enable.** Read-write. 1=The IC responds to shutdown special cycles by using INIT# to reset the processor. 0=The IC ignores shutdown special cycles. |
| 2:0 | **IO, memory, and master enable.** Read only. Hardwired in the enabled state. |

**LPC Bridge Revision and Class Code Register** **DevB:0x08**

Default: 0601 0004. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:8 | **CLASSCODE.** Provides the ISA bridge class code as defined in the PCI specification. |
| 7:0 | **REVISION.** LPC bridge silicon revision. |

**LPC Bridge BIST-Header-Latency-Cache Register** **DevB:0x0C**

Default: 0080 0000h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:24 | **BIST.** These bits fixed at their default values. |
| 23:16 | **HEADER.** These bits fixed at their default values. |
| 15:8 | **LATENCY.** These bits fixed at their default values. |
| 7:0 | **CACHE.** These bits fixed at their default values. |

**LPC Bridge Subsystem ID and Subsystem Vendor ID Register** **DevB:0x2C**

Default: 0000 0000h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:16 | **SSID: subsystem ID.** This field is write accessible through DevB:0x70. |
| 15:0 | **SSVENDORID: subsystem vendor ID.** This field is write accessible through DevB:0x70. |

**IO Control 1 Register** **DevB:0x40**

Default: 00h. Attribute: See below.

| Bits | Description |
|---|---|
| 7 | **NMIONERR: generate an NMI on error.** Read-write. 1=An NMI is generated when one of the error status bits specified by Section 4.1.2 is set. Note: see PM48[NMI2SMI_EN] for information on how NMI interrupts may be controlled. |
| 6 | **LPCERR: LPC transaction error status.** Read; set by hardware; write 1 to clear. The bit is set High by hardware when an LPC sync error occurs. |
| 5 | **SUBDEC: subtractive decoding off of the secondary PCI bus.** Read-write. 1=All memory mapped and IO mapped transactions received by the host that are not destined for any internally specified devices or busses are first sent to the secondary PCI bus. If DEVSEL is not asserted for these PCI bus cycles, then the IC asserts DEVSEL_L during the subtractive window, and asserts TRDY_L to complete the cycle. The cycle is then retransmitted to the LPC bus. If, during the PCI bus cycle, DEVSEL_L is asserted by an external component before the subtractive window, then the cycle is assumed to be for the secondary PCI bus and is allowed to complete. 0=All memory mapped and IO mapped transactions received by the host that are not destined for any internally specified devices or busses are sent directly to the LPC bus. |
| 4 | **LPC_IOR: LPC IO recovery.** Read-write. 1= IO recovery delay (specified by IORT) enforced for both LPC and legacy IO cycles. 0=IO recovery delay only enforced for legacy IO cycles (cycles to the DMA controller, legacy PIC, programmable interval timer, and real-time clock). |
| 3 | **IORT: IO recovery time.** Read-write. This bit specifies the amount of time enforced between internal legacy IO cycles (cycles to the DMA controller, legacy PIC, programmable interval timer, and real-time clock) and—if enabled via LPC_IOR—LPC cycles. 0=There are a minimum of 22 PCLK cycles between the end of each IO cycle and the beginning of the next IO cycle. 1=There are a minimum of 54 PCLK cycles between IO cycles. This bit does not affect memory cycles (only IO cycles). |
| 2 | **BLE: BIOS lock enable.** Read; write 1 only. 1=Setting DevB:0x40[RWR] from 0 to 1 will set PM44[IBIOS_STS] and generate an SMI. 0=Setting DevB:0x40[RWR] from 0 to 1 will not set PM44[IBIOS_STS] and not generate an SMI. Once BLE is set, it can only be cleared by RESET#. |
| 1 | **RSEA: received system error on APC host bus.** Read; set by hardware; write 1 to clear. This bit is set by hardware when A_SERR# is asserted. See Section 4.1.2 for details about the error handling logic. |
| 0 | **RWR: LPC ROM write.** Read-write. 1=Memory writes to BIOS ROM address space, as defined by DevB:0x43, are allowed to pass onto the LPC bus. 0=Memory writes to BIOS ROM address space are dropped. |

**IO Control 2 Register** **DevB:0x41**

Default: 00h. Attribute: See below.

| Bits | Description |
|---|---|
| 7 | **Must be Low.** Read-write. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 6 | Reserved. |
| 5 | **P92FR: port 92 fast reset.** Read-write. 1=Writes that attempt to set IO PORT92[0]—the fast processor reset bit—are enabled. 0=Writes to PORT92[0] do not generate a processor reset pulse using INIT#. |
| 4 | Reserved. |
| 3 | **Must be Low.** Read-write. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 2 | Reserved. |
| 1 | **NMIDIS: NMI disable.** Read only. This provides read access to RTC70[NMIDIS]. |
| 0 | **SHEN: shadow register access enable.** Read-write. 1=Shadowed IO access to legacy write-only registers is enabled. 0=Normal access of legacy registers. The following table shows all registers affected by this bit. |

| IO port | R/W | Normal mode | Shadow mode |
|---|---|---|---|
| DMA: 00h, 02h, 04h, 06h, C0h, C4h, C8h, CCh | W | Base address for DMA channel | Current address for DMA channel |
| | R | Current address for DMA channel | Base address for DMA channel |
| DMA: 01h, 03h, 05h, 07h, C2h, C6h, CAh, CEh | W | Base byte count for DMA channel | Current byte count for DMA channel |
| | R | Current byte count for DMA channel | Base byte count for DMA channel |
| DMA: 08h/D0h | W | Command Register DMA CH[3:0]/[7:4] | Status Register DMA CH[3:0]/[7:4] |
| | R | Status Register DMA CH[3:0]/[7:4] | First read: Command reg DMA CH[3:0]/[7:4]<br>Second read: Request reg DMA CH[3:0]/[7:4]<br>Third read: Mode register DMA CH0/4<br>Fourth read: Mode register DMA CH1/5<br>Fifth read: Mode register DMA CH2/6<br>Sixth read: Mode register DMA CH3/7 |
| DMA: 09h/D2h, 0Ah/D4h, 0Bh/D6h | W | See DMA controller | Reserved |
| DMA: 0Ch/D8h, 0Dh/DAh, 0Eh/DCh | W | See DMA controller | Same as normal mode |
| DMA: 0Fh/DEh | W | Write all masks [3:0]/[7:4] | Write all masks [3:0]/[7:4] |
| | R | Reserved | Read all masks [3:0]/[7:4] |
| PIT: 40h | R | Status byte counter 0 | First read: Status byte counter 0<br>Second read: CRL for counter 0<br>Third read: CRM for counter 0<br>Fourth read: CRL for counter 1<br>Fifth read: CRM for counter 1<br>Sixth read: CRL for counter 2<br>Seventh read: CRM for counter 2 |
| PIT: 41h | R | Status byte counter 1 | Status byte counter 1 |
| PIT: 42h | R | Status byte counter 2 | Status byte counter 2 |
| PIC: 20h | R | Interrupt request register for PIC 1 | First read: ICW1 for controller 1<br>Second read: ICW2 for controller 1<br>Third read: ICW3 for controller 1<br>Fourth read: ICW4 for controller 1<br>Fifth read: OCW1 for controller 1<br>Sixth read: OCW2 for controller 1<br>Seventh read: OCW3 for controller 1<br>Eighth read: ICW1 for controller 2<br>Ninth read: ICW2 for controller 2<br>Tenth read: ICW3 for controller 2<br>Eleventh read: ICW4 for controller 2<br>Twelfth read: OCW1 for controller 2<br>Thirteenth read: OCW2 for controller 2<br>Fourteenth read: OCW3 for controller 2 |
| PIC: 21h | R | In-service register for PIC 1 | In-service register for PIC 1 |
| PIC: A0h | R | Interrupt request register for PIC 2 | Interrupt request register for PIC 2 |
| PIC: A1h | R | In-service register for PIC 2 | In-service register for PIC 2 |

**Legacy Blocks Control Register** **DevB:0x42**

Default: 07h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:3 | Reserved. |
| 2 | **DMAEN: internal DMAC (Direct Memory Access Controller) enable.** 1=Enable internal 8237-based DMAC and associated logic; accesses to IO ports 00h through 0Fh, 80h though 8Fh, and C0h through DFh are routed to the internal DMAC. 0=Disable DMAC and associated logic; DMAC accesses are routed to the LPC bus. |
| 1 | **PITEN: internal PIT (Programmable Interval Timer) enable.** 1=Enable internal 8254-based PIT and associated logic; accesses to IO ports 40h through 43h and 61h are routed to the internal PIT. 0=Disable PIT and associated logic; PIT accesses are routed to the LPC bus. |
| 0 | **PICEN: internal PIC (Programmable Interrupt Controller) enable.** 1=Enable internal 8259-based PIC and associated logic; accesses to IO ports 20h, 21h, 92h, A0h, A1h, F0h, F1h, 4D0h, 4D1h as well as interrupt acknowledge cycles are routed to the internal PIC and associated logic. 0=Disable PIC and associated logic; PIC accesses are routed to the LPC bus. |

**ROM Decode Control Register** **DevB:0x43**

Default: 00h. Attribute: Read-write.

**SEGEN: ROM segment enables.** This register specifies the address space mapped to the BIOS ROM on the LPC bus. Each bit specifies the LPC bus enabled for BIOS. For each of these bits: 1=Enables an address range as a BIOS ROM access. 0=The corresponding address range is not decoded as a BIOS ROM access. The bits control the following address ranges (the last column shows the translated LPC bus addresses):

| Bits | Size | Host Address Range[31:0] | Address Translation for LPC Bus |
|---|---|---|---|
| 7 | 4 megabytes | FFC0_0000h–FFFF_FFFFh | FFC0_0000h–FFFF_FFFFh |
| 6 | 1 megabyte | FFB0_0000h–FFBF_FFFFh | FFB0_0000h–FFBF_FFFFh |
| 5 | 32K bytes | 000E_8000h–000E_FFFFh | FFFE_8000h–FFFE_FFFFh |
| 4 | 32K bytes | 000E_0000h–000E_7FFFh | FFFE_0000h–FFFE_7FFFh |
| 3 | 32K bytes | 000D_8000h–000D_FFFFh | FFFD_8000h–FFFD_FFFFh |
| 2 | 32K bytes | 000D_0000h–000D_7FFFh | FFFD_0000h–FFFD_7FFFh |
| 1 | 32K bytes | 000C_8000h–000C_FFFFh | FFFC_8000h–FFFC_FFFFh |
| 0 | 32K bytes | 000C_0000h–000C_7FFFh | FFFC_0000h–FFFC_7FFFh |

Note: the following ranges are always specified as BIOS address ranges:

| | Size | Host Address Range[31:0] | Address Translation for LPC Bus |
|---|---|---|---|
| | 64K bytes | FFFF_0000h–FFFF_FFFFh | FFFF_0000h–FFFF_FFFFh |
| | 64K bytes | 000F_0000h–000F_FFFFh | FFFF_0000h–FFFF_FFFFh |

Note: see DevB:0x80 for more information about how access to BIOS spaces may be controlled.

**Prefetchable Memory Control Register** **DevB:0x44**

Default: 0001h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:4 | **TOM[31:20]: top of memory bits[31:20].** This specifies the top of system memory. System memory space is treated as prefetchable by the PCI bridge. It is defined as follows:<br>`System_memory = (PCI_address[31:20] <= TOM[31:20]);`<br>Note: If ALLPF is set High, then TOM is ignored. |
| 3:1 | Reserved. |
| 0 | **ALLPF: all of memory space (4 gigabytes) is prefetchable.** 1=All 4 gigabytes of memory space is prefetched by the PCI bridge; when memory read transactions with PCI command encoding of 6h are initiated by PCI bus masters, then the data is prefetched, regardless of the address. 0=Only memory read accesses with PCI command encoding of Ch or Eh, or memory accesses with PCI command encoding 6h below the top of memory specified in the TOM field of this register are prefetched. |

**Miscellaneous Control Register** **DevB:0x47**

Default: 00h. Attribute: See below.

| Bits | Description |
|---|---|
| 7:6 | Reserved. |
| 5 | **ALLTOD: all internal PCI interrupts mapped to PIRQD#.** Read-write. 1=Internal PCI interrupts—including the USB interrupt, the AC97 interrupts, and the GPIO interrupts as specified by DevB:0x4B[MPIRQ]—are mapped to assert PIRQD# when they become active; i.e., all these interrupts are shared on PIRQD#. 0=Internal PCI interrupts are distributed across all four PIRQ[D:A]# pins as specified in Section 4.4.2.1 and by DevB:0x4B[MPIRQ]. |
| 4 | **Must be Low.** Read-write. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 3 | **CMLK_B8: CMOS RAM offsets B8b through BFh lock.** Read; write 1 only. 0=Accesses to the eight bytes of CMOS RAM (powered by the VDD_AL plane) addressed from B8h to BFh are read-write accessible. 1=Writes to these bytes are ignored and read always return FFh (regardless as to which of the IO ports from 70h to 73h are used for the access). After this bit is set High, it cannot be cleared again by software; it can only be cleared by PWROK reset. |
| 2 | **CMLK_38: CMOS RAM offsets 38h through 3Fh lock.** Read; write 1 only. 0=Accesses to the eight bytes of CMOS RAM (powered by the VDD_AL plane) addressed from 38h to 3Fh are read-write accessible. 1=Writes to these bytes are ignored and read always return FFh (regardless as to which of the IO ports from 70h to 73h are used for the access). After this bit is set High, it cannot be cleared again by software; it can only be cleared by PWROK reset. |
| 1 | **Must be Low.** Read-write. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 0 | **SWRST: software reset.** Write only. When this bit is written with 1, a reset pulse is generated over RESET# and CPURST#. This bit always reads as 0. |

**Function/Device Enable Register** **DevB:0x48**

Default: FFFFh. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:8 | **SECENS[7:0]: secondary PCI bus device enables.** Each of these bits apply to the first 8 internal devices on the secondary PCI bus. Bit[0] applies to device 0, etc. Bits that apply to device numbers that are not implemented internally are ignored. 1=The device's configuration space is enabled. 0=The device's configuration space is invisible; accesses to the space are master aborted; reads return all ones. |
| 7:0 | **PRIENS[7:0]: primary PCI bus function enables.** Each of these bits apply to Device B functions inside the IC (on the primary bus). Bit[1] applies to function 1, bit[3] to function 3, etc. However, bit[0] is ignored since function 0 cannot be disabled. Bits that apply to internal functions that do not exist in the IC are ignored as well. 1=The function's configuration space is enabled. 0=The function's configuration space is disabled; accesses to the space are master aborted; reads return all ones. |

**IOAPIC Configuration Register** **DevB:0x4B**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7 | **MPIRQ: multi-processor IRQ mode.** This bit is combined with the mask bits of IOAPIC redirection table entries 23 through 20 and used to specify if the GPIO[31:28] inputs will be mapped to drive the PIRQ[D:A]# pins Low, respectively (GPIO28 to PIRQA#, etc.). For each of these four pins:<br>`if (MPIRQ & MASK[23:20] & ~GPIO[31:28]) then PIRQ[D:A]# = 0;`<br>`else PIRQ[D:A]# = Z; // high impedance`<br>The polarity of GPIO[31:28], in the above equation, is as seen on the external pins; the polarity is not altered by the programming of DevB:3x[DF:DC].The four GPIO pins may all be mapped to PIRQD#, as specified by DevB:0x47[ALLTOD]. |
| 6 | **Must be Low.** Read-write. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 5 | **Must be Low.** Read-write. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 4:3 | **APICCKS: APIC clock select.** Selects the source and frequency of the PICCLK as follows:<br><br>APICCKS[1:0] — Frequency — Source<br>00b — PCLK divided by 4 (8.3 MHz max) — The IC drives PICCLK.<br>01b — PCLK divided by 2 (16.7 MHz max) — The IC drives PICCLK.<br>10b — PCLK (33.3 MHz max) — The IC drives PICCLK.<br>11b — Unknown. — External *<br><br>* In this mode, the external PICCLK is driven by an external component. The clock source is required to be 33 MHz or less. |
| 2:1 | Reserved. |
| 0 | **APICEN: IOAPIC enable.** 0=Accesses to the IOAPIC register space are ignored. 1=The IOAPIC is enabled. Operation of the INTR pin is not affected by this bit. |

**PCI Transaction Posted Write and Arbiter Control Register** **DevB:0x4C**

Default: 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:11 | Reserved. |
| 10 | **Must be High.** Read-write. This bit is required to be set High during initialization; if it is Low then undefined behavior will result. |
| 9 | **ISOCPRI: isochronous stream arbiter priority.** 1=The PCI arbiter gives priority access to isochronous streams. 0=The PCI arbiter uses a simple round robin algorithm. Isochronous streams come from AC97 audio and modem and the USB controller. When this bit is set, the highest priority requester is AC97, next is USB, and then all the rest of the requesters; the non-isochronous requesters priority is based on a round robin scheme. |
| 8 | **Must be Low.** Read-write. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 7:0 | **Must be Low.** Read-write. This field is required to be all zeros at all times; if any bits are High then undefined behavior will result. |

**Device and Subsystem ID Read-Write Register** **DevB:0x70**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:16 | **SSID: subsystem ID.** The value placed in this register is visible DevB:0x2C[31:16]. |
| 15:0 | **SSVENDORID: subsystem vendor ID.** The value placed in this register is visible DevB:0x2C[15:0]. |

**BIOS Access Control Registers** **DevB:0x80, DevB:0x84, and DevB:0x88**

Default: 0000 0000h (for each). Attribute: Read-write.

These registers consists of 24, 4-bit registers called OAR (open at reset) locks. Each 4-bit register applies to a sector of the BIOS in the 5 megabyte BIOS range at the top of the 4-gigabyte address space as follows:

DevB:0x84 and DevB:0x80 contain 16, 4-bit lock registers, called OARx where x ranges across [F:0]; each 4-bit register controls a 64Kbyte address range at the top megabyte of memory as follows: [FFFx_FFFFh:FFFx_0000h].

DevB:0x88 contains eight, 4-bit lock registers, called OARx where x ranges as [E, C, A, 8, 6, 4, 2, 0]. Each 4-bit register controls an 8Kbyte address range as follows: [FFBF_(x+1)FFFh:FFBF_x000h].

Accesses to BIOS space in the low megabyte (between 000C_0000h and 000F_FFFFh) are mapped to the top megabyte (between FFFC_0000h and FFFF_FFFFh) on the LPC bus; the OAR locks for these accesses apply to these accesses based on the remapped address at the top megabyte. Note: there is an additional OAR lock specified in DevB:0x8C. Note: OAR locks only apply to BIOS address space; if there is an access to an OAR lock address range that is not in BIOS address space as defined by DevB:0x43, then the OAR lock register is ignored. Note: the OAR locks only apply to the BIOS address space on the LPC bus; if DevB:3x48[PCIBIOS] = 1, then they are ignored.

As defined below, access to BIOS space can be limited to when the host is in system management mode (SMM). PCI special cycles are used to specify that the system is in SMM. The data phase for these special cycles are: enter SMM: 0005_0002h; exit SMM: 0006_0002h.

| Register | Bits [31:28] | Bits [27:24] | Bits [23:20] | Bits [19:16] | Bits [15:12] | Bits [11:8] | Bits [7:4] | Bits [3:0] |
|---|---|---|---|---|---|---|---|---|
| DevB:0x88 | OARE | OARC | OARA | OAR8 | OAR6 | OAR4 | OAR2 | OAR0 |
| DevB:0x84 | OARF | OARE | OARD | OARC | OARB | OARA | OAR9 | OAR8 |
| DevB:0x80 | OAR7 | OAR6 | OAR5 | OAR4 | OAR3 | OAR2 | OAR1 | OAR0 |

| Bits | Description |
|---|---|
| OARx[3] | **FLLOCK: full access to RD/WRLOCK lock.** Read; write 1 only. This bit can only be set High by software; it is cleared by RESET#. 0=Read-write access to RDLOCK and WRLOCK enabled. 1=Write access to RDLOCK and WRLOCK disabled (whether the system is in SMM mode or not). |
| OARx[2] | **SLLOCK: SMM access to RD/WRLOCK lock.** Read; write 1 only. This bit can only be set High by software; it is cleared by RESET#. 0=Read-write access to RDLOCK and WRLOCK enabled (if FLLOCK=0). 1=Write access to RDLOCK and WRLOCK only enabled in SMM mode (if FLLOCK=0). |
| OARx[1] | **WRLOCK: BIOS sector x write lock.** Read; write if enabled by SLLOCK and FLLOCK. 0=Write access to BIOS sector x enabled (if DevB:0x40[RWR]=1). 1=Write access to BIOS sector x disabled. |
| OARx[0] | **RDLOCK: BIOS sector x read lock.** Read; write if enabled by SLLOCK and FLLOCK. 0=Read access to BIOS sector x enabled. 1=Read access to BIOS sector x disabled. |

**OAR Control Register** **DevB:0x8C**

Default: 00h. Attribute: See below.

| Bits | Description |
|---|---|
| 7:6 | Reserved. |
| 5 | **SMIACK: system in locked state.** Read only. 1=The last SMI mode special cycle received by the IC indicated that the host is in system management mode. 0=The last SMI mode special cycle received by the IC indicated that the host is in not system management mode. |
| 4 | **LKLOCK: SMM access to the ROM access registers lock.** Read, write 1 only. This bit can only be set High by software; it is cleared by RESET#. 0=Write access to DevB:0x80, DevB:084, DevB:0x88, DevB:0x8C and DevB:0x43 enabled. 1=Write access to DevB:0x80, DevB:084, DevB:0x88, DevB:0x8C and DevB:0x43 only enabled in SMM mode (see DevB:0x80 or the definition of when the system is in SMM mode). |
| 3:0 | **OAR_ROB: OAR locks for rest of BIOS space.** Read-write. These four bits are defined identically to the OAR registers in DevB:0x80 and DevB:0x84. They apply to the BIOS ROM space across [FFEF_FFFFh:FFC0_0000h] (if the space is specified by DevB:0x43 to be BIOS). |

**Read-Write Register** **DevB:0x90**

Default: 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:0 | **RW.** Read-write. These bits are read-write accessible through software; they control no hardware. |

# 5.4 Legacy Registers

## 5.4.1 Miscellaneous Fixed IO Space Registers

These registers are in IO space, at fixed addresses. See Section 5.1.2 for a description of the register naming convention.

**AT Compatibility Register** **PORT61**

Default: 00h. Attribute: See below.

Fixed IO space; offset: 61h

| Bits | Description |
|---|---|
| 7 | **SERR: SERR# latch.** Read only. This bit is set High when SERR# is asserted and stays High until cleared by PORT61[CLRSERR]. The state of this bit is combined with RTC70[NMIDIS] and PORT61[IOCHK] to generate NMI interrupts. |
| 6 | **IOCHK: IOCHK# latch.** Read only. This bit is set High when the serial IRQ signal IOCHK# is asserted or if there is a *sync with error* message received on the LPC bus; it stays High until cleared by PORT61[CLRIOCHK]. The state of this bit is combined with RTC70[NMIDIS] and PORT61[SERR] to generate NMI interrupts. |
| 5 | **TMR2: programmable interval timer, timer number 2 output.** Read only. This bit provides the current state of the output signal from legacy PIT timer number 2. |
| 4 | **RSHCLK: refresh clock.** Read only. This bit toggles state at intervals specified by PIT timer 1 (normally, every 15 microseconds). |
| 3 | **CLRIOCHK: clear PORT61[IOCHK].** Read-write. 1=Bit[6] of this register, IOCHK, is asynchronously cleared. 0=PORT61[IOCHK] can be set High. |
| 2 | **CLRSERR: clear PORT61[SERR].** Read-write. 1=Bit[7] of this register, SERR, is asynchronously cleared. 0=PORT61[SERR] can be set High. |
| 1 | **SPKREN: speaker enable.** Read-write. 1=The output of PIT timer number 2 drives the SPKR pin. 0=SPKR is held Low. |
| 0 | **TMR2EN: programmable interval timer, timer number 2 enable.** Read-write. 1=PIT timer 2 is enabled to count. 0=PIT timer 2 is halted. |

**System Control Register** **PORT92**

Default: 00h. Attribute: See below.

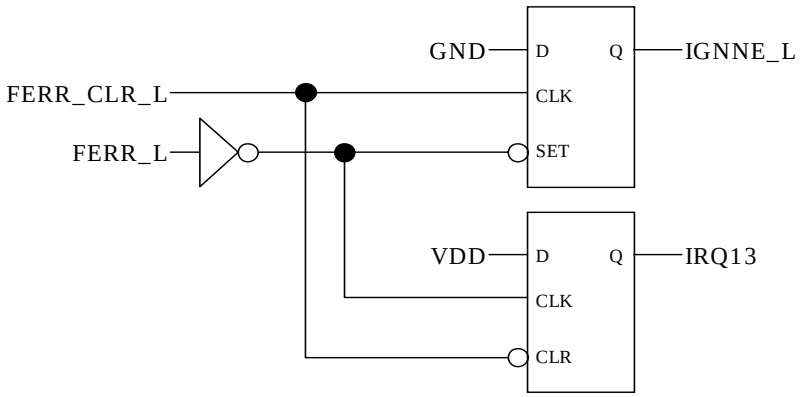
Fixed IO space; offset: 92h

| Bits | Description |
|---|---|
| 7:2 | Reserved. |
| 1 | **A20EN: CPU address bit 20 enable.** Write only; reads provide the current state of the A20M# pin rather than the state of the bit. The value written to this bit is ORed with the KA20G bit from the keyboard controller before being sent to the A20M# pin. In order for this register to control A20M#, KA20G must be Low. |
| 0 | **INITCPU: generate CPU initialization command.** Read-write. When this bit is Low and then written to a High, the IC asserts the INIT# pin. This bit must be written to a Low again before another INIT message can be sent. Note: use of this bit is enabled by DevB:0x41[P92FR]. |

**Fixed IO Ports F0 and F1 and the FERR# and IGNNE# Logic** **PORTF0 and PORTF1**

Default: 00h. Attribute: See below.

Fixed IO space; offset: F0h and F1h. FERR# is used to control IGNNE# and generate IRQ13 to the PIC and IOAPIC. The following diagram shows the logic. FERR_CLR# is asserted by (1) an IO write to F0h, (2) an IO write to F1h, (3) any processor reset command, and (4) PWROK reset; when any of these are active, FERR_CLR# goes Low.



**Level Sensitive IRQ Select Register** **PORT4D0**

Default: 0000h. Attribute: Read-write.

Fixed IO space; offset: 4D0h and 4D1h

| Bits | Description |
|---|---|
| 15:0 | **LIRQ: level sensitive IRQs.** Each of these 16 bits controls whether a corresponding IRQ line that enters the legacy PIC is edge sensitive (if the bit is Low) or level sensitive (if it is High). Edge sensitive interrupts must enter the PIC such that the rising edge generates the interrupt and level sensitive interrupts must enter the PIC as active Low; see Section 4.4.2.1 for details about how the interrupts are mapped to the PIC. The bit numbers correspond directly to the IRQ numbers (e.g., bit[12] controls IRQ12). Bits[0 and 2] are reserved (IRQ0 is always edge sensitive and IRQ2 does not exist). |

**System Reset Register** **PORTCF9**

Default: 00h. Attribute: See below.

Fixed IO space; offset: CF9h. Note: this register is enabled by DevB:3x41[PCF9EN]. Note: this register may be accessed only as a byte operation; 16- or 32-bit accesses to port CF8h are ignored by this register.

| Bits | Description |
|---|---|
| 7:4 | Reserved. |
| 3 | **FULLRST: full reset.** Read-write. 1=Full resets require the IC to place the system in the SOFF state for 3 to 5 seconds; full resets occur whenever (1) RSTCMD and SYSRST are both written High, (2) an AC power fail is detected (PWROK goes Low without the appropriate command), or (3) when PM46[2NDTO_STS] is set while DevB:3x48[NO_REBOOT]=0. 0=Full resets do not transition the system to SOFF; only the reset signals are asserted. |
| 2 | **RSTCMD: reset command.** Write-only; always reads as a zero. When this bit is written with a 1, a reset will be generated as specified by bits[3,1] of this register (bits[3,1] are observed in their state when RSTCMD is written to a 1; their previous value does not matter). |
| 1 | **SYSRST: system reset.** Read-write. This bit specifies whether a full system reset or a processor INIT is generated when PORTCF9[RSTCMD] is written to a 1. 1=Full system reset with RESET# and CPURST# asserted for about 1.8 milliseconds. 0=INIT# asserted for 16 PCI clocks. |
| 0 | Reserved. |

## 5.4.2 Legacy DMA Controller (DMAC) Registers

The legacy DMA controller (DMAC) in the IC supports the features required by the LPC I/F Specification Revision 1.0, which are a subset of legacy DMA Controllers. Single, demand, verify, and increment modes are supported. Block, decrement, cascade modes are not supported. Also, memory-to-memory transfers and external EOPs (end of process) are not supported.

There are 7 supported DMA channels. Channels 0-3 support 8-bit transfers and channels 5-7 support 16-bit transfers. There is no support for 32-bit DMA transfers. LPC Master device requests are made using channel 4.

Although not all registers in legacy DMA controllers are supported, the IO address locations for the unsupported registers are consistent with legacy logic. The implemented DMAC registers are listed in the following table.

| Name | Size | Number | Comments |
|---|---|---|---|
| Base Address Registers | 16 bits | 8 | 1 for each channel (0-7) (see note 1) |
| Base Word Count Registers | 16 bits | 8 | 1 for each channel (0-7) (see note 1) |
| Current Address Registers | 16 bits | 8 | 1 for each channel (0-7) (see note 1) |
| Current Word Count Registers | 16 bits | 8 | 1 for each channel (0-7) (see note 1) |
| Status Registers | 8 bits | 2 | 1 for Master and 1 for Slave DMAC |
| Command Registers | 1 bit | 2 | 1 for Master and 1 for Slave DMAC |
| Mode Registers | 5 bits | 8 | 1 for each channel (0-7) (see note 1) |
| Mask Registers | 4 bits | 2 | 1 for Master and 1 for Slave DMAC |

Note 1: although channel 4 base and current registers exist for compatibility, they are not used.

Note that not all bits in the command and mode registers of legacy DMA controllers are used in the IC's DMA controller. The bit usage for these registers are as follows.

Command Registers (Master and Slave DMAC)

| Bit | 8237 Function | DMAC Function of the IC |
|---|---|---|
| 7 | DACK sense | Obsolete |
| 6 | DREQ sense | Obsolete |
| 5 | Late/Extended write | Obsolete |
| 4 | Fixed/Rotating priority | Obsolete (always fixed priority) |
| 3 | Normal/Compressed timing | Obsolete |
| 2 | Controller enable/disable | Controller enable/disable |
| 1 | Ch0 address hold enable/disable | Obsolete |
| 0 | Memory-to-memory enable/disable | Obsolete |

Mode Registers (Master and Slave DMAC)

| Bit | 8237 Function | DMAC Function of the IC |
|---|---|---|
| 7:6 | 00b Demand mode select<br>01b Single mode select<br>10b Block mode select<br>11b Cascade mode select | 00b Demand mode select<br>01b Single mode select<br>10b Obsolete<br>11b Obsolete |
| 5 | Address increment/decrement select | Obsolete (always increment) |
| 4 | Auto initialization enable/disable | Auto initialization enable/disable |
| 3:2 | 00b Verify transfer<br>01b Write transfer<br>10b Read transfer<br>11b Illegal | 00b Verify transfer<br>01b Write transfer<br>10b Read transfer<br>11b Illegal |
| 1:0 | Channel select | Channel select |

Note 1: DMA channel 4 is hard-wired into cascade mode; however is obsolete for all other channels.

## 5.4.3 Legacy Programmable Interval Timer (PIT) Registers

These timers are halted from counting, if enabled to do so in DevB:3x4C[PIT_DIS], when PRDY is asserted.

Here are the ports used to access the legacy PIT:

| Offset | Access | Port |
|---|---|---|
| 40h | Write | Counter 0 write access port |
| | Read | Counter 0 read access port |
| 41h | Write | Counter 1 access port |
| | Read | Counter 1 read access port |
| 42h | Write | Counter 2 access port |
| | Read | Counter 2 read access port |
| 43h | Write | Control byte |
| | Read | Not supported |

**PIT Control Byte Register** **PORT43**

Default: 00h. Attribute: Write only.

Fixed IO space; offset: 43h

| Bits | Description |
|---|---|
| 7:6 | **SC[1:0]: select counter.** Specifies the counter that the command applies to as follows:<br>00b Counter 0.<br>01b Counter 1.<br>10b Counter 2.<br>11b Read back command. |
| 5:4 | **RW[1:0]: read-write command.** Specifies the read-write command as follows:<br>00b Counter latch command.<br>01b Read/write least significant byte only.<br>10b Read/write most significant byte only.<br>11b Read/write least significant byte followed by most significant byte. |
| 3:1 | **M[2:0]: counter mode.** Specifies the mode in which the counter selected by SC[1:0] will operate as follows:<br>000b Interrupt on terminal count.<br>001b Hardware retriggerable one-shot (not supported).<br>010b Rate generator.<br>011b Square wave mode.<br>100b Software triggered strobe.<br>101b Hardware triggered (retriggerable) strobe (not supported).<br>110b When this value is written, 010b is stored in the register, rate generator mode.<br>111b When this value is written, 011b is stored in the register, square wave mode. |
| 0 | **BCD: binary coded decimal.** 1=Counter specified by SC[1:0] operates in binary coded decimal. 0=Counter specified by SC[1:0] operates in 16-bit binary mode. |

## 5.4.4 Legacy Programmable Interrupt Controller (PIC)

The legacy dual-8259 programmable interrupt controller (PIC) includes a master, which is accessed through ports 20h and 21h and controls IRQ[7:0], and a slave, which is accessed through ports A0h and A1h and controls IRQ[15:8].

Here is a summary of the PIC registers.

| Offset | Access type | Register |
|---|---|---|
| 20h (master), A0h (slave) | Write only; D[4]=1b | Initialization command word 1 (ICW1) |
| | Write only; D[4:3]=00b | Operation command word 2 (OCW2) |
| | Read-write; D[4:3]=01b | Operation command word 3 (OCW3) |
| 21h (master), A1h (slave) | Write only | Initialization command word 2 (ICW2) |
| | Write only | Initialization command word 3 (ICW3) |
| | Write only | Initialization command word 4 (ICW4) |
| | Read-write | Operation command word 1 (OCW1) |

D[4:3] above refers to bits[4:3] of the associated 8-bit data field. Normally, once ICW1 is sent, ICW2, ICW3, and ICW4 are sent in that order before any OCW registers are accessed.

### Initialization Command Word 1 Register — ICW1

Fixed IO space; offset: 20h for master and A0h for slave; data bit[4] must be High. Attribute:Write only.

| Bits | Description |
|---|---|
| 7:5 | **A[7:5]: interrupt vector address.** These bits are not implemented. |
| 4 | This should always be High. |
| 3 | **LTIM: level triggered mode.** This bit is not implemented; PORT4D0 controls this function instead. |
| 2 | **ADI: call address interval.** This bit is not implemented. |
| 1 | **SNGL: single mode.** This bit must be programmed Low to indicate cascade mode. |
| 0 | **IC4: ICW4 needed.** This bit must be programmed High. |

### Initialization Command Word 2 Register — ICW2

Fixed IO space; offset: 21h for master and A1h for slave.Attribute: Write only.

| Bits | Description |
|---|---|
| 7:3 | **T[7:3].** Interrupt vector table base address bits[7:3]. |
| 2:0 | **A[10:8].** Obsolete. These bits must be programmed Low. |

### Initialization Command Word 3 for Master Register — ICW3M

Fixed IO space; offset: 21h. Attribute: Write only.

| Bits | Description |
|---|---|
| 7:0 | **SLAVES[7:0].** These bits must always be programmed to 04h. |

**Initialization Command Word 3 for Slave Register** **ICW3S**

Fixed IO space; offset: A1h. Attribute: Write only.

| Bits | Description |
|---|---|
| 7:3 | Reserved (must be programmed to all zeros). |
| 2:0 | **ID[2:0].** These bits must always be programmed to 02h. |

**Initialization Command Word 4 Register** **ICW4**

Fixed IO space; offset: 21h for master and A1h for slave.Attribute: Write only.

| Bits | Description |
|---|---|
| 7:5 | Reserved (must be programmed all zeros) |
| 4 | **SFNM. Special fully nested mode.** This bit is normally programmed Low. |
| 3:2 | **BUFF and MS.** These two are normally programmed to 00b for non-buffered mode. |
| 1 | **AEOI. Auto EOI.** This bit is ignored; the IC only operates in normal EOI mode (this bit Low). |
| 0 | **UPM. x86 mode.** This bit is ignored; the IC only operates in x86 mode (this bit High). |

**Operation Command Word 1 Register** **OCW1**

Fixed IO space; offset: 21h for master and A1h for slave.Attribute: Write only.

| Bits | Description |
|---|---|
| 7:0 | **MASK[7:0]. Interrupt mask.** 1=Interrupt is masked. Masking IRQ2 on the master interrupt controller will mask all slave-controller interrupts. |

**Operation Command Word 2 Register** **OCW2**

Fixed IO space; offset: 20h for master and A0h for slave; data bits[4:3] must be 00b. Attribute:Write only.

| Bits | Description |
|---|---|
| 7:5 | **R (bit 7), SL (bit 6), and EOI (bit 5).** These are decoded as:<br><br>R, SL, EOI — Function<br>000b — * Rotate in auto EOI mode clear.<br>001b — Non-specific EOI mode.<br>010b — No operation.<br>011b — Specific EOI command.<br>100b — * Rotate in auto EOI mode set<br>101b — Rotate on non-specific EOI command<br>110b — ** Set priority command<br>111b — ** Rotate on specific EOI command<br><br>* Not supported.<br>** Uses IRLEVEL field. |
| 4:3 | Reserved (must be programmed all zeros) |
| 2:0 | **IRLEVEL. Interrupt request level.** Specifies the interrupt request level to be acted upon. |

**Operation Command Word 3 Register** **OCW3**

Fixed IO space; offset: 20h for master and A0h for slave; data bits[4:3] must be 01b.Attribute:Write only.

| Bits | Description |
|---|---|
| 7 | Must be programmed Low. |
| 6:5 | **ESMM (bit 6) and SMM (bit 5).** Special mask mode. These are decoded as:<br>[ESMM, SMM] = 0Xb No action.<br>[ESMM, SMM] = 10b Reset special mask mode.<br>[ESMM, SMM] = 11b Set special mask mode. |
| 4:3 | 01b |
| 2 | **P: poll command.** 1=Poll enabled; next IO read of the interrupt controller treated like an interrupt acknowledge cycle. |
| 1:0 | **RR (bit 1) and RIS (bit 0). Read register command.** These are decoded as:<br>[RR,RIS] = 0Xb No action.<br>[RR,RIS] = 10b Read in-request (IR) register.<br>[RR,RIS] = 11b Read IS register. |

## 5.4.5 IOAPIC Registers

The IOAPIC register set for the 24 IOAPIC interrupts supported by the IC is indexed through two fixed-location, memory-mapped ports: FEC0_0000h, which provides the 8-bit index register, and FEC0_0010h, which provides the 32-bit data port. Writes to the 32-bit data port at FEC0_0010h must be 32-bit, aligned accesses; other than 32-bit writes result in undefined behavior. Reads provide all four bytes regardless of the byte enables.

The index register selects one of the following:

| Index | Description | Attribute | Default |
|---|---|---|---|
| 00h | APIC ID register. The ID is in bits[27:24]. All other bits are reserved. | Read-write | 0000 0000h |
| 01h | IOAPIC version register. | Read only | 0017 0011h |
| 02h | IOAPIC arbitration ID register. The ID is in bits[27:24]. All other bits are reserved. | Read only | 0000 0000h |
| 10h–3Fh | Redirection registers. Each of the 24 redirection registers utilizes two of these indexes. Bits[63:32] are accessed through the odd indexes and bits[31:0] are accessed through the even indexes. | Read-write | 0000 0000 0001 0000h |
| 40h–FFh | Reserved. | | |

The redirection registers are defined as follows:

| Bits | Description |
|---|---|
| 63:56 | **Destination.** In physical mode, bits[59:56] specify the APIC ID of the target processor. In logical mode bits[63:56] specify a set of processors. |
| 55:17 | Reserved. |
| 16 | **Interrupt mask.** 1=Interrupt is masked. |
| 15 | **Trigger mode.** 0=Edge sensitive. 1=Level sensitive. Note: this bit is ignored for delivery modes of SMI, NMI, Init, and ExtINT, which are always treated as edge sensitive. |
| 14 | **IRR: interrupt request receipt.** Set by hardware; cleared by hardware. This bit is not defined for edge-triggered interrupts. For level-triggered interrupts, this bit is set by the hardware after an interrupt is detected. It is cleared by receipt of EOI with the vector specified in bits[7:0]. |
| 13 | **Polarity.** 0=Active High. 1=Active Low. |
| 12 | **Delivery status.** 0=Idle. 1=Interrupt message pending. |
| 11 | **Destination mode.** 0=Physical mode. 1=Logical mode. |
| 10:8 | **Delivery mode.** 000b=fixed. 001b=Lowest priority. 010b=SMI. 011b=Reserved. 100b=NMI. 101=Init. 110b=Reserved. 111b=ExtINT. |
| 7:0 | **Interrupt vector.** |

Notes: normally all level triggered interrupts are programmed active Low and all edge triggered interrupts are programmed active High. Normally redirection register 0 (INTR) is programmed to be active High, edge triggered.

## 5.4.6 Real-Time Clock Registers

**Real-Time Clock Legacy Indexed Address** **RTC70**

IO mapped (fixed); offset: 70h. Default: 00. Attribute: Write only.

Note: RTC70[6:0] and RTC72 occupy the same physical register; after a write to RTC70, RTC72 will read back {0b, RTC70[6:0]}; after a write to RTC72, reads of RTC72 provide all 8 bits written. Note: RTC70 and RTC72 are on the VDD3 power plane; they are not preserved in the STR, STD, SOFF, or MOFF states.

| Bits | Description |
|---|---|
| 7 | **NMIDIS: NMI disable.** 1=Sources of NMIs (from serial IRQ logic and SERR# pin) are disabled from being able to generate NMI interrupts. Note: the state of this register is read accessible through DevB:0x41[NMIDIS]. |
| 6:0 | **RTCADDR: real-time clock address.** Specifies the address of the real-time clock CMOS RAM. The data port associated with this index is RTC71. Only the lower 128 bytes of the CMOS RAM are accessible through RTC70 and RTC71. |

### Real-Time Clock Legacy Data Port — RTC71

IO mapped (fixed); offset: 0071h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:0 | **RTCDATA: real-time clock data.** This is the data port for accesses to the real-time clock CMOS RAM that is indexed by RTC70. |

### Real-Time Clock 256-Byte Address and Data Port — RTC72 and RTC73

IO mapped (fixed); offsets: 0072h and 0073h. Attribute: Read-write.

These two 8-bit ports are similar to RTC70 and RTC71. However, RTC72, the address register, provides the full eight bits needed to access all 256 bytes of CMOS RAM. RTC73, the data port, provides access to the CMOS data indexed by RTC72. See RTC70 for details about reading RTC72.

### Real-Time Clock Alarm and Century Registers — RTC offsets 7F:7D

RTC indexed address space (indexed by RTC70); offsets: 7Dh, 7Eh, and 7Fh. Attribute: read-write. The day alarm, month alarm, and centenary value are stored in CMOS RAM indexed address space.

| RTC70; CMOS RAM offset | Function | Range for binary mode | Range for BCD mode |
|---|---|---|---|
| 7Dh | Date alarm | 01h–1Fh | 01h–31h |
| 7Eh | Month alarm | 01h–0Ch | 01h–12h |
| 7Fh | Century field | 13h–63h | 19h–99h |

Bits[7:6] of the date alarm (offset 7Dh) are reserved; writes to them have no effect and they always read back as zero. To place the RTC into 24-hour alarm mode, an invalid code must be written to bits[5:0] of the date alarm byte (any value other than 01h to 31h for BCD mode or 01h to F1h for hex mode). Refer to the ACPI specification for details of the month alarm field (offset 7Eh) and century field (offset 7Fh).

# 5.5 Enhanced IDE Controller Registers

## 5.5.1 Enhanced IDE Configuration Registers (DevB:1xXX)

These registers are located in PCI configuration space on the primary PCI interface, in the second device (device B), function 1. See Section 5.1.2 for a description of the register naming convention.

**EIDE Controller Vendor and Device ID Register** **DevB:1x00**

Default: 7441 1022h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:16 | **EIDE controller device ID.** |
| 15:0 | **Vendor ID.** |

**EIDE Controller Status and Command Register** **DevB:1x04**

Default: 0200 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:27 | Read only. These bits is fixed in the Low state. |
| 26:25 | **DEVSEL timing.** Read only. These bits are fixed at STATUS[10:9] = 01b. This specifies “medium” timing as defined by the PCI specification. |
| 24:3 | Read only. These bits are fixed at their default values. |
| 2 | **BMEN: bus master enable.** Read-write. 1=Enables IDE bus master capability. |
| 1 | **Memory space enable.** Read only. This bit is fixed in the Low state. |
| 0 | **IOEN: IO space enable.** Read-write. 1=Enables access to the IO space for the IDE controller. |

**EIDE Revision ID, Programming Interface, Sub Class and Base Registers** **DevB:1x08**

Default: 0101 8A04h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:24 | **BASECLASS.** Read only. These bits are fixed at 01h indicating a mass storage device. |
| 23:16 | **SUBCLASS.** Read only. These bits are fixed at 01h indicating an IDE controller. |
| 15 | **PROGIF[7]: master IDE capability.** Read only. This bit is fixed in the High state. |
| 14:12 | **PROGIF[6:4].** Read only. These bits are fixed in the Low state. |
| 11 | **PROG IF[3]: secondary native/compatibility mode selectable.** Read only. This is High to indicate that PROGIF[2] is read-write. |
| 10 | **PROGIF[2]: secondary native mode.** Read-write. 0=Compatibility mode for secondary port; DevB:1x18 and DevB:1x1C are ignored and not visible; address decode is based on legacy addresses 170h–177h, 376h; DevB:1x3C[7:0] read only zeros; DevB:1x3C[15:8] = 00h; IRQ15 may be used by the IDE controller. 1=Native mode; DevB:1x18 and DevB:1x1C are visible and used for address decode; DevB:1x3C[7:0] read-write; DevB:1x3C[15:8] = 01h; IRQ15 mapped to PIRQA per 4.4.2.1 and used exclusively by the secondary IDE port. |
| 9 | **PROGIF[1]: primary native/compatibility mode selectable.** Read only. This is High to indicate that PROGIF[0] is read-write. |
| 8 | **PROGIF[0]: primary native mode.** Read-write. 0=Compatibility mode for primary port; DevB:1x10 and DevB:1x14 are ignored and not visible; address decode is based on legacy addresses 1F0h–1F7h, 3F6h; DevB:1x3C[7:0] read only zeros; DevB:1x3C[15:8] = 00h; IRQ14 may be used by the IDE controller. 1=Native mode; DevB:1x10 and DevB:1x14 are visible and used for address decode; DevB:1x3C[7:0] read-write; DevB:1x3C[15:8] = 01h; IRQ14 mapped to PIRQA per 4.4.2.1 and used exclusively by the primary IDE port. |
| 7:0 | **REVISIONID.** Read only. EIDE Controller silicon revision. |

**EIDE Controller BIST, Header and Latency Register** **DevB:1x0C**

Default: 0000 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:24 | **BIST.** Read only. These bits fixed at their default values. |
| 23:16 | **HEADER.** Read only. These bits fixed at their default values. |
| 15:8 | **LATENCY.** Read-write. This field controls no hardware. |
| 7:0 | **CACHE.** Read only. These bits fixed at their default values. |

**EIDE Controller Primary Command Base Address** **DevB:1x10**

Default: 0000 01F1h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:3 | **BASE[31:3] Port Address.** Read-write. These bits specify an 8-byte IO address space that maps to the ATA-compliant command register set for the primary port (legacy IO space 1F0h through 1F7h). ***Note:*** *When DevB:1x08[8] is Low, the primary port is in compatibility mode and this register is ignored and not visible (reads as 0h). When DevB:1x08[8] is High, this register is visible regardless of DevB:1x40[PRIEN].* |
| 2:0 | Read only. 001b. |

**EIDE Controller Primary Control Base Address** **DevB:1x14**

Default: 0000 03F5h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:2 | **BASE[31:2] Port Address.** Read-write. These bits specify a 4-byte IO address space that maps to the ATA-compliant control register set for the primary port (legacy IO space 3F6h). ***Notes:*** *When DevB:1x08[8] is Low, the primary port is in compatibility mode and this register is ignored and not visible (reads as 0h).* *Only byte 2 of this space is used. BASE[2] must be 1.* *When DevB:1x08[8] is High, this register is visible regardless of DevB:1x40[PRIEN].* |
| 1:0 | Read only. 01b. |

**EIDE Controller Secondary Command Base Address** **DevB:1x18**

Default: 0000 0171h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:3 | **BASE[31:3] Port Address.** Read-write. These bits specify an 8-byte IO address space that maps to the ATA-compliant command register set for the secondary port (legacy IO space 170h through 177h). ***Note:*** *When DevB:1x08[10] is Low, the secondary port is in compatibility mode and this register is ignored and not visible (reads as 0h). When DevB:1x08[10] is High, this register is visible regardless of DevB:1x40[SECEN].* |
| 2:0 | Read only. 001b. |

**EIDE Controller Secondary Control Base Address** **DevB:1x1C**

Default: 0000 0375h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:2 | **BASE[31:2] Port Address.** Read-write. These bits specify a 4-byte IO address space that maps to the ATA-compliant control register set for the secondary port (legacy IO space 376h).<br>***Notes:*** *When DevB:1x08[10] is Low, the secondary port is in compatibility mode and this register is ignored and not visible (reads as 0h).*<br>*Only byte 2 of this space is used. BASE[2] must be 1.*<br>*When DevB:1x08[10] is High, this register is visible regardless of DevB:1x40[SECEN].* |
| 1:0 | Read only. 01b. |

**EIDE Controller Bus Master Control Registers Base Address** **DevB:1x20**

Default: 0000 CC01h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:4 | **BASE[31:4] Port Address.** Read-write. This field specifies the 16-byte IO address space that maps to the EIDE controller register set that is compliant with the SFF 8038I specification (Bus Master Programming Interface for IDE ATA Controllers), IBMx. |
| 3:0 | Read only. 0001b. |

**EIDE Subsystem ID and Subsystem Vendor ID Register** **DevB:1x2C**

Default: 0000 0000h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:16 | **SSID: subsystem ID register.** This field is write accessible through DevB:1x70. |
| 15:0 | **SSVENDORID: subsystem vendor ID register.** This field is write accessible through DevB:1x70. |

**EIDE Controller Interrupt Line, Interrupt Pin, Min. Grant, Max Latency Register** **DevB:1x3C**

Default: 0000 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:24 | **MAX LATENCY.** Read only. These bits are fixed at their default values. |
| 23:16 | **MIN GNT.** Read only. These bits are fixed at their default values. |
| 15:8 | **INTERRUPT PIN.** Read only. When either DevB:1x08[8] or DevB:1x08[10] is High, then field reads as 01h. When they are both Low, then it reads as 00h. |
| 7:0 | **INTERRUPT LINE.** This register is either read-write or read only based on the state of DevB:1x08[10,8]. When either DevB:1x08[8] or DevB:1x08[10] is High, then this is a read-write register. When they are both Low, then it is a read only register, reading 00h. |

**EIDE Controller Configuration Register** **DevB:1x40**

Default: 0000 04?0h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:24 | Reserved. |
| 23:20 | **RW.** Read-write. These bits are read-write accessible through software; they control no hardware. |
| 19:16 | **CABLE.** Read-write. These bits are intended to be programmed by BIOS to specify the cable type of each of the IDE drives to the driver software. 1=High speed 80-pin cable is present. The bits specify the following drive:<br>Bit[16]: primary master. Bit[18]: secondary master.<br>Bit[17]: primary slave. Bit[19]: secondary slave. |
| 15 | **RW.** Read-write. This bit is read-write accessible through software; it controls no hardware. |
| 14 | **PRIPWB: primary post write buffer.** Read-write. 1=The primary port posted-write buffer for PIO modes is enabled. Note: only 32-bit writes to the data port are allowed when the when this bit is set. |
| 13 | **RW.** Read-write. This bit is read-write accessible through software; it controls no hardware. |
| 12 | **SECPWB: secondary post write buffer.** Read-write. 1=The secondary port posted-write buffer for PIO modes is enabled. Note: only 32-bit writes to the data port are allowed when the when this bit is set. |
| 11 | **PHYOR: ATA-100 phy override.** Read-write. 1=UDMA100 phy layer slew rate controlled by DevB:1x40[PHYORSEL]. 0=UDMA100 phy slew rate controlled by phy select circuitry observed in DevB:1x40[PHYSEL]. |
| 10:8 | **PHYORSEL: ATA-100 phy override select.** Read-write. These specify the override value of the phy speed select, as specified by DevB:1x40[PHYSEL]. This field is ignored when DevB:1x40[PHYOR]=0. |
| 7:5 | **PHYSEL: phy speed select.** Read only. These specify the selected phy speed selection as follows: x00b=bigger phy resistor (fast corner); x10b=medium phy resistor; xx1b=smaller phy resistor (slow corner). The power-up default for these bits is device specific. |
| 4:2 | Reserved. These bits are fixed at their default values. The default for bit[4] is 0. |
| 1 | **PRIEN: primary channel enable.** Read-write. 1=The primary port of the EIDE controller is enabled. |
| 0 | **SECEN: secondary channel enable.** Read-write. 1=The secondary port of the EIDE controller is enabled. |

**EIDE Controller Drive Timing Control Register** **DevB:1x48**

Default: A8A8 A8A8h. Attribute: Read-write.

This register specifies timing for PIO data transfers (not 171h though 177h or 1F1h though 1F7h) and multi-word DMA transfers. The value in each 4-bit field, plus one, specifies a time in 30 nanosecond PCI clocks.

Note: the default state, A8h, results in a recovery time of 270ns and an active pulse width of 330ns for a 30ns PCI clock (total cycle time = 600ns) which corresponds to ATA PIO Mode 0.

***Note:*** *PIO modes are controlled via DevB:1x48 and DevB:1x4C. To set the timing associated with the various modes, DevB:1x4C should be left at its default value and the appropriate byte of DevB:1x48 should be programmed as follows: mode 0=A8h; mode 1=65h; mode 2=42h; mode 3=22h; mode 4=20h.*

| Bits | Description |
|---|---|
| 31:28 | **PD0PW[3:0]: primary drive 0 active pulse width.** |
| 27:24 | **PD0RT[3:0]: primary drive 0 minimum recovery time.** |
| 23:20 | **PD1PW[3:0]: primary drive 1 active pulse width.** |
| 19:16 | **PD1RT[3:0]: primary drive 1 minimum recovery time.** |
| 15:12 | **SD0PW[3:0]: secondary drive 0 active pulse width.** |
| 11:8 | **SD0RT[3:0]: secondary drive 0 minimum recovery time.** |
| 7:4 | **SD1PW[3:0]: secondary drive 1 active pulse width.** |
| 3:0 | **SD1RT[3:0]: secondary drive 1 minimum recovery time.** |

### EIDE Controller Cycle Time and Address Setup Time Register — DevB:1x4C

Default: FFFF 00FFh. Attribute: Read-write.

For bits[7:0] the value in each 2-bit field, plus one, specifies the address setup time in 30 nanosecond PCI clocks; this applies to all PIO and multi-word DMA cycles. For bits[31:16] the value in each 4-bit field, plus one, specifies the time in 30 nanosecond PCI clocks; this applies address ports 171h though 177h, 1F1h though 1F7h, 376h, and 3F6h; for 170h and 1F0h, see DevB:1x48.

| Bits | Description |
|---|---|
| 31:28 | **PXPW[3:0]: primary non-1F0 DIOR#/DIOW# active pulse width.** |
| 27:24 | **PXRT[3:0]: primary non-1F0 DIOR#/DIOW# recovery time.** |
| 23:20 | **SXPW[3:0]: secondary non-170 DIOR#/DIOW# active pulse width.** |
| 19:16 | **SXRT[3:0]: secondary non-170 DIOR#/DIOW# recovery time.** |
| 15:8 | Reserved. |
| 7:6 | **P0ADD[1:0]: primary drive 0 address setup time.** |
| 5:4 | **P1ADD[1:0]: primary drive 1 address setup time.** |
| 3:2 | **S0ADD[1:0]: secondary drive 0 address setup time.** |
| 1:0 | **S1ADD[1:0]: secondary drive 1 address setup time.** |

**EIDE Controller UDMA Extended Timing Control Register** **DevB:1x50**

Default: 0303 0303h. Attribute: Read-write.

The definition of each of the four 8-bit fields in this register are identical; they apply to different drives.

| Bits | Description |
|---|---|
| 31:24 | **P0UDMA: primary drive 0 UDMA timing control.** |
| 23:16 | **P1UDMA: primary drive 1 UDMA timing control.** |
| 15:8 | **S0UDMA: secondary drive 0 UDMA timing control.** |
| 7:0 | **S1UDMA: secondary drive 1 UDMA timing control.** |

Here is the definition of each 8-bit field:

| Bits | Description |
|---|---|
| 31, 23, 15, 7 | **[P0, P1, S0, S1]ENMODE: [primary, secondary] drive [0,1] ultra-DMA mode enable method.** 1=Enable ultra-DMA by setting bit 6 of this 8-bit register. 0=Enable ultra-DMA by detecting the "Set Feature" ATA command. |
| 30, 22, 14, 6 | **[P0, P1, S0, S1]UDMAEN: [primary, secondary] drive [0,1] ultra-DMA mode enable.** 1=Ultra-DMA mode is enabled. |
| 29:27, 21:19, 13:11, 5:3 | Reserved. |
| 26:24, 18:16, 10:8, 2:0 | **[P0, P1, S0, S1]CYCT[2:0]: [primary, secondary] drive [0,1] Cycle Time.**<br><br>**CYCT[2:0]** — **Ultra-DMA mode** — **Cycle time**<br>000b — UDMA mode 2 (ATA33) — 60 nanoseconds<br>001b — UDMA mode 1 — 90 nanoseconds<br>010b — UDMA mode 0 — 120 nanoseconds<br>011b — Slow UDMA mode 0 — 150 nanoseconds<br>100b — UDMA mode 3 (ATA44) — 45 nanoseconds<br>101b — UDMA mode 4 (ATA66) — 30 nanoseconds<br>110b — UDMA mode 5 (ATA100) — 20 nanoseconds |

**EIDE Power Management Register** **DevB:1x54**

Default: 00h. Attribute: See below.

This register controls the power state of the two IDE ports. When an IDE port is powered up, it is fully operational. When it is powered down, outputs DADDR[S,P][2:0], DCS1[S,P]#, DCS3[S,P]#, DDACK[S,P]#, DIO[R,W][S,P]# and DRST[S,P]# are forced Low; DDATA[S,P][15:0], DDRQ[S,P], and DRDY[S,P] are ignored and in high-impedance mode. When transitioning into the power-down state, DRST[S,P]# assertion leads control over the rest of the signals by about 1 microsecond. When transitioning into the power-up state, DRST[S,P]# deassertion lags control over the rest of the signals by about 1 microsecond.
***Note:*** *writes to [S,P]PWRDN cause [S,P]PWRX to be set High until the power state transition is complete; while [S,P]PWRX is High, writes to [S,P]PWRDN are ignored.*

| Bits | Description |
|---|---|
| 7: 6 | Reserved. |
| 5 | **SPWRX. Power state transition for secondary IDE port.** Read only. 1=The secondary IDE port is transitioning from either the power-down state to the power up state (if SPWRDN = 0) or from the power-up state to the power-down state (if SPWRDN = 1). |
| 4 | **SPWRDN. Power down secondary IDE port.** Writing a 1 to this field causes the hardware to transition the secondary port from the powered-up state to the powered-down state. Writing a 0 to this field causes the hardware to transition the secondary port from the powered-down state to the powered-up state. When read, this bit reflects the last state written to it; however, it cannot be altered when SPWRX is High. |
| 3:2 | Reserved. |
| 1 | **PPWRX. Power state transition for primary IDE port.** Read only. 1=The primary IDE port is transitioning from either the power-down state to the power up state (if PPWRDN = 0) or from the power-up state to the power-down state (if PPWRDN = 1). |
| 0 | **PPWRDN. Power down primary IDE port.** Writing a 1 to this field causes the hardware to transition the primary port from the powered-up state to the powered-down state. Writing a 0 to this field causes the hardware to transition the primary port from the powered-down state to the powered-up state. When read, this bit reflects the last state written to it; however, it cannot be altered when PPWRX is High. |

**Read-Write Register** **DevB:1x58**

Default: 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:0 | **RW.** Read-write. These bits are read-write accessible through software; they control no hardware. |

**EIDE Device and Subsystem ID Read-Write Register** **DevB:1x70**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:16 | **SSID: subsystem ID register.** The value placed in this register is visible in DevB:1x2C[31:16]. |
| 15:0 | **SSVENDORID: subsystem vendor ID register.** The value placed in this register is visible in DevB:1x2C[15:0]. |

## 5.5.2 EIDE Bus Master IO Registers

These registers are located in IO space. The base address register is DevB:1x20. See Section 5.1.2 for a description of the register naming convention.

These registers comply with SFF 8038i for control of DMA transfers between drives and system memory.

**Primary Bus Master IDE Command Register** **IBM0**

Default: 00h. Attribute: See below.

| Bits | Description |
|---|---|
| 7:4 | Reserved. |
| 3 | **RW: read or write control.** Read-write. 1=Read cycles specified (read from the drive; write to system memory). 0=Write cycles specified. |
| 2:1 | Reserved. |
| 0 | **STSP: start/stop bus master.** Write only; reads always return 0. |

**Primary Bus Master IDE Status Register** **IBM2**

Default: 00h. Attribute: See below.

| Bits | Description |
|---|---|
| 7 | **Simplex only.** Read only. |
| 6 | **DMA1C: drive 1 DMA capable.** Read-write |
| 5 | **DMA0C: drive 0 DMA capable.** Read-write. |
| 4:3 | Reserved. |
| 2 | **IRQ: interrupt.** Read; set by hardware; write 1 to clear. This bit is set by the rising edge of the IDE interrupt line. |
| 1 | **ERR: error.** Read; write 1 to clear. |
| 0 | **ACTV: bus master IDE active.** Read only. |

**Primary Bus Master IDE PRD Table Address Register** **IBM4**

Default: 0000 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:2 | **PPRDADD[31:2]: primary physical region descriptor table base address.** Read-write. |
| 1:0 | **PPRDADD[1:0].** Read only. These bits are fixed in the Low state. |

**Secondary Bus Master IDE Command Register** **IBM8**

Default: 00h. Attribute: See below.

| Bits | Description |
|---|---|
| 7:4 | Reserved. |
| 3 | **RW: read or write control.** Read-write. 1=Read cycles specified (read from the drive; write to system memory). 0=Write cycles specified. |
| 2:1 | Reserved. |
| 0 | **STSP: start/stop bus master.** Write only; reads always return 0. |

**Secondary Bus Master IDE Status Register** **IBMA**

Default: 00h. Attribute: See below.

| Bits | Description |
|---|---|
| 7 | **Simplex only.** Read only. |
| 6 | **DMA1C: drive 1 DMA capable.** Read-write |
| 5 | **DMA0C: drive 0 DMA capable.** Read-write. |
| 4:3 | Reserved. |
| 2 | **IRQ: interrupt.** Read; set by hardware; write 1 to clear. This bit is set by the rising edge of the IDE interrupt line. |
| 1 | **ERR: error.** Read; write 1 to clear. |
| 0 | **ACTV: bus master IDE active.** Read only. |

**Secondary Bus Master IDE PRD Table Address Register** **IBMC**

Default: 0000 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:2 | **SPRDADD[31:2]: secondary physical region descriptor table base address.** Read-write. |
| 1:0 | **SPRDADD[1:0].** Read only. These bits are fixed in the Low state. |

# 5.6 USB Controller Registers

## 5.6.1 USB Host Controller Configuration Registers (Dev0:0xXX)

These registers are located in PCI configuration space on the secondary PCI interface, device 0, function 0. See Section 5.1.2 for a description of the register naming convention.

**USB Controller Vendor and Device ID Register** **Dev:0:0x00**

Default: 7449 1022h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:16 | **USB controller device ID.** |
| 15:0 | **Vendor ID.** |

**USB Controller Status and Command Register** **Dev:0:0x04**

Default: 0280 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:30 | Reserved. |
| 29 | **Signaled master abort.** Read; write 1 to clear. This bit is set High by the hardware when a bus master cycle is terminated with a master abort. |
| 28 | **Received target abort.** Read; write 1 to clear. This bit is set High by the hardware when a target abort command is received during a master cycle. |
| 27 | Reserved. |
| 26:25 | **DEVSEL timing.** Read only. These bits are fixed at 01b and specifies “medium” timing as defined by the PCI specification. |
| 24:9 | Read only. These bits are fixed at their default values. |
| 8 | **SERR# detection enable.** Read-write. This bit has no effect on the hardware. |
| 7:5 | Reserved. |
| 4 | **Memory write and invalidate enable.** Read-write. 1=Enables bus master to issue memory write and invalidate cycles. |
| 3 | Reserved. |
| 2 | **Bus master enable.** Read-write. 1=Enables bus master capability. |
| 1 | **Memory space enable.** Read-write. 1=Enables access to the memory space for this device (the host controller registers). |
| 0 | **IO space enable.** Read-write. 1=Enables access to the IO space for this device (the keyboard/mouse controller ports for legacy emulation). |

**USB Revision ID, Programming Interface, Sub Class and Base Registers** **Dev:0:0x08**

Default: 0C03 1007h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:24 | **BASECLASS.** |
| 23:16 | **SUBCLASS.** |
| 15:8 | **PROGIF.** |
| 7:0 | **REVISIONID.** |

**USB Controller BIST, Header, Latency, and Cacheline Size Register** **Dev:0:0x0C**

Default: 0000 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:24 | **BIST.** Read only. These bits fixed at their default values. |
| 23:16 | **HEADER.** Read only. These bits fixed at their default values. |
| 15:8 | **LATENCY.** Bits[7:3] are read-write; bits[2:0] are read-only at their default value. |
| 7:0 | **CACHE.** Read-write. 08h=32 Bytes, 00h=0 Bytes. No other values are allowed. |

**USB Controller Base Address Register** **Dev:0:0x10**

Default: 0000 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:12 | **BASE[31:12] Base Address.** Read-write. These bits specify a 4-kilobyte non-prefetchable space that can be placed anywhere in 32-bit memory. |
| 11:0 | Read only. These bits fixed at their default values. |

**USB Subsystem ID and Subsystem Vendor ID Register** **Dev:0:0x2C**

Default: 0000 0000h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:16 | **SSID: subsystem ID register.** This field is write accessible through Dev0:0x70. |
| 15:0 | **SSVENDORID: subsystem vendor ID register.** This field is write accessible through Dev0:0x70. |

**Controller Interrupt Line, Interrupt Pin, Min. Grant, Max Latency Register** **Dev:0:0x3C**

Default: 5000 0400h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:24 | **MAX LATENCY.** Read only. This register indicates how often the USB controller requires host accesses. The value 50h indicates 20 microseconds. |
| 23:16 | **MIN GNT.** Read only. These bits are fixed at their default values. |
| 15:8 | **INTERRUPT PIN.** Read only. The value 04h indicates that USB interrupts are routed through PIRQD# |
| 7:0 | **INTERRUPT LINE.** Read-write. This field controls no hardware. |

**USB Buffer Control Register** **Dev:0:0x44**

Default: 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:9 | Reserved. |
| 8 | **PIPDIS: SIE pipelining disable.** Read-write. 1=Transfer descriptors are disabled from being pipelined with USB bus activity. |
| 7:1 | Reserved. |
| 0 | **DB16: data buffer region 16.** Read-write. 1=The size of the region for the data buffer is 16 bytes. 0=The region is 32 bytes. |

**USB Device and Subsystem ID Read-Write Register** **Dev:0:0x70**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:16 | **SSID: subsystem ID register.** The value placed in this register is visible in Dev0:0x2C[31:16]. |
| 15:0 | **SSVENDORID: subsystem vendor ID register.** The value placed in this register is visible in Dev0:0x2C[15:0]. |

## 5.6.2 USB Host Controller Memory-Mapped Registers

### 5.6.2.1 Summary

For a complete description of the following registers, see the *Open Host Controller Interface Specification Version 1.1* (OpenHCI).

| Offset | Register | Offset | Register |
|---|---|---|---|
| 00-03 | HcRevision | 34-37 | HcFmInterval |
| 04-07 | HcControl | 38-3B | HcFrameRemaining |
| 08-0B | HcCommandStatus | 3C-3F | HcFmNumber |
| 0C-0F | HcInterruptStatus | 40-43 | HcPeriodicStart |
| 10-13 | HcInterruptEnable | 44-47 | HcLSThreshold |
| 14-17 | HcInterruptDisable | 48-4B | HcRhDescriptorA |
| 18-1B | HcHCCA | 4C-4F | HcRhDescriptorB |
| 1C-1F | HcPeriodCurrentED | 50-53 | HcRhStatus |
| 20-23 | HcControlHeadED | 54-57 | HcRhPortStatus[1] |
| 24-27 | HcControlCurrentED | 58-5B | HcRhPortStatus[2] |
| 28-2B | HcBulkHeadED | 5C-5F | HcRhPortStatus[3] |
| 2C-2F | HcBulkCurrentED | 60-63 | HcRhPortStatus[4] |
| 30-33 | HcDoneHead | 100 | HceControl |
| | | 104 | HceInput |
| | | 108 | HceOutput |
| | | 10C | HceStatus |

#### 5.6.2.2 Implementation-Specific Items

- *HcRevision[7:0]* is 10h to indicate that it conforms to OpenHCI 1.0.
- *HcRevision[8]* is 1 to indicate that legacy keyboard & mouse emulation support is present.
- *HcFmInterval_FSLargestDataPacket* resets to 0.
- *HcRhDescriptorA_NumberDownstreamPorts* is hardwired to 4.
- *HcRhDescriptorA_NoPowerSwitching* resets to 1.
- *HcRhDescriptorA_PowerSwitchingMode* and *HcRhDescriptorA_OverCurrentProtectionMode* must not be set and reset to 0.
- *HcRhDescriptorA_PowerOnToPowerGoodTime* resets to 1 (representing 2 ms), and can only hold the values 0 to 3 (0 to 6 ms).
- *HcRhDescriptorA_NoOverCurrentProtection* resets to 0.
- *HcRhDescriptorB_DeviceRemovable* resets to 0 and should be set by BIOS if non-removable devices are attached.
- *HcRhDescriptorB_PortPowerControlMask* resets to 0 and should not be set.
- Because power switching is not implemented, the set and clear power bits in *HcRhStatus* and *HcRhPortStatus[1-4]* are not supported.
- *HceControl* and *HceStatus* reset to 00h.
- *HceInput* and *HceOutput* are not reset.
- *HcDoneHd[31:4]* should not be modified.
- *HcFmInterval_FSLargestDataPacket* is limited to 14 bits. Bit 15 is read-only 0.
- *HcFmNumber* should not be modified.

# 5.7 System Management Registers

## 5.7.1 System Management Configuration Registers (DevB:3xXX)

These registers are located in PCI configuration space on the primary PCI interface, in the second device (device B), function 3. See Section 5.1.2 for a description of the register naming convention.

**System Management Vendor and Device ID Register** **DevB:3x00**

Default: 7443 1022h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:16 | **System management device ID.** |
| 15:0 | **Vendor ID.** |

**System Management Status and Command Register** **DevB:3x04**

Default: 0280 0000h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:0 | These bits are fixed at their default values. |

**System Management Revision and Class Code Register** **DevB:3x08**

Default: 0000 0003h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:8 | **CLASSCODE.** This field is write accessible through DevB:3x60. |
| 7:0 | **REVISION.** System management silicon revision. |

**System Management BIST-Header-Latency-Cache Register** **DevB:3x0C**

Default: 0000 1600h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:24 | **BIST.** Read only. These bits fixed at their default values. |
| 23:16 | **HEADER.** Read only. These bits fixed at their default values. |
| 15:8 | **LATENCY.** Read-write. This field controls no hardware. |
| 7:0 | **CACHE.** Read only. These bits fixed at their default values. |

**System Management Subsystem ID and Subsystem Vendor ID Register** **DevB:3x2C**

Default: 0000 0000h. Attribute: Read only.

| Bits | Description |
|---|---|
| 31:16 | **SSID: subsystem ID register.** This field is write accessible through DevB:3x7C. |
| 15:0 | **SSVENDORID: subsystem vendor ID register.** This field is write accessible through DevB:3x7C. |

**General Configuration 1 Register** **DevB:3x40**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7 | **RNGEN: random number generated enable.** Read; write to 1 only. 1=The RNG (accessible through PMF0 and PMF4) is enabled to generate random numbers. 0=The RNG is disabled. This bit can only be written to a 1; writing a 0 has no effect. |
| 6 | **STOPTMR: stop ACPI timer from counting.** 1=ACPI timer, PM08, stops counting (frozen in its current state). 0=ACPI timer enabled to count. |
| 5:4 | **THMINEN: throttling minimum enable time.** These bits specify the minimum time in which STPCLK# is held in the deasserted state during throttling (normal or thermal), regardless of the state of the throttling duty cycle registers, DevB:3x4D and PM10. These bits do not affect the throttling cycle period; if the throttling duty cycle specifies a STPCLK# deassertion time that is less than specified by this register, then the STPCLK# assertion time is reduced. This has no effect on throttling in which the period is 244 microseconds.<br><br>THMINEN — Time<br>00b — None.<br>01b — 10 microseconds.<br>10b — 20 microseconds.<br>11b — Reserved. |
| 3 | **NTPER: normal throttling period.** 1=Normal throttling cycle period specified to be 244 microseconds (from an asserting edge of STPCLK# to the next asserting edge). 0=Normal throttling period specified to be 30 microseconds. |
| 2 | **TTPER: thermal throttling period.** 1=Thermal throttling cycle period specified to be 244 microseconds (from an asserting edge of STPCLK# to the next asserting edge). 0=Thermal throttling period specified to be 30 microseconds. |
| 1 | Reserved. |
| 0 | **TH2SD: throttling 2 second delay.** 1=There is a 2.0 to 2.5 second delay after THERM# is asserted before thermal throttling is initiated, as specified by DevB:3x4D. 0=Initiate throttling immediately after THERM# is asserted. |

**General Configuration 2 Register** **DevB:3x41**

Default: 40h. Attribute: See below.

| Bits | Description |
|---|---|
| 7 | **PMIOEN: system management IO space enable.** Read-write. 1=PMxx, the IO space specified by DevB:3x58, is enabled. |
| 6 | **TMRRST: ACPI timer reset.** Read-write. 1=The ACPI timer, PM08, is asynchronously cleared at all times. 0=The timer is allowed to count. |
| 5 | **PCF9EN: port CF9 enable.** Read-write. 1=Access to PORTCF9 is enabled. |
| 4 | **PBIN: power button in.** Read only. This bit reflect the current state of the PWRBTN# pin (before the debounce circuit). 0=PWRBTN# is currently asserted. |
| 3 | **TMR32: timer size selection.** Read-write. 0=The ACPI timer, PM08, is 24 bits. 1=The ACPI timer is 32 bits. |
| 2:1 | Reserved. |
| 0 | **W4SG: wait for Stop Grant before deasserting STPCLK#.** Read-write. 1=After STPCLK# is asserted for any reason, it will not be deasserted until the corresponding Stop Grant cycle is received. This bit should always be set High. Note: for power state transitions that use the Stop Grant cycle as part of the sequence, this bit is ignored and the Stop Grant cycle is always required. |

**SCI Interrupt Configuration Register** **DevB:3x42**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:4 | Reserved. |
| 3:0 | **SCISEL: SCI interrupt selection.** This field specifies the IRQ number routed to the interrupt controllers used for ACPI-defined SCI interrupts. A value of 0h disables SCI interrupts. Values of 2h, 8h, and Dh are reserved. All other values are valid. See 4.4.2.1 for details about SCI interrupt routing. |

**Previous Power State Register** **DevB:3x43**

Default: See field specifications below. Attribute: See below.

| Bits | Description |
|---|---|
| 7 | **VDDA_STS: VDD_AL reset status.** Read; set by hardware; write 1 to clear. 1=VDD_AL became invalid. This bit resides on the VDD_AL plane. |
| 6 | **G3TOS5: mechanical off (G3) to soft off (S5).** Read; write. 0=When power is applied to the VDD_AUX planes, the system automatically transitions into the FON state. 1=When power is a applied to the VDD_AUX planes, the system enters the SOFF state. This bit resides on the VDD_AL plane. When VDD_AL powers up, this bit defaults to 0; when there is a RESET# generated by a write to PORTCF9[RSTCMD, SYSRST] == 11b, then this bit is cleared. |
| 5:3 | **PWRFL_STS: power failure status.** Read; updated by hardware; write 1 to LSB to reset to 4h. If power fails (system enters MOFF or PWROK goes from 1 to 0 while PWRON# is asserted), then this register captures and retains the state the system was in when the failure occurred. This field resides on the VDD_AL plane. This field defaults to 4h when VDD_AL powers up. Writing a one to DevB:3x43[3] sets this field to 4h; writing a zero to DevB:3x43[3] or writing any value to any other bits in this field has no effect. Here are the possible states:<br><br>PWRFL_STS — Power state<br>0h — FON full on<br>1h — POS power on suspend<br>2h — C2<br>3h — C3<br>4h — No AC power failure<br>5h — STR suspend to RAM<br>6h — STD suspend to disk<br>7h — SOFF soft off |
| 2:0 | PPSTATE. Previous power state; Read only. This field holds the most previous power state from which the system came into the FON state. This field resides on the VDD_AUX plane. Here are the possible states:<br><br>PPSTATE — Power state<br>0h — Reserved<br>1h — POS power on suspend<br>2h — C2<br>3h — C3<br>4h — MOFF mechanical off<br>5h — STR suspend to RAM<br>6h — STD suspend to disk<br>7h — SOFF soft off |

**PNP IRQ Select Register** **DevB:3x44**

Default: 0000h. Attribute: Read-write.

Bits[11:0] assign PNPIRQ[2:0] pins to IRQs that are routed to interrupt controllers; see Section 4.4.2.1 for more details.

| Bits | Description |
|---|---|
| 15 | **TCO_INT_EN: TCO interrupt enable.** 1=Enable TCO IRQ selected by DevB:3x44[TCO_INT_SEL] (if PM22[TCOSCI_EN] = 0). |
| 14:12 | **TCO_INT_SEL: TCO interrupt select.** Specifies the IRQ line asserted by either PM46[INTRDR_STS] (if PM4A[INTRDR_SEL] selects IRQ) or PM44[TCO_INT_STS]. Note: if PM22[TCOSCI_EN] is set, then this field is ignored. Note: if one of IRQ[11:9] is selected, then the interrupt controller must be programmed as level sensitive for this IRQ.<br><br>TCO_INT_SEL / Interrupt: 0h IRQ9; 1h IRQ10; 2h IRQ11; 3h Reserved; 4h APIC IRQ20; 5h APIC IRQ21; 6h APIC IRQ22; 7h APIC IRQ23 |
| 11:8 | **IRQ2SEL: PNPIRQ2 interrupt select.** This selects the IRQ number for PNPIRQ2. IRQ0, IRQ2, IRQ8, and IRQ13 are reserved. If PMD5 does not select the PNPIRQ2 function then this field has no effect. See Section 4.4.2.1 for more details. |
| 7:4 | **IRQ1SEL: PNPIRQ1 interrupt select.** This selects the IRQ number for PNPIRQ1. IRQ0, IRQ2, IRQ8, and IRQ13 are reserved. If PMD4 does not select the PNPIRQ1 function then this field has no effect. See Section 4.4.2.1 for more details. |
| 3:0 | **IRQ0SEL: PNPIRQ0 interrupt select.** This selects the IRQ number for PNPIRQ0. IRQ0, IRQ2, IRQ8, and IRQ13 are reserved. If PMD3 does not select the PNPIRQ0 function then this field has no effect. See Section 4.4.2.1 for more details. |

**Pins Latched On The Trailing Edge Of Reset Register** **DevB:3x48**

Default: These bits are latched on the trailing edge of reset.Attribute:See below.

The default for these bits is specified by pull up or pull down resistors on pins during the trailing edge of the specified reset (PWROK). To latch a Low on these pins, a 10K to 100K ohm resistor to ground is placed on the signal. To latch a High on these pins, a 10K to 100K ohm resistor to the pin's power plane is placed on the signal.

| Bits | Description |
|---|---|
| 15 | **TBD15.** Read-write. The state of this bit is latched off of AD[15] at the trailing edge of PWROK reset. This bit controls no internal hardware. |
| 14 | **TBD14.** Read-write. The state of this bit is latched off of AD[14] at the trailing edge of PWROK reset. This bit controls no internal hardware. |

| Bits | Description (Continued) |
|---|---|
| 13 | **TBD13.** Read-write. The state of this bit is latched off of AD[13] at the trailing edge of PWROK reset. This bit controls no internal hardware. |
| 12 | **SPKRL: SPKR latch.** Read-write. The state of this bit is latched off of SPKR at the trailing edge of PWROK reset. This controls no internal logic. |
| 11 | **Must be Low.** Read-write. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 10 | **NO_REBOOT: do not reboot the system when a double TCO timer time out occurs.** Read-write. 0=Reboot system as specified by PORTCF9[FULLRST] when PM46[2NDTO_STS] is set. 1=Do not reboot the system. The state of this bit is latched off of AD[10] at the trailing edge of PWROK reset. |
| 9 | **Low strap required.** Read-write. The default state of this bit is latched off of AD[9] at the trailing edge of PWROK reset. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 8 | **TBD8.** Read-write. The state of this bit is latched off of AD[8] at the trailing edge of PWROK reset. This bit controls no internal hardware. |
| 7 | **High strap required.** Read-write. The default state of this bit is latched off of AD[7] at the trailing edge of PWROK reset. This bit is required to be High at all times; if it is Low then undefined behavior will result. |
| 6 | **Low strap required.** Read-write. The default state of this bit is latched off of AD[6] at the trailing edge of PWROK reset. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 5 | **High strap required.** Read-write. The default state of this bit is latched off of AD[5] at the trailing edge of PWROK reset. This bit is required to be High at all times; if it is Low then undefined behavior will result. |
| 4 | **Low strap required.** Read-write. The default state of this bit is latched off of AD[4] at the trailing edge of PWROK reset. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 3 | **High strap required.** Read only. The state of this bit is latched off of AD[3] at the trailing edge of PWROK reset. If this bit is strapped Low then undefined behavior will result. |
| 2 | **Low strap required.** Read-write. The default state of this bit is latched off of AD[2] at the trailing edge of PWROK reset. This bit is required to be Low at all times; if it is High then undefined behavior will result. |
| 1 | **TBD1.** Read-write. The state of this bit is latched off of AD[1] at the trailing edge of PWROK reset. This bit controls no internal hardware. |
| 0 | **PCIBIOS.** Read-write. This is specifies routing of accesses to BIOS address space (specified by DevB:0x43). 1=BIOS address space is located on the PCI bus. 0=BIOS address space is located on the LPC bus. The state of this bit is latched off of AD[0] at the trailing edge of reset. |

**Serial IRQ Control Register** **DevB:3x4A**

Default: 10h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7 | Reserved. |
| 6 | **CONTMD: continuous mode selected versus quiet mode.** 1=The serial IRQ logic is in continuous mode. 0=The serial IRQ logic is in quiet mode. In continuous mode, the start frame is initiated by the IC immediately following each stop frame. In quiet mode, start frames are initiated by external slave devices. |
| 5:2 | **FRAMES: number if IRQ frames for a serial IRQ cycle.** This specifies the number of 3-clock IRQ frames that the IC generates, during a serial IRQ cycle before, issuing the stop frame. Per the serial IRQ specification, the number of frames is 17 plus the value of this field. |
| 1:0 | **STARTCLKS: number of clocks in start pulse.** This specifies the size of the start pulse over SER-IRQ during the start frame of a serial IRQ cycle (including the slave cycle if in quiet mode) in PCLK cycles. 00b = 4 cycles. 01b = 6 cycles; 10b = 8 cycles and 11b = reserved. |

**PRDY Timer Control Register** **DevB:3x4C**

Default: 00h. Attribute: Read-write.

Each of these bits controls the ability of the PRDY input signal to disable internal counters. When PRDY becomes active then the counters that correspond to the active bits in this register stop counting until PRDY becomes inactive.

| Bits | Description |
|---|---|
| 7:3 | Reserved. |
| 2 | **SMT_DIS: system management timer disable.** 1=The all the system management timers specified by the PMxx space are disabled from counting while PRDY is active. These include the ACPI timer at PM08, re-trigger timers at PM[8C:50], the system inactivity timer at PM98, and the general purpose timer at PM94. |
| 1 | **RTC_DIS: real-time clock disable.** 1=The real-time clock counters that are clocked off of the 32-KHz clock are disabled from counting while PRDY is active. |
| 0 | **PIT_DIS: programmable interval timer disable.** 1=The clock to the three timers of the internal PIT are disabled when PRDY is active. |

**Thermal Throttling Register** **DevB:3x4D**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:6 | Reserved. |
| 5 | **TTHLOCK: thermal throttling lock.** Write 1 only. 1=Writes to TTH_EN and TTH_RATIO are disabled. Once set, this bit cannot be cleared by software. It is only cleared by a RESET#. TTH_EN and TTH_RATIO may change during the write command that sets TTHLOCK High. |
| 4 | **TTH_EN: thermal throttling enable.** 1=Thermal throttling is enabled when THERM# is asserted. 0=Thermal throttling cannot be enabled. |
| 3:1 | **TTH_RATIO: thermal throttling duty cycle.** These specify the duty cycle of STPCLK# when the system is in thermal throttling mode (initiated by the THERM# pin when enabled by TTH_EN). The field is decoded as follows:<br><br>TTH_RATIO – Description<br>0h – Reserved<br>1h – 87.5% in Stop Grant state<br>2h – 75.0% in Stop Grant state<br>3h – 62.5% in Stop Grant state<br>4h – 50.0% in Stop Grant state<br>5h – 37.5% in Stop Grant state<br>6h – 25.0% in Stop Grant state<br>7h – 12.5% in Stop Grant state |
| 0 | Reserved. |

**Square Wave Generation Register** **DevB:3x4E**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:4 | Reserved. |
| 3:0 | **SQWAVE: square wave frequency control.** When PMD8 selects square wave output function, then this field specifies the frequency of square wave output on the pin. Here is how this field is decoded:<br><br>SQWAVE – Frequency<br>0h – Output Low<br>1h – 256 Hz<br>2h – 128 Hz<br>3h – 8192 Hz<br>4h – 4096 Hz<br>5h – 2048 Hz<br>6h – 1024 Hz<br>7h – 512 Hz<br>8h – 256 Hz<br>9h – 128 Hz<br>Ah – 64 Hz<br>Bh – 32 Hz<br>Ch – 16 Hz<br>Dh – 8 Hz<br>Eh – 4 Hz<br>Fh – 2 Hz |

**C2/C3 State Control Register** **DevB:3x4F**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:5 | Reserved. |
| 4 | **CSTP_C3EN: enable CPUSTOP# assertion during C3.** 1=Enables the control of the CPUSTOP# pin during C3. 0=CPUSTOP# is always High. This bit has no effect if the PMC7 does not select the CPUSTOP# function. |
| 3 | **CSLP_C3EN: enable CPUSLEEP# assertion during C3.** 1=Enables the control of the CPU-SLEEP# pin during the C3 state transition. 0=CPUSLEEP# is always High. This bit has no effect if the PMC6 does not select the CPUSLEEP# function. |
| 2 | **ZZ_C3EN: enable CACHE_ZZ assertion during C3.** 1=Enables the control of the CACHE_ZZ pin when transitioning to the C3 state. 0=CACHE_ZZ is always Low. This bit has no effect if the PMC4 does not select the CACHE_ZZ function. |
| 1 | **C3EN: enable C3 command.** 1=Enables the IC to place the processor into the Stop Grant state by asserting STPCLK# when the C3 command is sent to PM15. Note, this bit must be High for ZZ_C3EN, CSTP_C3EN, and CSLP_C3EN bits to function during the transition to C3. |
| 0 | **C2EN: enable C2 command.** 1=Enables the IC to place the processor into the Stop Grant state by asserting STPCLK# when the C2 command is sent to PM14. 0=Disable. |

**Power On Suspend Control Register** **DevB:3x50**

Default: 8000h. Attribute: Read-write.

This register specifies the action taken by the IC when the sleep command is sent to PM04 with SLP_TYP indicating power on suspend. Note: if POSEN is Low, then the rest of the bits in this register are ignored.

| Bits | Description |
|---|---|
| 15 | **PITRSM#: enable the PIT to generate unmasked interrupts during POS.** 1=PIT will not generate IRQ0 to the PIC while in POS (starting from the time that the command to enter POS is sent to PM04); this may be used to prevent timer-tick interrupts from resuming the system while in POS. 0=PIT will generate IRQ0 to the PIC while in POS. |
| 14 | **MSRSM#: enable the mouse interrupt to generate unmasked interrupts during POS.** 1=Disable IRQ12 to the PIC while in POS (starting from the time that the command to enter POS is sent to PM04); this may be used to prevent mouse interrupts from resuming the system while in POS; this affects both the IRQ12 pin and IRQ 12 from the serial IRQ logic. 0=Enable IRQ12 to the PIC while in POS. |
| 13:9 | Reserved. |
| 8 | **SUSP: enable SUSPEND# assertion during POS.** 1=Enables the control of the SUSPEND# pin during POS. |
| 7 | Reserved. |
| 6 | **CSLP: enable CPUSLEEP# assertion during POS.** 1=Enables assertion of the CPUSLEEP# pin during POS. 0=Disable. This bit has no effect if the PMC6 does not select the CPUSLEEP# function. |
| 5 | **DCSTP: enable DCSTOP# assertion during POS.** 1=Enables assertion of the DCSTOP# pin during POS. |
| 4 | **ASTP: enable AGPSTOP# assertion during POS.** 1=Enables assertion of the AGPSTOP# pin during POS. This bit has no effect if the PMC1 does not select the AGPSTOP# function. |
| 3 | **PSTP: enable PCISTOP# assertion during POS.** 1=Enables the control of the PCISTOP# pin during POS. |
| 2 | **CSTP: enable CPUSTOP# assertion during POS.** 1=Enables control of the CPUSTOP# pin during POS. This bit has no effect if the PMC7 does not select the CPUSTOP# function. |
| 1 | **RW.** Read-write. This bit is read-write accessible through software; it controls no hardware. |
| 0 | **POSEN: enable Stop Grant during POS.** 1=Enables the IC to place the processor into the Stop Grant state by asserting STPCLK# when a POS commands is sent to PM04. This bit required to be set High for any other bits in this register to be enabled. |

**PLL Lock Timer Register** **DevB:3x54**

Default: 0Fh. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:4 | Reserved. |
| 3:0 | **PLLCNT: PLL lock timer count.** Specifies the PLL recovery time as follows:<br>`PLL synchronization time = (PLLCNT + 1) * 61.035 microseconds.`<br>See Section 4.7.1.5.4 and Section 4.7.1.5.6 for details about this timer. |

**PCI IRQ Routing Register** **DevB:3x56**

Default: 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:12 | **PIRQD# select.** See bits[3:0]. |
| 11:8 | **PIRQC# select.** See bits[3:0]. |
| 7:4 | **PIRQB# select.** See bits[3:0]. |
| 3:0 | **PIRQA# select.** These map the PCI IRQ pins to the internal interrupt controller (PIC and APIC). These are decoded as follows:<br><br>PIRQ[D,C,B,A]# Selects / Selected IRQ / PIRQ[D,C,B,A]# Selects / Selected IRQ<br>0h None 8h Reserved<br>1h IRQ1 9h IRQ9<br>2h Reserved Ah IRQ10<br>3h IRQ3 Bh IRQ11<br>4h IRQ4 Ch IRQ12<br>5h IRQ5 Dh Reserved<br>6h IRQ6 Eh IRQ14<br>7h IRQ7 Fh IRQ15 |

**PMxx System Management IO Space Pointer** **DevB:3x58**

Default: 0000 DD01h. Attribute: See below.

| Bits | Description |
|---|---|
| 31:16 | Reserved. |
| 15:8 | **PMBASE.** Read-write. Specifies PCI address bits[15:8] of the 256-byte block of IO-mapped registers used for system management (address space PMxx). Access to this address space is enabled by DevB:3x41[PMIOEN]. |
| 7:0 | **PMBLSB.** Read only. These fixed bits read 01h. |

**System Management Class Code Write Register** **DevB:3x60**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:8 | **CCWRITE.** The value placed in this register is visible in DevB:3x08. |
| 7:0 | Reserved. |

**System Management Device and Subsystem ID Read-Write Register** **DevB:3x7C**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:16 | **SSID: subsystem ID register.** The value placed in this register is visible in DevB:3x2C[31:16]. |
| 15:0 | **SSVENDORID: subsystem vendor ID register.** The value placed in this register is visible in DevB:3x2C[15:0]. |

**Read-Write Register** **DevB:3x80**

Default: 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:0 | **RW.** Read-write. These bits are read-write accessible through software; they control no hardware. |

**CardBus Trap 1 and 2 IO Address Register** **DevB:3xB4**

Default: 0000 0000h. Attribute: Read-write.

DevB:3xB4, DevB:3xB8, DevB:3xBC, and DevB:3xC0 combine to specify the address space for the CARDBUS0 and CARDBUS1 trap events. These events can be used to generate an SMIs or SCIs, load the associated re-trigger timers (PM6C and PM70), or load the system inactivity timer. The CARDBUS0 and CARDBUS1 trap events occur when the following is true:
CARDBUS0:

```
  ((AD[15:0]  | MASKPIO1 == ADDRPIO1 | MASKPIO1) & (PCI IO access) )
| ((AD[31:10] | MASKPME1 == ADDRPME1 | MASKPME1) & (PCI MEM access) );
```

CARDBUS1:

```
  ((AD[15:0]  | MASKPIO2 == ADDRPIO2 | MASKPIO2) & (PCI IO access) )
| ((AD[31:10] | MASKPME2 == ADDRPME2 | MASKPME2) & (PCI MEM access) );
```

Where AD is the address field of the host transaction. The mask bits for the IO addresses cover bits[7:2]. ADDRPIO[1:0] must be 00b. The mask bits for the memory addresses cover bits[17:10].

| Bits | Description |
|---|---|
| 31:16 | **ADDRPIO2.** IO address for the CARDBUS1 trap event. |
| 15:0 | **ADDRPIO1.** IO address for the CARDBUS0 trap event. |

**PCMCIA Trap 1 Memory Address Registers** **DevB:3xB8**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:10 | **ADDRPME1.** Memory address for the CARDBUS0 trap event. See DevB:3xB4 for details. |
| 9:0 | Reserved. |

**PCMCIA Trap 2 Memory Address Registers** **DevB:3xBC**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:10 | **ADDRPME2.** Memory address for the CARDBUS1 trap event. See DevB:3xB4 for details. |
| 9:0 | Reserved. |

**PCMCIA Trap Mask Registers** **DevB:3xC0**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:24 | **MASKPME2.** Address mask for the PCMCIA trap events. See DevB:3xB4 for details. |
| 23:16 | **MASKPME1.** Address mask for the PCMCIA trap events. See DevB:3xB4 for details. |
| 15:8 | **MASKPIO2.** Address mask for the PCMCIA trap events. See DevB:3xB4 for details. |
| 7:0 | **MASKPIO1.** Address mask for the PCMCIA trap events. See DevB:3xB4 for details. |

**Programmable IO Range Monitor 1 and 2 Trap Address Register** **DevB:3xC4**

Default: 0000 0000h. Attribute: Read-write.

DevB:3xC4, DevB:3xC8, and DevB:3xCC combine to specify the address space for programmable IO range monitor trap events (PIORM[4:1]). These events can be used to generate SMIs or SCIs, load the associated re-trigger timer (PM78, PM7C, PM80, and PM84), or load the system inactivity timer. The trap events occur when the following equations are true:

```
PIORM1: (AD[15:0] | MASKIO1) == (ADDRIO1 | MASKIO1);
PIORM2: (AD[15:0] | MASKIO2) == (ADDRIO2 | MASKIO2);
PIORM3: (AD[15:0] | MASKIO3) == (ADDRIO3 | MASKIO3);
PIORM4: (AD[15:0] | MASKIO4) == (ADDRIO4 | MASKIO4);
```

Where AD is the address field of a host IO cycle. The mask bits cover any combination of bits[7:2]. ADDRIO[1:0] must be 00b. Traps of accesses to the IDE IO registers are not allowed.

| Bits | Description |
|---|---|
| 31:16 | **ADDRIO2.** Address for the PIORM2 trap event. |
| 15:0 | **ADDRIO1.** Address for the PIORM1 trap event. |

**Programmable IO Range Monitor 3 and 4 Trap Address Register** **DevB:3xC8**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:16 | **ADDRIO4.** Address for the PIORM4 trap event. See DevB:3xC4 for details. |
| 15:0 | **ADDRIO3.** Address for the PIORM3 trap event. See DevB:3xC4 for details. |

**Programmable IO Range Monitor Trap Mask Register** **DevB:3xCC**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:24 | MASKIO4**.** Address masks for the PIORM4 trap events. See DevB:3xC4 for details. |
| 23:16 | MASKIO3**.** Address masks for the PIORM3 trap events. See DevB:3xC4 for details. |
| 15:8 | MASKIO2**.** Address masks for the PIORM2 trap events. See DevB:3xC4 for details. |
| 7:0 | MASKIO1**.** Address masks for the PIORM1 trap events. See DevB:3xC4 for details. |

**Programmable Memory/Configuration Range Monitor 1 Trap Address Register DevB:3xD0**

Default: 0000 0000h. Attribute: Read-write.

DevB:3xD0, DevB:3xD4, and DevB:3xD8 combine to specify the address space for the programmable memory or configuration space range monitor 1 and 2 trap events (PMEMRM[1,2]). These events can be used to generate SMIs or SCIs, load the associated re-trigger timers (PM88 and PM8C), or load the system inactivity timer. These trap events occur when the following equations are true:

```
PMEMRM1:   (AD[31:2] | MASKMEM1 == ADDRMEM1[31:2] | MASKMEM1) & MEMSP & ~CFGSPEN1
         | (AD[15:2] | MASKMEM1 == ADDRMEM1[15:2] | MASKMEM1) & CFGSP &  CFGSPEN1 &
             ~AD[24] & ~ADDRMEM1[24]
         | (AD[23:2] | MASKMEM1 == ADDRMEM1[23:2] | MASKMEM1) & CFGSP &  CFGSPEN1 &
             AD[24] &  ADDRMEM1[24];
PMEMRM2:   (AD[31:2] | MASKMEM2 == ADDRMEM2[31:2] | MASKMEM2) & MEMSP & ~CFGSPEN2
         | (AD[15:2] | MASKMEM2 == ADDRMEM2[15:2] | MASKMEM2) & CFGSP &  CFGSPEN2 &
             ~AD[24] & ~ADDRMEM2[24]
         | (AD[23:2] | MASKMEM2 == ADDRMEM2[23:2] | MASKMEM2) & CFGSP &  CFGSPEN2 &
             AD[24] &  ADDRMEM1[24];
```

Where AD is the address field of a host transaction, MEMSP indicates a memory space transaction and CFGSP indicates a configuration space transaction. The mask bits cover address bits[17:2]. Note that for configuration traps, AD[24] and ADDRMEM[2,1][24] carry the determination of whether the trap is a type 0 or type 1 configuration cycle; if it is type 0, then the bus number bits are ignored.
Traps of accesses to Device B, function 1 DevA:0xE8 are not allowed.

| Bits | Description |
|---|---|
| 31:2 | **ADDRMEM1.** Memory address for the PMEMRM1 trap event. |
| 1 | Reserved. |
| 0 | **CFGSPEN1: configuration space enable 1.** 1=PMEMRM1 is a configuration space trap. 0=PMEMRM1 is a memory space trap. |

**Programmable Memory/Configuration Range Monitor 2 Trap Address Register DevB:3xD4**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:2 | **ADDRMEM2.** Memory address for the PMEMRM2 trap event. See DevB:3xD0 for details. |
| 1 | Reserved. |
| 0 | **CFGSPEN2: configuration space enable 2.** 1=PMEMRM2 is a configuration space trap. 0=PMEMRM2 is a memory space trap. See DevB:3xD0 for details. |

**Programmable Memory/Configuration Range Monitor Trap Mask Registers** **DevB:3xD8**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:16 | **MASKMEM2.** Address mask for the PMEMRM2 trap event. See DevB:3xD0 for details. |
| 15:0 | **MASKMEM1.** Address mask for the PMEMRM1 trap event. See DevB:3xD0 for details. |

## 5.7.2 System Management IO Mapped Registers (PMxx)

These registers are located in IO space. The base address registers for these registers is DevB:3x58. See Section 5.1.2 for a description of the register naming convention.

**Power Management 1 Status Register (ACPI PM1a_STS)** **PM00**

Default: 0000h. Attribute: Read; set by hardware; write 1 to clear.

Each of these bits are status bits set by hardware events. Most have the ability to generate an SCI/SMI interrupt, if they are enabled to do so in PM02.

| Bits | Description |
|---|---|
| 15 | **WAK_STS: wake status.** This bit is set by hardware when the system is in any sleep state (POS, STR, STD, or SOFF) and an enabled resume event occurs. Upon setting this bit, the system will resume. |
| 14:12 | Reserved. |
| 11 | **PBOR_STS: power button override status.** This bit is set by hardware when a power button override event occurs. A power button override event will occur if PM26[PBOR_DIS] is Low and PWRBTN# is held in the active state for more than four seconds or if PM26[SBOR_DIS] is Low, the SLPBTN# function is enabled by PMD7, and SLPBTN# is held in the active state for more than four seconds. This bit resides on the VDD_AUX power plane. |
| 10 | **RTC_STS: real-time clock status.** This bit is set by hardware when the real-time clock generates an interrupt. This bit resides on the VDD_AUX power plane. |
| 9 | **SLPBTN_STS: sleep button status.** 1=Indicates that the sleep button (SLPBTN#) has been asserted. The debounce circuitry causes a 12-to-16 millisecond delay from the time the input signal stabilizes until this bit changes. If the GPIO debounce circuitry specified by PMD7 is enabled, then the debounce period will be twice as long before setting the status bit. If the SLPBTN# function is not selected by PMD7, then this bit will not be set. If PM26[SBOR_DIS] is Low and SLPBTN# is held Low for more than four seconds, then this bit is cleared and PBOR_STS is set. This bit resides on the VDD_AUX power plane. Note: the debounce circuit functions in the High-to-Low and Low-to-High directions. |

| Bits | Description (Continued) |
|---|---|
| 8 | **PWRBTN_STS: power button status.** 1=Indicates that the power button (PWRBTN#) has been asserted. The debounce circuitry causes a 12-to-16 millisecond delay from the time the input signal stabilizes until this bit changes. If PM26[PBOR_DIS] is Low and PWRBTN# is held Low for more than four seconds, then this bit is cleared and PBOR_STS is set. This bit resides on the VDD_AUX power plane. Note: the debounce circuit functions in the High-to-Low and Low-to-High directions. |
| 7:6 | Reserved. |
| 5 | **GBL_STS: global status.** This bit is set by hardware when a 1 is written to PM2C[BIOS_RLS]. |
| 4 | **BM_STS: bus master status.** This bit is set by hardware when a secondary PCI bus request signal becomes active or any internal source requests access to the host. Based on the state of PM04[BM_RLD], this may result in a power state transition. |
| 3:1 | Reserved. |
| 0 | **TMR_STS: ACPI timer status.** This bit is set by hardware when the MSB (either bit 23 or 31 based on DevB:3x41[3]) of the ACPI timer (PM08) toggles (from 0 to 1 or 1 to 0). |

**Power Management 1 Enable Register (ACPI PM1a_EN)** **PM02**

Default: 0100h. Attribute: Read-write.

Most of these bits work in conjunction with the corresponding STS bits in PM00 to generate SCI or SMI interrupts (based on the state of PM04[SCI_EN]).

| Bits | Description |
|---|---|
| 15:11 | Reserved. |
| 10 | **RTC_EN: real-time clock SCI/SMI enable.** 1=Enable an SCI or SMI interrupt when PM00[RTC_STS] is set High. This bit resides on the VDD_AUX power plane.<br>Note: This enables all sources of interrupt from the RTC (Alarm, Periodic, and Update Ended). Any of the sources of interrupt that are unwanted should be masked in RTC Register B, and PM00[RTC_STS] should be cleared before setting this bit. |
| 9 | **SLPBTN_EN: sleep button SCI/SMI enable.** 1=Enable an SCI or SMI interrupt when PM00[SLPBTN_STS] is set High. This bit resides on the VDD_AUX power plane. |
| 8 | **PWRBTN_EN: power button SCI/SMI enable.** 1=Enable an SCI or SMI interrupt when PM00[PWRBTN_STS] is set High. This bit resides on the VDD_AUX power plane. |
| 7:6 | Reserved. |
| 5 | **GBL_EN: global SCI enable.** 1=Enable an SCI interrupt when PM00[GBL_STS] is set High. Note: this results in an SCI interrupt, regardless as to the state of PM04[SCI_EN]. |
| 4:1 | Reserved. |
| 0 | **TMR_EN: ACPI timer SCI enable.** 1=Enable an SCI interrupt when PM00[TMR_STS] is set High. Note: this results in an SCI interrupt, regardless as to the state of PM04[SCI_EN]. |

**Power Management 1 Control Register (ACPI PM1_CNTa)** **PM04**

Default: 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 15:14 | Reserved. |
| 13 | **SLP_EN: sleep enable.** Write only; reads back as 0. Writing a 1 to this bit causes the system to sequence into the sleep state specified by SLP_TYP. |
| 12:10 | **SLP_TYP: sleep type.** Read-write. Specifies the type of sleep state the system enters when SLP_EN is set High.<br><br>0 FON, S0. Full on.<br>1 POS, S1. Power on suspend. Power state transition specified by DevB:3x50.<br>2-4 Reserved.<br>5 STR, S3. Suspend to RAM.<br>6 STD, S4. Suspend to disk.<br>7 SOFF, S5. Soft off. |
| 9:3 | Reserved. |
| 2 | **GBL_RLS: global release.** Read; write 1 only; cleared by hardware. When this bit is set High, the hardware sets PM28[BIOS_STS] High. GBL_RLS is cleared by the hardware when PM28[BIOS_STS] is cleared by software. |
| 1 | **BM_RLD: bus master reload.** Read-write. 1=Enables the transition of the processor power state from C3 to C0 to be triggered by any bus master requests (when PM00[BM_STS] is set). |
| 0 | **SCI_EN: SCI-SMI select.** Read-write. Selects the type of interrupt generated by power management events. 0=SMI interrupt. 1=SCI interrupt. Note that certain power management events can be programmed individually to generate SMI interrupts independent of the state of this bit. See Section 4.7.1.1 for details. Also, TMR_STS and GBL_STS always generate SCI interrupts regardless as to the state of this bit. |

**ACPI Power Management Timer (ACPI PM_TMR)** **PM08**

Default: 0000 0000h. Attribute: Read only.

This is either a 24- or 32-bit counter, based on the state of DevB:3x41[3]. It is a free-running, incrementing counter clocked off of a 3.579545-MHz clock. It does not count when the system is in MOFF, SOFF, STD, or STR state. When the MSB toggles (either bit[23] or bit[31]) then PM00[TMR_STS] is set. This timer is asynchronously cleared when DevB:3x41[TMRRST] is High.

| Bits | Description |
|---|---|
| 31:24 | **ETM_VAL: extended timer value.** If DevB:3x41[3] is High, then these are the 8 MSBs of the ACPI power management timer. If DevB:3x41[3] is Low, then this field always reads back as all zeros. |
| 23:0 | **TMR_VAL: timer value.** Read only. This field returns the running count of the ACPI power management timer. |

**Processor Clock Control Register (ACPI P_CNT)** **PM10**

Default: 0000 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:5 | Reserved. |
| 4 | **NTH_EN: normal throttling enable.** 1=Normal throttling (duty cycle specified by NTH_RATIO) is enabled. Normal throttling is disabled when thermal throttling. 0=Normal throttling is not enabled. |
| 3:1 | **NTH_RATIO: normal throttling duty cycle.** These bits specify the duty cycle of the STPCLK# pin when the system is in normal throttling mode, enabled by NTH_EN. The field is decoded as follows:<br><br>NTH_RATIO Description NTH_RATIO Description<br>0h Reserved 4h 50.0% in Stop Grant state<br>1h 87.5% in Stop Grant state 5h 37.5% in Stop Grant state<br>2h 75.0% in Stop Grant state 6h 25.0% in Stop Grant state<br>3h 62.5% in Stop Grant state 7h 12.5% in Stop Grant state |
| 0 | Reserved. |

**Processor Level 2 Register (ACPI P_LVL2)** **PM14**

Default: 00h. Attribute: Read only.

| Bits | Description |
|---|---|
| 7:0 | **P_LVL2.** Reads from this register place the processor into the C2 power state, as specified by DevB:3x4F. Reads from this register always return 00h. This register is byte readable only. |

**Processor Level 3 Register (ACPI P_LVL3)** **PM15**

Default: 00h. Attribute: Read only.

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| Bits | Description |
|---|---|
| 7:0 | **P_LVL3.** Reads from this register place the processor into the C3 power state, as specified by DevB:3x4F. Reads from this register always return 00h. This register is byte readable only. |

**Software SMI Trigger Register** **PM1E (PM2F)**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:0 | This address accesses the same physical register located at PM2F. I.e., both accesses to PM1E and PM2F identically access the same register and both can be used to set PM28[SWI_STS]. |

**Fan RPM Count Register** **PM1F**

Default: 00h. Attribute: Read only.

| Bits | Description |
|---|---|
| 7:0 | **RPMCNT: FANRPM Count Register.** This provides the state of a counter that increments on every rising edge of the signal FANRPM. If the FANRPM function is not selected by PMCA, then this register will not change. |

**General Purpose 0 Status Register (ACPI GPE0_STS)** **PM20**

Default: 0000h. Attribute: Read; set by hardware; write 1 to clear.

Most of the bits in this register may be enabled to generate SCI or SMI interrupts (based on the state of PM04[SCI_EN]) via PM22 or may be enabled to generate SMI interrupts via PM2A and PM2C.

| Bits | Description |
|---|---|
| 15 | **USBRSM_STS: USB-defined resume event status.** This bit is set High by the hardware when a USB-defined resume event has occurred. This bit resides on the VDD_AUX power plane. |
| 14 | **RI_STS: RI# pin status.** This bit is set High by the hardware when the RI# pin is asserted. This bit resides on the VDD_AUX power plane. |
| 13 | **LID_STS: LID Status.** This bit is set High by the hardware when the LID signal has changed state indicating that the LID has either opened or closed. This bit resides on the VDD_AUX power plane. |
| 12 | **ACAV_STS: AC change status.** This bit is set High by the hardware when the ACAV signal has changed state indicating that AC power has either been added or removed from the system. This bit resides on the VDD_AUX power plane. Note: the default value of this bit (from MOFF) is indeterminate. |
| 11 | **SMBUS_STS: SMBus status.** This bit is set High if an SMBus status bit in PME0[SNP_STS, HSLV_STS, and SMBA_STS] is High while enabled by PME2[SNP_EN, HSLV_EN, and SMBA_EN], respectively, or if any of PME0[ABRT_STS, COL_STS, PRERR_STS, HCYC_STS, TO_STS] are set High while enabled by PME2[HCYC_EN]. Note: only PME0[SMBA_EN, HSLV_STS, SNP_STS] can be enabled to wake the system out of sleep states. This bit resides on the VDD_AUX power plane. |
| 10 | **THERM_STS: THERM# pin status.** This bit is set High by the hardware when the THERM# pin is asserted. |
| 9 | **EXTSMI_STS: external SMI pin status.** This bit is set High by the hardware when the EXTSMI# pin is asserted. This bit resides on the VDD_AUX power plane. |

| Bits | Description (Continued) |
|---|---|
| 8 | **PME_STS: PME# pin status.** This bit is set High by the hardware when the PME# pin is asserted Low. This bit resides on the VDD_AUX power plane. |
| 7 | **TCOSCI_STS: TCO SCI interrupt status.** This bit is set High by the hardware when there is a 0 to 1 transition on PM46[INTRDR_STS] or PM44[TCO_INT_STS]. |
| 6 | Reserved. |
| 5 | **SIT_STS: system inactivity timer time out status.** This bit is set High by the hardware when the system inactivity timer times out. |
| 4 | Reserved. |
| 3 | Reserved. |
| 2 | Reserved. |
| 1 | **AC97_STS: AC97 wake event status.** This bit is set High by the hardware when the AC97 link generates a wake event. This bit resides on the VDD_AUX power plane. |
| 0 | **DM_STS: hardware device monitor (parent) event status.** This bit is set High by the hardware when any of the device monitor event status bits in PMA0 become active when enable by the corresponding bits in PMA4. |

**General Purpose 0 ACPI Interrupt Enable Register (ACPI GPE0_EN) PM22**

Default: 0000h. Attribute: Read-write.

For each of the bits in this register: 1=Enable a corresponding status bit in PM20 to generate an SMI or SCI interrupt (based on the state of PM04[SCI_EN]). 0=Do not enable the SMI or SCI interrupt.

| Bits | Description |
|---|---|
| 15 | **USBRSM_EN.** USB resume event ACPI interrupt enable. This bit resides on the VDD_AUX power plane. |
| 14 | **RI_EN.** RI# pin ACPI interrupt enable. This bit resides on the VDD_AUX power plane. |
| 13 | **LID_EN.** LID pin ACPI interrupt enable. This bit resides on the VDD_AUX power plane. |
| 12 | **ACAV_EN.** ACAV pin ACPI interrupt enable. This bit resides on the VDD_AUX power plane. |
| 11 | **SMBUS_EN.** SMBus (parent) ACPI interrupt enable. This bit resides on the VDD_AUX power plane. |
| 10 | **THERM_EN.** THERM# pin ACPI interrupt enable. |
| 9 | **EXTSMI_EN.** External SMI pin ACPI interrupt enable. This bit resides on the VDD_AUX power plane. |
| 8 | **PME_EN.** PME# pin ACPI interrupt enable. This bit resides on the VDD_AUX power plane. |
| 7 | **TCOSCI_EN.** TCO SCI enable. Note: when this is High, DevB:3x44[TCO_INT_SEL] is ignored. |
| 6 | Reserved. |
| 5 | **SIT_EN.** System inactivity timer time out ACPI interrupt enable. |
| 4 | Reserved. |
| 3 | TBD3. Read-write. This bit controls no internal logic. This bit resides on the VDD_AUX power plane. |
| 2 | TBD3. Read-write. This bit controls no internal logic. This bit resides on the VDD_AUX power plane. |
| 1 | **AC97_EN.** AC97 wake event enable. This bit resides on the VDD_AUX power plane. |
| 0 | **DM_EN.** Device monitor (parent) ACPI interrupt enable. |

**Sleep State Resume Enable Register** **PM26**

Default: 2000h. Attribute: Read-write.

All the bits in this register reside in the VDD_AUX power plane.

| Bits | Description |
|---|---|
| 15 | **BATLOW_CTL: battery low enable control.** 1=Enable BATLOW# assertion to prevent a system resume from any sleep state (POS, STD, STR, or SOFF). All resume events except that associated with ACAV_STS are affected by this bit. |
| 14 | **MINSLEEP: minimum sleep time.** 1=The minimum time in which PWRON# is deasserted in support of STR, STD, or SOFF is 500 to 800 milliseconds. I.e., resume events that occur shortly after entry into these sleep states will not be acted upon until this minimum time has transpired. 0=There is no minimum time in which PWRON# is deasserted. |
| 13 | **SBOR_DIS: SLPBTN# override disable.** 1=The power button override event from the SLPBTN# pin (holding SLPBTN# active for four seconds) will not set PM00[PBOR_STS] High and will not automatically transition the system into SOFF. 0=The power button override event from the SLPBTN# pin is enabled to set PM00[PBOR_STS] High and place the system into the SOFF mode. |
| 12 | Reserved. |
| 11 | **PBOR_DIS: power button override disable.** 1=The power button override event (holding PWRBTN# active for four seconds) will not set PM00[PBOR_STS] High and will not automatically transition the system into SOFF. 0=The power button override event is enabled to set PM00[PBOR_STS] High and place the system into the SOFF mode. |
| 10:0 | Reserved. |

**Global Status Register** **PM28**

Default: 0000h. Attribute: See below.

Each of the EVT bits specify SMI-interrupt-enabled status bits in other registers. These are not sticky bits; they reflect the combinatorial equation of: _EVT = (status1 & SMI enable1) | (status2 & SMI enable2)...

| Bits | Description |
|---|---|
| 15 | **MISC_EVT: miscellaneous SMI event.** Read only. This bit is read as 1 when there are set status bits in PM30 that are enabled in PM32. |
| 14 | Reserved. |
| 13 | **GPE0_EVT: general purpose event 0 event status.** Read only. This bit goes High when any of the PM20 status bits that are SMI enabled by PM2A or PM2C become active (this does not include PM20[DM_STS]). Note: PM20[TCOSCI_STS] is not included. |
| 12 | **USB_EVT: USB SMI event.** Read only. This bit is read as 1 when one of the USB-defined SMI events occurs. This occurs when HcControl[8] is High and an enabled interrupt occurs (HcInterrupt-Status and HcInterruptControl). This bit is not affected by PM20[USBRSM_STS]. |
| 11 | **SMBUS_EVT: SMBus event status.** Read only. This bit is read as 1 when an SMBus status bit in PME0[SNP_STS, HSLV_STS, and SMBA_STS] is High while enabled by PME2[SNP_EN, HSLV_EN, and SMBA_EN], respectively, or when any of PME0[ABRT_STS, COL_STS, PRERR_STS, HCYC_STS, TO_STS] are set High while enabled by PME2[HCYC_EN]. |
| 10:8 | Reserved. |
| 7 | **SWI_STS: software SMI status.** Read; set by hardware; write 1 to clear. This bit is set High by the hardware when a write of any value is sent to PM1E or PM2F. This bit can trigger SMI interrupts if enabled by PM2A[SWISMI_EN]. |
| 6 | **BIOS_STS: BIOS status.** Read; set by hardware; write 1 to clear. This bit is set High by the hardware when PM04[GBL_RLS] is set High. BIOS_STS is cleared when a 1 is written to it; writing a 1 to BIOS_STS also causes the hardware to clear PM04[GBL_RLS]. This bit can trigger SMI interrupts if enabled by PM2A[BIOSSMI_EN]. |
| 5 | Reserved. |
| 4 | **IRQRSM_STS: IRQ Resume Status.** Read; set by hardware; write 1 to clear. 1=System was resumed from POS due to an unmasked interrupt assertion and PM2A[IRQ_RSM] is High. 0=System was not resumed from POS due to an interrupt. Note: this bit is set only by resumes from POS. Note: DevB:3x50[PITRSM#, MSRSM#] can be set to inhibit timer tick and mouse interrupts during POS. |
| 3 | **GPIO_EVT: GPIO interrupt status.** Read only. This bit is read as 1 when any of the general purpose IO status bits in PMB0 that are SMI enabled by PMB8 become active. |
| 2 | **PM1_EVT: Power management 1 status.** Read only. This bit is read as 1 when any of the status bits in PM00 are active (they do not need to be enabled by PM02). |
| 1 | **TCO_EVT: TCO SMI interrupt event.** Read only. This bit is read as 1 when any of PM44[NMI2SMI_STS, SW_TCO_SMI, TOUT_STS, IBIOS_STS] are set. |
| 0 | **DM_EVT: hardware device monitor event status.** Read only. This bit is read as 1 when any of the device monitor status bits in PMA0 that are SMI enabled by PMA8 become active. |

**Global SMI Enable Register** **PM2A**

Default: 0000h. Attribute: Read-write.

Most of these bits enable the status bits to generate SMI interrupts. For each of these bits: 1=enable the corresponding STS bit in the specified register to generate an SMI interrupt, regardless as to the state of PM04[SCI_EN].

| Bits | Description |
|---|---|
| 15 | **USBSMI_EN: USB resume SMI enable.** Generate SMI when PM20[USBRSM_STS]=1. |
| 14 | **RISMI_EN: RI# pin SMI enable.** Generate SMI when PM20[RI_STS]=1. |
| 13 | **SBSMI_EN: SLPBTN# pin SMI enable.** Generate SMI when PM00[SLPBTN_STS]=1. |
| 12 | **PBSMI_EN: PWRBTN# pin SMI enable.** Generate SMI when PM00[PWRBTN_STS]=1. |
| 11 | **SMBSMI_EN: SMBus event SMI enable.** Generate SMI when PM28[SMBUS_EVT]=1. |
| 10 | **THMSMI_EN: THERM# pin SMI enable.** Generate SMI when PM20[THERM_STS]=1. |
| 9 | **EXTSMI_EN: external SMI pin SMI enable.** Generate SMI when PM20[EXTSMI_STS]=1. |
| 8 | **PMESMI_EN: PME# pin SMI enable.** Generate SMI when PM20[PME_STS]=1. |
| 7 | **SWISMI_EN: software SMI enable.** Generate SMI when PM28[SWI_STS]=1. |
| 6 | **BIOSSMI_EN: BIOS SMI enable.** Generate SMI when PM28[BIOS_STS]=1. |
| 5 | **SITSMI_EN: system inactivity timer time out SMI enable.** Generate SMI when PM20[SIT_STS]=1. |
| 4 | **IRQ_RSM: resume from POS on unmasked interrupt.** 1=Enable resume from POS when PM28[IRQRSM_STS] is set High. |
| 3 | **BMSMI_EN: bus master SMI enable.** Generate SMI when PM00[BM_STS]=1. |
| 2 | **LIDSMI_EN: LID pin SMI enable.** Generate SMI when PM20[LID_STS]=1. |
| 1 | **TCO_EN: TCO SMI interrupt enable.** Generate SMI when PM28[TCO_EVT]=1. Note: if PM48[NMI2SMI_EN]=1, PM44[NMI2SMI_STS] will generate SMI interrupts regardless of the state of this bit. Even if the TCO_EN bit is 0, NMIs are routed to generate SMIs. |
| 0 | **ACAVSMI_EN: ACAV pin SMI enable.** Generate SMI when PM20[ACAV_STS]=1. |

**Global SMI Control Register** **PM2C**

Default: 0000h. Attribute: See below.

| Bits | Description |
|---|---|
| 15:8 | Reserved. |
| 7 | TBD7. Read-write. This bit controls no internal logic. |
| 6 | TBD6. Read-write. This bit controls no internal logic. |
| 5 | **SMIACT: SMI active.** Read; set by hardware; write 1 to clear. This bit is set High by the hardware on the leading edge of the SMI output. If SMILK is High, then SMIACT holds the SMI# pin in the active state. If SMILK is Low, then SMIACT has no effect on the SMI signal. |
| 4 | **SMILK: SMI lock control.** Read-write. 1=The SMI# pin is locked into the active state by a latch after it is asserted. The latch is controlled by SMIACT. 0=The state of SMIACT does not affect SMI#. |
| 3 | **EOS: end of SMI.** Write only. Writing a 1 to this bit forces the SMI# pin to be deasserted for 4 PCI clocks. This bit always reads as a 0. |
| 2 | **AC97SMI_EN: AC97 wake event SMI enable.** Read-write. 1=Generate SMI when PM20[AC97_STS] goes High. |
| 1 | **BIOS_RLS: BIOS SCI/SMI lock release.** Read; write 1 only; cleared by hardware. This bit is set High by software to indicate the release of the SCI/SMI lock. When this bit is set High, PM00[GBL_STS] is set High by the hardware. BIOS_RLS is cleared by the hardware when PM00[GBL_STS] is cleared by software. Note that if PM02[GBL_EN] is set, then setting this bit will generate an SCI interrupt. |
| 0 | **SMI_EN: SMI enable control.** Read-write. 1=Enable generation of SMIs from the system management logic (including all SMI sources in the system management logic and the SMI from the serial IRQ logic, but not SMIs from the IOAPIC, USB, TCO events, or General Purpose Event 0). 0=Disable SMIs from the system management logic (however, if SMIACT is set and SMI_EN is cleared, SMI# will remain asserted until SMIACT is cleared). |

**Advanced Power Management Status Register** **PM2E**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:0 | **APM_STATUS.** This has no affect on hardware. This register may be used to pass status information between the OS and the SMI handler. |

**Software SMI Trigger Register** **PM2F**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:0 | **SMI_CMD: SMI command.** Writes to this register set PM28[SWI_STS]. If PM2A[SWISMI_EN] is set, then writes to this port generate SMI interrupts. Reads of this register provide the data last written to it. This register is accessible through PM1E as well. |

**Miscellaneous SMI Status Register** **PM30**

Default: 0000h. Attribute: Read; set by hardware; write 1 to clear.

These bits may be enabled to generate SMI interrupts via PM32.

| Bits | Description |
|---|---|
| 15:5 | Reserved. |
| 4 | **64MS_STS: 64 millisecond timer status.** After PM32[64MS_EN] is set High, the 64 millisecond timer will count out 64 +/- 4 milliseconds and then set this bit. The timer will continue counting the next 64 millisecond period after this bit is set. |
| 3 | **1MIN_STS: one minute status bit.** After entering the FON state, this bit is set every 60 +/- 4 seconds. |
| 2 | **SIRQSMI_STS: serial IRQ SMI status.** This bit is set when an SMI is transferred into the IC via the serial IRQ. |
| 1 | **RWR_STS: BIOS ROM write enable status.** This bit is set when DevB:0x40[RWR] is written from a 0 to a 1. |
| 0 | **SLPCMD_STS.** This bit is set if there is a write of PM04[SLP_EN] to a High. |

**Miscellaneous SMI Enable Register** **PM32**

Default: 0000h. Attribute: Read-write.

For each of the bits in this register: 1=enable a corresponding status bit in PM30 to generate an SMI interrupt. 0=Do not enable the SMI interrupt.

| Bits | Description |
|---|---|
| 15:5 | Reserved. |
| 4 | **64MS_EN: 64 millisecond SMI enable.** 1=Enable the 64 millisecond counter, as well as the corresponding SMI interrupt. 0=The 64 millisecond timer is cleared. |
| 3 | **1MIN_EN.** One minute SMI enable. |
| 2 | **SIRQSMI_EN.** Serial IRQ SMI enable. |
| 1 | **RWR_EN: BIOS ROM write enable SMI enable.** Read, write to 1 only. Once this bit is set, it can only be cleared by RESET#. |
| 0 | **SLPCMD_EN: enable SMI on sleep command.** Note: when this bit is set High and the sleep command is sent to PM04, the system power state is disabled from changing. It is expected that the SMI interrupt service routine will clear PM30[SLPCMD_STS], clear this bit, and then re-issue the command in order to change the system power state. |

**TCO Timer Reload and Current Value Register** **PM40**

Default: 04h. Attribute: Read; write command.

The TCO timer is a decrementing counter that is clocked approximately every 0.6 seconds providing times of up to 38 seconds. If it decrements past zero, it will set PM44[TOUT_STS], rollover to the value in PM41, and keep counting.

| Bits | Description |
|---|---|
| 7:6 | Reserved. |
| 5:0 | **TCORLD: TCO timer.** Reads of this register return the current count of the TCO timer. Writes of any value to this register cause the TCO timer to be reloaded with the value in PM41. |

**TCO Timer Initial Value Register** **PM41**

Default: 04h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:6 | Reserved. |
| 5:0 | **TCOTIME: TCO timer reload value.** Specifies the value to be loaded into the TCO timer, PM40. |

**TCO SMI Data In Register** **PM42**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:0 | **TCOSMI: TCO SMI data.** Writes to this register set PM44[SW_TCO_SMI] and generate an SMI. |

**TCO SMI Data Out Register** **PM43**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:0 | **TCOOUT: TCO output data to OS.** Writes to this register set PM44[TCO_INT_STS] and generate an IRQ as specified by DevB:3x44[TCO_INT_SEL] and PM22[TCOSCI_EN]. |

**TCO Status 1 Register** **PM44**

Default: 0000h. Attribute: Read; set by hardware; write 1 to clear.

| Bits | Description |
|---|---|
| 15:9 | Reserved. |
| 8 | **IBIOS_STS: BIOS illegal access status.** 1=Hardware sets this bit and an SMI is generated (if PM2A[TCO_EN]=1) as a result of an illegal access to BIOS address space; this occurs when: (1) there is a read to a read-locked address or a write to a write-locked address as specified by DevB:0x40[RWR], DevB:0x80, DevB:0x84, DevB:0x88, and DevB:0x8C[3:0] or (2) DevB:0x40[BLE]=1, and DevB:0x40[RWR] is written from a 0 to a 1. |
| 7:4 | Reserved. |
| 3 | **TOUT_STS: TCO timer timeout status.** 1=Hardware sets this bit and an SMI is generated (if PM2A[TCO_EN]=1) as a result of the TCO timer (PM40) counting past zero. |
| 2 | **TCO_INT_STS: TCO interrupt status.** 1=Hardware sets this bit and an IRQ is generated (as specified by DevB:3x44[TCO_INT_SEL] and PM22[TCOSCI_EN]) by a write to PM43. |
| 1 | **SW_TCO_SMI: software-generated SMI status.** 1=Hardware sets this bit and an SMI is generated (if PM2A[TCO_EN]=1) by a write to PM42. |
| 0 | **NMI2SMI_STS: NMI to SMI status.** 1=Hardware sets this bit and an SMI is generated as a result of an NMI while PM48[NMI2SMI_EN] is High. Note: PM48[NMI_NOW] does not set this status bit. |

**TCO Status 2 Register** **PM46**

Default: 00h. Attribute: Read; set by hardware; write 1 to clear.

| Bits | Description |
|---|---|
| 7:3 | Reserved. |
| 2 | **BOOT_STS: boot status.** 1=Hardware sets this bit when PM46[2NDTO_STS] changes from 0 to 1 after any RESET# before any ROM accesses have occurred. This bit resides on the VDD_AUX power plane. |
| 1 | **2NDTO_STS: second TCO time out status.** 1=Hardware sets this bit when the TCO timer, PM40, times out a second time before PM44[TOUT_STS] is cleared. If enabled by DevB:3x48[NO_REBOOT], this may trigger a reboot of the system. This bit resides on the VDD_AUX power plane. |
| 0 | **INTRDR_STS: intruder detect status.** 1=Hardware sets this bit when the INTRUDER# pin is asserted for more than 60 microseconds (debounce time); this bit functions in all power states (unless VDD_AL is not powered). This bit resides in the VDD_AL power plane; when VDD_AL is powered, this bit defaults to 0. This may trigger an interrupt as specified by PM4A[INTRDR_SEL]. |

**TCO Control 1 Register** **PM48**

Default: 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:12 | Reserved. |
| 11 | **TCOHALT: TCO timer halt.** 1=Freeze the TCO timer (PM40) in its current state; PM44[TOUT_STS] and PM46[2NDTO_STS] cannot be set. |
| 10 | Reserved. |
| 9 | **NMI2SMI_EN: NMI interrupts generate SMI interrupts.** 1=Whenever an NMI is detected, PM44[NMI2SMI_STS] is set and no NMI is generated; this bit does not affect NMI_NOW (setting NMI_NOW generates an NMI regardless of the state of NMI2SMI_EN). Note: if this bit is set and RTC70[NMIDIS] is set, then no NMIs or the associated SMIs will be generated. |
| 8 | **NMI_NOW: Generate NMI.** 1=Generate NMI. It is expected that the NMI handler clears this bit. ***Note:*** *Setting this bit will not cause the SIT timer to be reloaded, regardless of PMAC[NMIRL].* |
| 7:0 | Reserved. |

**TCO Control 2 Register** **PM4A**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:3 | Reserved. |
| 2:1 | **INTRDR_SEL.** Select the action to take if PM46[INTRDR_STS] is set. 00b=Reserved; 01b=IRQ (as specified by DevB:3x44[TCO_INT_SEL]); 10b=SMI; 11b=Reserved. |
| 0 | Reserved. |

**Read write Register** **PM4C**

Default: 0000h. Attribute: Read-write.

All these bits reside on the VDD_AUX power plane.

| Bits | Description |
|---|---|
| 31:24 | Reserved. |
| 23:0 | **RW.** These bits control no hardware. |

**Timer and Device Monitor Registers** **PM[8C:50] bits[19:0]**

Default: 0000h (for each register). Attribute: See below.
Offset: 8Fh–40h (four bytes for each register).

Each of these registers provide access to the re-trigger timers. Each timer decrements at a rate specified by CLKSRC when enabled. Each timer is associated with device monitor events including address traps, DMA acknowledge cycles and interrupt requests. Each time a device monitor event associated with a re-trigger timer occurs, the timer is reloaded. So, if the hardware is regularly accessed, then the timer never reaches zero. If the timer decrements past zero, then it is disabled from counting further (staying at zero) and the appropriate device monitor status bit is set. Here is a summary of the device monitor events associated with these registers:

| Register | Function | Address specification; DMA channels; IRQs |
|---|---|---|
| PM50 | Access to the primary or secondary floppy disk controllers. | IO space 3F0h–3F5h, 3F7h, or 370h–375h, 377h fixed; DMA channel 2 in PM50 |
| PM54 | Access to the parallel ports. | See PM54; one of DMA[3:0]; see note 1. |
| PM58 | Access to serial port COMA. (modem) | See PM58 |
| PM5C | Access to serial port COMB. (IR) | See PM5C |
| PM60 | Access to the audio hardware. | See PM60; any or all or DMA[7:5, 3:0] |
| PM64 | User Interface: access to the video adapter; access to the legacy keyboard and PS/2 mouse ports; PCI bus utilization | Memory space 0A0000h–0BFFFFh fixed; IO space 3B0h–3DFh, 60h, 64h; IRQ1, IRQ12 |
| PM68 | PIO access to any IDE drives. | IO address space specified by DevB:1xXX |
| PM6C | Access to CARDBUS 0. | Address in space DevB:3xB4, DevB:3xB8, DevB:3xBC, DevB:3xC0 |
| PM70 | Access to CARDBUS 1. | |
| PM74 | Timer. | None. |
| PM78 | Access to programmable IO range monitor 1. | Address in space DevB:3xC4, DevB:3xC8, DevB:3xCC |
| PM7C | Access to programmable IO range monitor 2. | |
| PM80 | Access to programmable IO range monitor 3. | |
| PM84 | Access to programmable IO range monitor 4. | |
| PM88 | Access to programmable memory/config range monitor 1. | Address in space DevB:3xD0, DevB:3xD4, DevB:3xD8 |
| PM8C | Access to programmable memory/config range monitor 2. | |

Note 1: PM54 can alternately be used as an inactivity timer for PCI bus master activity based on REQ[6:0]#, PREQ#, and internal master requests.

The following provides the field definitions for bits[19:0] common to each of the twenty 32-bit registers from PM50 to PM8C. See PM50-PM8C bits[31:20], below, for the unique bit definitions.

| Bits | Description |
|---|---|
| 31:20 | See PM50-PM8C below |
| 19 | Reserved. |
| 18 | **TMR_EN: re-trigger timer enable.** Read-write. 1=Enable the re-trigger timer to decrement and to set the corresponding bit in the device monitor status register (PMA0) to generate an SMI or SCI interrupt. 0=Disable. If the timer is enabled and decrements past zero, then the PMA0 status bit is set and the timer stops (at zero). Also, whenever a High is written to TMR_EN, the corresponding re-trigger timer is loaded with its reload value. |
| 17 | **SIT_RLD: system inactivity timer reload on device monitor event.** Read-write. 1=Enable system inactivity timer (PM98) to be reloaded by associated device monitor events; the event (not the associated STS bit) causes the SIT to be reloaded. 0=SIT not reloaded by associated device monitor event. |
| 16 | Reserved. |
| 15:14 | **CLKSRC: clock source.** Read-write. Specifies the clock to the re-trigger timer per the following table.<br><br>CLKSRC / Clock period / Maximum time (clock times 128)<br>00b / 1 millisecond / 128 milliseconds<br>01b / 32 milliseconds / 4.1 seconds<br>10b / 1 second / 128 seconds = 2.13 minutes<br>11b / 64 seconds / 136.5 minutes = 2.28 hours |
| 13:7 | **CURCOUNT.** Read only. Re-trigger timer current count value. |
| 6:0 | **RELOAD: re-trigger timer reload value.** Read-write. Device monitor events cause the re-trigger timer to be loaded with the state of this register. Also, writes to this field cause the re-trigger counter CURCOUNT to be updated. |

**Floppy Disk Controller Device Monitor Unique Controls** **PM50 bits[31:20]**

Default: 0000 0000h. Attribute: Read-write.

See PM[8C:50], above, for bits[19:0].

| Bits | Description |
|---|---|
| 31:23 | Reserved. |
| 22 | **FDCDEC_EN: floppy disk controller decode enable.** 1=Enable accesses to floppy disk controller address range specified by PM50[FDCDEC_SEL] to generate a device monitor event. 0=Disable. |
| 21 | **FDCDEC_SEL: floppy disk controller decode select.** This selects the floppy disk controller IO address range for the FDC device monitor events. 1=Secondary FDC Address (370h–375h, 377h). 0=Primary FDC Address (3F0h–3F5h, 3F7h). |
| 20 | **FDCDMA_EN: floppy disk controller DMA enable.** 1=Enable DMA channel 2 to generate the FDC device monitor event. 0=Disable. |

**Parallel Port Device Monitor Unique Controls** **PM54 bits[31:20]**

Default: 0000 0000h. Attribute: Read-write.

See PM[8C:50], above, for bits[19:0].

| Bits | Description |
|---|---|
| 31:27 | Reserved. |
| 26 | **BMIT_EN: bus master inactivity timer enable.** 1=Re-trigger timer associated with PM54 is reloaded whenever a master access is indicated by REQ[6:0]#, PREQ#, or internal masters. 0=Re-trigger timer associated with PM54 is reloaded by parallel port device monitor events specified by LPTDEC_EN and LPTDMA_EN. |
| 25 | **LPTDEC_EN: LPT Port Monitoring enable.** 1=Enable accesses to the IO address range selected by PM54[LPTDEC_SEL] to generate a parallel port device monitor event. |
| 24:23 | **LPTDEC_SEL: LPT controller decode select.** Selects the IO address range used for parallel port device monitor events.<br>Bits[24:23] LPT Decode<br>00 3BCh–3BFh, 7BCh–7BEh<br>01 378h–37Fh, 778h–77Ah<br>10 278h–27Fh, 678h–67Ah<br>11 Reserved |
| 22 | **LPTDMA_EN: LPT DMA enable.** 1=Enable the DMA channel selected by PM54[LPTDMA_SEL] to generate a parallel port device monitor event. |
| 21:20 | **LPTDMA_SEL: LPT DMA select.** Selects the DMA channel used for the parallel port device monitor event.<br>Bits[21:20] DMA channel<br>00 DMA channel 0<br>01 DMA channel 1<br>10 DMA channel 3<br>11 Reserved |

**Serial Port A Device Monitor Unique Controls** **PM58 bits[31:20]**

Default: 0000 0000h. Attribute: Read-write.

See PM[8C:50], above, for bits[19:0].

| Bits | Description |
|---|---|
| 31:24 | Reserved. |
| 23 | **CMADEC_EN: serial port A monitor enable.** 1=Enable accesses to the IO address range selected by PM58[CMADEC_SEL] to generate a serial port A device monitor event. |
| 22:20 | **CMADEC_SEL: serial port A decode select.** Selects the IO address range used for serial port A device monitor events.<br><br>Bits[22:20] Serial A Decode — Bits[22:20] Serial A Decode<br>000 3F8h–3FFh (COM1) — 100 238h–23Fh<br>001 2F8h–2FFh (COM2) — 101 2E8h–2EFh (COM4)<br>010 220h–227h — 110 338h–33Fh<br>011 228h–22Fh — 111 3E8h–3EFh (COM3) |

**Serial Port B and Audio Device Monitor Unique Controls** **PM5C bits[31:20]**

Default: 0000 0000h. Attribute: Read-write.

See PM[8C:50], above, for bits[19:0]. Note: bits[31:24] of this register apply to the audio device monitor controls at PM60.

| Bits | Description |
|---|---|
| 31:29 | Reserved. |
| 28 | **MSS_EN: Microsoft sound system decode enable.** 1=Enable accesses to the IO address range selected by PM5C[MSS_SEL] to generate an audio device monitor event. Note: this bit applies to the audio device monitor, PM60. |
| 27:26 | **MSS_SEL: Microsoft sound system decode select.** Selects the MSS IO address range used for audio device monitor events. Note: this bit applies to the audio device monitor, PM60.<br><br>Bits[4:3] MSS Decode<br>00 530h–537h<br>01 604h–60Bh<br>10 E80h–E87h<br>11 F40h–F47h |
| 25 | **GAME_EN: game port enable.** 1=Enable accesses to the IO address range 200h–207h to generate audio device monitor events. Note: this bit applies to the audio device monitor, PM60. |
| 24 | **MIDI_EN: MIDI enable.** 1=Enable accesses to the IO address range selected by PM60[MIDI_SEL] to generate an audio device monitor event. Note: this bit applies to the audio device monitor, PM60. |
| 23 | **CMBDEC_EN: serial port B monitor enable.** 1=Enable accesses to the IO address range selected by PM5C[CMBDEC_SEL] to generate a serial port B device monitor event. |
| 22:20 | **CMBDEC_SEL: serial port B decode select.** Selects the IO address range used for serial port B device monitor events.<br><br>Bits[22:20] Serial B Decode<br>000 3F8h–3FFh (COM1)<br>001 2F8h–2FFh (COM2)<br>010 220h–227h<br>011 228h–22Fh<br>Bits[22:20] Serial B Decode<br>100 238h–23Fh<br>101 2E8h–2EFh (COM4)<br>110 338h–33Fh<br>111 3E8h–3EFh (COM3) |

**Audio Device Monitor Unique Controls** **PM60 bits[31:20]**

Default: 0000 0000h. Attribute: Read-write.

See PM[8C:50], above, for bits[19:0]. Note: PM5C[31:24] contains some control bits for the audio device monitors as well as PM60.

| Bits | Description |
|---|---|
| 31:30 | **MIDI_SEL: MIDI decode select.** Selects the MIDI IO range used for audio device monitor events (the enable for this range is PM5C[MIDI_EN]).<br><br>Bits [31:30] MIDI Decode<br>00 300h–303h<br>01 310h–313h<br>10 320h–323h<br>11 330h–333h |
| 29 | Reserved. |
| 28 | **SB_EN: Sound Blaster 8/16 decode enable.** 1=Enable accesses to the IO address range selected by the SB_SEL field and to 388h–38Bh to generate audio device monitor events. |
| 27:26 | **SB_SEL: Sound Blaster decode select.** Selects the Sound Blaster IO address range used for audio device monitor events.<br><br>Bits [27:26] SB_SEL Decode<br>00 220h–233h<br>01 240h–253h<br>10 260h–273h<br>11 280h–293h |
| 25:20 | **ADMA_EN: audio DMA enable.** Each of these bits specifies whether a DMA channel is enabled for audio device monitor events. Bit[20] specifies DMA channel 0; bit[21] specifies DMA channel 1; bit[22] specifies DMA channel 3; bit[23] specifies DMA channel 5; bit[24] specifies DMA channel 6; bit[25] specifies DMA channel 7. 1=Enable the corresponding DMA request signal to generate an audio device monitor event. 0=Disable. |

**User Interface Device Monitor Unique Controls** **PM64 bits[31:20]**

Default: 0000 0000h. Attribute: Read-write.

See PM[8C:50], above, for bits[19:0].

| Bits | Description |
|---|---|
| 31:25 | Reserved. |
| 24 | **GRAB_EN: graphics A/B segment memory enable.** 1=Enable accesses to VGA frame buffer memory address ranges A_0000h through B_FFFFh to generate user interface device monitor events. |
| 23 | **GRIO_EN: graphics IO enable.** 1=Enable accesses to VGA IO addresses 3B0h–3DFh to generate user interface device monitor events. |
| 22 | **KBC_EN: keyboard enable.** 1=Enable accesses to the keyboard controller IO address range (ports 60h and 64h) to generate user interface device monitor events. |
| 21 | **IRQ1_EN: IRQ1 enable.** 1=Enable IRQ1 (keyboard activity) to generate a user interface device monitor event. |
| 20 | **IRQ12_EN: IRQ12 enable.** 1=Enable IRQ12 (mouse activity) to generate user interface device monitor events. |

**General Purpose Timer** **PM94**

Default: 0000h. Attribute: Read-write.

The purpose of this timer is to generate an interrupt at a specified time in the future.

| Bits | Description |
|---|---|
| 15:13 | Reserved. |
| 12 | **GPT_CLK: general purpose timer clock source.** Specifies the clock to the general purpose timer as follows:<br><br>GPT_CLK — Clock period — Maximum time (clock times 4096)<br>0 — 30.52 microseconds — 125 milliseconds<br>1 — 31.25 milliseconds — 128 seconds |
| 11:0 | **GPT_CNT: general purpose timer count value.** Reads provide the current state of the general purpose timer. Writes to this field load a value in the timer. Once loaded—if either PMA4[GPT_EN] or PMA8[GPTSMI_EN] is set High—the timer counts down to zero and stops. On the clock after GPT_CNT reaches zero, PMA0[GPT_STS] is set High. If PMA4[GPT_EN] and PMA8[GPTSMI_EN] are Low, then the general purpose timer does not count and PMA0[GPT_STS] cannot be set High. |

**System Inactivity Timer Register** **PM98**

Default: 0000 0000h. Attribute: See below.

The system inactivity timer is a counter that may be reloaded by device monitor events as specified by PM[8C:50][SIT_RLD] or by events specified by PMAC. When it reaches zero, it will set PM20[SIT_STS] and may be enabled to generate interrupts.

| Bits | Description |
|---|---|
| 31:18 | Reserved. |
| 17:16 | **CLKSRC: clock source.** Read-write. Specifies the clock to the system inactivity timer per the following table.<br><br>CLKSRC / Clock period / Maximum time (clock times 128)<br>00b / 1 millisecond / 128 milliseconds<br>01b / 32 milliseconds / 4.1 seconds<br>10b / 1 second / 128 seconds = 2.13 minutes<br>11b / 64 seconds / 136.5 minutes = 2.28 hours |
| 15:8 | **CURCOUNT.** Read only. System inactivity timer current count value. |
| 7:0 | **RELOAD: system inactivity timer reload value.** Read-write. Writes to this field cause the system inactivity counter to be reloaded with the value written. |

**Device Monitor Status Register** **PMA0**

Default: 0000 0000h. Attribute: Read; set by hardware; write 1 to clear.

Each of status bits[19:0] is set by a device monitor event (an access to an IO or memory address range, an IRQ or a DMA request as specified by PM[8C:50] or a re-trigger timer time out) and bit[20] is set by the general purpose timer (specified by PM94). If any of these events occur, then the status bit is set. If any of these status bits are High and the corresponding enable bit is High (PMA4 and PMA8), then an interrupt is generated.

| Bits | Description |
|---|---|
| 31:21 | Reserved. |
| 20 | **GPT_STS.** General purpose timer status. This bit is set High by the hardware on the clock after PM94[GPT_CNT] reaches zero. However, if PMA4[GPT_EN] and PMA8[GPTSMI_EN] are both Low, then the PMA0[GPT_STS] will not be set High. |
| 19 | **PMM2_DM_STS.** Programmable memory range monitor 2 device monitor status. |
| 18 | **PMM1_DM_STS.** Programmable memory range monitor 1 device monitor status. |
| 17 | **PRM4_DM_STS.** Programmable range monitor 4 device monitor status. |
| 16 | **PRM3_DM_STS.** Programmable range monitor 3 device monitor status. |
| 15 | **PRM2_DM_STS.** Programmable range monitor 2 device monitor status. |
| 14 | **PRM1_DM_STS.** Programmable range monitor 1 device monitor status. |
| 13 | **GPT_DM_STS.** General purpose timer timeout device monitor status. |
| 12 | **CARDBUS1_DM_STS.** CARDBUS1 access device monitor status. |
| 11 | **CARDBUS0_DM_STS.** CARDBUS0 access device monitor status. |
| 10 | Reserved. |
| 9 | **USRINT_DM_STS.** User interface device monitor status. |
| 8 | **AUD_DM_STS.** Audio functions device monitor status. |
| 7 | **CMB_DM_STS.** Serial port B (COM B) device monitor status. |
| 6 | **CMA_DM_STS.** Serial port A (COM A) device monitor status. |
| 5 | **LPT_DM_STS.** Parallel port (LPT) device monitor status. |
| 4 | **FDD_DM_STS.** Floppy disk drive device monitor status. |
| 3 | **DSS_DM_STS.** IDE secondary slave port device monitor status. |
| 2 | **DSM_DM_STS.** IDE secondary master port device monitor status. |
| 1 | **DPS_DM_STS.** IDE primary slave port device monitor status. |
| 0 | **DPM_DM_STS.** IDE primary master port device monitor status. |

**Device Monitor ACPI Interrupt Enable Register** **PMA4**

Default: 0000 0000h. Attribute: Read-write.

For each of these bits: 1=Enable either an SCI or an SMI interrupt based on the state of PM04[SCI_EN] if the corresponding status bit in PMA0 is set.

| Bits | Description |
|---|---|
| 31:21 | Reserved. |
| 20 | **GPT_EN.** General purpose timer ACPI interrupt enable. |
| 19 | **PMM2_DM_EN.** Programmable memory range monitor 2 device monitor ACPI interrupt enable. |
| 18 | **PMM1_DM_EN.** Programmable memory range monitor 1 device monitor ACPI interrupt enable. |
| 17 | **PRM4_DM_EN.** Programmable range monitor 4 device monitor ACPI interrupt enable. |
| 16 | **PRM3_DM_EN.** Programmable range monitor 3 device monitor ACPI interrupt enable. |
| 15 | **PRM2_DM_EN.** Programmable range monitor 2 device monitor ACPI interrupt enable. |
| 14 | **PRM1_DM_EN.** Programmable range monitor 1 device monitor ACPI interrupt enable. |
| 13 | **GPT_DM_EN.** General purpose timer timeout device monitor ACPI interrupt enable. |
| 12 | **CARDBUS1_DM_EN.** CARDBUS1 access device monitor ACPI interrupt enable. |
| 11 | **CARDBUS0_DM_EN.** CARDBUS0 access device monitor ACPI interrupt enable. |
| 10 | Reserved. |
| 9 | **USRINT_DM_EN.** User interface device monitor ACPI interrupt enable. |
| 8 | **AUD_DM_EN.** Audio functions device monitor ACPI interrupt enable. |
| 7 | **CMB_DM_EN.** Serial port B (COM B) device monitor ACPI interrupt enable. |
| 6 | **CMA_DM_EN.** Serial port A (COM A) device monitor ACPI interrupt enable. |
| 5 | **LPT_DM_EN.** Parallel port (LPT) device monitor ACPI interrupt enable. |
| 4 | **FDD_DM_EN.** Floppy disk drive device monitor ACPI interrupt enable. |
| 3 | **DSS_DM_EN.** IDE secondary slave port device monitor ACPI interrupt enable. |
| 2 | **DSM_DM_EN.** IDE secondary master port device monitor ACPI interrupt enable. |
| 1 | **DPS_DM_EN.** IDE primary slave port device monitor ACPI interrupt enable. |
| 0 | **DPM_DM_EN.** IDE primary master port device monitor ACPI interrupt enable. |

**Device Monitor SMI Interrupt Enable Register** **PMA8**

Default: 0000 0000h. Attribute: Read-write.

For each of these bits: 1=Enable SMI interrupt if the corresponding status bit in PMA0 is set.

| Bits | Description |
|---|---|
| 31:21 | Reserved. |
| 20 | **GPTSMI_EN.** General purpose timer SMI enable. |
| 19 | **PMM2_DMSMI_EN.** Programmable memory range monitor 2 device monitor SMI enable. |
| 18 | **PMM1_DMSMI_EN.** Programmable memory range monitor 1 device monitor SMI enable. |
| 17 | **PRM4_DMSMI_EN.** Programmable range monitor 4 device monitor SMI enable. |
| 16 | **PRM3_DMSMI_EN.** Programmable range monitor 3 device monitor SMI enable. |
| 15 | **PRM2_DMSMI_EN.** Programmable range monitor 2 device monitor SMI enable. |
| 14 | **PRM1_DMSMI_EN.** Programmable range monitor 1 device monitor SMI enable. |
| 13 | **GPT_DMSMI_EN.** General purpose timer timeout device monitor SMI enable. |
| 12 | **CARDBUS1_DMSMI_EN.** CARDBUS1 access device monitor SMI enable. |
| 11 | **CARDBUS0_DMSMI_EN.** CARDBUS0 access device monitor SMI enable. |
| 10 | Reserved. |
| 9 | **USRINT_DMSMI_EN.** User interface device monitor SMI enable. |
| 8 | **AUD_DMSMI_EN.** Audio functions device monitor SMI enable. |
| 7 | **CMB_DMSMI_EN.** Serial port B (COM B) device monitor SMI enable. |
| 6 | **CMA_DMSMI_EN.** Serial port A (COM A) device monitor SMI enable. |
| 5 | **LPT_DMSMI_EN.** Parallel port (LPT) device monitor SMI enable. |
| 4 | **FDD_DMSMI_EN.** Floppy disk drive device monitor SMI enable. |
| 3 | **DSS_DMSMI_EN.** IDE secondary slave port device monitor SMI enable. |
| 2 | **DSM_DMSMI_EN.** IDE secondary master port device monitor SMI enable. |
| 1 | **DPS_DMSMI_EN.** IDE primary slave port device monitor SMI enable. |
| 0 | **DPM_DMSMI_EN.** IDE primary master port device monitor SMI enable. |

**IRQ Reload Enable For System Inactivity Timer Register** **PMAC**

Default: 0000 0000h. Attribute: Read-write.

Each of these bits enable an event to trigger a reload of the system inactivity timer (SIT). In the case of the IRQRL signals, they cause the SIT to be reloaded whenever they toggle.

| Bits | Description |
|---|---|
| 31:20 | Reserved. |
| 19 | **BMREQRL.** 1=Any condition that sets PM00_BM_STS causes a reload of the system inactivity timer. |
| 18 | **EXTSMIRL.** 1=The status bit associated with the assertion of the EXTSMI# pin (PM20[EXSMI_STS]) causes a reload of the system inactivity timer. Note: as long as the status bit is set, the system inactivity timer will be held in its reload value and it will not decrement. |
| 17 | Reserved. |
| 16 | **NMIRL: NMI reload for the system inactivity timer.** 1=Enables NMI interrupt to reload the system inactivity timer. 0=NMI does affect the system inactivity timer. |
| 15:0 | **IRQRL: IRQs reload the system inactivity timer.** Each of these bits corresponds to an IRQ (e.g., bit 12 corresponds to IRQ12). The exception to this is bit 2, which corresponds to the interrupt output of the legacy PIC (APIC if DevB:0x4B[APICEN]=1). For each bit: 1=Enable the corresponding IRQ signal to cause the system inactivity timer to reload whenever it changes state (High to Low or Low to High). 0=IRQ signal does affect the system inactivity timer. |

**GPIO Pin Interrupt Status Register (ACPI GPE1_STS)** **PMB0**

Default: 0000 0000h (see note below). Attribute: Read; set by hardware; write 1 to clear.

Each of these status bits is driven by the output of the input circuit associated with the GPIO pins. Bit 0 corresponds to GPIO 0; bit 1 corresponds to GPIO1, and so forth. The latch associated with each GPIO input circuit is cleared when the corresponding bit in this register is written with a 1; writing a 0 has no effect.

| Bits | Description |
|---|---|
| 31:0 | GPIO IRQ status bits. |

**GPIO Pin ACPI Interrupt Enable Register (ACPI GPE1_EN** **PMB4**

Default: 0000 0000h. Attribute: Read-write.

For each of these bits: 1=Enable either an SCI or SMI interrupt based on the state of PM04[SCI_EN] if the corresponding status bit in PMB0 is set.

| Bits | Description |
|---|---|
| 31:0 | GPIO SCI/SMI enable bits. |

**GPIO Pin SMI Interrupt Enable Register** **PMB8**

Default: 0000 0000h. Attribute: Read-write.

For each of these bits: 1=Enable an SMI interrupt if the corresponding status bit in PMB0 is set.

| Bits | Description |
|---|---|
| 31:0 | GPIO SMI enable bits. |

**GPIO Output Clock 0 and 1 Register** **PMBC**

Default: FFFF FFFFh. Attribute: Read-write.

This register specifies the High time and the Low time for the GPIO output clocks. These clocks can be selected as the output for any of the GPIO pins. These output clocks consist of a 7-bit down counter that is alternately loaded with the High time and the Low time. The clock for the counters is selected by CLK[1,0]BASE.

| Bits | Description |
|---|---|
| 31:30 | **CLK1BASE.** See bits[15:14]. |
| 29:23 | **CLK1HI.** See bits[13:7]. |
| 22:16 | **CLK1LO.** See bits[6:0]. |
| 15:14 | **CLK0BASE. GPIO output clock timer base.** Specifies the clock for the counter that generates the GPIO output clock. 00b=250 microseconds; 01b=2 milliseconds; 10b=16 milliseconds; 11b=128 milliseconds. CLK0BASE specifies the clock for GPIO output clock 0 and CLK1BASE specifies the clock for GPIO output clock 1. |
| 13:7 | **CLK0HI. GPIO output clock High time.** Specifies the High time for the GPIO output clocks in increments of clock specified by CLK[1,0]BASE (if the base is 16 milliseconds, then 0 specifies 16 milliseconds, 1 specifies 32 milliseconds, etc.). CLK0HI specifies the High time for GPIO output clock 0 and CLK1HI specifies the High time for GPIO output clock 1. |
| 6:0 | **CLK0LO. GPIO output clock Low time.** Specifies the Low time for the GPIO output clocks in increments of the clock specified by CLK[1,0]BASE (if the base is 16 milliseconds, then 0 specifies 16 milliseconds, 1 specifies 32 milliseconds, etc.). CLK0LO specifies the Low time for GPIO output clock 0 and CLK1LO specifies the Low time for GPIO output clock 1. |

**General Purpose IO Pins GPIO[31:0] Select Registers** **PM[DF:C0]**

Default: Default: see the MODE field definition. Attribute: See below.
Offset: DFh–C0h (one single-byte register for each GPIO pin).

See Section 4.7.5 for details about the GPIO hardware.

Usage note: to set a GPIO pin as a software-controlled output, its corresponding GPIO register should be written with the value 04h for a Low and the value 05h for a High.

| Bits | Description |
|---|---|
| 7 | Reserved. |
| 6 | **LTCH_STS: GPIO latch status.** Read; set by hardware; write 1 to clear. This provides the current state of the latch associated with the input path for the GPIO pin that corresponds to the register. |
| 5 | **RTIN: real time in.** Read only. This provides the current, not-inverted state of the pad for the GPIO pin that corresponds to the register. |
| 4 | **DEBOUNCE: debounce the input signal.** Read-write. 1=The input signal is required to be held active without glitches for 12 to 16 milliseconds before being allowed to set the GPIO latch or being capable of being passed along to the circuitry being controlled by the output of the input path. |
| 3:2 | **MODE[1:0]: pin mode select.** Read-write. These specify the GPIO pin mode as follows:<br>MODE[1:0] GPIO pin mode<br>00b GPIO input<br>01b GPIO output<br>1Xb Pin performs alternate function (non-GPIO mode). |
| 1:0 | **X[1:0].** Read-write. If the GPIO function is not used by the pin (if the pin is programmed as an alternative to the GPIO function, e.g. CPUSLEEP#), then this field does not matter. If the GPIO function is selected, then based on whether the GPIO pin is an input or an output (selected by MODE also), this register has the meanings shown in the table below. |

:

| IO mode | Bits | Name | Function |
|---|---|---|---|
| Input | X0 | ACTIVEHI | 0=The pin is active Low and the signal is inverted as it is brought into the input path. 1=The pin is active High and therefore not inverted as it is brought through the input path. Note: the IRQ1, IRQ8, IRQ12 and PNPIRQ[2:0] signals that pass through the GPIO input path are inverted in the interrupt routing logic before being passed to the PIC; therefore, for an active High IRQx or PNPIRQ pin, ACTIVEHI should be set High for active-Low (level triggered) interrupts and Low for active-High (edge triggered) interrupts. |
| Input | X1 | LATCH | 0=The latched version of the signal is not selected. 1=The latched version is selected. |
| Output | X[1:0]=0h | | Output is forced Low. |
| Output | X[1:0]=1h | | Output is forced High. |
| Output | X[1:0]=2h | | GPIO output clock 0 (specified by PMBC[15:0]). |
| Output | X[1:0]=3h | | GPIO output clock 1 (specified by PMBC[31:16]). |

The table below shows the default states for these registers and the pin definitions base on the state of MODE[1:0]. The “Default” field shows the defaults for all the bits in the register. The “Mode” field shows the

value required in order to enable the function specified in the "Signal Name" column ("x" specifies that the bit does not matter). The "Input Path" field shows how the alternate function signal is mapped into internal logic; "GPIO" specifies that the signal passes through the GPIO input path (and can therefore use the polarity, latch and debounce controls from the GPIO circuit); "Direct" specifies that the signal comes directly from the pad; "N/A" specifies that it is an output signal.

| GPIO name | Control Reg | Signal Name | Default | Mode | Input Path | Notes |
|---|---|---|---|---|---|---|
| GPIO0 | PMC0 | ACAV | 08h (ACAV input) | 1Xb | GPIO | 2 |
| GPIO1 | PMC1 | AGPSTOP# | 05h (GPIO1 output, High) | 1Xb | N/A | |
| GPIO2 | PMC2 | BATLOW# | 08h (BATLOW# input) | 1Xb | GPIO | 2 |
| GPIO3 | PMC3 | C32KHZ | 08h (C32KHZ output) | 1Xb | N/A | 2 |
| GPIO4 | PMC4 | CACHE_ZZ | 04h (GPIO4 output, Low) | 1Xb | N/A | |
| GPIO5 | PMC5 | GPIO5 | 00h (GPIO input) | 1Xb | Direct | |
| GPIO6 | PMC6 | CPUSLEEP# | 05h (GPIO6 output, High) | 1Xb | N/A | |
| GPIO7 | PMC7 | CPUSTOP# | 05h (GPIO7 output, High) | 1Xb | N/A | |
| GPIO8 | PMC8 | GPIO8 | 05h (GPIO8 output, High) | 1Xb | N/A | |
| GPIO9 | PMC9 | FANCON1 | 08h (FANCON1 output) | 1Xb | N/A | |
| GPIO10 | PMCA | FANRPM | 08h (FANRPM input) | 1Xb | direct | |
| GPIO11 | PMCB | INTIRQ8# | 05h (GPIO11 output, High) | 1Xb | N/A | |
| GPIO12 | PMCC | IRQ1 | 09h (IRQ1 input) | 1Xb | GPIO | 3 |
| GPIO13 | PMCD | IRQ6 | 09h (IRQ6 input) | 1Xb | GPIO | 3 |
| GPIO14 | PMCE | GPIO14 | 00h (GPIO14 input) | 0Xb | N/A | 2 |
| GPIO15 | PMCF | IRQ12 | 09h (IRQ12 input) | 1Xb | GPIO | 3 |
| GPIO16 | PMD0 | GPIO16 | 00h (GPIO input) | 0Xb | N/A | |
| GPIO17 | PMD1 | GPIO17 | 00h (GPIO input) | 0Xb | N/A | |
| GPIO18 | PMD2 | LID | 00h (GPIO input) | 1Xb | Direct | 2 |
| GPIO19 | PMD3 | PNPIRQ0 | 09h (PNPIRQ0 input) | 1Xb | GPIO | |
| GPIO20 | PMD4 | PNPIRQ1 | 09h (PNPIRQ1 input) | 1Xb | GPIO | |
| GPIO21 | PMD5 | PNPIRQ2 | 09h (PNPIRQ2 input) | 1Xb | GPIO | |
| GPIO22 | PMD6 | SMBALERT# | 08h (SMBALERT# input) | 1Xb | Direct | 2 |
| GPIO23 | PMD7 | SLPBTN# | 08h (SLPBTN# input) | 1Xb | GPIO | 2 |
| GPIO24 | PMD8 | SQWAVE | 04h (GPIO24 output, Low) | 1Xb | N/A | |
| GPIO25 | PMD9 | SUSPEND# | 08h (SUSPEND# output) | 1Xb | N/A | |
| GPIO26 | PMDA | GPIO26 | 00h (GPIO input) | 0Xb | N/A | |
| GPIO27 | PMDB | GPIO27 | 00h (GPIO input) | 0Xb | N/A | |
| GPIO28 | PMDC | GPIO28 | 00h (GPIO28 input) | 0Xb | N/A | 1 |
| GPIO29 | PMDD | GPIO29 | 00h (GPIO29 input) | 0Xb | N/A | 1 |
| GPIO30 | PMDE | GPIO30 | 00h (GPIO30 input) | 0Xb | N/A | 1 |
| GPIO31 | PMDF | GPIO31 | 00h (GPIO31 input) | 0Xb | N/A | 1 |

Note 1: The input path from the IO cell for GPIO[31:28] goes to the IOAPIC to drive the interrupt request inputs to some of the redirection-table entries. Also, see DevB:0x4B[MPIRQ] for details on how GPIO[31:28] may be mapped to PIRQ[D:A]#. The polarity that enters the IOAPIC is determined by the ACTIVEHI control of X0 (0=inverted from the external pin).

Note 2: These pins, corresponding registers, and GPIO logic reside on the VDD_AUX power plane and are reset by RST_SOFT. All the other GPIO pins reside on the main power supply.

Note 3: When Serial IRQ is being used for IRQs 1, 6, or 12, the corresponding GPIO pin (12, 13, or 15) must be pulled High and Mode[1] must be set to 1.

**SMBus Global Status Register** **PME0**

Default: 0000h. Attribute: Read; set by hardware; write 1 to clear.

| Bits | Description |
|---|---|
| 15:12 | Reserved. |
| 11 | **SMB_BSY: SMBus busy.** Read only. 1=The SMBus is currently busy with a cycle generated by either the host or another SMBus master. |
| 10 | **SMBA_STS: SMBALERT# interrupt status.** This bit is set High by the hardware when SMBALERT# is asserted Low. This bit is not set unless the SMBALERT# function is selected by PMD6 and the IC is in the FON state. This bit may trigger an SMI or SCI interrupt if enabled to do so by PME2[SMBA_EN]. |
| 9 | **HSLV_STS: host-as-slave address match status.** This bit is set High by the hardware when an SMBus master (including the host controller) generates an SMBus write cycle with a 7-bit address that matches the one specified by PMEE. This bit is not set until the end of the acknowledge bit after the last byte is transferred; however, if a time out occurs after the address match occurs and before last acknowledge, then this bit is not set. This may trigger an SMI or SCI interrupt if enabled to do so by PME2[HSLV_EN]. This bit resides on the VDD_AUX power plane. |
| 8 | **SNP_STS: snoop address match status.** This bit is set High by the hardware when an SMBus master (including the host controller) generates an SMBus cycle with a 7-bit address that matches the one specified by PMEF. This bit is not set until the end of the acknowledge bit after the last byte is transferred; however, if a time out occurs after the address match occurs and before the last acknowledge, then this bit is not set. This bit may trigger an SMI or SCI interrupt if enabled to do so by PME2[SNP_EN]. This bit resides on the VDD_AUX power plane. |
| 7:6 | Reserved. |
| 5 | **TO_STS: time out error status.** This bit is set High by the hardware when a slave device forces a time out by holding the SMBUSC pin Low for more than 25 milliseconds. This bit may trigger an SMI or SCI interrupt if enabled to do so by PME2[HCYC_EN]. |
| 4 | **HCYC_STS: host cycle complete status.** This bit is set High by the hardware when a host cycle completes successfully. This bit may trigger an SMI or SCI interrupt if enabled to do so by PME2[HCYC_EN]. Note: it is illegal for SW to attempt to clear this bit when it is not yet set. |
| 3 | **HST_BSY: host controller busy.** Read only. 1=The SMBus host controller is busy with a cycle. |
| 2 | **PRERR_STS: protocol error status.** This bit is set High by the hardware when a slave device does not generate an acknowledge at the appropriate time during a host SMBus cycle. This bit may trigger an SMI or SCI interrupt if enabled to do so by PME2[HCYC_EN]. |
| 1 | **COL_STS: host collision status.** This bit is set High by the hardware when a host transfer is initiated at the same time another master is initiaing a cycle. This bit may trigger an SMI or SCI interrupt if enabled to do so by PME2[HCYC_EN]. Note: If the SMBus is detected busy prior to the command to initiate a host transfer, then the IC waits for the initial transaction to complete before executing the host transfer and this bit is not set; this bit may only be set when host transactions start at approximately the same time as other transactions. |
| 0 | **ABRT_STS: host transfer abort status.** This bit is set High by the hardware after a host transfer is aborted by PME2[ABORT] command. This bit may trigger an SMI or SCI interrupt if enabled to do so by PME2[HCYC_EN]. |

**SMBus Global Control Register** **PME2**

Default: 0000h. Attribute: Read-write.

Most of these bits enable either an SCI or an SMI interrupt based on the state of PM04[SCI_EN] if the corresponding status bit is set.

| Bits | Description |
|---|---|
| 15:11 | Reserved. |
| 10 | **SMBA_EN: SMBALERT# interrupt enable.** 1=Enables an SMI or SCI interrupt when PME0[SMBA_STS] is set High. This bit has no effect unless the SMBALERT# function is selected by PMD6. |
| 9 | **HSLV_EN: host-as-slave address match interrupt enable.** 1=Enables an SMI or SCI interrupt when PME0[HSLV_STS] is set High. This bit resides on the VDD_AUX power plane. |
| 8 | **SNP_EN: snoop address match interrupt enable.** 1=Enables an SMI or SCI interrupt when PME0[SNP_STS] is set High. This bit resides on the VDD_AUX power plane. |
| 7:6 | Reserved. |
| 5 | **ABORT: abort current host transfer command.** Write only. 1=The SMBus logic generates a stop event on the SMBus pins as soon as possible (there may be a delay if the SMBus slave is generating zeros during a read cycle). After the stop event is generated, PME0[ABRT_STS] is set High. |
| 4 | **HCYC_EN: host SMBus controller interrupt enable.** 1=The SMBus host controller status bits, PME0[TO_STS, HCYC_STS, PRERR_STS, COL_STS, ABRT_STS], are enabled to generate SMI or SCI interrupts. |
| 3 | **HOSTST: host start command.** Write only. 1=The SMBus host logic initiates the SMBus cycle specified by CYCTYPE. Writes to this field are ignored while PME0[HST_BSY] is active. |
| 2:0 | **CYCTYPE.** Host-generated SMBus cycle type. Writes to this field are ignored while PME0[HST_BSY] is active. This field specifies the type of SMBus cycle that is generated when it is initiated by the HOSTST command. Here is how it is decoded (for each of the registers, the slave address is specified by PME4[7:1] and “receive” or “read” versus “send” or “write” is specified by PME4[0]):<br><br>CYCTYPE — SMBus Cycle Type — Registers<br>000b — Quick command — Data bit in PME4[0]<br>001b — Receive or send byte — Data in PME6[7:0]. If the address in PME4 is 0001_1001b and data received is 111_0XXXb, then another byte will be received in PME6[15:8]; see also the SMBALERT description in Section 4.7.3.<br>010b — Read or write byte — Command in PME8; data in PME6[7:0]<br>011b — Read or write word — Command in PME8; data in PME6[15:0]<br>100b — Process call — Command in PME8; write data is placed in PME6[15:0]; then this data is replaced with the read data in the second half of the command<br>101b — Read or write block — Command in PME8; count data in PME6[5:0]; block data in the PME9 FIFO<br>11Xb — Reserved |

**SMBus Host Address Register** **PME4**

Default: 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:8 | **HST10BA: host 10-bit address LSBs.** This field stores the second byte of the address, used in 10-bit SMBus host-as-master transfers. If HSTADDR == 1111_0XXb, then the cycle is specified to use 10-bit addressing. If HSTADDR is any other value, then HST10BA is not utilized. |
| 7:1 | **HSTADDR: host cycle address.** This specifies the 7-bit address to the SMBus generated by the host (as a master) during SMBus cycles that are initiated by PME02[HOSTST]. |
| 0 | **READCYC: host read (High) write (Low) cycle.** 1=Specifies that the cycle generated by a write to PME02[HOSTST] is a read or receive command. 0=Cycle is a write or send command. |

**SMBus Host Data Register** **PME6**

Default: 0000h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 15:0 | **HSTDATA: host cycle data.** This register is written to by software to specify the data to be passed to the SMBus during write and send cycles. It is read by software to specify the data passed to host controller by the SMBus during read and receive cycles. Bit[0] specifies the data written or read during the quick command cycle. Bits[7:0] specify the data for byte read and write cycles, send byte cycles, and receive byte cycles. Bits[15:0] are used for word read and write cycles and process calls. Bits[5:0] are used to specify the count for block read and write cycles. |

**SMBus Host Command Field Register** **PME8**

Default: 00h. Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:0 | **HSTCMD: host cycle command.** This specifies the command field passed to the SMBus by the host controller during read byte, write byte, read word, write word, process call, block read, and block write cycles. Host cycles are initiated by PME2[HOSTST]. |

**SMBus Host Block Data FIFO Access Port** **PME9**

Default: 00h. Attribute: See below.

| Bits | Description |
|---|---|
| 7:0 | **HSTFIFO: host block read-write FIFO.** For block write commands, software loads 1 to 32 bytes into this port before sending them to the SMBus via the PME2[HOSTST] command. For block read commands, software reads 1 to 32 bytes from this port after the block read cycle is complete. If, during a block read or write, an error occurs, then the FIFO is flushed by the hardware. Read and write accesses to this port while the host is busy (PME0[HST_BSY]) are ignored. |

**SMBus Host-As-Slave Data Register** **PMEA**

Default: 0000h. Attribute: Read only.

| Bits | Description |
|---|---|
| 15:0 | **HSLVDATA: host-as-slave data.** When the logic detects that the current SMBus cycle is directed to the host's slave logic (because the address matches PMEE), then the data transmitted to the IC during the cycle is latched in this register. Also, if the address matches the snoop address in PMEF, then the cycle type is assumed to be a write word and the data is stored in this register. This register resides on the VDD_AUX power plane. |

**SMBus Host-As-Slave Device Address Register** **PMEC**

Default: 0000h. Attribute: Read only.

This register resides on the VDD_AUX power plane.

| Bits | Description |
|---|---|
| 15:8 | **HSLV10DA: host-as-slave 10-bit device address LSBs.** This field stores the second byte of the device address used in 10-bit SMBus transfers to the host as a slave. If HSLVDA == 1111_0XXb, then the cycle is specified by the SMBus specification to transmit a 10-bit device address to the host-as-slave logic and the second byte of that device address is stored in this field. If HSLVDA is any other value, then HSLV10BA is not utilized. |
| 7:1 | **HSLVDA: host-as-slave device address.** When the logic detects that the current SMBus cycle is directed to the host's slave logic (because the address matches PMEE), then the device address transmitted to the IC during the "command" phase of the cycle is latched in this register. Also, if the SMBus address matches the snoop address in PMEF, then the cycle type is assumed to be a write word and bits[7:1] of the command field for the cycle are placed in this field. |
| 0 | **SNPLSB: snoop command LSB.** If the SMBus cycle address matches PMEF, then the cycle type is assumed to be a write word. The LSB of the command field for the cycle is placed in this bit (and the other 7 bits are placed in HSLVDA). |

**SMBus Host-As-Slave Host Address Register** **PMEE**

Default: 10h. Attribute: Read-write.

This register resides on the VDD_AUX power plane.

| Bits | Description |
|---|---|
| 7:1 | **HSLVADDR: host-as-slave address.** The IC compares the address generated by masters over the SMBus to this field to determine if there is a match (also, for a match to occur, the read-write bit is required to specify a write command). If a match occurs, then the cycle is assumed to be a write word command to the host, with the slave's device address transmitted during the normal command phase. The device address is captured in PMEC and the data is capture in PMEA for the cycle. After the cycle is complete, PME0[HSLV_STS] is set. |
| 0 | Reserved. |

**SMBus Snoop Address Register** **PMEF**

Default: 10h. Attribute: Read-write.

This register resides on the VDD_AUX power plane.

| Bits | Description |
|---|---|
| 7:1 | **SNPADDR: snoop address.** The IC compares the address generated by masters over the SMBus to this field to determine if there is a match (regardless as to whether it is a read or a write). If there is a match, then PME0[SNP_STS] is set High after the cycle completes. If the address specified here matches PMEE, then PME0[SNP_STS] will not be set High. |
| 0 | Reserved. |

**Random Number Register** **PMF0**

Default: not deterministic. Attribute: Read only.

PMF0 and PMF4 together support the random number generator (RNG) function. When PMF4[RNGDONE] is 1, then the value in PMF0 has been updated. Reading PMF0 clears RNGDONE until the next valid random number is available in PMF0. New random numbers are generated approximately 128 microseconds after PMF0 is read. If PMF0 is read while RNGDONE = 0, then the value returned is all zeros.

| Bits | Description |
|---|---|
| 31:0 | **RANDOM_NUM.** Random number. |

**Random Number Status Register** **PMF4**

Default: 0000 0001h (see note in bit 0). Attribute: Read only.

| Bits | Description |
|---|---|
| 31:1 | Reserved. |
| 0 | **RNGDONE.** Random number generator number generation process complete. See PMF0. Note: this bit is Low after the trailing edge of RESET# and only goes High after the first random number is valid in PMF0, less than 500 microseconds later. |

**Fan Control Register** **PMF8**

Default: 0000h. Attribute: Read-write.

This register specifies the frequency and duty cycle for the FANCON[1:0] signals. The FANCON signals are clocks with a period specified by FC[1:0]FQ and a duty cycle specified by FC[1:0]HI. Bits[7:0] specify FANCON0 and bits[15:8] specify FANCON1. The system sleep state and these configuration bits interact to specify the FANCON[1:0] signal behavior as follows:

```
if ((system state=POS) & (FCxPOS=1)) then FANCONx=0;
  else if((FCxTHERM=1) & (THERM#=0)) then FANCONx=1;
  else FANCONx is controlled by the FCxFQ and FCxHI fields;
```

Note that this register defaults to both fans off, so BIOS must write this register to enable the fans.

| Bits | Description |
|---|---|
| 15 | Reserved. |
| 14 | **FC1POS.** See bit 6. |
| 13 | **FC1THERM.** See bit 5. |
| 12 | **FC1FQ.** See bit 4. |
| 11:8 | **FC1HI.** See bits[3:0]. |
| 7 | Reserved. |
| 6 | **FC0POS: FANCON0 power-on-suspend control.** 1=When the system is placed into the POS state, FANCON0 goes Low. 0=The system sleep state has no effect on FANCON0. |
| 5 | **FC0THERM: FANCON0 THERM# control.** 1=If the THERM# pin is asserted then FANCON0 goes High. 0=THERM# has no effect on FANCON0. This bit is ignored if the system is in POS and FC0POS is High. |
| 4 | **FC0FQ. FANCON0 frequency.** The frequency of FANCON[1:0] is specified by this bit. 0=A FANCON[1:0] period of 15 milliseconds. 1=A FANCON[1:0] period of 240 milliseconds. |
| 3:0 | **FC0HI. FANCON0 High time.** Specifies the percentage of time that FANCON[1:0] is High as:<br>`PERCENT HIGH TIME = FC[1:0]HI/15;`<br>(the rest of the time of the clock period, FANCON[1:0] is Low). E.g. if FC1HI == 0, then the FANCON1 is Low all the time; if FC1HI = 1, then FANCON1 is High 1/15$^{th}$ of the time; if FC1HI == 15, then FANCON1 is High all the time. |

# 5.8 AC ’97 Controller

## 5.8.1 AC’97 Audio Registers

### 5.8.1.1 AC’97 Audio PCI Configuration Registers

These registers are located in PCI configuration space on the primary PCI interface, in the second device (device B), function 5. See Section 5.1.2 for a description of the register naming convention.

**AC’97 Audio Controller Vendor and Device Id** **DevB:5x00**

Default: 7445_1022h Attribute: Read; write once.

| Bits | Description |
|---|---|
| 31:16 | **AC97 audio device ID.** |
| 15:0 | **Vendor ID.** |

**AC’97 Audio Controller Command and Status** **DevB:5x04**

Default: 0200_0000h Attribute: See below.

| Bits | Description |
|---|---|
| 31:3 | Read only. These bits fixed in their default state. |
| 2 | **BMEN: master enable.** Read-write. 1=Enables this function to initiate cycles to the host. |
| 1 | Reserved. |
| 0 | **IOEN: IO enable.** Read-write. 1=Enables access to the IO space for this function. |

**AC’97 Audio Controller Revision Id and Class Code** **DevB:5x08**

Default: 0401_0001h Attribute: Read only

| Bits | Description |
|---|---|
| 31:8 | **CLASSCODE.** Provides the class code for this function. |
| 7:0 | **REVID.** Audio controller silicon revision. |

**AC'97 Audio Controller BIST, Header and Latency** **DevB:5x0C**

Default: 0000_0000h Attribute: See below.

| Bits | Description |
|---|---|
| 31:24 | **BIST.** Read only. These bits fixed at their default values. |
| 23:16 | **HEADER.** Read only. These bits fixed at their default values. |
| 15:8 | **LATENCY.** Read-write. This field controls no hardware. |
| 7:0 | **CACHE.** Read only. These bits fixed at their default values. |

**AC'97 Audio Mixer Base Address** **DevB:5x10**

Default: 0000_0001h Attribute: See below.

| Bits | Description |
|---|---|
| 31:8 | **AMBA: audio mixer base address.** Read-write. This field specifies bits [31:8] of the 256-byte IO space used to access the audio interface mixer registers. |
| 7:0 | Read only. These bits fixed at their default values. |

**AC'97 Audio Controller Bus Master Base Address** **DevB:5x14**

Default: 0000_0001h Attribute: See below.

| Bits | Description |
|---|---|
| 31:6 | **ABMBA: audio bus master base address.** Read-write. This field specifies bits [31:6] of the 64-byte IO space used to access the audio bus master control registers. |
| 5:0 | Read only. These bits fixed at their default values. |

**AC'97 Audio Controller Subsystem and Subsystem Vendor Id** **DevB:5x2C**

Default: 0000_0000h Attribute: Read; write once.

| Bits | Description |
|---|---|
| 31:16 | **SUBSYSID: subsystem ID register.** |
| 15:0 | **SUBVENID subsystem vendor ID register.** |

**AC'97 Audio Controller Interrupt Line and Interrupt Pin** **DevB:5x3C**

Default: 0200h Attribute: See below.

| Bits | Description |
|---|---|
| 15:11 | Read only. These bits fixed at their default values. |
| 10:8 | **INTPIN.** Read only. This field specifies the PCI interrupt request pin is used for the AC '97 audio interrupt. It is hardwired to 010b to select PIRQB_L. |
| 7:0 | **INTLINE.** Read-write. This field controls no hardware. |

**AC'97 Audio Controller PCM Out Descriptor Shadow** **DevB:5x40**

Default: 0000_0000h Attribute: Read only

| Bits | Description |
|---|---|
| 31:1 | **DESCR.** Descriptor current value. This field provides the current PCM-out descriptor value. |
| 0 | Reserved. |

**AC'97 Audio Controller PCM In Descriptor Shadow** **DevB:5x44**

Default: 0000_0000h Attribute: Read only

| Bits | Description |
|---|---|
| 31:1 | **DESCR.** Descriptor current value. This field provides the current PCM-in descriptor value. |
| 0 | Reserved. |

**AC'97 Audio Controller Microphone In Descriptor Shadow** **DevB:5x48**

Default: 0000_0000h Attribute: Read only

| Bits | Description |
|---|---|
| 31:1 | **DESCR.** Descriptor current value. This field provides the current microphone-in descriptor value. |
| 0 | Reserved. |

**AC'97 Audio Controller General Control** **DevB:5x4C**

Default: 00h Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:1 | Reserved. |
| 0 | **PCTRL: PCM channel control.** 0=The left channel sample is always placed in the least significant sample of the stereo information pair. I.e. the stereo audio data stream written to host memory starts with a left channel sample. 1=The right channel sample is always placed in the least significant sample of the stereo information pair. |

### 5.8.1.2 AC '97 Audio Mixer Registers

The audio mixer registers are expected to reside in the codec. Accesses to these registers are forwarded through the AC link. Writes to the codec are completed when the data is inserted in the output slot.

The following table provides the offset addresses for the audio mixer registers. These registers are accessed via IO space. The base address register for these registers is DevB:5x10.

| Offset | Audio Mixer Register |
|---|---|
| 00h | Reset |
| 02h | Master Volume Mute |
| 04h | Headphone Volume Mute |
| 06h | Master Volume Mono Mute |
| 08h | Master Tone (R & L) |
| 0Ah | PC_BEEP Volume Mute |
| 0Ch | Phone Volume Mute |
| 0Eh | Mic Volume Mute |
| 10h | Line In Volume Mute |
| 12h | CD Volume Mute |
| 14h | Video Volume Mute |
| 16h | Aux Volume Mute |
| 18h | PCM Out Volume Mute |
| 1Ah | Record Select |
| 1Ch | Record Gain Mute |
| 1Eh | Record Gain Mic Mute |
| 20h | General Purpose |
| 22h | 3D Control |
| 24h | AC'97 RESERVED |

| Offset | Audio Mixer Register (Continued) |
|---|---|
| 26h | Powerdown Ctrl/Stat |
| 28h | Extended Audio |
| 2Ah | Extended Audio Ctrl/Stat |
| 2Ch | PCM Front DAC Rate |
| *2Eh* | *PCM Surround DAC Rate* |
| *30h* | *PCM LFE DAC Rate* |
| 32h | PCM ADC Rate |
| 34h | MIC ADC Rate |
| *36h* | *6Ch Vol: C, LFE Mute* |
| *38h* | *6Ch Vol: L, R Surround Mute* |
| 3Ah:56h | RESERVED |
| **58h** | **Vendor Reserved** |
| **7Ah** | **Vendor Reserved** |
| **7Ch** | **Vendor ID1** |
| **7Eh** | **Vendor ID2** |

Notes:
- Registers in bold are multiplexed between audio and modem functions.
- Registers in italics are for functions not supported by the IC.
- The IC does not support audio as a secondary codec.

#### 5.8.1.3 AC ’97 Audio Controller Bus Master Registers

These registers are accessed via IO space. They reside within the AC '97 controller. The three channels, PCM Out, PCM In, and Microphone In, each have their own set of bus mastering registers. The following register descriptions apply to all three channels.

The base address register for these registers is DevB:5x14. See Section 5.1.2 for a description of the register naming convention.

| Mnemonic | Register Name | Default |
|---|---|---|
| AC00 | PCM In Buffer Descriptor List Base Address | 0000_0000h |
| AC04 | PCM In Current Index Value | 00h |
| AC05 | PCM In Last Valid Index | 00h |
| AC06 | PCM In Status | 0001h |
| AC08 | PCM In Position in Current Buffer | 0000h |
| AC0A | PCM In Prefetched Index Value | 00h |
| AC0B | PCM In Control | 00h |

| Mnemonic | Register Name (Continued) | Default |
|---|---|---|
| AC10 | PCM Out Buffer Descriptor List Base Address | 0000_0000h |
| AC14 | PCM Out Current Index Value | 00h |
| AC15 | PCM Out Last Valid | 00h |
| AC16 | PCM Out Status | 0001h |
| AC18 | PCM Out Position in Current Buffer | 0000h |
| AC1A | PCM Out Prefetched Index | 00h |
| AC1B | PCM Out Control | 00h |
| AC20 | Mic. In Buffer Descriptor List Base Address | 0000_0000h |
| AC24 | Mic. In Current Index Value | 00h |
| AC25 | Mic. In Last Valid | 00h |
| AC26 | Mic. In Status | 0001h |
| AC28 | Mic. In Position in Current Buffer | 0000h |
| AC2A | Mic. In Prefetched Index | 00h |
| AC2B | Mic. In Control | 00h |
| AC2C | Global Control | 0000_0000h |
| AC30 | Global Status | 0030_0000h |
| AC34 | Codec Access Semaphore | 00h |

### AC'97 Audio Controller Buffer Descriptor List Base Address — AC00, AC10, AC20

Default: 0000_0000h Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:3 | **BDLBA: buffer descriptor list base address bits[31:3].** |
| 2:0 | Reserved. |

### AC'97 Audio Controller Current Index Value — AC04, AC14, AC24

Default: 00h Attribute: Read only.

| Bits | Description |
|---|---|
| 7:5 | Reserved. |
| 4:0 | **CIV: current index value.** These bits provides the buffer descriptor within the list of 32 descriptors that is currently being processed. |

### AC'97 Audio Controller Last Valid Index — AC05, AC15, AC25

Default: 00h Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:5 | Reserved. |
| 4:0 | **LVI: last valid index.** These bits provide the last valid descriptor in the list. |

### AC'97 Audio Controller Status — AC06, AC16, AC26

Some of the bits in this register may be enabled by AC0B, AC1B, AC2B to generate interrupts.

Default: 0001h Attribute: See below.

| Bits | Description |
|---|---|
| 15:5 | Reserved. |
| 4 | **FIFOERR: FIFO error.** Read; set by hardware; write 1 to clear. 1=A FIFO under-run or over-run has occurred as follows:<br>• AC[26, 06][FIFOERR] indicates a FIFO over-run. Incoming data was lost.<br>• AC16[FIFOERR] indicates a FIFO under-run. A sample was repeated because the next valid sample was not provided by the host in time for transmission over the AC97 link.<br>• |
| 3 | **BCIS: buffer completion interrupt status.** Read; set by hardware; write 1 to clear. 1=The last sample of a buffer has been processed and the Interrupt on Completion (IOC) bit in the command byte of the buffer descriptor was set. |
| 2 | **LVBCI: last valid buffer completion interrupt.** Read; set by hardware; write 1 to clear. 1=The last valid buffer has been processed. |
| 1 | **CELV: current equals last valid.** Read only. 1=The Current Index Value (ACx4[CIV]) is equal to the value in the Last Valid Index register (ACx5[LVI]) and the buffer pointed to by the CIV has been processed. |
| 0 | **BMCH: bus master controller halted.** Read only. 1=The bus master controller is halted. This may result from clearing the run/pause bit (ACxB[RUNBM]); in this case the IC may wait for the current transaction to complete before this bit goes High. This bit may also go High when the controller has processed the last valid buffer; in this case the IC will set ACx6[CELV] and halt. 0=The bus master controller resumes operation; this occurs when both the run/pause bit is set and the ACx6[CELV] is clear. |

### AC'97 Audio Controller Position in Current Buffer — AC08, AC18, AC28

Default: 0000h Attribute: Read only

| Bits | Description |
|---|---|
| 15:0 | **PICB: position in current buffer.** This field provides the number of samples left to be processed in the current buffer. |

**AC'97 Audio Controller Prefetched Index Value** **AC0A, AC1A, AC2A**

Default: 00h Attribute: Read only

| Bits | Description |
|---|---|
| 7:5 | Reserved. |
| 4:0 | **PIV: prefetched index value.** This field provides the current buffer descriptor in the list that has been prefetched. |

**AC'97 Audio Controller Control Register** **AC0B, AC1B, AC2B**

Default: 00h Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:5 | Reserved. |
| 4 | **IOCEN: interrupt on completion enable.** 1=Enable interrupt when corresponding bit in ACx6[BCIS] is set. |
| 3 | **FEIEN: FIFO error interrupt enable.** 1=Enable interrupt when corresponding bit in ACx6[FIFOERR] is set. |
| 2 | **LVBIEN: last valid buffer interrupt enable.** 1=Enable interrupt when corresponding bit in ACx6[LVBCI] is set. |
| 1 | **REGRST: register reset.** Read-write; cleared by hardware. 1=Contents of all registers of the bus master engine including the FIFOs are reset, except the interrupt enable bits (bits[4, 3, and 2] of this register). It is required that RUNBM (bit[0] of this register) be cleared and ACx6[BMCH] be asserted before this bit may be set. Setting it when either RUNBM is asserted or when ACx6[BMCH] is deasserted results in undefined behavior. 0=Not in reset condition. |
| 0 | **RUNBM: run/pause bus master.** 1=Enable bus master operation. 0=Disable bus master. If this bit is cleared during bus master activity, then all state information is retained. Bus master operation may be stopped and then resumed. |

**AC'97 Audio Controller Global Control** **AC2C**

Note: AC2C and MC3C provide access to the a single set of registers.

Default: 0000_0000h Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:6 | Reserved. |
| 5 | **SRIEN: secondary resume interrupt enable.** 1=Enable interrupt when AC30[SRINT] is set. |
| 4 | **PRIEN: primary resume interrupt enable.** 1=Enable interrupt when AC30[PRINT] is set. |
| 3 | **SHUTOFF: AC'97 shut off.** 1=Disable the AC'97signals; drive all AC'97 outputs Low and ignore all AC'97 inputs. 0=Enable the AC'97 signals. |
| 2 | **WRST: AC'97 warm reset.** Read-write; cleared by hardware. 1=A warm reset on the AC-link is generated. A warm reset will wake a suspended codec without clearing its internal registers. A warm reset can only occur in the absence of ACCLK. If this bit is set while ACCLK is operational, the write is ignored and the bit remains unchanged. |
| 1 | **CRST_L: AC'97 cold reset, active Low.** 0=A cold reset on the AC-link is generated and all data in the codec is lost. This bit is required to be Low for at lease 1 microsecond before being set High again. Reads of this bit reflect the state of the ACRST_L pin. |
| 0 | **GPIIEN: GPI interrupt enable.** This bit specifies whether a change in status of any codec GPI (General Purpose Input/Output, configured as an input) cause interrupts. 1=Enable interrupt when AC30[GPIINT] is set. |

**AC'97 Audio Controller Global Status** **AC30**

Note: AC30 and MC40 provide access to the a single set of registers.

Default: 0030_0000h Attribute: See below.

| Bits | Description |
|---|---|
| 31:18 | Reserved. |
| 17 | **MD3: power down semaphore for modem.** Read-write. This bit may be used by software in conjunction with the AD3 bit to coordinate the entry of the two codecs into the D3 state. This bit resides on the VDD_AUX power plane. It controls no hardware. |
| 16 | **AD3: power down semaphore for audio.** Read-write. This bit may be used by software in conjunction with the MD3 bit to coordinate the entry of the two codecs into the D3 state. This bit resides on the VDD_AUX power plane. It controls no hardware. |
| 15 | **RCSTAT: read complete status.** Read; set by hardware; write 1 to clear. 1=Codec read failed due to one of the following errors: (1) a time-out; (2) ACCLK detected to not be operating adequately. |
| 14 | **S12BIT3.** Bit 3 of slot 12. Read only. Provides bit 3 of the most recent slot 12 from the modem codec. |
| 13 | **S12BIT2.** Bit 2 of slot 12. Read only. Provides bit 2 of the most recent slot 12 from the modem codec. |
| 12 | **S12BIT1.** Bit 1 of slot 12. Read only. Provides bit 1 of the most recent slot 12 from the modem codec. |
| 11 | **SRINT: secondary resume interrupt.** Read; set by hardware; write 1 to clear. 1=A resume event occurred on ACSIDN[1]. |
| 10 | **PRINT: primary resume interrupt.** Read; set by hardware; write 1 to clear. 1=A resume event occurred on ACSIDN[0]. |
| 9 | **SCRDY: secondary codec ready.** Read only. Reflects the state of the codec ready bit in ACSDIN[1]. This bit is required to be High before bus masters activity may be initiated. This bit is cleared with assertion of AC2C[SHUTOFF] or when ACCLK is detected to not be operating. |
| 8 | **PCRDY: primary codec ready.** Read only. Reflects the state of the codec ready bit in ACSDIN[0]. This bit is required to be High before bus masters activity may be initiated. This bit is cleared with assertion of AC2C[SHUTOFF] or when ACCLK is detected to not be operating. |
| 7 | **MICINT: mic-in interrupt.** Read only. 1=One of the mic-in channel interrupts occurred. When the specific interrupt is cleared, this bit is cleared automatically. |
| 6 | **POINT: PCM-out interrupt.** Read only. 1=One of the PCM-out channel interrupts occurred. When the specific interrupt is cleared, this bit is cleared automatically. |
| 5 | **PIINT: PCM-in interrupt.** Read only. 1=One of the PCM-in channel interrupts occurred. When the specific interrupt is cleared, this bit is cleared automatically. |
| 4 | Reserved. |
| 3 | Reserved. |
| 2 | **MOINT: modem-out interrupt.** Read only. 1=One of the modem-out channel interrupts occurred. When the specific interrupt is cleared, this bit is cleared automatically. |
| 1 | **MIINT: modem-in interrupt.** Read only. 1=One of the modem-in channel interrupts occurred. When the specific interrupt is cleared, this bit is cleared automatically. |
| 0 | **GPIINT: GPI status change interrupt.** Read; set by hardware; write 1 to clear. This bit is set whenever bit 0 of slot 12 is set. This occurs when the value of any of the GPIOs defined as inputs changes. |

**AC'97 Audio Controller CODEC Access Semaphore** **AC34**

Note: AC34 and MC44 provide access to the a single set of registers.

Default: 00h Attribute: See below.

| Bits | Description |
|---|---|
| 7:1 | Reserved. |
| 0 | **CAS: codec access semaphore.** Read; set when read; cleared by hardware or by software. This bit may be used by software to determine if a codec access is currently in progress. Reading this register causes this bit to be set. If the bit is read as Low, then a codec IO access may be initiated. When the codec IO access is complete, or if ACCLK is detected to not be operating adequately, the bit is automatically cleared. 0=No codec access is in progress. If CAS=1 and a codec access has not yet been requested, CAS may be cleared by writing a 1 to this bit position. |

## 5.8.2 AC '97 Modem Registers

### 5.8.2.1 AC '97 Modem PCI Configuration Registers

These registers are located in PCI configuration space on the primary PCI interface, in the second device (device B), function 6. See Section 5.1.2 for a description of the register naming convention.

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**AC'97 Modem Controller Vendor and Device Id** **DevB:6x00**

Default: 7446_1022h Attribute: Read; write once.

| Bits | Description |
|---|---|
| 31:16 | **AC97 modem device ID.** |
| 15:0 | **Vendor ID.** |

**AC'97 Modem Controller Command and Status** **DevB:6x04**

Default: 0200_0000h Attribute: See below.

| Bits | Description |
|---|---|
| 31:3 | Read only. These bits are fixed in their default state. |
| 2 | **BMEN: master enable.** Read-write. 1=Enables this function to initiate cycles to the host. |
| 1 | Reserved. |
| 0 | **IOEN: IO enable.** Read-write. 1=Enables access to the IO space for this function. |

**AC'97 Modem Controller Revision Id and Class Code** **DevB:6x08**

Default: 0703_0001h Attribute: Read only

| Bits | Description |
|---|---|
| 31:8 | **CLASSCODE.** Provides the class code for this function. |
| 7:0 | **REVID.** AC '97 modem controller silicon revision. |

**AC'97 Modem Controller BIST, Header and Latency** **DevB:6x0C**

Default: 0000_0000h Attribute: See below.

| Bits | Description |
|---|---|
| 31:24 | **BIST.** Read only. These bits fixed at their default values. |
| 23:16 | **HEADER.** Read only. These bits fixed at their default values. |
| 15:8 | **LATENCY.** Read-write. This field controls no hardware. |
| 7:0 | **CACHE.** Read only. These bits fixed at their default values. |

**AC'97 Modem Mixer Base Address** **DevB:6x10**

Default: 0000_0001h Attribute: See below.

| Bits | Description |
|---|---|
| 31:8 | **MMBA: modem mixer base address.** Read-write. This field specifies bits [31:8] of the 256-byte IO space used to access the modem interface mixer registers. |
| 7:0 | Read only. These bits fixed at their default values. |

**AC'97 Modem Controller Bus Master Base Address** **DevB:6x14**

Default: 0000_0001h Attribute: See below.

| Bits | Description |
|---|---|
| 31:7 | **MBMBA: modem bus master base address.** Read-write.This field specifies bits [31:7] of the 128-byte IO space used to access the modem bus master control registers. |
| 6:0 | Read only. These bits fixed at their default values. |

**AC'97 Modem Controller Subsystem and Subsystem Vendor Id** **DevB:6x2C**

Default: 0000_0000h Attribute: Read, write once

| Bits | Description |
|---|---|
| 31:16 | **SUBSYSID: subsystem ID register.** |
| 15:0 | **SUBVENID: subsystem vendor ID register.** |

**AC'97 Modem Controller Interrupt Line and Interrupt Pin** **DevB:6x3C**

Default: 0200h Attribute: See below.

| Bits | Description |
|---|---|
| 15:11 | Read only. These bits fixed at their default values. |
| 10:8 | **INTPIN.** Read only. This field specifies the PCI interrupt request pin is used for the AC '97 audio interrupt. It is hardwired to 010b to select PIRQB_L. |
| 7:0 | **INTLINE.** Read-write. This field controls no hardware. |

**AC'97 Modem Controller Modem Out Descriptor Shadow** **DevB:6x40**

Default: 0000_0000h Attribute: Read only

| Bits | Description |
|---|---|
| 31:1 | **DESCR.** Descriptor current value. This field provides the current modem-out descriptor value. |
| 0 | Reserved. |

**AC'97 Modem Controller Modem In Descriptor Shadow** **DevB:6x44**

Default: 0000_0000h Attribute: Read only

| Bits | Description |
|---|---|
| 31:1 | **DESCR.** Descriptor current value. This field provides the current modem-in descriptor value. |
| 0 | Reserved. |

#### 5.8.2.2 AC ’97 Modem Mixer Registers

The modem mixer registers are expected to reside in the codec. Accesses to these registers are forwarded through the AC link. Writes to the codec are completed when the data is inserted in the output slot.

In the case of the split codec implementation (i.e., separate primary and secondary codecs), accesses to the modem mixer registers in different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec and address offsets 80h–FFh for the secondary codec.

The following table provides the offset addresses for the modem mixer registers. These registers are accessed via IO space. The base address register for these registers is DevB:6x10.

| **Offset** | | |
|---|---|---|
| **Primary** | **Secondary** | **Modem Mixer Register** |
| 00h:38h | 80h:B8h | RESERVED |
| 3Ch | BCh | Extended Modem ID |
| 3Eh | BEh | Extended Modem Stat/Ctrl |
| 40h | C0h | Line 1 DAC/ADC Rate |
| *42h* | *C2h* | *Line 2 DAC/ADC Rate* |
| *44h* | *C4h* | *Handset DAC/ADC Rate* |
| 46h | C6h | Line 1 DAC/ADC Level Mute |
| *48h* | *C8h* | *Line 2 DAC/ADC Level Mute* |
| *4Ah* | *CAh* | *Handset DAC/ADC Level Mute* |
| 4Ch | CCh | GPIO Pin Config |
| 4Eh | CEh | GPIO Polarity/Type |
| 50h | D0h | GPIO Pin Sticky |
| 52h | D2h | GPIO Pin Wake Up |
| 54h | D4h | GPIO Pin Status |
| 56h | D6h | Misc. Modem AFE Stat/Ctrl |
| **58h** | **D8h** | **Vendor Reserved** |
| **7Ah** | **FAh** | **Vendor Reserved** |
| **7Ch** | **FCh** | **Vendor ID1** |
| **7Eh** | **FEh** | **Vendor ID2** |

Notes:
- Registers in bold are multiplexed between audio and modem functions.
- Registers in italics are for functions not supported by the IC.
- The IC supports a modem codec as either primary or secondary codec, but does not support two modem codecs.

### 5.8.2.3 AC ’97 Modem Controller Bus Master Registers

These registers are accessed via IO space. They reside within the AC ’97 controller. The two channels, Modem In and Modem Out, each have their own set of bus mastering registers. The following register descriptions apply to both channels.

The base address register for these registers is DevB:6x14. See Section 5.1.2 for a description of the register naming convention.

| Mnemonic | Name | Default |
|---|---|---|
| MC00 | Modem In Buffer Descriptor List Base Address | 0000_0000h |
| MC04 | Modem In Current Index Value | 00h |
| MC05 | Modem In Last Valid Index | 00h |
| MC06 | Modem In Status | 0001h |
| MC08 | Modem In Position in Current Buffer | 0000h |
| MC0A | Modem Prefetch Index Value | 00h |
| MC0B | Modem In Control | 00h |
| MC10 | Modem Out Buffer Descriptor List Base Address | 0000_0000h |
| MC14 | Modem Out Current Index Value | 00h |
| MC15 | Modem Out Last Valid | 00h |
| MC16 | Modem Out Status | 0001h |
| MC18 | Modem Out Position in Current Buffer | 0000h |
| MC1A | Modem Out Prefetched Index | 00h |
| MC1B | Modem Out Control | 00h |
| MC3C | Global Control | 0000_0000h |
| MC40 | Global Status | 0030_0000h |
| MC44 | Codec Access Semaphore | 00h |
| MC48 | GPIO Pin Status | 0000h |

**AC’97 Modem Controller Buffer Descriptor List Base Address** **MC00, MC10**

Default: 0000_0000h Attribute: Read-write.

| Bits | Description |
|---|---|
| 31:3 | **BDLBA: buffer descriptor list base address bits[31:3].** |
| 2:0 | Reserved. |

### AC'97 Modem Controller Current Index Value — MC04, MC14

Default: 00h Attribute: Read only.

| Bits | Description |
|---|---|
| 7:5 | Reserved. |
| 4:0 | **CIV: current index value.** These bits provides the buffer descriptor within the list of 32 descriptors that is currently being processed. |

### AC'97 Modem Controller Last Valid Index — MC05, MC15

Default: 00h Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:5 | Reserved. |
| 4:0 | **LVI: last valid index.** These bits provide the last valid descriptor in the list. |

### AC'97 Modem Controller Status — MC06, MC16

Some of the bits in this register may be enabled by MC0B and MC1B to generate interrupts.

Default: 0001h Attribute: See below.

| Bits | Description |
|---|---|
| 15:5 | Reserved. |
| 4 | **FIFOERR: FIFO error.** Read; set by hardware; write 1 to clear. 1=A FIFO under-run or over-run has occurred as follows:<br>• MC06[FIFOERR] indicates a FIFO over-run. Incoming data was lost.<br>• MC16[FIFOERR] indicates a FIFO under-run. A sample was repeated because the next valid sample was not provided by the host in time for transmission over the AC97 link. |
| 3 | **BCIS: buffer completion interrupt status.** Read; set by hardware; write 1 to clear. 1=The last sample of a buffer has been processed and the Interrupt on Completion (IOC) bit in the command byte of the buffer descriptor was set. |
| 2 | **LVBCI: last valid buffer completion interrupt.** Read; set by hardware; write 1 to clear. 1=The last valid buffer has been processed. |
| 1 | **CELV: current equals last valid.** Read only. 1=The Current Index Value (MCx4[CIV]) is equal to the value in the Last Valid Index register (MCx5[LVI]) and the buffer pointed to by the CIV has been processed. |
| 0 | **BMCH: bus master controller halted.** Read only. 1=The bus master controller is halted. This may result from clearing the run/pause bit (MCxB[RUNBM]); in this case the IC may wait for the current transaction to complete before this bit goes High. This bit may also go High when the controller has processed the last valid buffer; in this case the IC will set MCx6[CELV] and halt. 0=The bus master controller resumes operation; this occurs when both the run/pause bit is set and the MCx6[CELV] is clear. |

**AC'97 Modem Controller Position in Current Buffer** **MC08, MC18**

Default: 0000h Attribute: Read only

| Bits | Description |
|---|---|
| 15:0 | **PICB: position in current buffer.** This field provides the number of samples left to be processed in the current buffer. |

**AC'97 Modem Controller Prefetched Index Value** **MC0A, MC1A**

Default: 00h Attribute: Read only

| Bits | Description |
|---|---|
| 7:5 | Reserved. |
| 4:0 | **PIV: prefetched index value.** This field provides the current buffer descriptor in the list that has been prefetched. |

**AC'97 Modem Controller Control Register** **MC0B, MC1B**

Default: 00h Attribute: Read-write.

| Bits | Description |
|---|---|
| 7:5 | Reserved. |
| 4 | **IOCEN: interrupt on completion enable.** 1=Enable interrupt when corresponding bit in MCx6[BCIS] is set. |
| 3 | **FEIEN: FIFO error interrupt enable.** 1=Enable interrupt when corresponding bit in MCx6[FIFOERR] is set. |
| 2 | **LVBIEN: last valid buffer interrupt enable.** 1=Enable interrupt when corresponding bit in MCx6[LVBCI] is set. |
| 1 | **REGRST: register reset.** Read-write; cleared by hardware. 1=Contents of all registers of the bus master engine including the FIFOs are reset, except the interrupt enable bits (bits[4, 3, and 2] of this register). It is required that RUNBM (bit[0] of this register) be cleared and MCx6[BMCH] be asserted before this bit may be set. Setting it when either RUNBM is asserted or when MCx6[BMCH] is deasserted results in undefined behavior. 0=Not in reset condition. |
| 0 | **RUNBM: run/pause bus master.** 1=Enable bus master operation. 0=Disable bus master. If this bit is cleared during bus master activity, then all state information is retained. Bus master operation may be stopped and then resumed. |

### AC'97 Modem Controller Global Control — MC3C

AC2C and MC3C provide two access addresses to the same set of registers. See AC2C for the definition.

### AC'97 Modem Controller Global Status — MC40

AC30 and MC40 provide two access addresses to the same set of registers. See AC30 for the definition.

### AC'97 Modem Controller CODEC Access Semaphore — MC44

AC34 and MC44 provide two access addresses to the same set of registers. See AC34 for the definition.

### AC'97 Modem GPIO Status — MC48

Default: 00h Attribute: Read only.

| Bits | Description |
|---|---|
| 15:0 | **GPIO.** This register is updated automatically with each valid slot 12 input to reflect or mirror the current state of the modem codec GPIO pins. |

# 6 Electrical Data

## 6.1 Absolute Ratings

The IC is not designed to operate beyond the parameters shown in the following table.

***Note:*** *The absolute ratings in the following table and associated conditions must be adhered to in order to avoid damage to the IC and motherboard. Systems using the IC must be designed to ensure that the power supply and system logic board do not violate these parameters. VIOLATION OF THE ABSOLUTE RATINGS WILL VOID THE PRODUCT WARRANTY.*

| Parameter | Minimum | Maximum | Comments |
|---|---|---|---|
| VDD3, VDD_AUX3, VDD_RTC, VDD_USB | –0.5 V | 3.6 V | |
| VDD_CORE, VDD_AUX2 | –0.5 V | 2.75 V | |
| VDD_REF | –0.5 V | 5.25 V | |
| $V_{PIN}$ PCI, LPC, SM, AC97 | –0.5 V | Smaller of 4.0 V or VDD3 + 0.5V | Host or Secondary PCI Interfaces, LPC Interface, System Management pins, and AC97 Interface |
| $V_{PIN}$ CPU | –0.5 V | | Processor Interface |
| $V_{PIN}$ IDE | –0.5 V | | |
| $V_{PIN}$ USB | –0.5 V | | |
| $T_{CASE}$ (Under Bias) | –65 C | 85 C | |
| $T_{STORAGE}$ | –65 C | 150 C | |
| ***Note:*** *This table contains preliminary information, which is subject to change.* | | | |

# 6.2 Operating Ranges

The IC is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in the following table.

| Parameter | Minimum | Typical | Maximum |
|---|---|---|---|
| VDD3, VDD_AUX3, VDD_RTC, VDD_USB | 3.135 V | 3.3 V | 3.465 V |
| VDD_CORE, VDD_AUX2 | 2.375 V | 2.5 V | 2.625 V |
| VDD_REF | 4.75 V | 5.0 V | 5.25 V |
| $T_{CASE}$ | 0 C | | 70 C |

***Note:*** *This table contains preliminary information, which is subject to change.*

# 6.3 DC Characteristics

DC characteristics for the host and secondary PCI interfaces are available in the PCI specification. DC characteristics for the processor interface, LPC interface, and system management pins match those of the PCI interfaces. DC characteristics for the EIDE interface are available in the ATA specification. DC characteristics for the USB interface are available from the USB specification. DC characteristics for the AC97 interface are available from the AC97 specification.

# 6.4 Power Dissipation

The following table provides current consumption of the IC while it is operational.

| Supply | Static | Dynamic |
|---|---:|---:|
| VDD_CORE | 47 mA | 350 mA |
| VDD3 | 160 mA | 200 mA |
| VDD_AUX3 | 16 mA | 16 mA |
| VDD_AUX2 | 400 uA | 2 mA |
| VDD_RTC | 8 uA | 8 uA |
| VDD_USB | 17 mA | 30 mA |
| VDD_REF | 200 uA | 500 uA |

***Note:*** *This table contains preliminary information, which is subject to change.*

# 6.5 Switching Characteristics

Switching characteristics for the host and secondary PCI interfaces are available in the PCI specification. Switching characteristics for the processor interface, LPC interface, and system management pins match those of the PCI interfaces. Switching characteristics for the EIDE interface are available in the ATA specification. Switching characteristics for the USB interface are available from the USB specification. Switching characteristics for the AC97 interface are available from the AC97 specification.

# 7 Pin Designations

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | A20M# | PICD1# | INTR | PICD0# | AGP STOP# | DDATA_S15 | DDATA_S1 | DDATA_S13 | DDATA_S3 | DDATA_S10 | DDATA_S5 | DDATA_S8 | DDATA_S7 | DDATA_P0 | DDATA_P14 | DDATA_P2 | DDATA_P11 | DDATA_P4 | DDATA_P9 | DDATA_P7 | STRAP L22 | GPIO17 | STRAP H3 | SUS PEND# | VSS | A |
| B | SPARE_17 | PRDY | VSS | CPU STOP# | STP CLK# | VSS | GPIO28 | DDATA_S14 | VSS | DDATA_S12 | DDATA_S4 | VSS | DDATA_S6 | DDRQP | VSS | DDATA_P1 | DDATA_P12 | VSS | DDATA_P10 | DDATA_P6 | VSS | SPARE_18 | NC32 | VSS | STRAP L23 | PNP IRQ2 | B |
| C | SPARE_15 | VSS | FERR# | GPIO8 | INIT# | IGNNE# | PCI STOP# | DDATA_S0 | DCS1S# | DDATA_S2 | DDATA_S11 | DRDYS | DDATA_S9 | DDATA_P15 | DCS1P# | DDATA_P13 | DDATA_P3 | DRDYP | DDATA_P5 | DDATA_P8 | TEST# | STRAP L24 | VDD_REF | THERM# | VSS | PNP IRQ0 | C |
| D | STRAP L8 | NC20 | NC24 | VSS | SMI# | VDD3 | GPIO27 | DRSTP# | VDD3 | DADDR_S0 | IRQ15 | VDD3 | DIOWS# | DDRQS | VDD3 | DADDR_P0 | IRQ14 | VDD3 | DIOWP# | SPARE_9 | VDD3 | STRAP L25 | VDD3 | INT IRQ8# | PNPIRQ1 | OSC | D |
| E | STRAP L0 | VSS | NC31 | NC30 | STRAP H0 | PICCLK | NMI | DRSTS# | DCS3S# | DADDR_S2 | DADDR_S1 | DDACKS# | DIORS# | DCS3P# | DADDR_P2 | DADDR_P1 | DDACKP# | DIORP# | SPARE_7 | SPARE_8 | SQ WAVE | SPARE_6 | GPIO26 | FAN RPM | FAN CON0 | KA20G | E |
| F | STRAP L17 | STRAP L1 | STRAP L9 | VSS | NC27 | VSS | VSS | VDD_CORE | VDD_CORE | VDD_CORE | | | | | | | VDD_CORE | VDD_CORE | VDD_CORE | VSS | VSS | LFRAME# | VDD3 | FAN CON1 | VSS | LAD0 | F |
| G | STRAP L16 | VSS | STRAP L12 | STRAP L4 | NC21 | VSS | | | | | | | | | | | | | | | VSS | SPKR | CACHE_ZZ | LDRQ0# | KBRC# | SERIRQ | G |
| H | STRAP L11 | STRAP L2 | STRAP L10 | VSS | STRAP L13 | VDD_CORE | | | | | | | | | | | | | | | VDD_CORE | GPIO16 | IRQ6 | IRQ1 | SPARE_5 | LAD2 | H |
| J | STRAP L3 | VSS | STRAP L14 | STRAP L6 | STRAP L5 | VDD_CORE | | | | | | | | | | | | | | | VDD_CORE | IRQ12 | VDD3 | LDRQ1# | VSS | USBCLK | J |
| K | NC18 | STRAP L18 | STRAP L19 | VSS | STRAP L15 | VDD_CORE | | | | | | | | | | | | | | | VDD_CORE | CPU SLEEP# | USB OC1# | USB OC0# | GPIO31 | VSS_USB | K |
| L | NC19 | VSS | NC22 | NC23 | STRAP L7 | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | LAD3 | USBN0 | USBP0 | USBN1 | USBP1 | L |
| M | NC2 | NC11 | NC3 | STRAP L21 | VSS | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | LAD1 | VDD3 | USBN3 | VSS | USBN2 | M |
| N | NC10 | VSS | NC15 | NC7 | NC6 | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | VDD_USB | RTCX_IN | RTCX_OUT | USBP3 | USBP2 | N |
| P | NC1 | NC17 | NC16 | VSS | NC14 | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | SM BUSD | VDD_AUX3 | SPARE_2 | VDD_RTC | INTRUDER# | P |
| R | NC9 | VSS | NC13 | NC5 | NC4 | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | SMB ALERT# | VDD3 | VDD_AUX2 | VSS | ACAV | R |
| T | STRAP L20 | NC8 | NC0 | VSS | NC12 | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | STRAP H2 | RESET# | SM BUSC | SLP BTN# | C32KHZ | T |
| U | NC28 | WSC# | A_AD0 | A_AD16 | A_AD17 | VDD_CORE | | | | | | | | | | | | | | | VDD_CORE | PWR ON# | PWROK | PWR BTN# | RI# | SPARE_4 | U |
| V | SPARE_14 | VSS | A_IDSELB | VDD3 | A_AD18 | VDD_CORE | | | | | | | | | | | | | | | VDD_CORE | RPWR ON | VDD3 | PME# | VSS | SPARE_0 | V |
| W | A_AD1 | A_AD2 | A_AD4 | A_IDSELA | A_AD20 | VDD_CORE | | | | | | | | | | | | | | | VDD_CORE | PCLK66 | LID | CPU RST# | DC STOP# | BAT LOW# | W |
| Y | A_AD3 | A_AD5 | A_AD6 | A_AD19 | A_AD21 | VSS | | | | | | | | | | | | | | | VSS | ACSYNC | STRAP H1 | SPARE_1 | ACSDI1 | GPIO14 | Y |
| AA | A_AD7 | VSS | A_AD23 | VDD3 | A_AD24 | VSS | VSS | VDD_CORE | VDD_CORE | VDD_CORE | | | | | | | VDD_CORE | VDD_CORE | VDD_CORE | VSS | VSS | REQ6# | VDD3 | NC26 | VSS | EXT SMI# | AA |
| AB | A_CBE_L0 | A_AD8 | A_M66EN | A_CBE_L3 | A_AD25 | A_GNT# | A_AD28 | A_AD30 | GPIO30 | GPIO29 | CBE_L1 | AD13 | AD12 | AD9 | AD2 | AD0 | CBE_L0 | AD3 | AD8 | PREQ# | AD10 | GNT6# | GPIO5 | ACSDO | SPARE_3 | ACSDI0 | AB |
| AC | A_AD9 | A_AD11 | A_AD10 | VDD3 | A_AD26 | VDD3 | A_AD29 | A_AD31 | VDD3 | AD15 | AD14 | VDD3 | AD19 | AD21 | VDD3 | AD6 | AD5 | VDD3 | AD7 | PGNT# | VDD3 | SPARE_16 | VDD3 | NC25 | ACCLK | ACRST# | AC |
| AD | A_AD12 | VSS | A_AD22 | A_PAR | A_STOP# | A_AD27 | A_FRAME# | A_ISA REQ# | PAR | PERR# | IRDY# | AD11 | AD17 | AD24 | AD4 | AD27 | AD30 | AD1 | PIRQC# | GNT1# | REQ5# | SPARE_10 | GNT5# | STOP# | VSS | PCLK | AD |
| AE | A_AD13 | A_AD14 | VSS | A_SERR# | A_DEVSEL# | VSS | A_CBE_L2 | SPARE_11 | VSS | DEVSEL# | FRAME# | VSS | AD18 | AD23 | VSS | AD25 | AD29 | VSS | PIRQA# | REQ0# | VSS | GNT2# | GNT3# | VSS | PIRQB# | NC29 | AE |
| AF | VSS | A_AD15 | A_CBE_L1 | A_REQ# | A_TRDY# | A_IRDY# | SPARE_13 | SPARE_12 | SERR# | TRDY# | CBE_L2 | AD16 | AD20 | AD22 | CBE_L3 | AD26 | AD28 | AD31 | PIRQD# | GNT0# | REQ1# | REQ2# | REQ3# | GNT4# | REQ4# | VSS | AF |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |

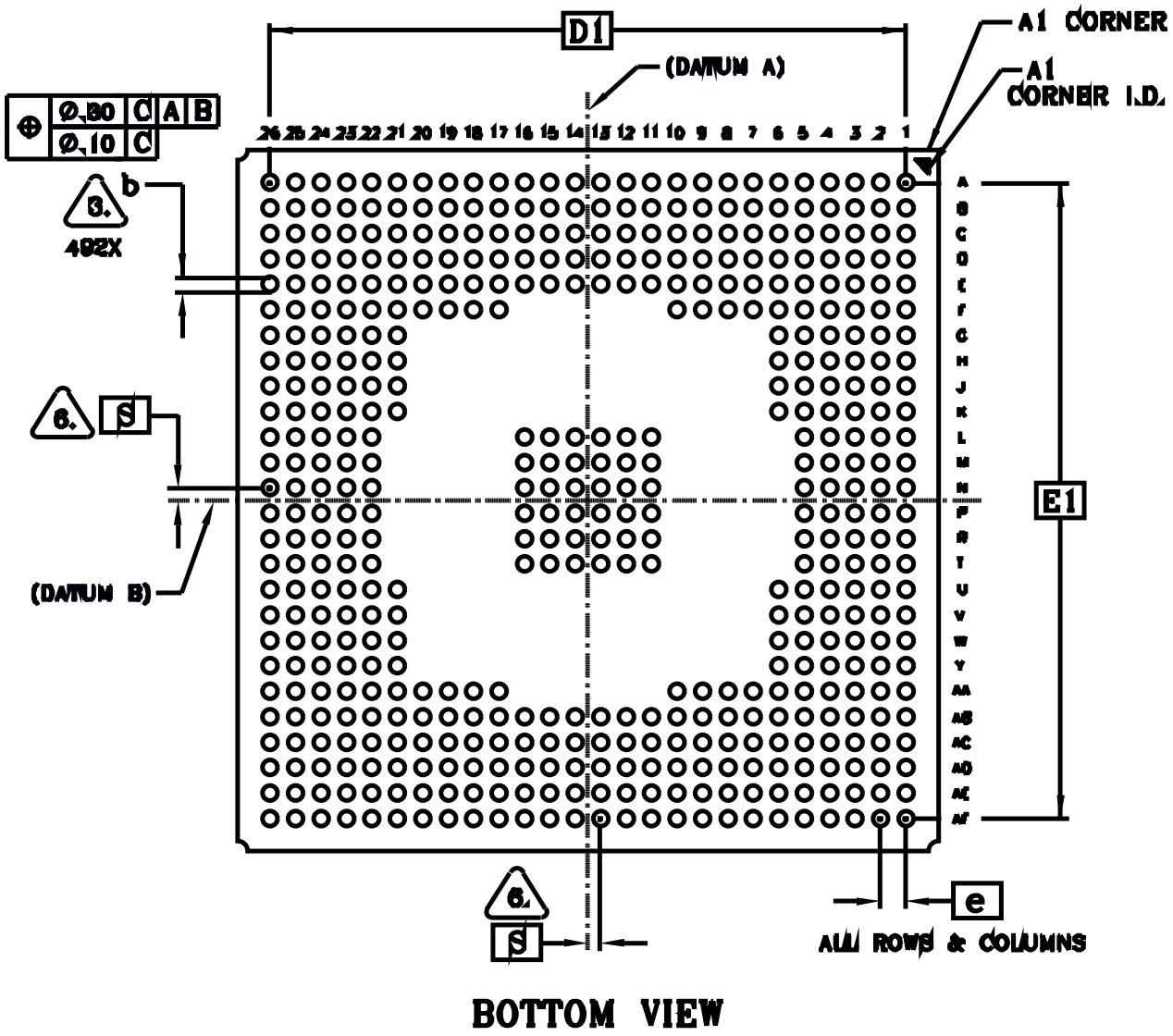
Top side view.

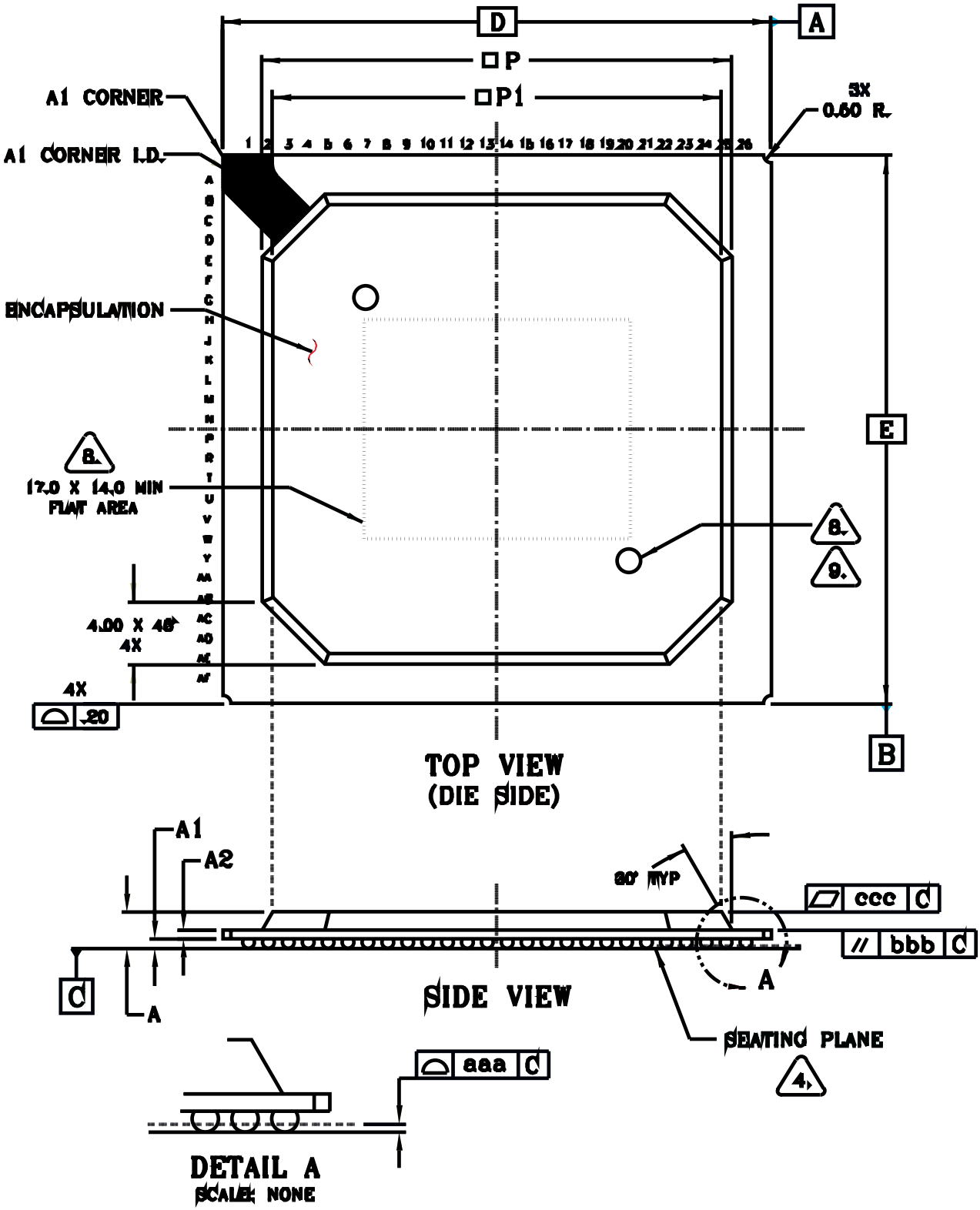
Alphabetical listing of signals and corresponding BGA designators.

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|---|---|---|---|
| A_AD0 | U3 | ACRST# | AC26 | DADDR_S1 | E11 | EXTSMI# | AA26 | NC7 | N4 |
| A_AD1 | W1 | ACSDI0 | AB26 | DADDR_S2 | E10 | FANCON0 | E25 | NC8 | T2 |
| A_AD2 | W2 | ACSDI1 | Y25 | DCS1P# | C15 | FANCON1 | F24 | NC9 | R1 |
| A_AD3 | Y1 | ACSDO | AB24 | DCS1S# | C9 | FANRPM | E24 | NC10 | N1 |
| A_AD4 | W3 | ACSYNC | Y22 | DCS3P# | E14 | FERR# | C3 | NC11 | M2 |
| A_AD5 | Y2 | AD0 | AB16 | DCS3S# | E9 | FRAME# | AE11 | NC12 | T5 |
| A_AD6 | Y3 | AD1 | AD18 | DCSTOP# | W25 | GNT0# | AF20 | NC13 | R3 |
| A_AD7 | AA1 | AD2 | AB15 | DDACKP# | E17 | GNT1# | AD20 | NC14 | P5 |
| A_AD8 | AB2 | AD3 | AB18 | DDACKS# | E12 | GNT2# | AE22 | NC15 | N3 |
| A_AD9 | AC1 | AD4 | AD15 | DDATA_P0 | A15 | GNT3# | AE23 | NC16 | P3 |
| A_AD10 | AC3 | AD5 | AC17 | DDATA_P1 | B16 | GNT4# | AF24 | NC17 | P2 |
| A_AD11 | AC2 | AD6 | AC16 | DDATA_P2 | A17 | GNT5# | AD23 | NC18 | K1 |
| A_AD12 | AD1 | AD7 | AC19 | DDATA_P3 | C17 | GNT6# | AB22 | NC19 | L1 |
| A_AD13 | AE1 | AD8 | AB19 | DDATA_P4 | A19 | GPIO5 | AB23 | NC20 | D2 |
| A_AD14 | AE2 | AD9 | AB14 | DDATA_P5 | C19 | GPIO8 | C4 | NC21 | G5 |
| A_AD15 | AF2 | AD10 | AB21 | DDATA_P6 | B20 | GPIO14 | Y26 | NC22 | L3 |
| A_AD16 | U4 | AD11 | AD12 | DDATA_P7 | A21 | GPIO16 | H22 | NC23 | L4 |
| A_AD17 | U5 | AD12 | AB13 | DDATA_P8 | C20 | GPIO17 | A23 | NC24 | D3 |
| A_AD18 | V5 | AD13 | AB12 | DDATA_P9 | A20 | GPIO26 | E23 | NC25 | AC24 |
| A_AD19 | Y4 | AD14 | AC11 | DDATA_P10 | B19 | GPIO27 | D7 | NC26 | AA24 |
| A_AD20 | W5 | AD15 | AC10 | DDATA_P11 | A18 | GPIO28 | B7 | NC27 | F5 |
| A_AD21 | Y5 | AD16 | AF12 | DDATA_P12 | B17 | GPIO29 | AB10 | NC28 | U1 |
| A_AD22 | AD3 | AD17 | AD13 | DDATA_P13 | C16 | GPIO30 | AB9 | NC29 | AE26 |
| A_AD23 | AA3 | AD18 | AE13 | DDATA_P14 | A16 | GPIO31 | K25 | NC30 | E4 |
| A_AD24 | AA5 | AD19 | AC13 | DDATA_P15 | C14 | IGNNE# | C6 | NC31 | E3 |
| A_AD25 | AB5 | AD20 | AF13 | DDATA_S0 | C8 | INIT# | C5 | NC32 | B23 |
| A_AD26 | AC5 | AD21 | AC14 | DDATA_S1 | A8 | INTIRQ8# | D24 | NMI | E7 |
| A_AD27 | AD6 | AD22 | AF14 | DDATA_S2 | C10 | INTR | A4 | OSC | D26 |
| A_AD28 | AB7 | AD23 | AE14 | DDATA_S3 | A10 | INTRUDER# | P26 | PAR | AD9 |
| A_AD29 | AC7 | AD24 | AD14 | DDATA_S4 | B11 | IRDY# | AD11 | PCISTOP# | C7 |
| A_AD30 | AB8 | AD25 | AE16 | DDATA_S5 | A12 | IRQ1 | H24 | PCLK | AD26 |
| A_AD31 | AC8 | AD26 | AF16 | DDATA_S6 | B13 | IRQ12 | J22 | PCLK66 | W22 |
| A_CBE_L0 | AB1 | AD27 | AD16 | DDATA_S7 | A14 | IRQ14 | D17 | PERR# | AD10 |
| A_CBE_L1 | AF3 | AD28 | AF17 | DDATA_S8 | A13 | IRQ15 | D11 | PGNT# | AC20 |
| A_CBE_L2 | AE7 | AD29 | AE17 | DDATA_S9 | C13 | IRQ6 | H23 | PICCLK | E6 |
| A_CBE_L3 | AB4 | AD30 | AD17 | DDATA_S10 | A11 | KA20G | E26 | PICD0# | A5 |
| A_DEVSEL# | AE5 | AD31 | AF18 | DDATA_S11 | C11 | KBRC# | G25 | PICD1# | A3 |
| A_FRAME# | AD7 | AGPSTOP# | A6 | DDATA_S12 | B10 | LAD0 | F26 | PIRQA# | AE19 |
| A_GNT# | AB6 | BATLOW# | W26 | DDATA_S13 | A9 | LAD1 | M22 | PIRQB# | AE25 |
| A_IDSELA | W4 | C32KHZ | T26 | DDATA_S14 | B8 | LAD2 | H26 | PIRQC# | AD19 |
| A_IDSELB | V3 | CACHE_ZZ | G23 | DDATA_S15 | A7 | LAD3 | L22 | PIRQD# | AF19 |
| A_IRDY# | AF6 | CBE_L0 | AB17 | DDRQP | B14 | LDRQ0# | G24 | PME# | V24 |
| A_ISAREQ# | AD8 | CBE_L1 | AB11 | DDRQS | D14 | LDRQ1# | J24 | PNPIRQ0 | C26 |
| A_M66EN | AB3 | CBE_L2 | AF11 | DEVSEL# | AE10 | LFRAME# | F22 | PNPIRQ1 | D25 |
| A_PAR | AD4 | CBE_L3 | AF15 | DIORP# | E18 | LID | W23 | PNPIRQ2 | B26 |
| A_REQ# | AF4 | CPURST# | W24 | DIORS# | E13 | NC0 | T3 | PRDY | B2 |
| A_SERR# | AE4 | CPUSLEEP# | K22 | DIOWP# | D19 | NC1 | P1 | PREQ# | AB20 |
| A_STOP# | AD5 | CPUSTOP# | B4 | DIOWS# | D13 | NC2 | M1 | PWRBTN# | U24 |
| A_TRDY# | AF5 | DADDR_P0 | D16 | DRDYP | C18 | NC3 | M3 | PWROK | U23 |
| A20M# | A2 | DADDR_P1 | E16 | DRDYS | C12 | NC4 | R5 | PWRON# | U22 |
| ACAV | R26 | DADDR_P2 | E15 | DRSTP# | D8 | NC5 | R4 | REQ0# | AE20 |
| ACCLK | AC25 | DADDR_S0 | D10 | DRSTS# | E8 | NC6 | N5 | REQ1# | AF21 |

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|---|---|---|---|
| REQ2# | AF22 | STRAPL12 | G3 | VDD_CORE | K6 | VSS | AF26 | VSS | P15 |
| REQ3# | AF23 | STRAPL13 | H5 | VDD_CORE | U21 | VSS | B12 | VSS | P16 |
| REQ4# | AF25 | STRAPL14 | J3 | VDD_CORE | U6 | VSS | B15 | VSS | P4 |
| REQ5# | AD21 | STRAPL15 | K5 | VDD_CORE | V21 | VSS | B18 | VSS | R11 |
| REQ6# | AA22 | STRAPL16 | G1 | VDD_CORE | V6 | VSS | B21 | VSS | R12 |
| RESET# | T23 | STRAPL17 | F1 | VDD_CORE | W21 | VSS | B24 | VSS | R13 |
| RI# | U25 | STRAPL18 | K2 | VDD_CORE | W6 | VSS | B3 | VSS | R14 |
| RPWRON | V22 | STRAPL19 | K3 | VDD_REF | C23 | VSS | B6 | VSS | R15 |
| RTCX_IN | N23 | STRAPL20 | T1 | VDD_RTC | P25 | VSS | B9 | VSS | R16 |
| RTCX_OUT | N24 | STRAPL21 | M4 | VDD_USB | N22 | VSS | C2 | VSS | R2 |
| SERIRQ | G26 | STRAPL22 | A22 | VDD3 | AA23 | VSS | C25 | VSS | R25 |
| SERR# | AF9 | STRAPL23 | B25 | VDD3 | AA4 | VSS | D4 | VSS | T11 |
| SLPBTN# | T25 | STRAPL24 | C22 | VDD3 | AC12 | VSS | E2 | VSS | T12 |
| SMBALERT# | R22 | STRAPL25 | D22 | VDD3 | AC15 | VSS | F20 | VSS | T13 |
| SMBUSC | T24 | STRAPH0 | E5 | VDD3 | AC18 | VSS | F21 | VSS | T14 |
| SMBUSD | P22 | STRAPH1 | Y23 | VDD3 | AC21 | VSS | F25 | VSS | T15 |
| SMI# | D5 | STRAPH2 | T22 | VDD3 | AC23 | VSS | F4 | VSS | T16 |
| SPARE_0 | V26 | STRAPH3 | A24 | VDD3 | AC4 | VSS | F6 | VSS | T4 |
| SPARE_1 | Y24 | SUSPEND# | A25 | VDD3 | AC6 | VSS | F7 | VSS | V2 |
| SPARE_2 | P24 | TEST# | C21 | VDD3 | AC9 | VSS | G2 | VSS | V25 |
| SPARE_3 | AB25 | THERM# | C24 | VDD3 | D12 | VSS | G21 | VSS | Y21 |
| SPARE_4 | U26 | TRDY# | AF10 | VDD3 | D15 | VSS | G6 | VSS | Y6 |
| SPARE_5 | H25 | USBCLK | J26 | VDD3 | D18 | VSS | H4 | VSS_USB | K26 |
| SPARE_6 | E22 | USBN0 | L23 | VDD3 | D21 | VSS | J2 | WSC# | U2 |
| SPARE_7 | E19 | USBN1 | L25 | VDD3 | D23 | VSS | J25 | | |
| SPARE_8 | E20 | USBN2 | M26 | VDD3 | D6 | VSS | K4 | | |
| SPARE_9 | D20 | USBN3 | M24 | VDD3 | D9 | VSS | L11 | | |
| SPARE_10 | AD22 | USBOC0# | K24 | VDD3 | F23 | VSS | L12 | | |
| SPARE_11 | AE8 | USBOC1# | K23 | VDD3 | J23 | VSS | L13 | | |
| SPARE_12 | AF8 | USBP0 | L24 | VDD3 | M23 | VSS | L14 | | |
| SPARE_13 | AF7 | USBP1 | L26 | VDD3 | R23 | VSS | L15 | | |
| SPARE_14 | V1 | USBP2 | N26 | VDD3 | V23 | VSS | L16 | | |
| SPARE_15 | C1 | USBP3 | N25 | VDD3 | V4 | VSS | L2 | | |
| SPARE_16 | AC22 | VDD_AUX2 | R24 | VSS | A1 | VSS | M11 | | |
| SPARE_17 | B1 | VDD_AUX3 | P23 | VSS | A26 | VSS | M12 | | |
| SPARE_18 | B22 | VDD_CORE | AA10 | VSS | AA2 | VSS | M13 | | |
| SPKR | G22 | VDD_CORE | AA17 | VSS | AA20 | VSS | M14 | | |
| SQWAVE | E21 | VDD_CORE | AA18 | VSS | AA21 | VSS | M15 | | |
| STOP# | AD24 | VDD_CORE | AA19 | VSS | AA25 | VSS | M16 | | |
| STPCLK# | B5 | VDD_CORE | AA8 | VSS | AA6 | VSS | M25 | | |
| STRAPL0 | E1 | VDD_CORE | AA9 | VSS | AA7 | VSS | M5 | | |
| STRAPL1 | F2 | VDD_CORE | F10 | VSS | AD2 | VSS | N11 | | |
| STRAPL2 | H2 | VDD_CORE | F17 | VSS | AD25 | VSS | N12 | | |
| STRAPL3 | J1 | VDD_CORE | F18 | VSS | AE12 | VSS | N13 | | |
| STRAPL4 | G4 | VDD_CORE | F19 | VSS | AE15 | VSS | N14 | | |
| STRAPL5 | J5 | VDD_CORE | F8 | VSS | AE18 | VSS | N15 | | |
| STRAPL6 | J4 | VDD_CORE | F9 | VSS | AE21 | VSS | N16 | | |
| STRAPL7 | L5 | VDD_CORE | H21 | VSS | AE24 | VSS | N2 | | |
| STRAPL8 | D1 | VDD_CORE | H6 | VSS | AE3 | VSS | P11 | | |
| STRAPL9 | F3 | VDD_CORE | J21 | VSS | AE6 | VSS | P12 | | |
| STRAPL10 | H3 | VDD_CORE | J6 | VSS | AE9 | VSS | P13 | | |
| STRAPL11 | H1 | VDD_CORE | K21 | VSS | AF1 | VSS | P14 | | |

# 8 Package Specification




D
A
P
P1
A1 CORNER
A1 CORNER I.D.
3X
0.60 R.
ENCAPSULATION
E
8.
17.0 X 14.0 MIN
FLAT AREA
8.
9.
4.00 X 45°
4X
4X
.20
B
TOP VIEW
(DIE SIDE)
A1
A2
30° TYP
ccc C
// bbb C
C
A
SIDE VIEW
SEATING PLANE
4.
aaa C
DETAIL A
SCALE: NONE

| Symbol | Description |
|---|---|
| 1 | Dimensions and tolerances conform to ASME Y14.5M–1994. |
| 2 | All dimensions are in millimeters. |
| 3 | Dimension ‘b’ is measured at the maximum solder ball diameter on a plane parallel to Datum C. |
| 4 | Datum C and the seating plane are defined by the spherical crowns of the solder balls. |
| 5 | The number of peripheral rows and columns. |
| 6 | ‘S’ is measured with respect to Datums A and B, and defines the position of the solder balls nearest the package centerlines. |
| 7 | Conforms to JEP-95, MO-151, Issue 9, Variation Bal-2. |
| 8 | The minimum flat area top side of the package is used for marking and pickup. The flatness specification applied to this area. Any ejector marks must be outside of this area. |
| 9 | Optional features. |

| Symbol | Minimum | Nominal | Maximum | Description |
|---|---|---|---|---|
| A | 2.20 | 2.33 | 2.46 | Overall thickness |
| A1 | 0.50 | 0.60 | 0.70 | Ball height |
| A2 | 0.51 | 0.56 | 0.61 | Body thickness |
| D | | 35.00 BSC. | | Body size |
| D1 | | 31.75 BSC. | | Ball footprint |
| E | | 35.00 BSC. | | Body size |
| E1 | | 31.75 BSC. | | Ball footprint |
| M | | 26 x 26 | | Ball matrix size |
| N | | 492 | | Total ball count |
| MR | | 5 | | Number of rows 5 |
| b | 0.60 | 0.75 | 0.90 | Ball diameter |
| e | | 1.27 BSC. | | Ball pitch |
| P | 29.9 | 30.0 | 30.1 | Encapsulation area |
| P1 | | 28.0 Minimum | | Flat encapsulation area |
| S | | 0.635 BSC. | | Solder ball placement |

| Symbol | Tolerance | Description |
|---|---|---|
| aaa | 0.15 | Coplanarity |
| bbb | 0.15 | Parallelism |
| ccc | 0.15 | Flatness |

# 9 Test

The IC includes five NAND trees for continuity testing. It is also possible to place all the IO pins into the high-impedance state. These modes are entered by asserting the following pins:

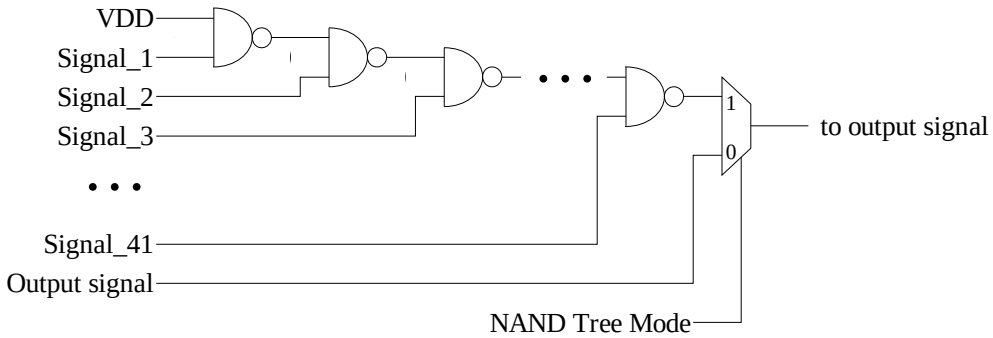
| Mode | Equation to enable mode |
|---|---|
| High Impedance | `~TEST# & PWROK & ~PREQ# & ~SERR#` |
| NAND Tree | `~TEST# & PWROK & ~PREQ# &  SERR#` |

## 9.1 High Impedance Mode

When in high impedance mode, all the signals on the IC are placed into the high impedance state.

## 9.2 NAND Tree Mode

There are six NAND trees in the IC. The following diagram shows how these are connected.




The following tables provide the signal order and output signal for each NAND tree.

Nand tree 1: output signal is DADDR_P0.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | WSC# | 11 | A_AD17 | 21 | A_AD9 | 31 | A_AD22 | 41 | A_DEVSEL# |
| 2 | SPARE_14 | 12 | A_AD4 | 22 | A_AD11 | 32 | A_AD15 | 42 | A_TRDY# |
| 3 | A_AD0 | 13 | A_CBE_L0 | 23 | A_M66EN | 33 | A_AD25 | 43 | A_AD27 |
| 4 | A_AD16 | 14 | A_AD6 | 24 | A_AD21 | 34 | A_GNT# | 44 | A_AD28 |
| 5 | A_AD1 | 15 | A_IDSELA | 25 | A_AD12 | 35 | A_CBE_L1 | 45 | A_IRDY# |
| 6 | A_AD3 | 16 | A_AD8 | 26 | A_AD13 | 36 | A_PAR | 46 | A_AD29 |
| 7 | A_AD2 | 17 | A_AD23 | 27 | A_AD24 | 37 | A_AD26 | 47 | A_FRAME# |
| 8 | A_IDSELB | 18 | A_AD20 | 28 | A_CBE_L3 | 38 | A_SERR# | 48 | A_AD30 |
| 9 | A_AD7 | 19 | A_AD18 | 29 | A_AD10 | 39 | A_REQ# | 49 | A_CBE_L2 |
| 10 | A_AD5 | 20 | A_AD19 | 30 | A_AD14 | 40 | A_STOP# | 50 | SPARE_13 |

Nand tree 2: output signal is DADDR_P2.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GPIO30 | 11 | DEVSEL# | 21 | AD19 | 31 | AD26 | 41 | AD31 |
| 2 | A_AD31 | 12 | TRDY# | 22 | AD17 | 32 | AD25 | 42 | PIRQD# |
| 3 | ISAREQ# | 13 | AD14 | 23 | AD18 | 33 | AD27 | 43 | AD1 |
| 4 | SPARE_11 | 14 | IRDY# | 24 | AD20 | 34 | AD6 | 44 | GNT0# |
| 5 | SPARE_12 | 15 | AD13 | 25 | AD22 | 35 | AD2 | 45 | PIRQA# |
| 6 | PAR | 16 | FRAME# | 26 | AD21 | 36 | AD9 | 46 | PIRQC# |
| 7 | GPIO29 | 17 | CBE_L2 | 27 | AD24 | 37 | AD28 | 47 | REQ1# |
| 8 | AD15 | 18 | AD12 | 28 | AD23 | 38 | AD29 | 48 | AD0 |
| 9 | PERR# | 19 | AD11 | 29 | CBE_L3 | 39 | AD30 | 49 | REQ0# |
| 10 | CBE_L1 | 20 | AD16 | 30 | AD4 | 40 | AD5 | | |

Nand tree 3: output signal is DCS1P#.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | AD3 | 11 | GNT3# | 21 | STOP# | 31 | CACHE_ZZ | 41 | GPIO26 |
| 2 | AD7 | 12 | SPARE_10 | 22 | NC25 | 32 | FANCON1 | 42 | CPUSLEEP# |
| 3 | REQ2# | 13 | AD10 | 23 | GPIO5 | 33 | LAD3 | 43 | LFRAME# |
| 4 | GNT1# | 14 | GNT4# | 24 | ACSYNC | 34 | FANCON0 | 44 | INTIRQ8# |
| 5 | AD8 | 15 | SPARE_16 | 25 | ACSDO | 35 | GPIO16 | 45 | PNPIRQ2 |
| 6 | PGNT# | 16 | GNT5# | 26 | ACCLK | 36 | OSC | 46 | SPARE_6 |
| 7 | REQ3# | 17 | REQ4# | 27 | STRAPH1 | 37 | SPKR | 47 | THERM# |
| 8 | GNT2# | 18 | PIRQB# | 28 | STRAPH2 | 38 | FANRPM | 48 | STRAPL23 |
| 9 | CBE_L0 | 19 | GNT6# | 29 | NC26 | 39 | PNPIRQ1 | 49 | SQWAVE |
| 10 | REQ5# | 20 | REQ6# | 30 | KA20G | 40 | PNPIRQ0 | 50 | STRAPL25 |

Nand tree 4: output signal is DCS3P#.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | USBP3 | 11 | ACRST# | 21 | SMBALERT# | 31 | SMBUSD | 41 | LAD2 |
| 2 | USBN3 | 12 | RPWRON | 22 | DCSTOP# | 32 | SPARE_4 | 42 | SPARE_5 |
| 3 | USBP2 | 13 | LID | 23 | GPIO14 | 33 | C32KHZ | 43 | SERIRQ |
| 4 | USBN2 | 14 | SPARE_1 | 24 | PWRBTN# | 34 | ACAV | 44 | LAD1 |
| 5 | USBP1 | 15 | ACSDI0 | 25 | BATLOW# | 35 | SPARE_2 | 45 | IRQ1 |
| 6 | USBN1 | 16 | CPURST# | 26 | RESET# | 36 | GPIO31 | 46 | KBRC# |
| 7 | USBP0 | 17 | PWRON# | 27 | SMBUSC | 37 | USBOC0# | 47 | IRQ12 |
| 8 | USBN0 | 18 | ACSDI1 | 28 | RI# | 38 | USBCLK | 48 | LAD0 |
| 9 | INTRUDER# | 19 | EXTSMI# | 29 | SPARE_0 | 39 | USBOC1# | 49 | LDRQ0# |
| 10 | SPARE_3 | 20 | PME# | 30 | SLPBTN# | 40 | LDRQ1# | 50 | IRQ6 |

Nand tree 5: output signal is DADDR_S1.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | SUSPEND# | 11 | DDACKP# | 21 | DDATA_P9 | 31 | DDRQS |
| 2 | SPARE_8 | 12 | DIORP# | 22 | DDATA_P3 | 32 | DDATA_P15 |
| 3 | STRAPH3 | 13 | DDATA_P8 | 23 | DDATA_P4 | 33 | DDRQP |
| 4 | NC32 | 14 | STRAPL22 | 24 | DDATA_P12 | 34 | DDATA_S7 |
| 5 | STRAPL24 | 15 | DDATA_P5 | 25 | DDATA_P13 | 35 | DDATA_S8 |
| 6 | SPARE_9 | 16 | DDATA_P6 | 26 | DDATA_P11 | 36 | DIOWS# |
| 7 | SPARE_7 | 17 | DDATA_P7 | 27 | DDATA_P1 | 37 | DDATA_S9 |
| 8 | GPIO17 | 18 | DRDYP | 28 | DDATA_P2 | 38 | DDATA_S6 |
| 9 | SPARE_18 | 19 | IRQ14 | 29 | DDATA_P14 | 39 | DDATA_S5 |
| 10 | DIOWP# | 20 | DDATA_P10 | 30 | DDATA_P0 | 40 | DRDYS |

Nand tree 6: output signal is DADDR_S2.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | DIORS# | 11 | DDACKS# | 21 | DRSTP# | 31 | PICCLK | 41 | NC24 |
| 2 | DDATA_S10 | 12 | DDATA_S1 | 22 | GPIO27 | 32 | SMI# | | |
| 3 | DDATA_S4 | 13 | DCS1S# | 23 | DRSTS# | 33 | CPUSTOP# | | |
| 4 | DDATA_S3 | 14 | DDATA_S14 | 24 | PICD0# | 34 | PICD1# | | |
| 5 | DDATA_S11 | 15 | DDATA_S15 | 25 | IGNNE# | 35 | A20M# | | |
| 6 | IRQ15 | 16 | DDATA_S0 | 26 | STPCLK# | 36 | GPIO8 | | |
| 7 | DDATA_S12 | 17 | GPIO28 | 27 | NMI | 37 | FERR# | | |
| 8 | DDATA_S13 | 18 | DCS3S# | 28 | INTR | 38 | SPARE_17 | | |
| 9 | DDATA_S2 | 19 | AGPSTOP# | 29 | INIT# | 39 | SPARE_15 | | |
| 10 | DADDR_S0 | 20 | PCISTOP# | 30 | PRDY | 40 | STRAPH0 | | |

The following pins are not part of the NAND tree: RTCX_IN, RTCX_OUT, PWROK, PCLK, PCLK66, TEST#, PREQ#, and SERR#.

# 10 Appendixes

## 10.1 Glossary

**FON.** Full on system power state; see Section 4.7.1.5.
**IOAPIC.** IO advanced programmable interrupt controller.
**MOFF.** Mechanical off system power state; see Section 4.7.1.5.
**MP.** Multiprocessor.
**PIC.** Programmable interrupt controller. This is the internal legacy dual-8259-based interrupt controller.
**PIT.** Programmable interval timer. This is the internal legacy 8254 timer.
**POS.** Power on suspend system power state; see Section 4.7.1.5.
**Power button override event.** This event occurs when PWRBTN# or SLPBTN# is held active for at least four seconds. See PM00[PBOR_STS].
**RST_SOFT.** This is an internal reset signal that is applied to the logic, registers, and pins that reside on the VDD_AUX power planes. See Section 4.7.1.5.2.
**SOFF.** Soft off system power state; see Section 4.7.1.5.
**STD.** System suspend to disk system power state; see Section 4.7.1.5.
**STR.** System suspend to RAM system power state; see Section 4.7.1.5.
**USB.** Universal serial bus.

## 10.2 References

*Advanced Configuration and Power Interface Specification Revision 1.0.* By Intel, Microsoft, and Toshiba. Copyright 1996, 1997.
*Low Pin Count (LPC) Interface Specification, revision 1.0.* From Intel Corporation.
*Multiprocessor Specification, Version 1.4, August 1996.* From Intel Corporation.
*OpenHCI for USB.* Release 1.1, dated 14-Sep-99, by Compaq, Microsoft, and National Semiconductor.
*Mobile PC/PCI DMA Arbitration and Protocols.* Revision 2.2, dated 22-Apr-96, by Intel Corporation.
*PCI IDE Controller Specification, revision 1.0.* Dated 4-Mar-94. By the PCI Special Interest Group, PO Box 14070, Portland, OR, 97214, (800) 433-5177.
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*PCI System Architecture, Third Edition.* By Tom Shanley and Don Anderson. Copyright 1995, by MindShare, Inc., ISBN: 0-201-40993-3.
*PCI-to-PCI Bridge Architecture Specification, Revision 1.1.* 18-Dec-98. PCI Special Interest Group, 2575 N.E. Kathryn #17, Hillsboro, Oregon 97124, 1-800-433-5177 (USA). Copyright 1994, 1998.
*Revision 2.1 PCI Specification.* By the PCI Special Interest Group, PO Box 14070, Portland, OR, 97214, (800) 433-5177. Copyright 1992, 1993, and 1995 by the PCI Special Interest Group.
*Serial IRQ Specification Version 1.0.* VESA (Video Electronics Standards Association), 2150 North First Street, Suite 440, San Jose, CA, 95131-2029, Phone: (408) 435-0333.

*System Management Bus Specification Revision 1.0.* Dated 15-Feb-95. Copyright 1996. Written by Benchmarq Microelectronics Inc., Duracell Inc., Energizer Power Systems, Intel Corporation, Linear Technology Corporation, Maxim Integrated Products, Mitsubishi Electric Corporation, National Semiconductor Corporation, Toshiba Battery Co., Varta Batterie AG.
*Universal Serial Bus Specification Revision 1.1*. Dated 23-Sep-98. By Compaq, Intel, Microsoft, NEC.

# 10.3 Conventions

Most values in this document are appended with “b” to indicate a binary value or “h” to indicate a hexadecimal value. Otherwise, the value is presumed to be a decimal value.

In this document, formulae follow Verilog numerical conventions. Here is a summary:

| | |
|---|---|
| y‘hx | ‘h indicates that the number that follows it, x, is in hexadecimal format. If there is a number before the ‘h, y, specifies the number of bits in x. |
| {} | Brackets are used to indicate a group of bits that are concatenated together. |
| \| | Logical OR operator. |
| & | Logical AND operator. |
| ~ | Logical NOT operator. |
| == | Logical “is equal to” operator. |
| != | Logical “is not equal to” operator. |
| * | Multiply. |

The order in which logical operators are applied is: ~ first, & second, and | last.