# HGTG32N60E2

April 1995

# 32A, 600V N-Channel IGBT

## Features

- 32A, 600V
- · Latch Free Operation
- Typical Fall Time 600ns
- · High Input Impedance
- Low Conduction Loss

# Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This device incorporates generation two design techniques which yield improved peak current capability and larger short circuit withstand capability than previous designs.

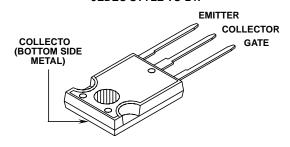
### **PACKAGING AVAILABILITY**

PART NUMBER	PACKAGE	BRAND		
HGTG32N60E2	TO-247	G32N60E2		

NOTE: When ordering, use the entire part number.

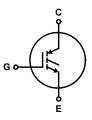
## Package

#### **JEDEC STYLE TO-247**



# Terminal Diagram

#### **N-CHANNEL ENHANCEMENT MODE**



## **Absolute Maximum Ratings** T<sub>C</sub> = +25°C, Unless Otherwise Specified

	HGTG32N60E2	UNITS
Collector-Emitter Voltage	600	V
Collector-Gate Voltage $R_{GE} = 1M\Omega \dots V_{CGR}$	600	V
Collector Current Continuous at T <sub>C</sub> = +25°C	50	Α
at $V_{GE} = 15V$ , at $T_C = +90^{\circ}C$ $I_{C90}$	32	Α
Collector Current Pulsed (Note 1)	200	Α
Gate-Emitter Voltage Continuous	±20	V
Gate-Emitter Voltage Pulsed	±30	V
Switching Safe Operating Area at T <sub>J</sub> = +150°C	200A at 0.8 BV <sub>CES</sub>	-
Power Dissipation Total at $T_C = +25^{\circ}C$	208	W
Power Dissipation Derating T <sub>C</sub> > +25°C	1.67	W/°C
Operating and Storage Junction Temperature Range	-55 to +150	°C
Maximum Lead Temperature for Soldering	260	°C
Short Circuit Withstand Time (Note 2)at V <sub>GE</sub> = 15Vt <sub>SC</sub>	3	μs
at V <sub>GF</sub> = 10V	15	μs

- NOTES:
- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.  $V_{CE(PEAK)} = 360V$ ,  $T_C = +125^{\circ}C$ ,  $R_{GE} = 25\Omega$ .

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4,364,07	3 4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,71	3 4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,16	2 4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,43	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,08	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,02	7						

# Specifications HGTG32N60E2

# **Electrical Specifications** $T_C = +25$ °C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV <sub>CES</sub>	$I_C = 250 \mu A, V_{GE} = 0 V$		600	-	-	V
Collector-Emitter Leakage Voltage	I <sub>CES</sub>	V <sub>CE</sub> = BV <sub>CES</sub>	T <sub>C</sub> = +25°C	-	-	250	μΑ
		V <sub>CE</sub> = 0.8 BV <sub>CES</sub>	$T_C = +125^{\circ}C$	-	-	4.0	mA
Collector-Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	V <sub>GF</sub> = 15V	$T_{C} = +25^{\circ}C$	-	2.4	2.9	V
			$T_C = +125^{\circ}C$	-	2.4	3.0	V
Gate-Emitter Threshold Voltage	V <sub>GE(TH)</sub>	$I_C = 1$ mA, $V_{CE} = V_{GE}$ $T_C = +25$ °C		3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I <sub>GES</sub>	V <sub>GE</sub> = ±20V		-	-	±500	nA
Gate-Emitter Plateau Voltage	V <sub>GEP</sub>	$I_{C} = I_{C90}, V_{CE} = 0.5 \text{ BV}_{CES}$		-	6.5	-	V
On-State Gate Charge	Q <sub>G(ON)</sub>	$I_{C} = I_{C90},$ $V_{CE} = 0.5 \text{ BV}_{CES}$	V <sub>GE</sub> = 15V	-	200	260	nC
			V <sub>GE</sub> = 20V	-	265	345	nC
Current Turn-On Delay Time	t <sub>D(ON)I</sub>	$L = 500\mu H$ , $I_C = I_{C90}$ , $R_G = 25\Omega$ , $V_{GE} = 15V$ , $T_J = +125^{\circ}C$ , $V_{CE} = 0.8 \; BV_{CES}$		-	100	-	ns
Current Rise Time	t <sub>RI</sub>			-	150	-	ns
Current Turn-Off Delay Time	t <sub>D(OFF)I</sub>	1	-	630	820	ns	
Current Fall Time	t <sub>Fl</sub>	1	-	620	800	ns	
Turn-Off Energy (Note 1)	W <sub>OFF</sub>	1	-	3.5	-	mJ	
Thermal Resistance	$R_{ heta JC}$			-	0.5	0.6	°C/W

#### NOTE:

# **Typical Performance Curves**

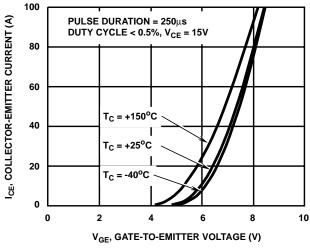


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

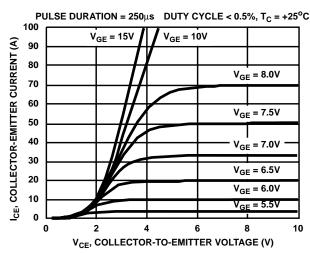


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

Turn-Off Energy Loss (W<sub>OFF</sub>) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I<sub>CE</sub> = 0A) The HGTG32N60E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

#### Typical Performance Curves (Continued) 1.0 50 V<sub>CE</sub> = 240V 0.8 DC COLLECTOR CURRENT 40 FALL TIME (µs) $V_{GE} = 10V$ 0.6 V<sub>CE</sub> = 480V 30 0.4 20 ij. V<sub>GE</sub> = 10V AND 15V 0.2 10 $T_J = +150$ °C, $R_G = 25\Omega$ $L = 50 \mu H$ 0.0 +50 +75 +100 +125 +150 +25 10 100 I<sub>CE</sub>, COLLECTOR-EMITTER CURRENT (A) T<sub>C</sub>, CASE TEMPERATURE (°C) FIGURE 3. MAXIMUM DC COLLECTOR CURRENT vs CASE FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT **TEMPERATURE** 600 10 12000 COLLECTOR-EMITTER VOLTAGE (V) f = 1MHz GATE-EMITTER VOLTAGE (V) V<sub>CC</sub> = BV<sub>CES</sub> V<sub>CC</sub> = BV<sub>CES</sub> 10000 450 GATE-**EMITTER** VOLTAGE 8000 C, CAPACITANCE (pF) $\mathbf{c}_{\text{iss}}$ 6000 300 0.75 BV<sub>CES</sub> 0.75 BV<sub>CES</sub> 0.50 BV<sub>CES</sub> 0.50 BV<sub>CES</sub> 4000 0.25 BV<sub>CES</sub> 0.25 BV<sub>CES</sub> 150 $c_{oss}$ I<sub>G(REF)</sub> = 2.75mA V<sub>GE</sub>, ( 2000 $V_{GE} = 10V$ V<sub>CE</sub>, ( COLLECTOR-EMITTER VOLTAGE 0 0 10 25 I<sub>G(REF)</sub> I<sub>G(REF)</sub> 20 TIME (µs) 80 V<sub>CE</sub>, COLLECTOR-TO-EMITTER VOLTAGE (V) I<sub>G(ACT)</sub> I<sub>G(ACT)</sub> FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CON-STANT GATE CURRENT. (REFER TO APPLICATION **NOTES AN7254 AND AN7260).** 20 6 $T_J = +150$ °C WoFF, TURN-OFF SWITCHING LOSS (mJ) $T_{.1} = +150^{\circ}C$ $R_G = 25\Omega$ 10 5 $L = 50 \mu H$ V<sub>CE(ON)</sub>, SATURATION VOLTAGE (V) $V_{GE} = 10V$ 4 V<sub>CE</sub> = 480V, V<sub>GE</sub> = 10V, 15V 3 1.0 $V_{GE} = 15V$ V<sub>CE</sub> = 240V, V<sub>GE</sub> = 10V, 15V 2 0.1 1 10 100 100 I<sub>CE</sub>, COLLECTOR-EMITTER CURRENT (A) I<sub>CE</sub>, COLLECTOR-EMITTER CURRENT (A) FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-**CURRENT EMITTER CURRENT**

# Typical Performance Curves (Continued)

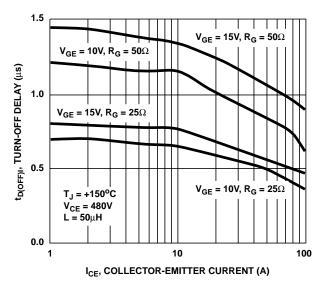
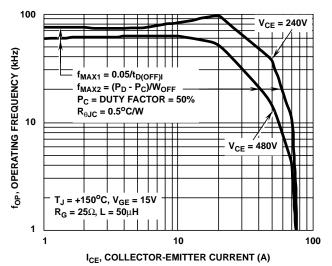


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER
CURRENT



 $P_D$  = ALLOWABLE DISSIPATION  $P_C$  = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

# **Operating Frequency Information**

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current ( $I_{CE}$ ) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows  $f_{MAX1}$  or  $f_{MAX2}$  whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

 $f_{MAX1}$  is defined by  $f_{MAX1}=0.05/t_{D(OFF)I}.\ t_{D(OFF)I}$  deadtime (the denominator) has been arbitrarily held to 10% of the onstate time for a 50% duty factor. Other definitions are possible.  $t_{D(OFF)I}$  is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional

frequency limiting condition for an application other than  $T_{\mathsf{JMAX}}$ .  $t_{\mathsf{D}(\mathsf{OFF})\mathsf{I}}$  is important when controlling output ripple under a lightly loaded condition.

 $f_{MAX2}$  is defined by  $f_{MAX2}$  =  $(P_D$  -  $P_C)/W_{OFF}$ . The allowable dissipation  $(P_D)$  is defined by  $P_D$  =  $(T_{JMAX}$  -  $T_C)/R_{\theta JC}$ . The sum of device switching and conduction losses must not exceed  $P_D$ . A 50% duty factor was used (Figure 10) so that the conduction losses  $(P_C)$  can be approximated by  $P_C$  =  $(V_{CE} \ x \ I_{CE})/2$ .  $W_{OFF}$  is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero  $(I_{CE}$  - 0A).

The switching power loss (Figure 10) is defined as  $f_{MAX1} \times W_{OFF}$ . Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

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