

E-paper Display Interface Timing

Description	For 1.44", 2", 2.7", 3", 4.41", 7.4", 8.1", 10.2" EPD module (EPD+TCon) with Eink FPL
Date	2012/06/27
Doc. No.	4P009-00
Revision	01

	Design Engineering		
	Approval	Check	Design
			



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Date: May 15, 2012

TO: Microtips Technology, LLC (Microtips USA)

In continuing to develop and promote the strategic partnership between Data International Co., Ltd. (DV) and Microtips USA (MTUSA), DV is pleased to announce that we have entered into an agreement with MTUSA to support customers and reps in North America.

MTUSA will offer DV standard, semi-custom, or custom flat display modules with a DV part number which manufactured by DV but support and logistics of the sales will be handled by MTUSA.

DV is confident that this arrangement between two companies will ultimately benefit to the end customer.

Sincerely,

A handwritten signature in black ink, appearing to read 'Debbie Chang'.

Debbie Chang/Sales Manager
Data International Co., Ltd.

Table of Contents

Revision History	6
Glossary of Acronyms	7
1 General Description	8
1.1 Overview.....	8
1.2 Demo kit diagram.....	8
1.3 The hardware of TCon board	9
1.4 How to connect with ZIF Connector.....	11
2 Input Terminal Pin Assignment.....	13
2.1 Input Terminal Pin Assignment	13
2.2 Input Connector Drawing.....	15
3 Interface Timing	16
3.1 Power ON/OFF Sequence	16
3.2 Data Transmission Sequence.....	18
3.3 Parameter settings	19
4 Bitmap Data Format	21
4.1 1.44" (128 x 96) EPD panel	21
4.2 2" (200 x 96) EPD panel.....	22
4.3 2.7" (264 x 176) EPD panel	23
4.4 3" (240 x 320) EPD panel	24
4.5 4.41" (400 x 300) EPD panel.....	25
4.6 7.4" (480 x 800) EPD panel	26
4.7 8.1" (768 x 1024) EPD panel.....	27
4.8 10.2" (1024 x 1280) EPD panel	28
5 Sample code of SPI Interface Timing	30
5.1 Introduction	30
5.2 Driving Flowchart	30
5.3 Sample Code Explanation	30

List of Figures

Figure 1-1	1.44", 2", 2.7" TCon board	9
Figure 1-2	3" TCon board.....	9
Figure 1-3	4.41" TCon board	9
Figure 1-4	7.4" TCon board.....	10
Figure 1-5	8.1" and 10.2" TCon board	10
Figure 1-6	Pull the ZIF Connector.....	11
Figure 1-7	Input FFC cable.....	11
Figure 1-8	Push the ZIF Connector.....	12
Figure 2-1	The different Pin definition.....	14
Figure 2-2	Input Connector Drawing.....	15
Figure 3-1	Power ON/OFF Sequence of 1.44" ~ 2.7"	16
Figure 3-2	Power ON/OFF Sequence of 3" ~ 10.2".....	17
Figure 3-3	Data Transmission Sequence.....	18
Figure 4-1	1.44" (128 x 96) EPD panel	21
Figure 4-2	2" (200 x 96) EPD panel.....	22
Figure 4-3	2.7" (264 x 176) EPD panel	23
Figure 4-4	3" (240 x 320) EPD panel.....	24
Figure 4-5	4.41" (400 x 300) EPD panel.....	25
Figure 4-6	7.4" (480 x 800) EPD panel	26
Figure 4-7	8.1" (768 x 1024) EPD panel.....	27
Figure 4-8	10.2" (1024 x 1280) EPD panel	28
Figure 5-1	Driving Flowchart	30

Revision History

Version	Date	Page (New)	Section	Description
Ver.01	2012/06/27	All	All	Approval specification first Issued.

Glossary of Acronyms

EPD	Electrophoretic Display (e-Paper Display)
EPD Panel	EPD
TCon	Timing Controller
SPI	Serial Peripheral Interface
COG	Chip on Glass

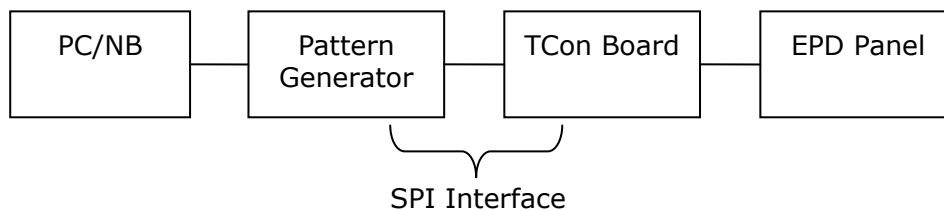
1 General Description

1.1 Overview

This document describes the interface and function of the SPI between TCon board and pattern generator. PDi designs the different TCon boards for each EPD panel ([1.44", 2", 2.7"], 3", 4.41", 7.4", [8.1", 10.2"]), but arranges the same 10 pins of ZIF connector on each TCon board. You will understand how to transmit data and command to TCon board, and find the differences for each size in this document.

1.2 Demo kit diagram

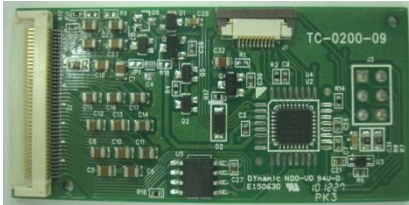
This diagram shows the relative connection between the pattern generator, TCon board and the panel. The SPI here is the communication interface between pattern generator and TCon board. This document will describe the SPI protocol and how to work with it.



1.3 The hardware of TCon board

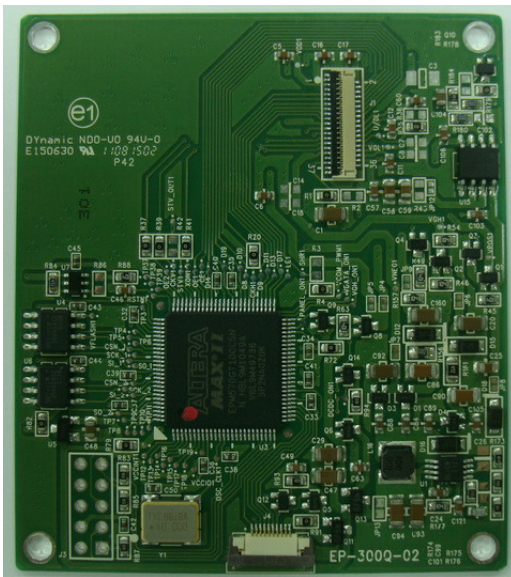
- 1.44", 2", 2.7" TCon board

Figure 1-1 1.44", 2", 2.7" TCon board



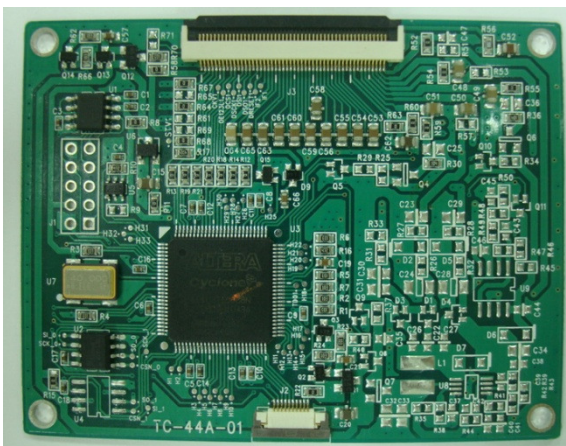
- 3" TCon board

Figure 1-2 3" TCon board



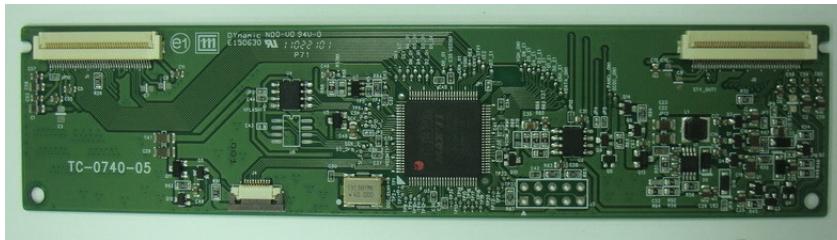
- 4.41" TCon board

Figure 1-3 4.41" TCon board



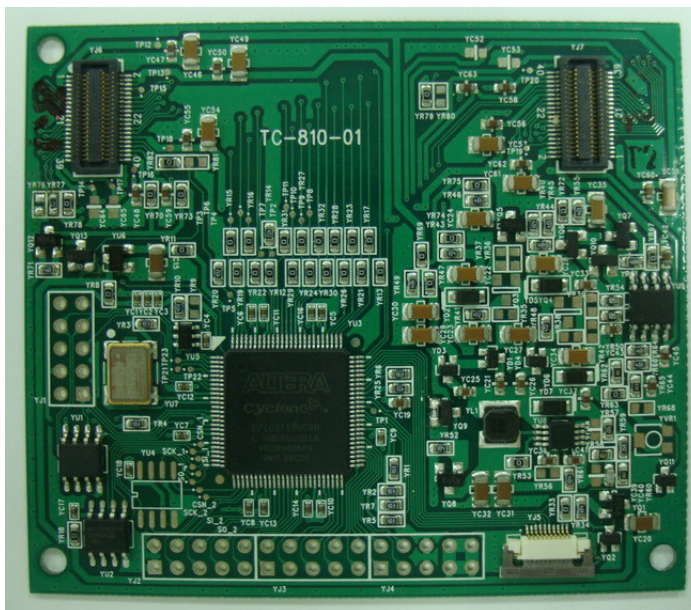
- 7.4" TCon board

Figure 1-4 7.4" TCon board



- 8.1" and 10.2" TCon board

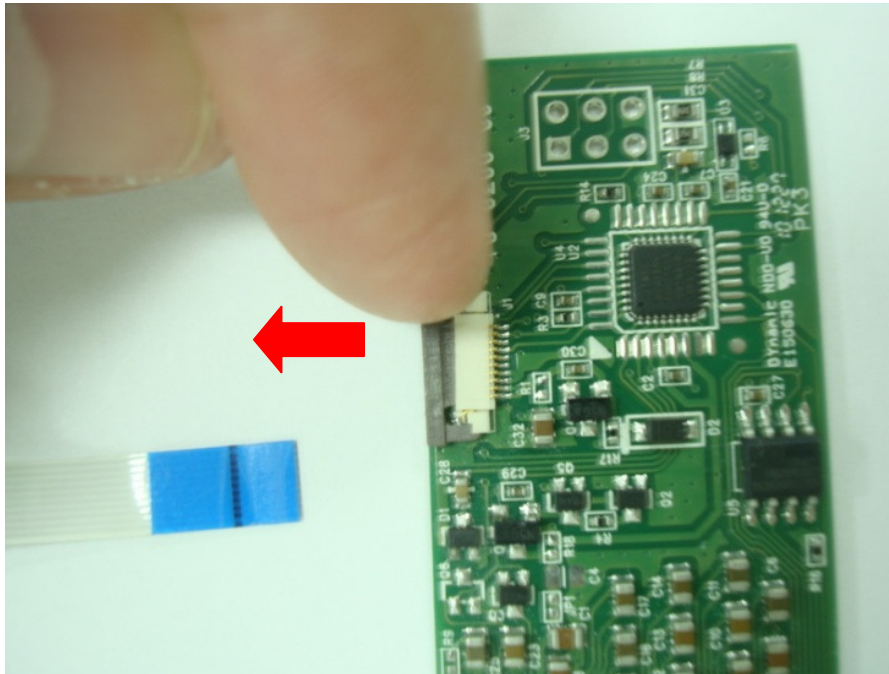
Figure 1-5 8.1" and 10.2" TCon board



1.4 How to connect with ZIF Connector

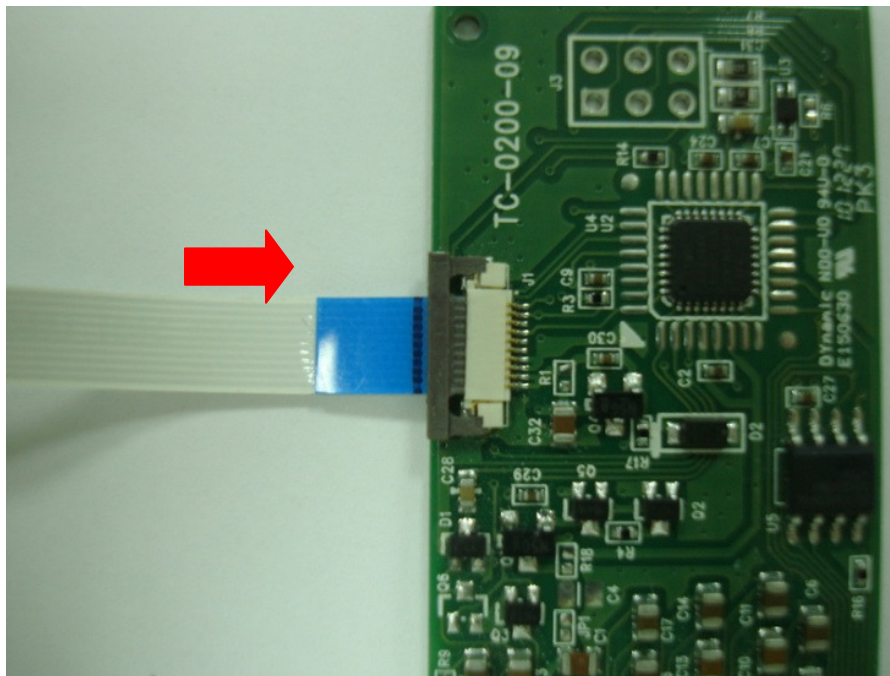
- Pull the ZIF Connector

Figure 1-6 Pull the ZIF Connector



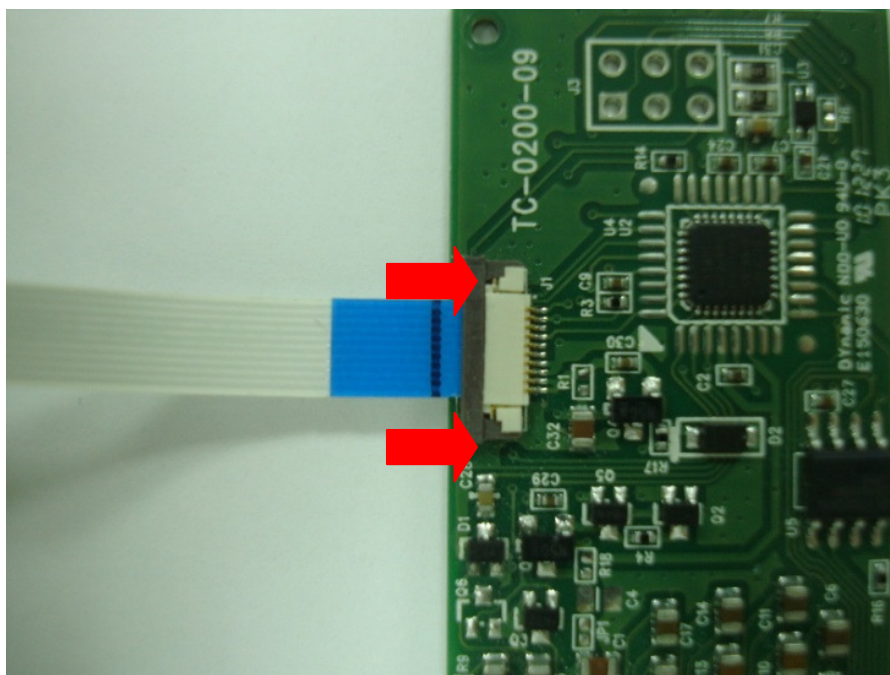
- Input FFC cable to ZIF Connector

Figure 1-7 Input FFC cable



- Push the ZIF Connector

Figure 1-8 Push the ZIF Connector



2 Input Terminal Pin Assignment

2.1 Input Terminal Pin Assignment

Table 2-1 Input Terminal Pin Assignment

No.	Signal	I/O	Connected to	Function
1	BUSY	O	MCU	When BUSY = 1, EPD stays in busy state that EPD ignores any input data from SPI.
2	/RESET	I	MCU	/RESET must be "H" when host MCU uses EPD. Apply to 1.44", 2", 2.7" EPD
	ON			ON must be "H" when host MCU uses EPD. Apply to 3", 4.41", 7.4", 8.1", 10.2" EPD
3	SO	O	MCU	Serial output from EPD to host MCU
4	SI	I	MCU	Serial input from host MCU to EPD
5	SCLK	I	MCU	Clock for SPI
6	/CS	I	MCU	Chip select. Low enable
7	GND	P	Ground	
8	GND	P	Ground	
9	V _{CC}	P	V _{CC}	Power for analog circuit
10	V _{DD}	P	V _{DD}	Power for digital circuit

Note (1): Connector type: ACES 88297 10 pins pitch 0.5mm

Note (2): I: Input

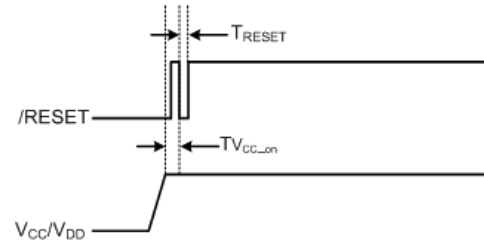
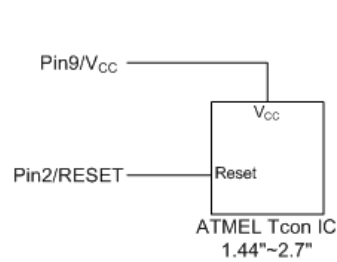
O: Output

P: Power

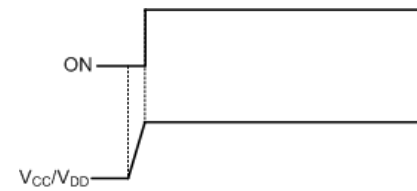
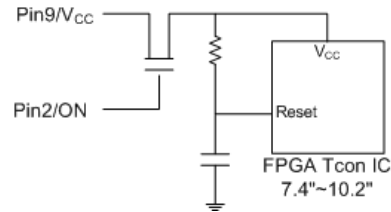
Note (3):

Figure 2-1 The different Pin definition**1.44" ~ 2.7"**

- Pin1/BUSY
- Pin2/RESET
- Pin3/SO
- Pin4/SI
- Pin5/SCLK
- Pin6/CS
- Pin7/GND
- Pin8/GND
- Pin9/VCC
- Pin10/VDD

**3" ~ 10.2"**

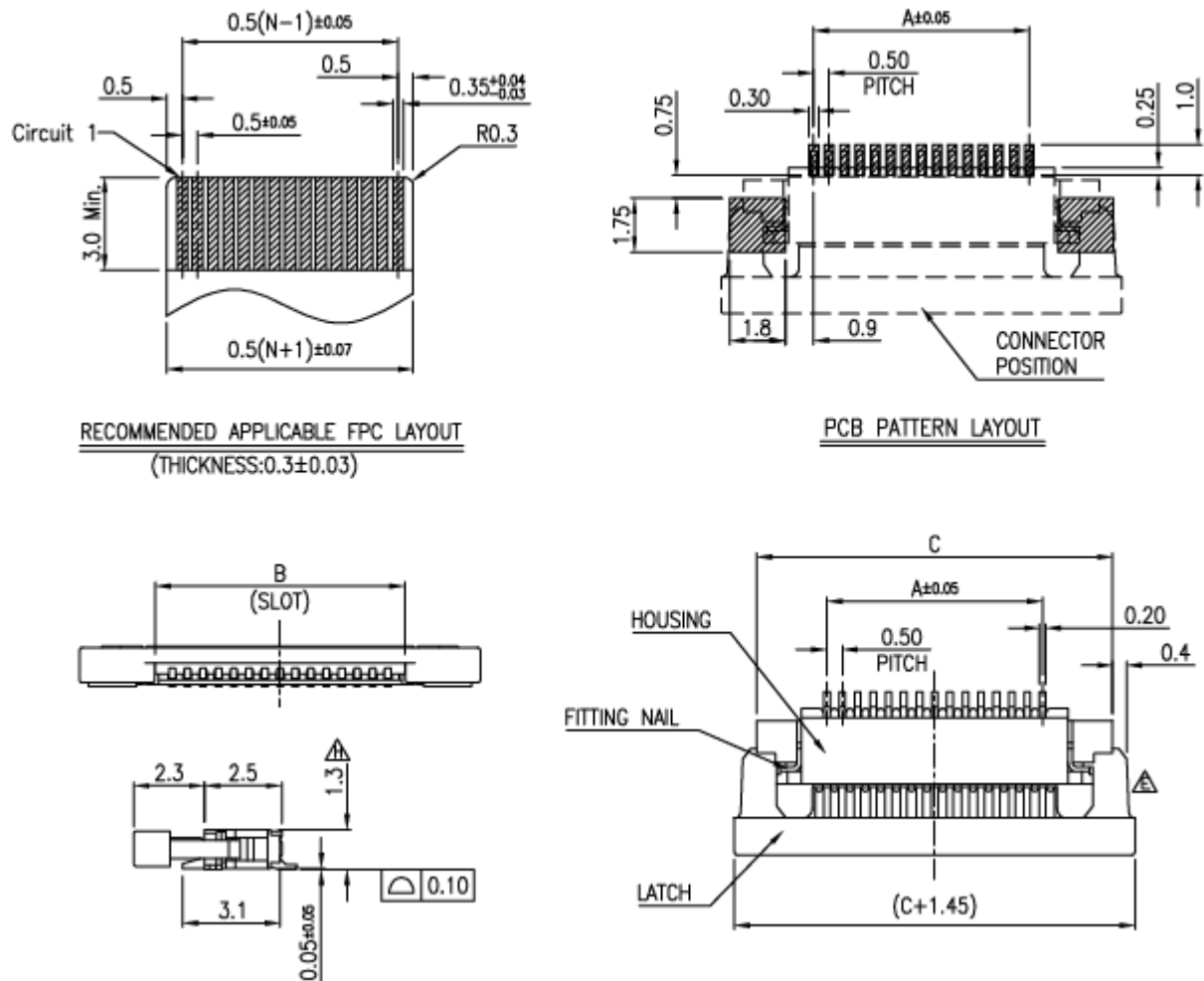
- Pin1/BUSY
- Pin2/ON
- Pin3/SO
- Pin4/SI
- Pin5/SCLK
- Pin6/CS
- Pin7/GND
- Pin8/GND
- Pin9/VCC
- Pin10/VDD



2.2 Input Connector Drawing

1.44", 2", 2.7", 3", 4.41", 7.4", 8.1", 10.2" TCon board support the same 10 pins SPI connector.

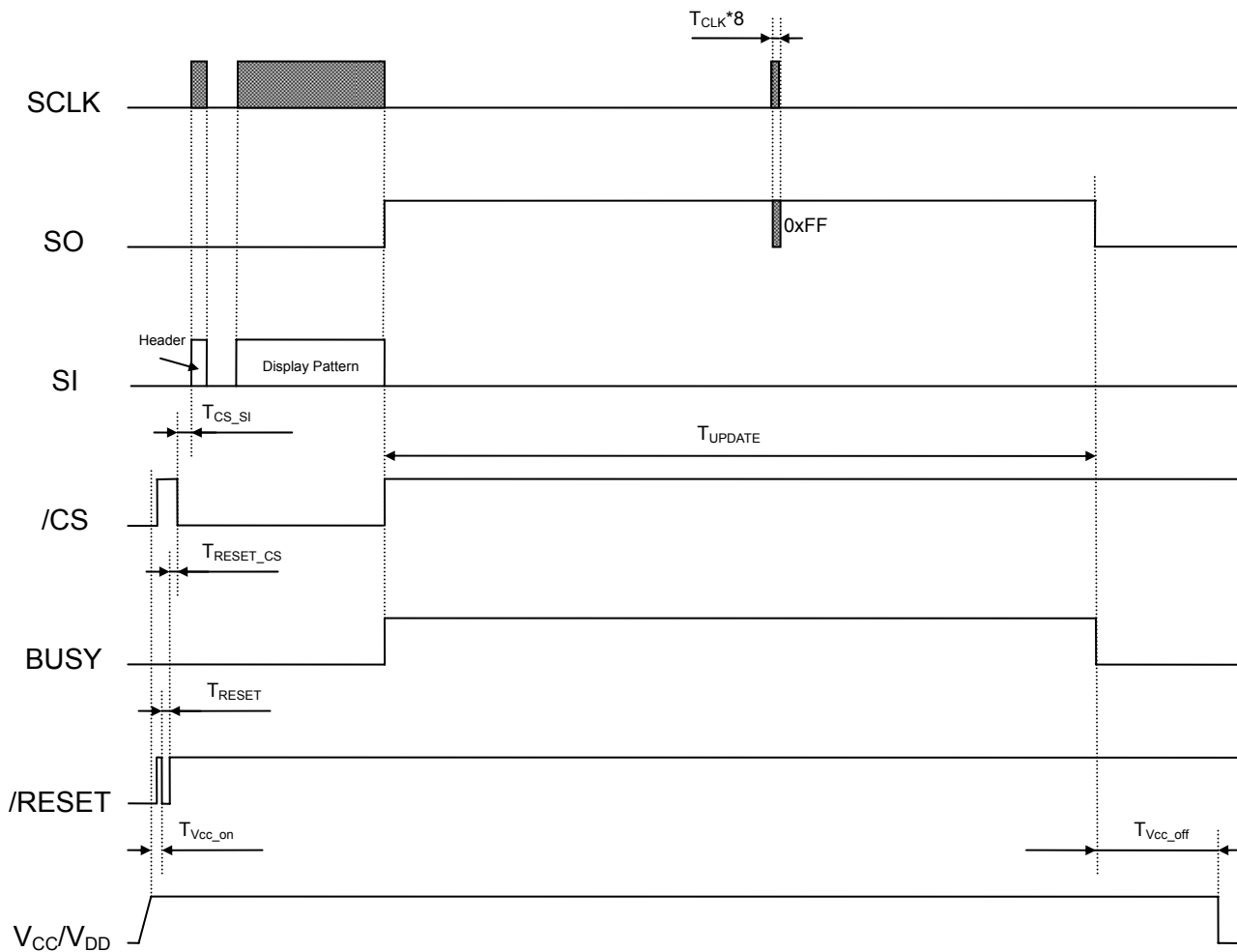
Figure 2-2 Input Connector Drawing



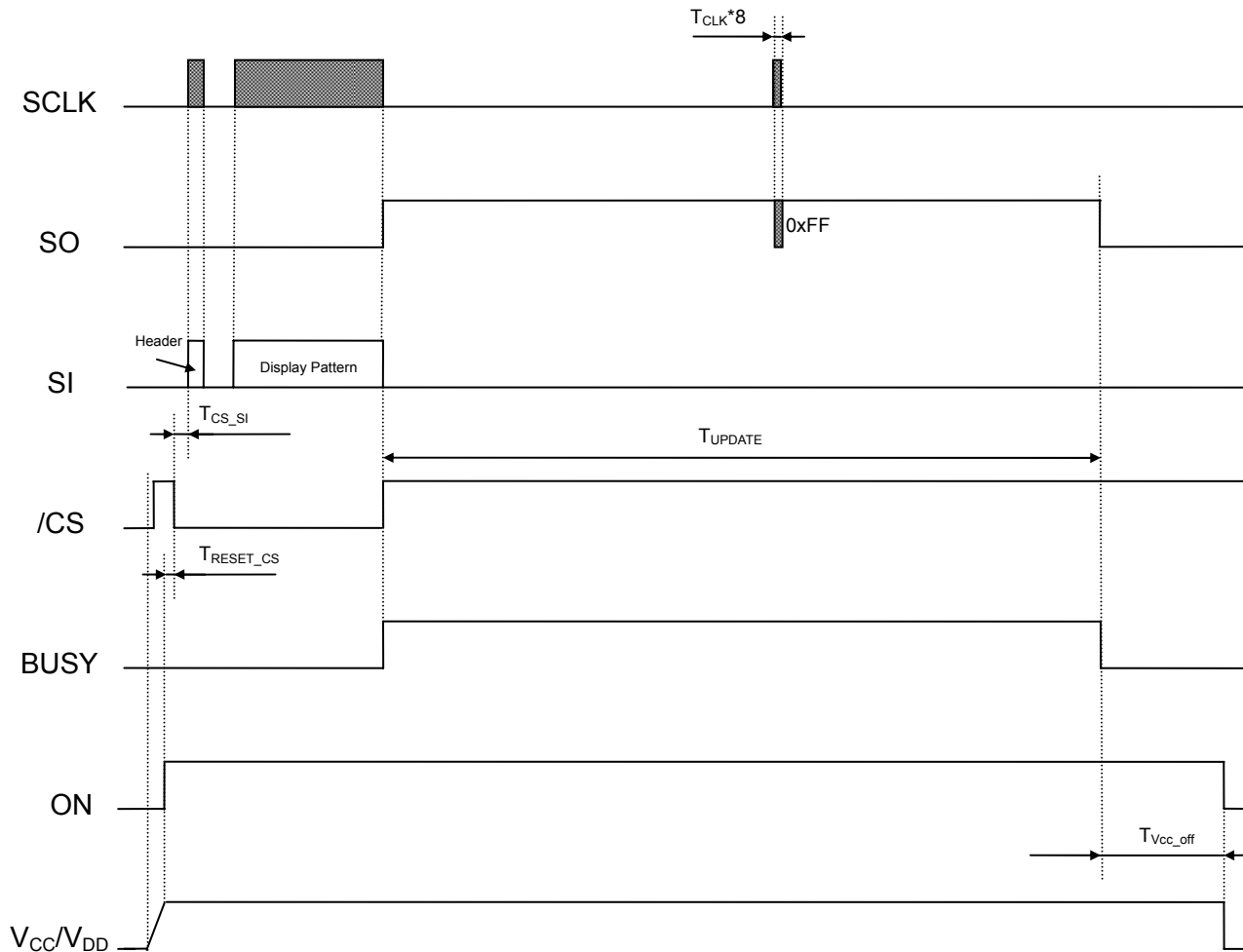
3 Interface Timing

3.1 Power ON/OFF Sequence

Figure 3-1 Power ON/OFF Sequence of 1.44" ~ 2.7"



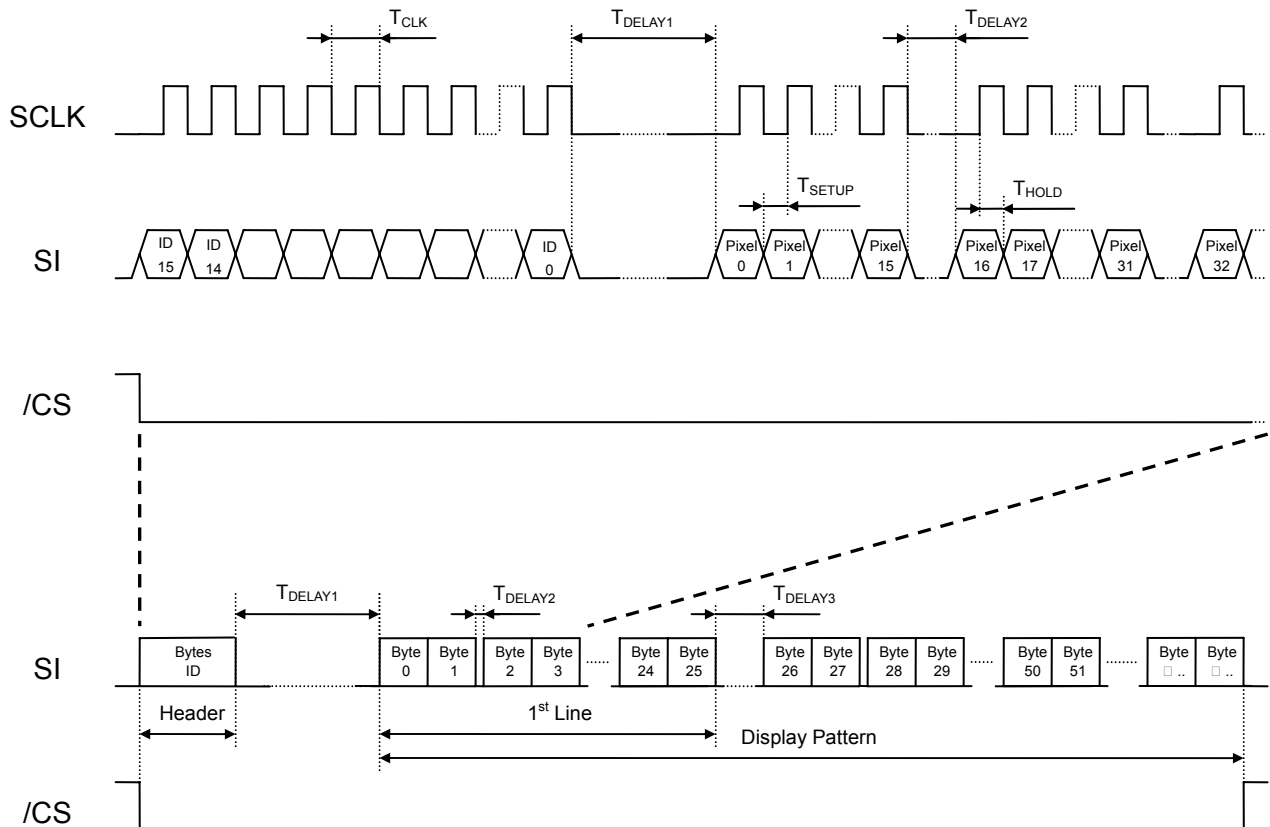
- *1. User can check whether Timing Controller finish update by transmitting eight clocks by SCLK. If Timing Controller finish update, it replies 0x00 by SO. If not finish, Timing Controller replies 0xFF.
- *2. All input signal, SI, SCLK, /CS, and /RESET must be kept to low until Vcc is stable when power on.
- *3. T_{UPDATE} increases as lower environment temperature.

Figure 3-2 Power ON/OFF Sequence of 3" ~ 10.2"

- *1. User can check whether Timing Controller finish update by transmitting eight clocks by SCLK. If Timing Controller finish update, it replies 0x00 by SO. If not finish, Timing Controller replies 0xFF.
- *2. All input signal, SI, SCLK, /CS, and ON must be kept to low until Vcc is stable when power on.
- *3. T_{UPDATE} increases as lower environment temperature.

3.2 Data Transmission Sequence

Figure 3-3 Data Transmission Sequence



- *1. In T_{DELAY1} , T_{DELAY2} , and T_{DELAY3} must set SDA and SCLK at low state.
- *2. T_{DELAY1} : The delay between Header and Display Pattern.
- *3. T_{DELAY2} : The delay between each two bytes happened only in Display Pattern.
- *4. T_{DELAY3} : The delay between each scan line happened only in Display Pattern.
- *5. Bytes ID: Header byte number, please refer below sheet.

Panel Size	ID[15..0]
1.44", 2", 2.7"	0x03A0
3", 4.41", 7.4"	0x04A0
8.1"	0x05A0
10.2"	0x06A0

3.3 Parameter settings

Table 3-1 Parameter settings of 1.44" ~ 2.7"

Item	Symbol	Min.	Typ.	Max.	Unit	Note
V _{CC} /V _{DD} range	V _{CC} /V _{DD}	2.7	3.0	3.3	Volt	
V _{CC} setup time	T _{V_{CC}_on}	10	-	-	ms	
V _{CC} hold time	T _{V_{CC}_off}	1	-	500	ms	
SCLK clock period	T _{CLK}	16	16	-	us	
SI setup time	T _{SETUP}	40	50	60	%	% of T _{CLK}
Delay time 1	T _{DELAY1}	120	-	150	ms	
Delay time 2	T _{DELAY2}	1	1	-	T _{CLK}	
Delay time 3	T _{DELAY3}	1	-	-	ms	
Reset time	T _{RESET}	5	-	-	ms	
Update time	T _{UPDATE}	-	1	5	sec	
Reset CS Time	T _{RESET_CS}	19	-	-	ms	T _{RESET_CS} +T _{CS_SI} must ≥ 20ms.
CS SI time	T _{CS_SI}	1	-	-	ms	

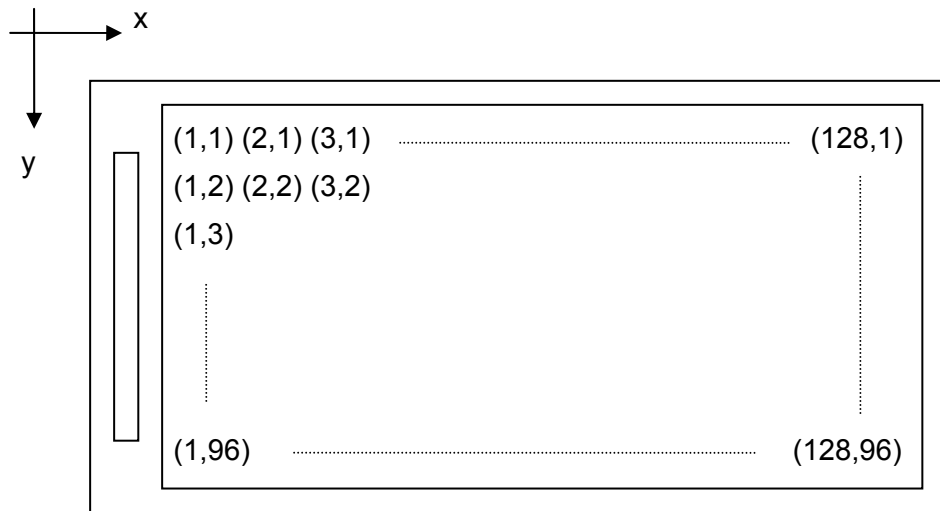
Table 3-2 Parameter settings of 3" ~ 10.2"

Item	Symbol	Panel Size	Min.	Typ.	Max.	Unit	Note
V _{CC} /V _{DD} range	V _{CC} /V _{DD}	All	3.0	3.3	3.6	Volt	
V _{CC} setup time	T _{V_{CC}_on}	All	20	-	-	ms	
V _{CC} hold time	T _{V_{CC}_off}	All	0	-	500	ms	
SCLK clock period	T _{CLK}	3"~8.1"	2	2.5	-	us	
		10.2"	0.1		1,000		
SI setup time	T _{SETUP}	All	40	50	60	%	% of T _{CLK}
SI hold time	T _{HOLD}	All	-	-	-	%	% of T _{CLK}
		10.2"	45	50	60		
Delay time 1	T _{DELAY1}	All	5	-	-	ms	
Delay time 2	T _{DELAY2}	All	0	-	-	T _{CLK}	
Delay time 3	T _{DELAY3}	All	5	-	-	ms	
Update time	T _{UPDATE}	All	-	2.5	5	sec	
Reset CS Time	T _{RESET_CS}	All	19	-	-	ms	T _{RESET_CS} +T _{CS_SI} must ≥ 20ms.
CS SI time	T _{CS_SI}	3", 4.41", 8.1", 10.2"	1	-	-	ms	
		7.4"	60	70	-	ms	

4 Bitmap Data Format

4.1 1.44" (128 x 96) EPD panel

Figure 4-1 1.44" (128 x 96) EPD panel



Gate Line 1: (1,1) → (2,1) → (3,1) → ... → (128,1) →

Gate Line N: (1,N) → (2,N) → (3,N) → ... → (128,N) →

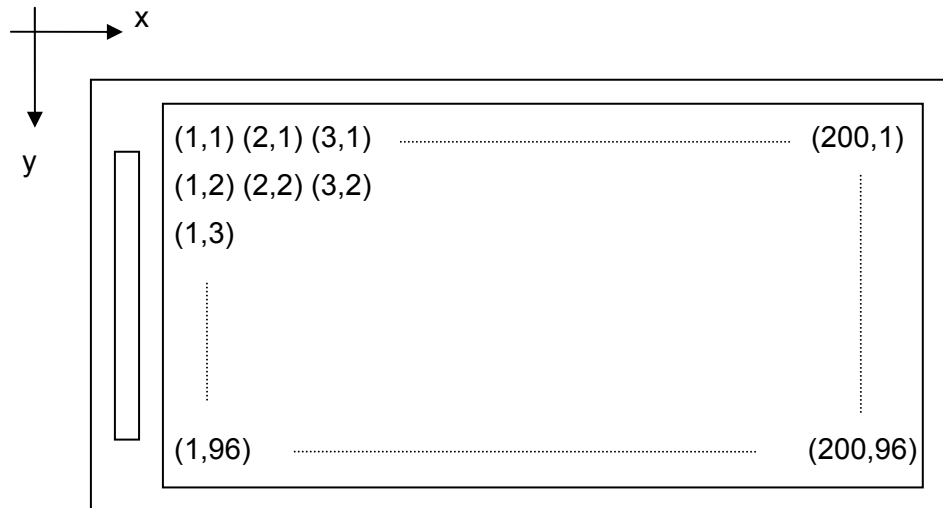
Gate Line 96: (1,96) → (2,96) → (3,96) → ... → (128,96)

* 1 Input sequence: Line 1 → Line 2 → ... → Line 96

* 2 Total data quantity: 128 x 96 = 12,288 bits = 1,536 bytes

4.2 2" (200 x 96) EPD panel

Figure 4-2 2" (200 x 96) EPD panel



Gate Line 1: (1,1) → (2,1) → (3,1) → ... → (200,1) → "00000000" →

Gate Line N: (1,N) → (2,N) → (3,N) → ... → (200,N) → "00000000" →

Gate Line 96: (1,96) → (2,96) → (3,96) → ... → (200,96) → "00000000"

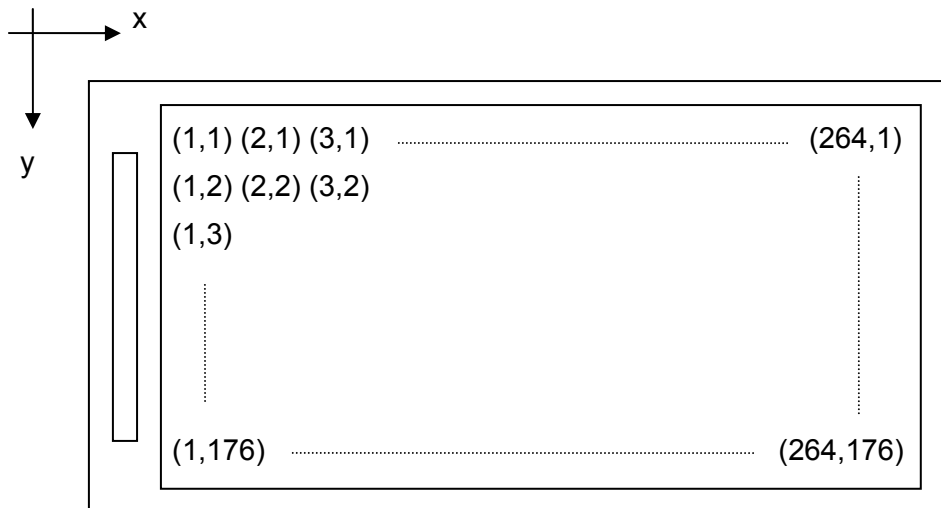
* 1 Must eight "0" after each line.

* 2 Input sequence: Line 1 → Line 2 → ... → Line 96

* 3 Total data quantity: (200+8) x 96 = 19,968 bits = 2,496 bytes

4.3 2.7" (264 x 176) EPD panel

Figure 4-3 2.7" (264 x 176) EPD panel



Gate Line 1: (1,1) → (2,1) → (3,1) → ... → (264,1) → "00000000" →

Gate Line N: (1,N) → (2,N) → (3,N) → ... → (264,N) → "00000000" →

Gate Line 176: (1,176) → (2,176) → (3,176) → ... → (264,176) → "00000000"

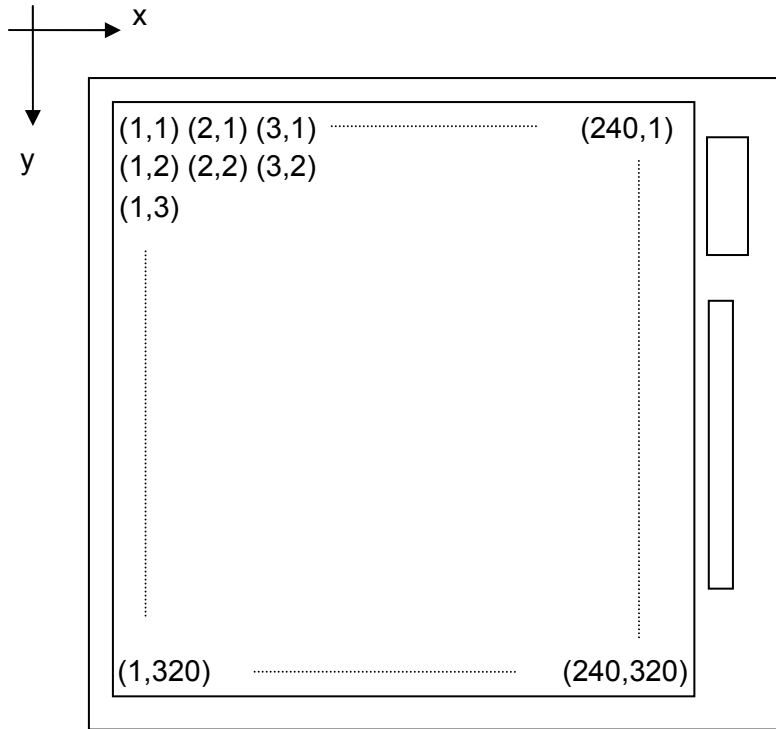
* 1 Must eight "0" after each line.

* 2 Input sequence: Line 1 → Line 2 → ... → Line 176

* 3 Total data quantity: $(264+8) \times 176 = 47,872$ bits = 5,984 bytes

4.4 3" (240 x 320) EPD panel

Figure 4-4 3" (240 x320) EPD panel



Gate Line 1: (1,1) → (2,1) → (3,1) → ... → (240,1) →

Gate Line N: (1,N) → (2,N) → (3,N) → ... → (240,N) →

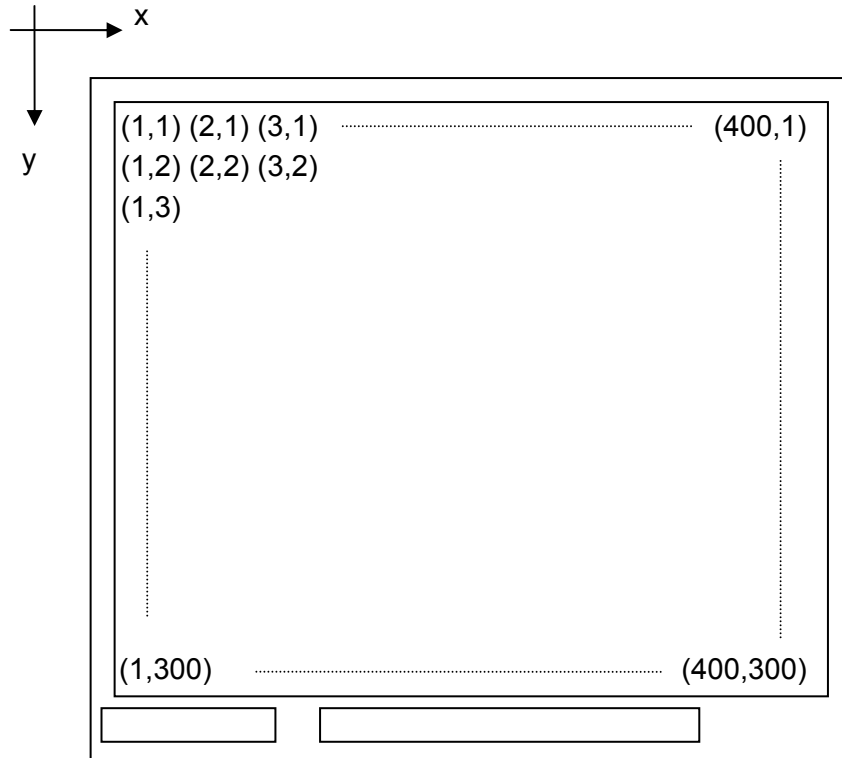
Gate Line 320: (1,320) → (2,320) → (3,320) → ... → (240,320)

* 1 Input sequence: Line 1 → Line 2 → ... → Line 320

* 2 Total data quantity: 240 x 320 = 76,800 bits = 9,600 bytes

4.5 4.41" (400 x 300) EPD panel

Figure 4-5 4.41" (400 x 300) EPD panel



Gate Line 1: (1,1) → (2,1) → (3,1) → ... → (400,1) →

⋮

Gate Line N: (1,N) → (2,N) → (3,N) → ... → (400,N) →

⋮

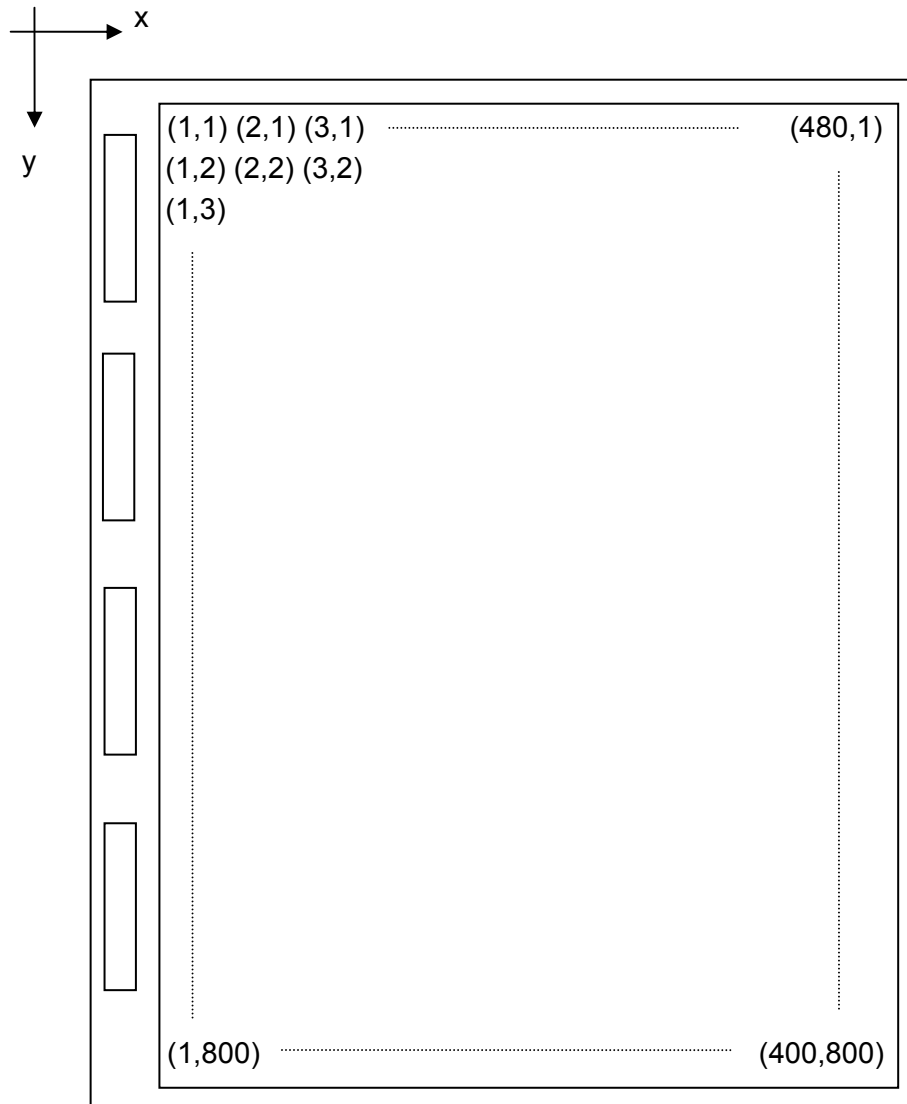
Gate Line 300: (1,300) → (2,300) → (3,300) → ... → (400,300)

* 1 Input sequence: Line 1 → Line 2 → ... → Line 300

* 2 Total data quantity: 400 x 300 = 120,000 bits = 15,000 bytes

4.6 7.4" (480 x 800) EPD panel

Figure 4-6 7.4" (480 x 800) EPD panel



Gate Line 1: (1,1) → (2,1) → (3,1) → ... → (480,1) →

Gate Line N: (1,N) → (2,N) → (3,N) → ... → (480,N) →

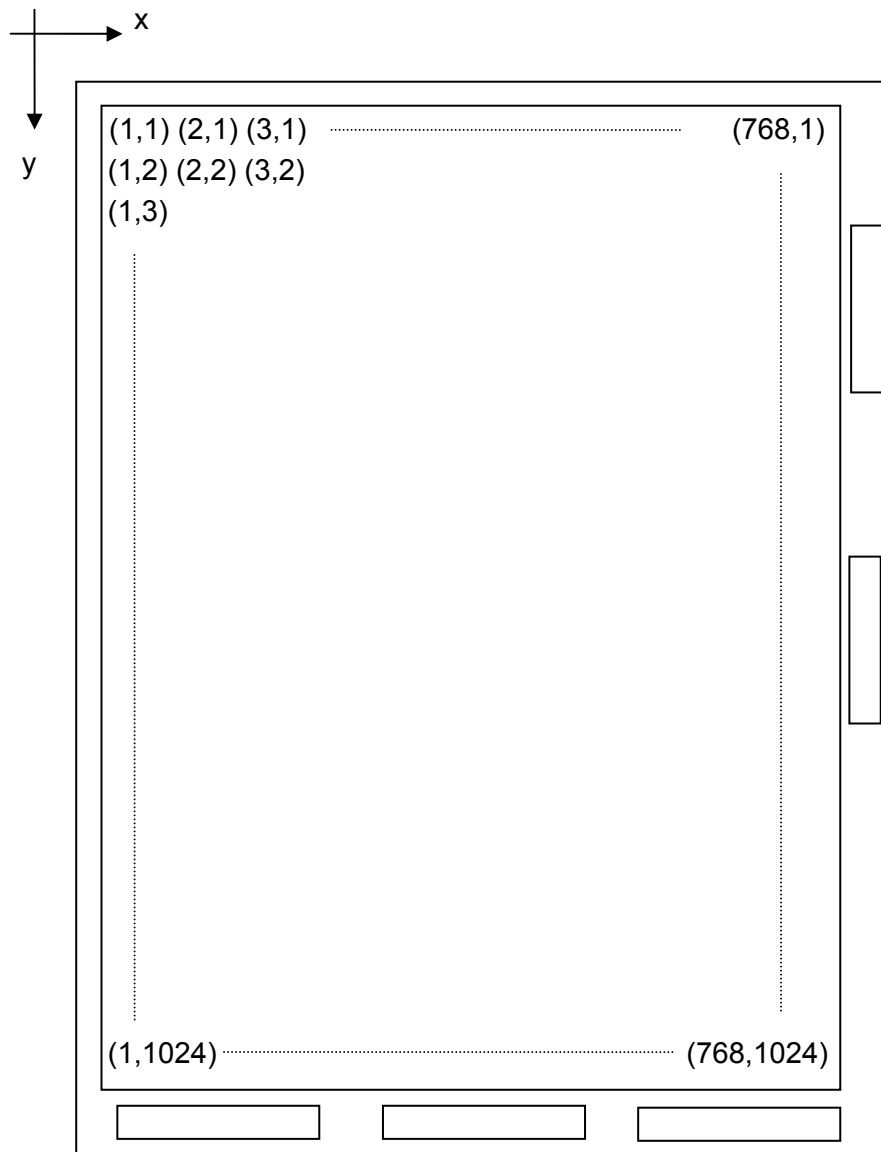
Gate Line 800: (1,800) → (2,800) → (3,800) → ... → (480,800)

* 1 Input sequence: Line 1 → Line 2 → ... → Line 800

* 2 Total data quantity: 480 x 800 = 384,000 bits = 48,000 bytes

4.7 8.1" (768 x 1024) EPD panel

Figure 4-7 8.1" (768 x 1024) EPD panel



Gate Line 1: (1,1) → (2,1) → (3,1) → ... → (768,1) →

⋮

Gate Line N: (1,N) → (2,N) → (3,N) → ... → (768,N) →

⋮

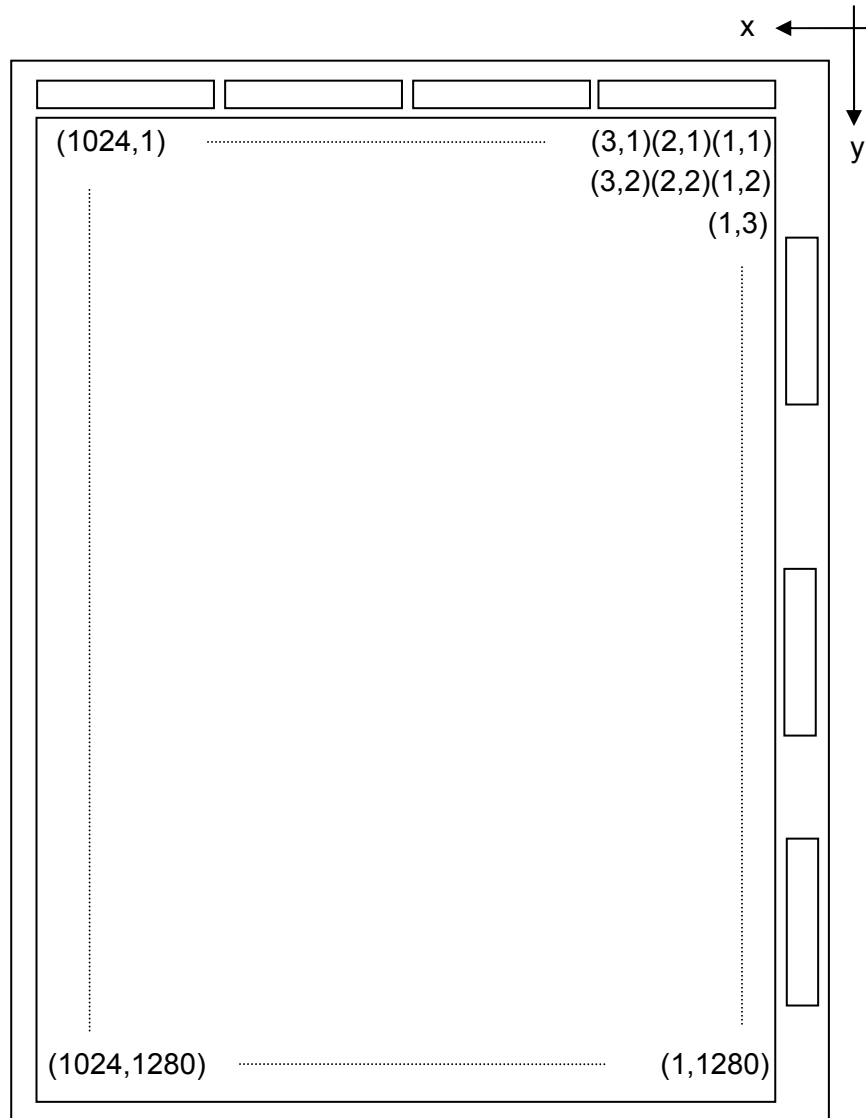
Gate Line 1024: (1,1024) → (2,1024) → (3,1024) → ... → (768,1024)

* 1 Input sequence: Line 1 → Line 2 → ... → Line 1024

* 2 Total data quantity: $768 \times 1204 = 786,432$ bits = 98,304 bytes

4.8 10.2" (1024 x 1280) EPD panel

Figure 4-8 10.2" (1024 x 1280) EPD panel



Gate Line 1: $(1,1) \rightarrow (2,1) \rightarrow (3,1) \rightarrow \dots \rightarrow (1024,1) \rightarrow$

Gate Line N: $(1,N) \rightarrow (2,N) \rightarrow (3,N) \rightarrow \dots \rightarrow (1024,N) \rightarrow$

Gate Line 1280: $(1,1280) \rightarrow (2,1280) \rightarrow (3,1280) \rightarrow \dots \rightarrow (1024,1280)$

* 1 Input sequence: Line 1 $\rightarrow$ Line 2 $\rightarrow \dots \rightarrow$ Line 1280

* 2 Total data quantity: $1024 \times 1280 = 1,310,720$ bits = 163,840 bytes

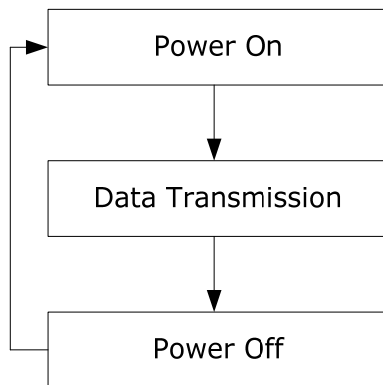
5 Sample code of SPI Interface Timing

5.1 Introduction

The sample code provides design reference for 2.7 inch EPD with its TCon board sending data via SPI interface. It follows PDi's SPI specification and data transmission sequence.

5.2 Driving Flowchart

Figure 5-1 Driving Flowchart



5.3 Sample Code Explanation

- Power On

```

Set  $T_{CLK} = 16;$            // Set  $T_{CLK} = 16\mu s$ 
Set  $T_{SETUP} = 8;$          // Set  $T_{SETUP} = 40\% \times T_{CLK} \sim 60\% \times T_{CLK}$ 
CS_SPI = 0;               // Chip Select get low
RESET_SPI = 0;            // RESET get low
Delay(10);                //  $T_{VCC\_on} > 10\ ms$ 

//Reset Display TCON
CS_SPI = 1;               // Chip Select get high
RESET_SPI = 1;            // RESET get high
Delay_ms (5);             // Delay 5 ms
RESET_SPI = 0;            // RESET get low
Delay_ms (5);             // Delay  $T_{RESET} > 5\ ms$ 
RST_SPI = 1;              // Reset high
Delay_ms (19);            //  $T_{RESET\_CS} > 19\ ms$ 
  
```

- Data Transmission

```

CS_SPI = 0;           // Chip Select get low
Delay_ms (1);         // Delay  $T_{CS\_SI} > 1\text{ ms}$  ;  $T_{RESET\_CS} + T_{CS\_SI} \geq 20\text{ms}$ 

// Send Header Byte
Send_Data (0x03);
Send_Data (0xA0);     // Send Header Byte ID = 0x03A0 (for 1.44, 2 and 2.7" EPD)
Delay_ms (120);       //  $120\text{ ms} \leq T_{DELAY1} \leq 150\text{ ms}$ 

// Transmit Display Pattern
for (i=0 ; i < 176 ; i++) //2.7" EPD resolution= 264 x 176
{
    for (j=0 ; j < 16 ; j++) // 1 Line of pixels, 264/8/2=16.5 Bytes
    {
        Send_Data (0xFF); // Byte1, "Black" for example
        Send_Data (0xFF); // Byte2, "Black" for example
        Delay_us (100); //  $T_{DELAY2} = 1 \times T_{CLK}$  us after every 2 bytes
    }
    Send_Data (0xFF); // Send last 8 bits(1 Byte) of pixels
    WriteSPI (0x00); // Last 8 bits of line must be 00 for 2.7" EPD
    Delay_ms (1); //  $T_{DELAY3} = 1\text{ ms}$  after each line
}

// Update Display
White (If BUSY_SPI = 1)
{
    CS_SPI = 1;           // Chip Select get high
    Delay_s (2.5);        //  $T_{UPDATE} = 2.5 \sim 5\text{ seconds}$ 
    CS_SPI = 0;           // Chip Select get low
}

```

- Power Off

```

Delay_ms (500);       //  $T_{VCC\_off} \leq 500\text{ ms}$ 
VCC & VDD → OFF      // Please make sure power and signal need to be set to "OFF"

```