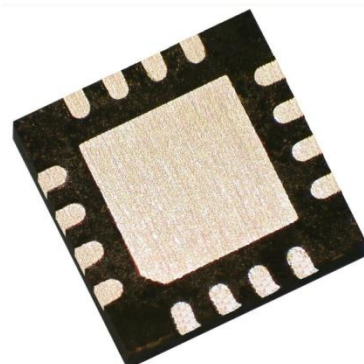


# HRF-AT4521

## 31.0 dB, DC - 2.5GHz, 5 Bit Serial Digital Attenuator

The Honeywell HRF-AT4521 is a 5-bit digital attenuator that is ideal for use in broadband communication system applications that require accuracy, speed and low power consumption. The HRF-AT4521 is manufactured with Honeywell's patented Silicon On Insulator (SOI) CMOS manufacturing technology, which provides the performance of GaAs with the economy and integration capabilities of conventional CMOS. These attenuators are DC coupled to improve lower operating frequency, frequency response and reduce the number of DC bias points required.



*HRF-AT4521 in VQFN Package*

### FEATURES

- Very Low DC Power Consumption
- Attenuation In Steps From 1 dB To 31 dB
- Single Positive Power Supply Voltage
- Serial Data Interface
- 50 Ohm Impedance
- DC-coupled, bi-directional RF path
- Space Saving VQFN Surface Mount Packaging
- Lead-free, RoHS compliant and halogen-free

### RF ELECTRICAL SPECIFICATIONS @ + 25°C (1)

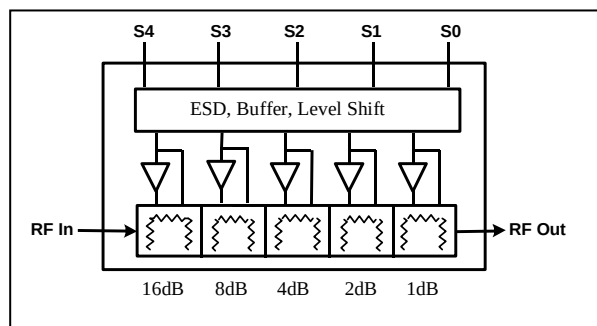
Results @  $V_{DD} = 5.0 \pm 10\%$ ,  $V_{SS} = 0$  unless otherwise stated,  $Z_0 = 50$  Ohms  
Contact Honeywell for relative performance at other supply configurations

| Parameter                       | Test Condition                                                          | Frequency | Minimum                            | Typical | Maximum | Units |
|---------------------------------|-------------------------------------------------------------------------|-----------|------------------------------------|---------|---------|-------|
| Insertion Loss                  |                                                                         | 1.0 GHz   |                                    | 2.0     | 2.6     | dB    |
|                                 |                                                                         | 2.0 GHz   |                                    | 2.2     | 2.8     | dB    |
|                                 |                                                                         | 2.5 GHz   |                                    | 2.8     | 3.4     | dB    |
| 1dB Compression                 | $V_{SS} = 0V$ , Input Power                                             | 2.0 GHz   |                                    | 22      |         | dBm   |
|                                 | $V_{SS} = -3V$ , Input Power                                            | 2.0 GHz   |                                    | 28      |         | dBm   |
| Input IP3                       | $V_{SS} = 0V$<br>Two-tone inputs, up to +5 dBm<br>@ 0 dBm attenuation   | 2.0 GHz   |                                    | 36      |         | dBm   |
| Input IP3                       | $V_{SS} = -3V$<br>Two-tone inputs, up to + 5 dBm<br>@ 0 dBm attenuation | 2.0 GHz   |                                    | >36     |         | dBm   |
| Return Loss                     | Any Combination of Bits                                                 |           | -11                                | -13     |         | dB    |
| Attenuation Accuracy            | All attenuation states                                                  | 1.0 GHz   | + (0.25 + 2.5 %), - (0.10 + 5.0 %) |         |         | dB    |
|                                 | All attenuation states                                                  | 2.0 GHz   | + 0.45, - (0.20 + 8.0 %)           |         |         | dB    |
|                                 | All attenuation states                                                  | 2.5 GHz   | + 0.35, - (-0.40 + 10.5%)          |         |         | dB    |
| Trise, Tfall<br>Ton, Toff (Tpd) | 10% To 90%                                                              |           |                                    | 10      |         | nS    |
|                                 | 50% Cntl To 90%/10%RF                                                   |           |                                    | 15      |         | nS    |
| T clock Period (Tprd)           | T high / T low = ½ minimum clock period                                 |           | 50                                 |         |         | nS    |
| T data set up (Tsup)            | Set up to rising edge of clock                                          |           | 5                                  |         |         | nS    |
| T data hold (Thld)              | Data hold after rising edge of clock                                    |           | 2                                  |         |         | nS    |
| T latch set up (Tlsup)          | Data set up to rising edge of OE                                        |           | 5                                  |         |         | nS    |

Note 1 - For higher accuracy designs, please consider HRF-AT4610/HRF-AT4611.

# HRF-AT4521

## FUNCTIONAL SCHEMATIC



## DC ELECTRICAL SPECIFICATIONS @ + 25°C

| Parameter             | Minimum          | Typical | Maximum  | Units |
|-----------------------|------------------|---------|----------|-------|
| $V_{DD}$              | 3.3 <sup>1</sup> | 5.0     | 5.5      | V     |
| $V_{SS}$              | -5.0             |         |          | V     |
| $I_{DD}$              |                  | <5.0    | 50       | uA    |
| CMOS Logic level (0)  | 0                |         | 0.8      | V     |
| CMOS Logic level (1)  | $V_{DD} - 0.8$   |         | $V_{DD}$ | V     |
| Input Leakage Current |                  |         | 10       | uA    |

Note 1, the performance curves are for  $V_{DD} = +5.0 \pm 10\%$

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

| Parameter                  | Absolute Maximum                 | Units |
|----------------------------|----------------------------------|-------|
| Input Power                | + 35                             | dBm   |
| $V_{DD}$                   | +6.0                             | V     |
| $V_{SS}$                   | -5.5                             | V     |
| ESD Voltage <sup>2</sup>   | 400                              | V     |
| Operating Temperature      | -40 To +85                       | °C    |
| Storage Temperature        | -65 To +125                      | °C    |
| Moisture Sensitivity Level | Level 3 @ 260°C                  |       |
| Digital Inputs             | $V_{DD} + 0.6$ max to $-0.6$ min | V     |

Note 1 - Operation of this device beyond any of these parameters may cause permanent damage.

Note 2 - Although the HRF-AT4521 contains ESD protection circuitry on all digital inputs, precautions should be taken to ensure that the Absolute Maximum Ratings are not exceeded.

**Latch-Up:** Unlike conventional CMOS digital attenuators, Honeywell's HRF-AT4521 is immune to latch-up.

# HRF- AT4521

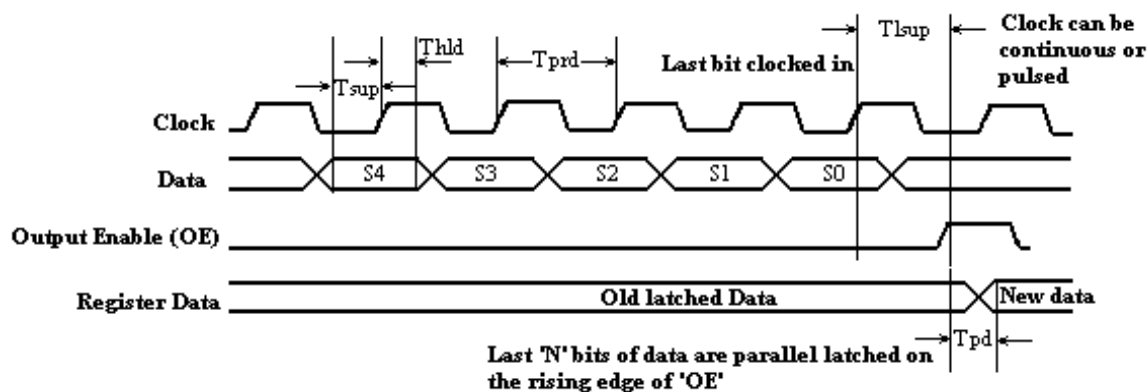
## PIN CONFIGURATIONS

| Pin | Function | Pin | Function  |
|-----|----------|-----|-----------|
| 1   | VDD      | 9   | GROUND    |
| 2   | GROUND   | 10  | RF OUTPUT |
| 3   | RF INPUT | 11  | GROUND    |
| 4   | GROUND   | 12  | VSS       |
| 5   | GROUND   | 13  | GROUND    |
| 6   | GROUND   | 14  | OE        |
| 7   | GROUND   | 15  | CLK       |
| 8   | GROUND   | 16  | DATA      |

**Note:** Bottom ground plate must be grounded for proper RF performance.

## SERIAL DATA LOAD

Serial data is shifted into the register on the rising edge of clock, MSB first. The state of "OE" will not affect the shifting of data. The rising edge of the "OE" signal will be the clock for the transfer of shifted data. Latched new data occurs one prop delay after the rising edge of "OE". See the Electrical Spec Table for AC parameters.



## TRUTH TABLE

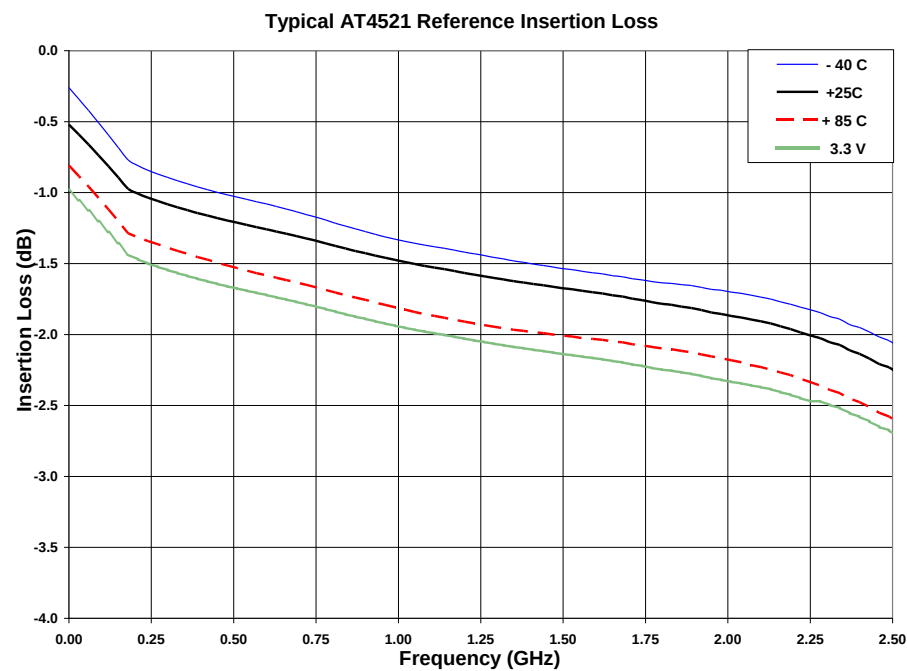
| S4 | S3 | S2 | S1 | S0 | Output          |
|----|----|----|----|----|-----------------|
| 0  | 0  | 0  | 0  | 0  | Reference Input |
| 0  | 0  | 0  | 0  | 1  | 1 dB            |
| 0  | 0  | 0  | 1  | 0  | 2 dB            |
| 0  | 0  | 1  | 0  | 0  | 4 dB            |
| 0  | 1  | 0  | 0  | 0  | 8 dB            |
| 1  | 0  | 0  | 0  | 0  | 16 dB           |
| 1  | 1  | 1  | 1  | 1  | 31 dB           |

Operation: Data on serial input D is clocked into internal registers on the low to high transition of the Clock signal (CK). The register output is enabled when Output Enable (OE) is in the low state. "0" = CMOS Low, "1" = CMOS High.

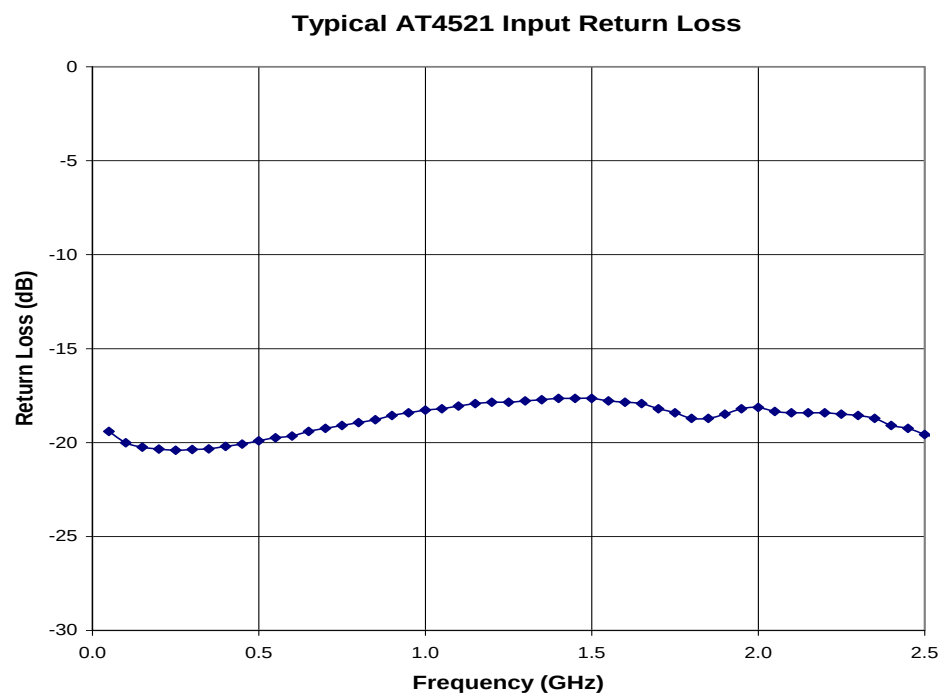
# HRF-AT4521

## PERFORMANCE CURVES

### Insertion Loss

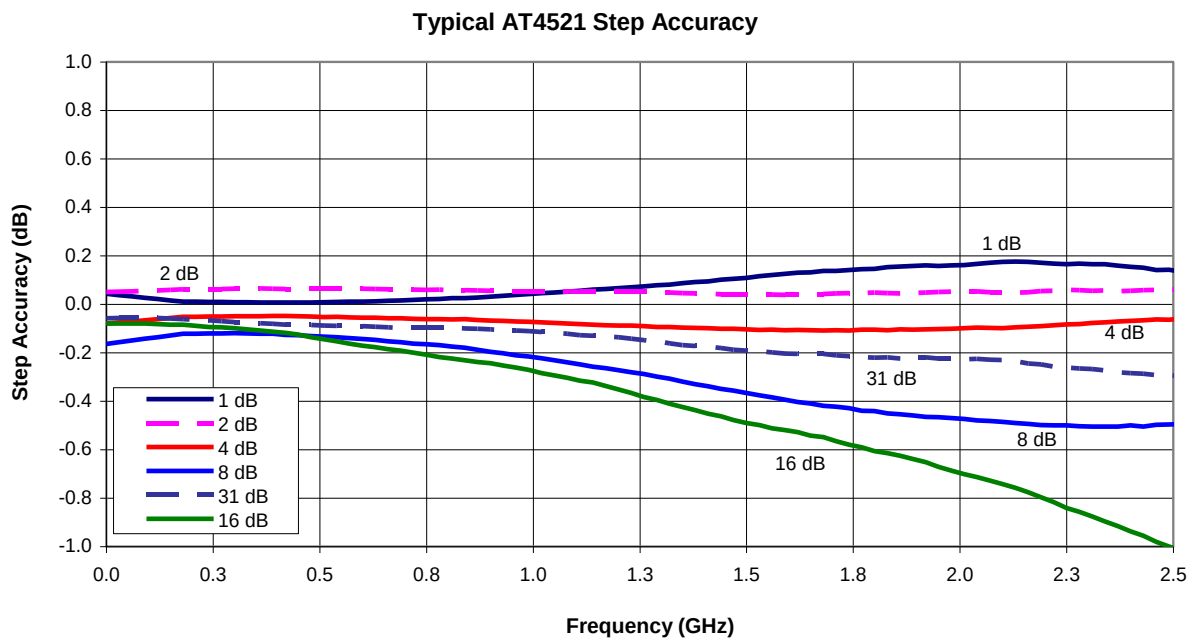


### Return Loss

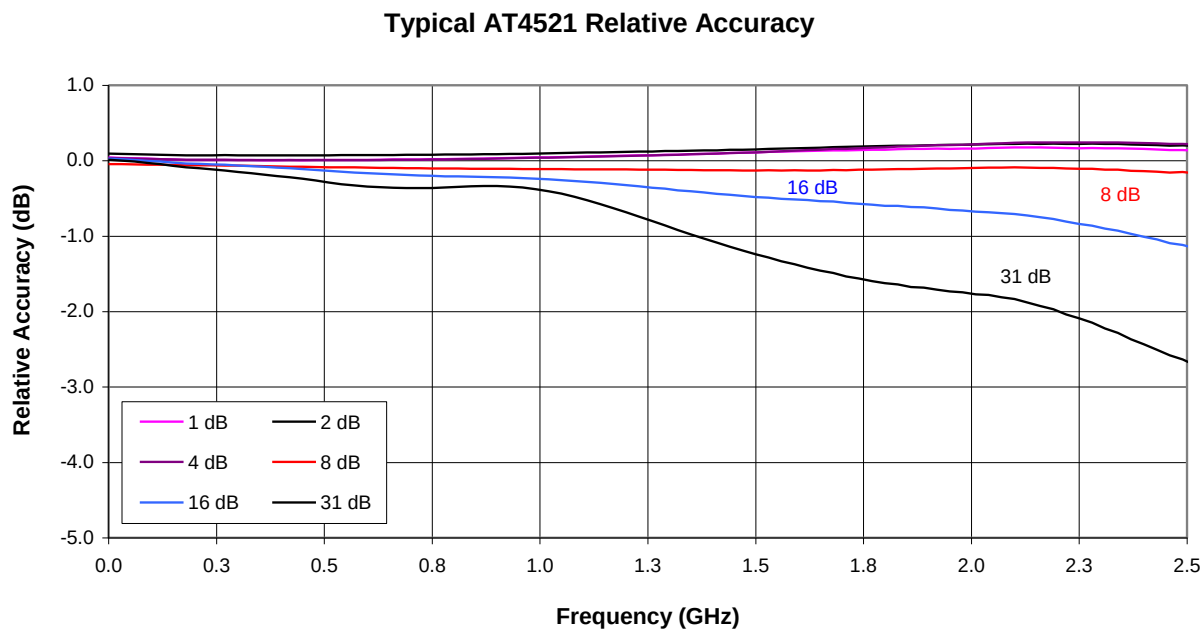


# HRF- AT4521

## Step Accuracy



## Relative Accuracy

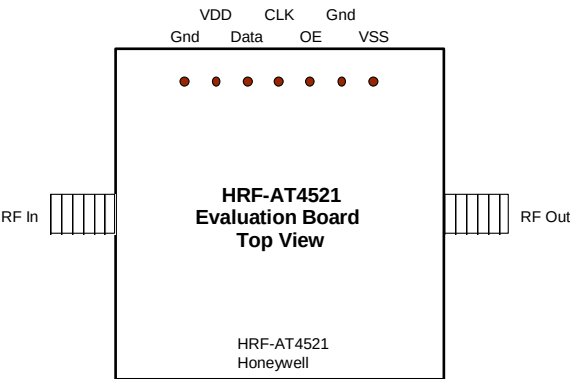
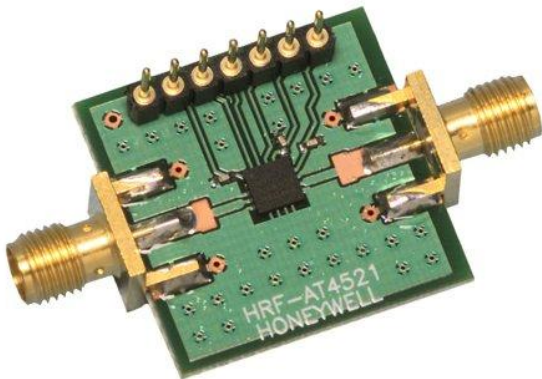




# HRF- AT4521

## EVALUATION CIRCUIT BOARD

Honeywell's evaluation board provides an easy to use method of evaluating the RF performance of our attenuator. Simply connect power, DC and RF signals to be measuring attenuator performance in less than 10 minutes.



HRF-AT4521 Evaluation Board

## EVALUATION CIRCUIT BOARD LAYOUT DESIGN DETAILS

| Item           | Description                                                    |
|----------------|----------------------------------------------------------------|
| PCB            | Impedance Matched Multi-Layer FR4                              |
| Attenuator     | HRF-AT4521 Digital Attenuator                                  |
| Chip Capacitor | Panasonic Model ECU-E1C103KBQ Capacitor, .01uf 0402 10% 16V    |
| RF Connector   | Johnson Connectors Model 142-0701-801 SMA RF Coaxial Connector |
| DC Pin         | Mil-Max Model 800-10-064-10-001 Header Pins                    |

## ORDERING INFORMATION

| Ordering Number  | Delivery Method  | Units Per Shipment  |
|------------------|------------------|---------------------|
| HRF-AT4521-FL-TR | Tape and Reel    | 2500 Units per Reel |
| HRF-AT4521-E     | Evaluation Board | One Board Per Box   |

The new –FL attenuators replace and are electrically equivalent to the –GR attenuators. The –GR attenuators are obsolete.

## FIND OUT MORE

For more information on Honeywell’s Microwave Products visit us online at [www.honeywellmicrowave.com](http://www.honeywellmicrowave.com) or contact us at 800-323-8295 (763-954-2474 internationally).

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