IC1000

Data/Clock Extraction IC

- ***Provides start-of-data detection and data clock recovery***
- ***Supports data rates from 2400 to 19200 bps***
- ***Allows unsquelched receiver operation for improved sensitiviy***
- ***Compatible with RFM's TR-Series ASH transceivers***

The IC1000 Data/Clock Extraction IC detects a start-of-data pulse sequence and then provides clocking pulses in the middle of each following data bit. The IC1000 is designed to support a host protocol processor which can be in sleep mode until interrupted into active operation by the start-of-data detect pulse. The IC1000 is compatible with RFM's 2nd generation ASH transceivers and receivers and allows these radios to operate with no threshold for improved system sensitivity.

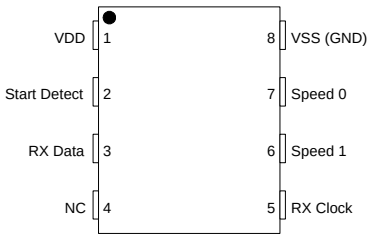
Absolute Maximum Ratings

Please refer to the latest revision of Microchip Technology's data sheet for the PIC12LC508A-04I\SN

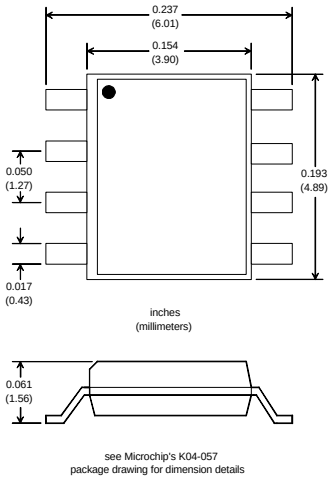
Electrical Characteristics Summary

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Supply Voltage	VDD		2.5		5.5	V
Supply Current	IDD			450		µA
Logic Low Input	VIL				0.2	VDD
Logic High Input	VIH		0.8			VDD
Logic Low Output	VOL				0.6	V
Logic High Output	VOH		VDD - 0.7			V
Supported Data Rates:						
Speed0 = 0, Speed1 = 0				2400		bps
Speed0 = 1, Speed1 = 0				4800		bps
Speed0 = 0, Speed1 = 1				9600		bps
Speed0 = 1, Speed1 = 1				19200		bps
Transmitted Bit Rate Tolerance					±1	%
Operating Temperature Range			-40		85	°C

IC1000 Pin Out



IC1000 Outline Drawing



Operation

A typical IC1000 application is shown in Figure 1. The RX Data output from the 2nd generation ASH transceiver (or receiver) is buffered by a inverting buffer and is applied to Pin 3 of the IC1000 and the Data In pin of the host microprocessor. The IC1000 detects the presence of a specific start-of-data pulse sequence and outputs a Start Detect pulse on Pin 2. This pulse is applied to an interrupt pin on the host processor. The IC1000 generates data clocking (data valid) pulses in the middle of each following bit period using an oversampled PLL clock extraction method. The IC1000 is designed to continuously search for the start-of-data pulse sequence and will operate with noise present between data transmissions. This allows the ASH radio to operate with little or no data slicer (DS1) threshold for improved system sensitivity.

The IC1000 supports four data rates - 2400, 4800, 9600, and 19200 bits per second (bps). The data rate is selected by setting the logic input levels to Pin 6 (Speed 1) and Pin 7 (Speed 0). The logic levels to these pins are read at power on reset. It is necessary to recycle the power to the IC1000 to select a new data rate.

The IC1000 is implemented in an industrial temperature range PIC12LC508A-04I\SN microcontroller using internal clocking. Please refer to the latest revision of Microchip Technology's data sheet (DS40139 series) for detailed electrical and mechanical specifications.

Start-of-Data Pulse Sequence Generation

The IC1000 start-of-data pulse sequence is a steady low pulse of eight bit periods, followed by a sequence of eight bits in an alternating high-low-high-low… pattern. This pulse sequence is very unlikely to occur in a stream of white noise (data sliced), providing good false triggering performance. The IC1000 outputs the Start Detect pulse when the RX Data input line to the IC1000 has remained a steady low for eight bit periods. Data is valid on the first clock pulse after the falling edge of the Start Detect Pulse. After eight bit periods of a steady low, the data input should begin the eight-bit sequence of alternating high and low bits. Thereafter, the data clocking pulses will adjust to stay centered in the averaged middle of each bit period, provided the data has been encoded as discussed below. The eight-bit alternating high-low sequence provides data clocking alignment training under low signal-to-noise conditions (data edge jitter) and should be used for best results.

Note that the ASH radio RX Data output signal is inverted before being applied to the IC1000. The steady low pulse that begins the start-of-data pulse sequence to the IC1000 is generated by the reception of an eight-bit long RF transmission. This pulse also helps "train" the base-band coupling capacitor in the ASH radio for best data slicer noise rejection. The host processor should generate inverted data for transmission by the ASH radio and should input the same inverted data that drives the IC1000.

Data Encoding

Data should be encoded to provide frequent logic state transitions (edges) to facilitate data clock alignment, and should exhibit good dynamic DC-balance (50% high bits and 50% low bits over any interval of 16 bits or less) to maintain the radio's base-band capacitor training for best noise performance.

The IC1000 uses the encoding method of byte-to-12 bit symbolizing, which encodes each byte as a pattern of 12 bits, always with six one bits and six zero bits. Symbolizing requires fewer bits than Manchester to encode a message, and also provides frequent state transitions and good DC-balance. Both techniques provide good results. An example of 12-bit symbolizing can be found in section 3.3 of the ASH Transceiver Designer's Guide.

Note that the IC1000 has no provisions for detecting end-of-data. This provides flexibility in message length and data encoding, but requires the message length and/or an end-of-data symbol to be embedded in the data by the user.

Timing Accuracy

It is recommended that all pulses (bits and sequences of bits of the same logic state) generated for use with the IC1000 be accurate to 1% of the target bit period: This level of timing accuracy provides a tolerance for operation under low signal-to-noise conditions where edge jitter occurs on the edges of the data.

Data Rate	Bit Period	Timing Accuracy/Bit	Speed 0	Speed 1
2400 bps	417 µs	4 µs	0	0
4800 bps	208 µs	2 µs	1	0
9600 bps	104 µs	1 µs	0	1
19200 bps	52 µs	0.5 µs	1	1

Data/Clock Extraction IC

Pin Desciptions

Pin	Name	Description
1	VDD	This pin is the positive power supply input for the IC1000. This pin should be bypassed with a 1000 pF ceramic capacitor connected with short leads between this pin and Pin 8. The IC1000 is designed to operate over a 2.7 to 5.0 Vdc power supply voltage range.
2	Start Detect	This output pin generates a positive pulse 1 to 1.5 bit periods wide upon the detection of the start-of-data pulse sequence. Data is valid on the first RX Clock pulse following the falling edge of the Start Detect pulse.
3	RX Data	This input pin is driven by a inverting buffer on the ASH transceiver RX Data output pin. The IC1000 RX Clock extraction PLL and start-of-data detect routines are driven from the input to this pin.
4	NC	This pin is not used and should be left unconnected.
5	RX Clock	The RX Clock signal extracted from the RX Data input is provided on this output pin. The RX Clock pulse occurs near the middle of each bit period (valid after the falling edge of the Start Detect pulse).
6	Speed 1	This input pin, in conjunction with Speed 0 (Pin 7), selects the data rate for the PLL clock extraction. One of four data rates can be selected - 2400, 4800, 9600 and 19,200 bits per second. This pin is read once when the IC1000 is powered up.
7	Speed 0	This input pin, in conjunction with Speed 1 (Pin 6), selects the data rate for the PLL clock extraction. One of four data rates can be selected - 2400, 4800, 9600 and 19,200 bits per second. This pin is read once when the IC1000 is powered up.
8	VSS (GND)	This pin is the power supply return pin.

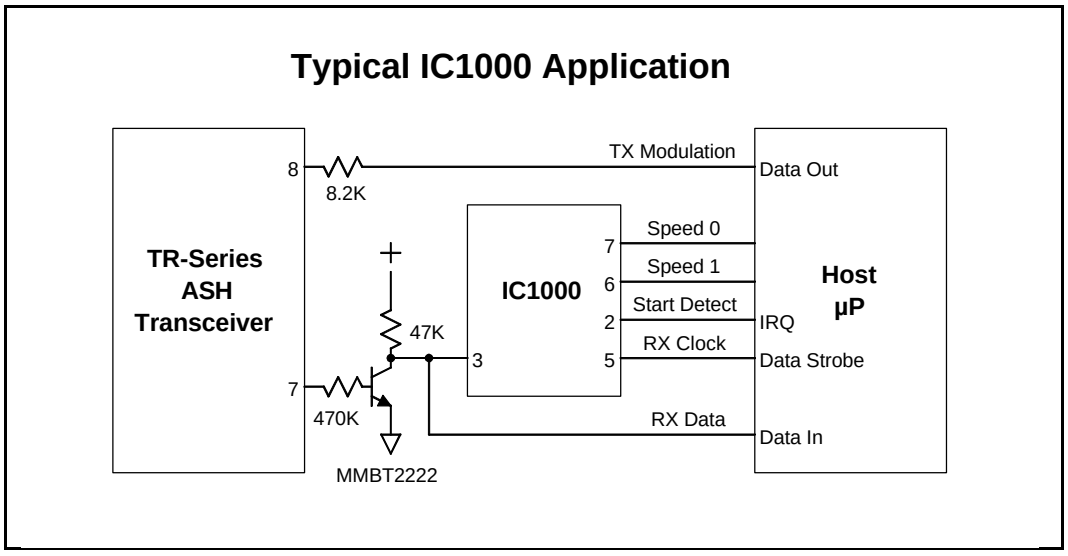


Figure 1

Data/Clock Extraction IC