features

- **10-Bit Voltage Output DAC**
- **Programmable Settling Time vs Power Consumption**
  - **3 μs in Fast Mode**
  - **9 μs in Slow Mode**
- **Ultra Low Power Consumption:**
  - **900 μW Typ in Slow Mode at 3 V**
  - **2.1 mW Typ in Fast Mode at 3 V**
- **Differential Nonlinearity . . . <0.2 LSB Typ**
- **Compatible With TMS320 and SPI Serial Ports**
- **Power-Down Mode (10 nA)**

- **Buffered High-Impedance Reference Input**
- **Voltage Output Range . . . 2 Times the Reference Input Voltage**
- **Monotonic Over Temperature**
- **Available in MSOP Package**

applications

- **Digital Servo Control Loops**
- **Digital Offset and Gain Adjustment**
- **Industrial Process Control**
- **Machine and Motion Control Devices**
- **Mass Storage Devices**

description

The TLV5606 is a 10-bit voltage output digital-to-analog converter (DAC) with a flexible 4-wire serial interface. The 4-wire serial interface allows glueless interface to TMS320, SPI, QSPI, and Microwire serial ports. The TLV5606 is programmed with a 16-bit serial string containing 4 control and 10 data bits. Developed for a wide range of supply voltages, the TLV5606 can operate from 2.7 V to 5.5 V.

D OR DGK PACKAGE
(TOP VIEW)

DIN	1	8	V_{DD}
SCLK	2	7	OUT
$\overline{CS}$	3	6	REFIN
FS	4	5	AGND

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. The settling time of the DAC is programmable to allow the designer to optimize speed versus power dissipation. The settling time is chosen by the control bits within the 16-bit serial input string. A high-impedance buffer is integrated on the REFIN terminal to reduce the need for a low source impedance drive to the terminal.

Implemented with a CMOS process, the TLV5606 is designed for single supply operation from 2.7 V to 5.5 V. The device is available in an 8-terminal SOIC package. The TLV5606C is characterized for operation from 0°C to 70°C. The TLV5606I is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

	PACKAGE	
T_A	SMALL OUTLINE† (D)	MSOP† (DGK)
0°C to 70°C	TLV5606CD	TLV5606CDGK
−40°C to 85°C	TLV5606ID	TLV5606IDGK

† Available in tape and reel as the TLV5606CDR, TLV5606IDR, TLV5606CDGKR, and the TLV5606IDGKR

TEXAS INSTRUMENTS

functional block diagram
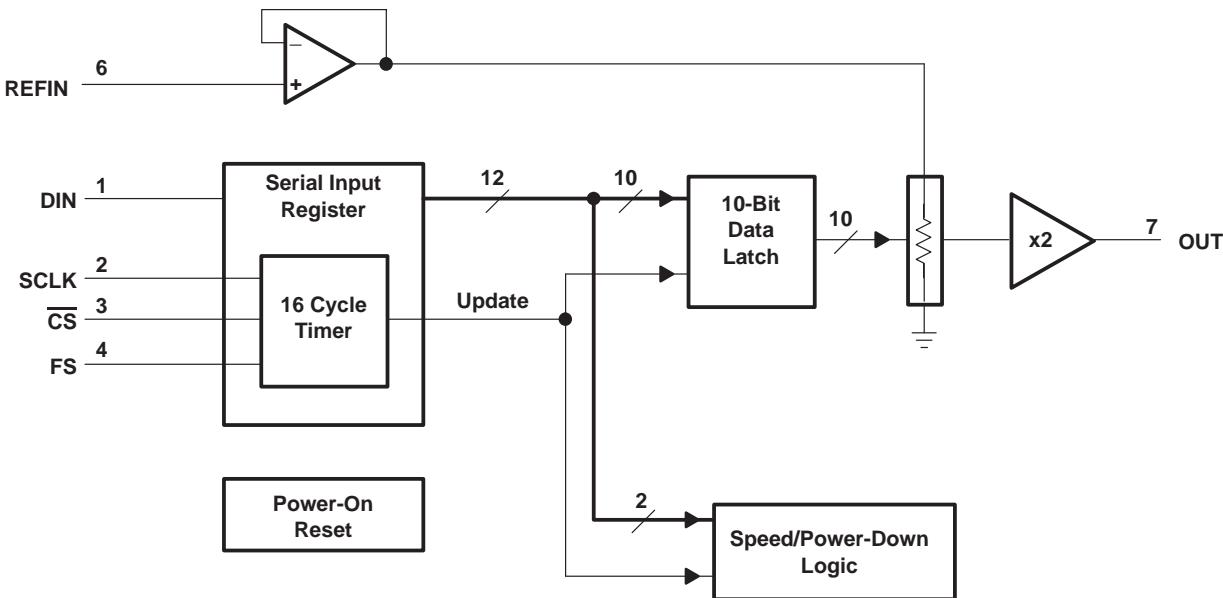
Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	5		Analog ground
$\overline{CS}$	3	I	Chip select. Digital input used to enable and disable inputs, active low.
DIN	1	I	Serial digital data input
FS	4	I	Frame sync. Digital input used for 4-wire serial interfaces such as the TMS320 DSP interface.
OUT	7	O	DAC analog output
REFIN	6	I	Reference analog input voltage
SCLK	2	I	Serial digital clock input
V_{DD}	8		Positive power supply

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INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND)	7 V
Reference input voltage range	− 0.3 V to V_{DD} + 0.3 V
Digital input voltage range	− 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5606C	0°C to 70°C
TLV5606I	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD} = 5 V	4.5	5	5.5	V
	V_{DD} = 3 V	2.7	3	3.3	V
High-level digital input voltage, V_{IH}	DV_{DD} = 2.7 V	2			V
	DV_{DD} = 5.5 V	2.4			V
Low-level digital input voltage, V_{IL}	DV_{DD} = 2.7 V			0.6	V
	DV_{DD} = 5.5 V			1	V
Reference voltage, V_{ref} to REFIN terminal	V_{DD} = 5 V (see Note 1)	AGND	2.048	V_{DD}−1.5	V
Reference voltage, V_{ref} to REFIN terminal	V_{DD} = 3 V (see Note 1)	AGND	1.024	V_{DD}−1.5	V
Load resistance, R_L		2	10		kΩ
Load capacitance, C_L				100	pF
Clock frequency, f_{CLK}				20	MHz
Operating free-air temperature, T_A	TLV5606C	0		70	°C
	TLV5606I	−40		85	°C

NOTE 1:   Due to the x2 output buffer, a reference input voltage ≥ $V_{DD}/2$ causes clipping of the transfer function.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD} Power supply current		V_{DD} = 5 V, VREF = 2.048 V, No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	Fast		0.9	1.35	mA
			Slow		0.4	0.6	mA
		V_{DD} = 3 V, VREF = 1.024 V No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	Fast		0.7	1.1	mA
			Slow		0.3	0.45	mA
Power down supply current (see Figure 12)					10		nA
PSRR Power supply rejection ratio	Zero scale	See Note 2			−80		dB
	Full scale	See Note 3			−80		
Power on threshold voltage, POR					2		V

NOTES: 2.   Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:
        PSRR = 20 log [($E_{ZS}(V_{DD}max) − E_{ZS}(V_{DD}min))/V_{DD}max$]
        3.   Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by:
        PSRR = 20 log [($E_G(V_{DD}max) − E_G(V_{DD}min))/V_{DD}max$]

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

static DAC specifications R_L = 10 kΩ, C_L = 100 pF

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10	10	bits
INL	Integral nonlinearity	See Note 4		± 0.5	±1.5	LSB
DNL	Differential nonlinearity	See Note 5		± 0.2	± 1	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)	See Note 6			±10	mV
	Zero-scale-error temperature coefficient	See Note 7		10		ppm/°C
E_G	Gain error	See Note 8			±0.6	% of FS voltage
	Gain-error temperature coefficient	See Note 9		10		ppm/°C

NOTES: 4. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors. Tested from code 10 to code 1023.
5. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code. Tested from code 10 to code 1023.
6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
7. Zero-scale-error temperature coefficient is given by: E_{ZS} TC = [E_{ZS} (T_{max}) – E_{ZS} (T_{min})]/$V_{ref} \times 10^6$/(T_{max} – T_{min}).
8. Gain error is the deviation from the ideal output ($2V_{ref}$ – 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
9. Gain temperature coefficient is given by: E_G TC = [E_G(T_{max}) – E_G (T_{min})]/$V_{ref} \times 10^6$/(T_{max} – T_{min}).

output specifications

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L = 10 kΩ	0		AV_{DD}−0.1	V
	Output load regulation accuracy	R_L = 2 kΩ, vs 10 kΩ		0.1	±0.25	% of FS voltage

reference input (REF)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage range			0		V_{DD}−1.5	V
R_I	Input resistance				10		MΩ
C_I	Input capacitance				5		pF
	Reference input bandwidth	REFIN = 0.2 V_{pp} + 1.024 V dc	Slow		525		kHz
			Fast		1.3		MHz
	Reference feed through	REFIN = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 10)			−75		dB

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.

digital inputs

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	V_I = V_{DD}			±1	µA
I_{IL}	Low-level digital input current	V_I = 0 V			±1	µA
C_I	Input capacitance			3		pF

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INSTRUMENTS
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operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

analog output dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	$R_L = 10$ kΩ, See Note 11	$C_L = 100$ pF,	Fast		3	5.5	μs
				Slow		9	20	
$t_{s(CC)}$	Output settling time, code to code	$R_L = 10$ kΩ, See Note 12	$C_L = 100$ pF,	Fast		1		μs
				Slow		2		μs
SR	Slew rate	$R_L = 10$ kΩ, See Note 13	$C_L = 100$ pF,	Fast		3.6		V/μs
				Slow		0.9		
	Glitch energy	Code transition from 0x7FF to 0x800				10		nV–s
S/N	Signal to noise	fs = 400 KSPS fout = 1.1 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF, BW = 20 kHz				62		dB
S/(N+D)	Signal to noise + distortion					60		dB
THD	Total harmonic distortion					–61		dB
	Spurious free dynamic range					68		dB

NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x080 to 0x3FF or 0x3FF to 0x080. Not tested, ensured by design.
12. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. Code change from 0x1FF to 0x200. Not tested, ensured by design.
13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

digital input timing requirements

|		MIN	NOM	MAX	UNIT
$t_{su(CS–FS)}$	Setup time, $\overline{CS}$ low before FS$\downarrow$	10			ns
$t_{su(FS–CK)}$	Setup time, FS low before first negative SCLK edge	8			ns
$t_{su(C16–FS)}$	Setup time, sixteenth negative edge after FS low on which bit D0 is sampled before rising edge of FS	10			ns
$t_{su(C16–CS)}$	Setup time, sixteenth positive SCLK edge (first positive after D0 is sampled) before $\overline{CS}$ rising edge. If FS is used instead of the sixteenth positive edge to update the DAC, then the setup time is between the FS rising edge and $\overline{CS}$ rising edge.	10			ns
t_{wH}	Pulse duration, SCLK high	25			ns
t_{wL}	Pulse duration, SCLK low	25			ns
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	8			ns
$t_{h(D)}$	Hold time, data held valid after SCLK falling edge	5			ns
$t_{wH(FS)}$	Pulse duration, FS high	20			ns

TLV5606
2.7-V TO 5.5-V LOW POWER 10-BIT DIGITAL-TO-ANALOG
CONVERTERS WITH POWER DOWN
SLAS259B – DECEMBER 1999 – REVISED APRIL 2004

PARAMETER MEASUREMENT INFORMATION
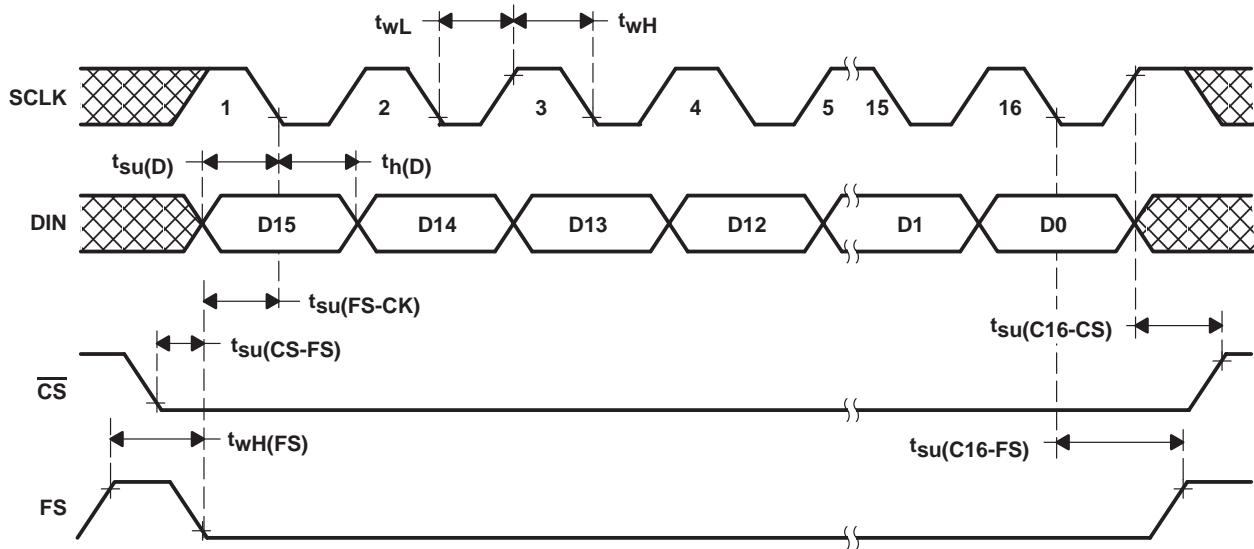
Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
LOAD CURRENT

Figure 2

OUTPUT VOLTAGE
vs
LOAD CURRENT

Figure 3

OUTPUT VOLTAGE
vs
LOAD CURRENT

Figure 4

OUTPUT VOLTAGE
vs
LOAD CURRENT
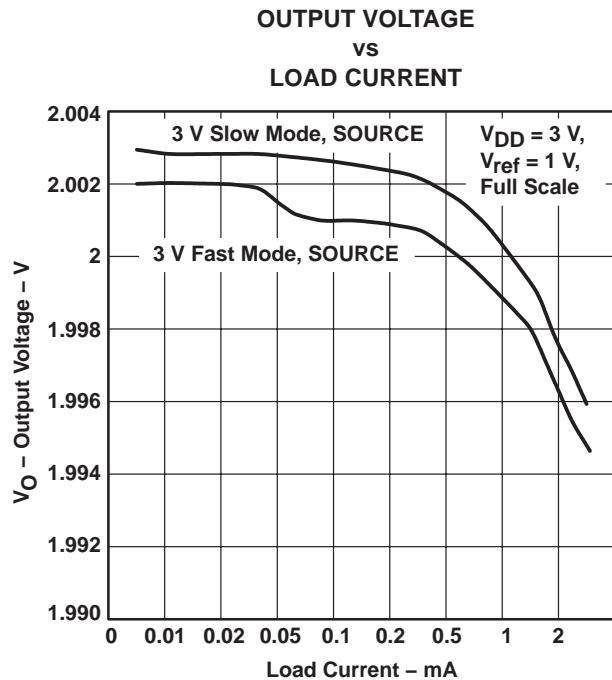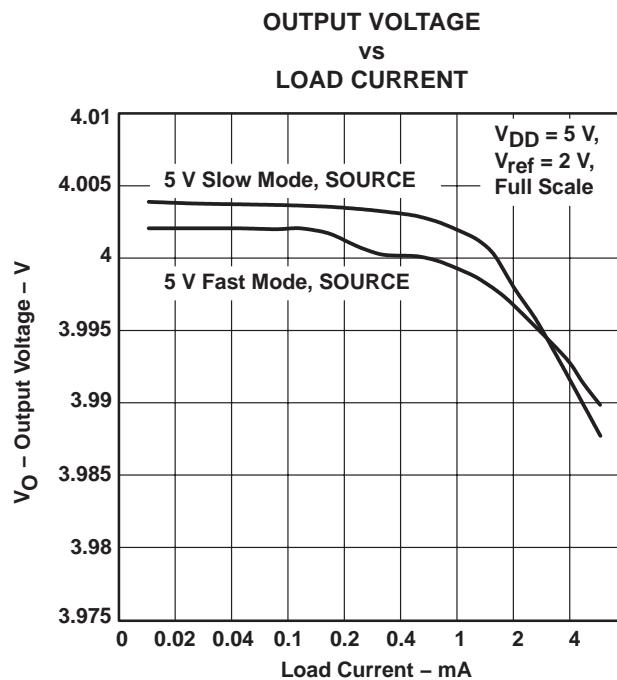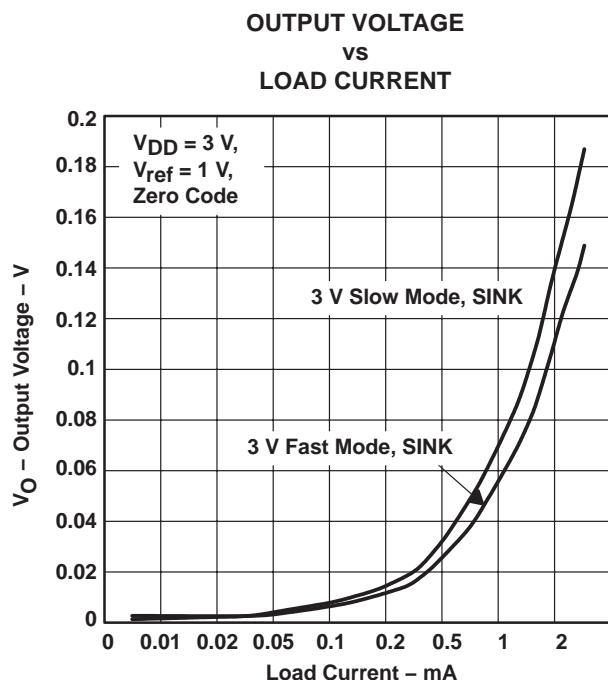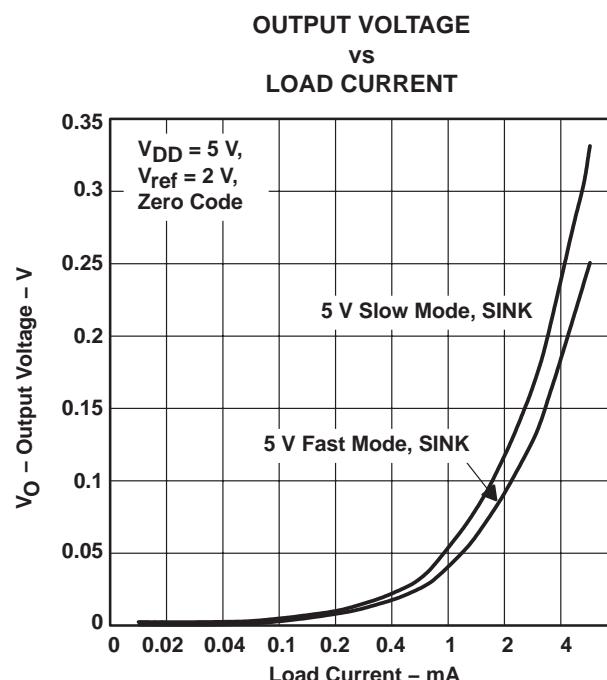
Figure 5

TYPICAL CHARACTERISTICS
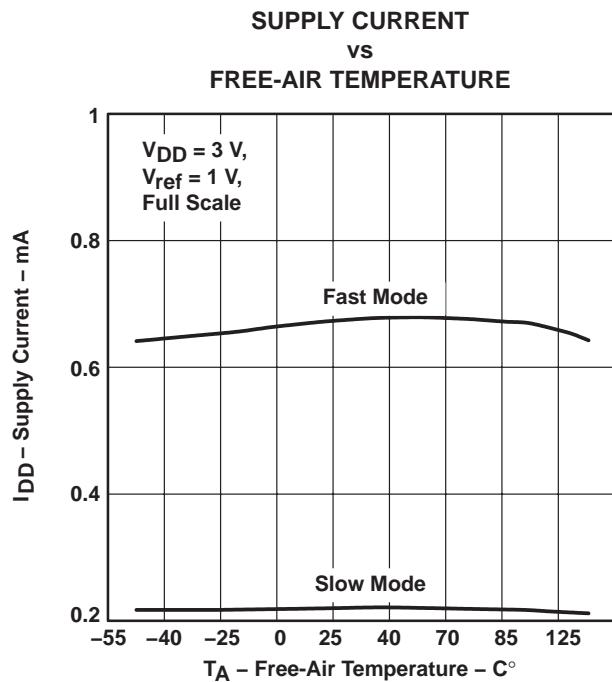
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 6

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 7

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

Figure 8

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

Figure 9

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TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION AND NOISE
vs
FREQUENCY

V_{ref} = 1 V dc + 1 V p/p Sinewave,
Output Full Scale

Fast Mode

Figure 10

TOTAL HARMONIC DISTORTION AND NOISE
vs
FREQUENCY

V_{ref} = 1 V dc + 1 V p/p Sinewave,
Output Full Scale

Slow Mode

Figure 11

SUPPLY CURRENT
vs
TIME (WHEN ENTERING POWER-DOWN MODE)
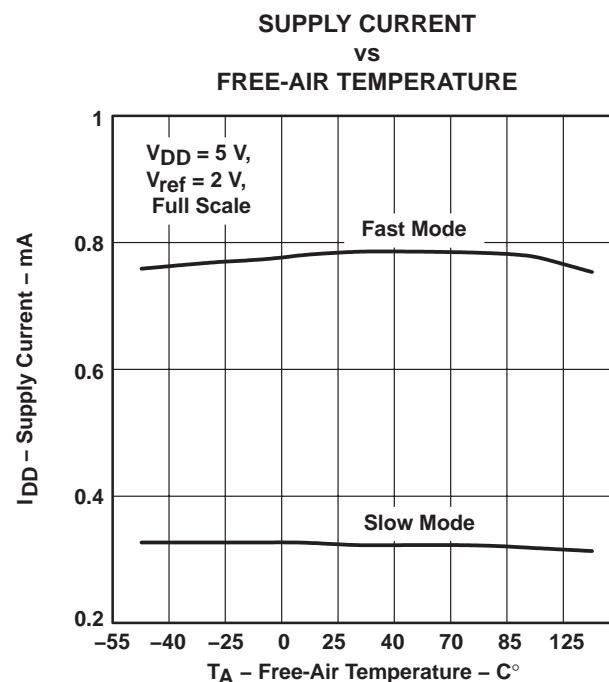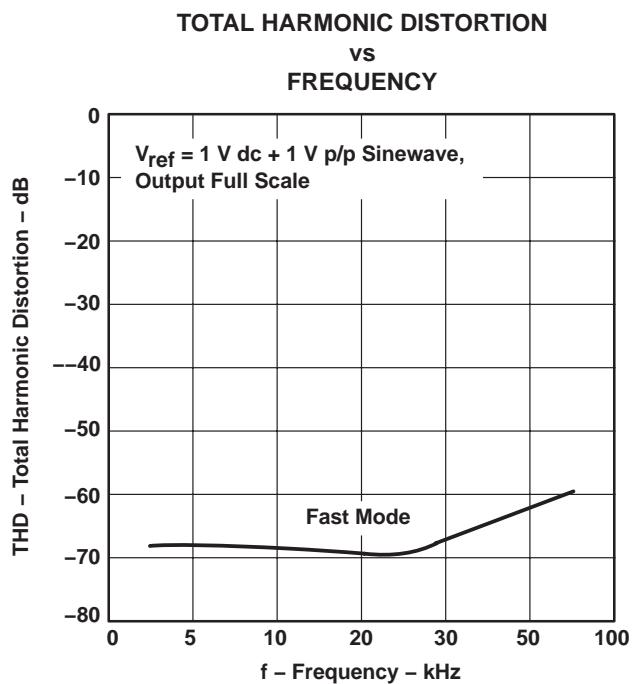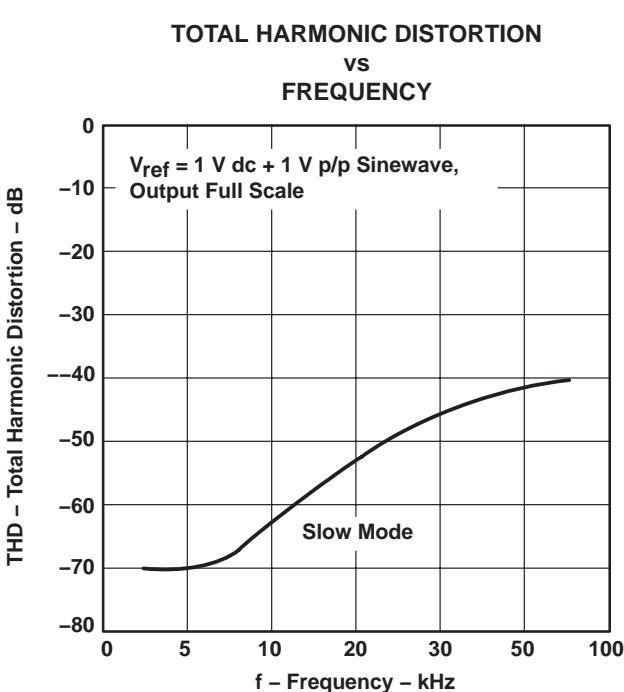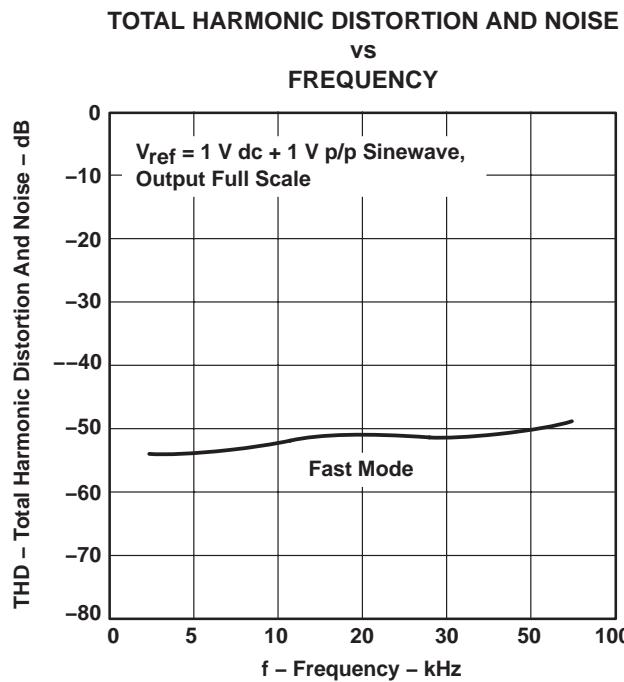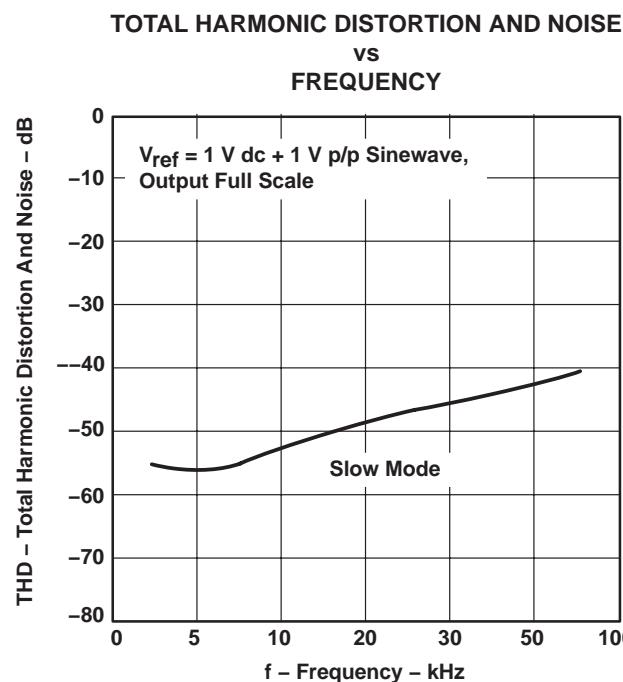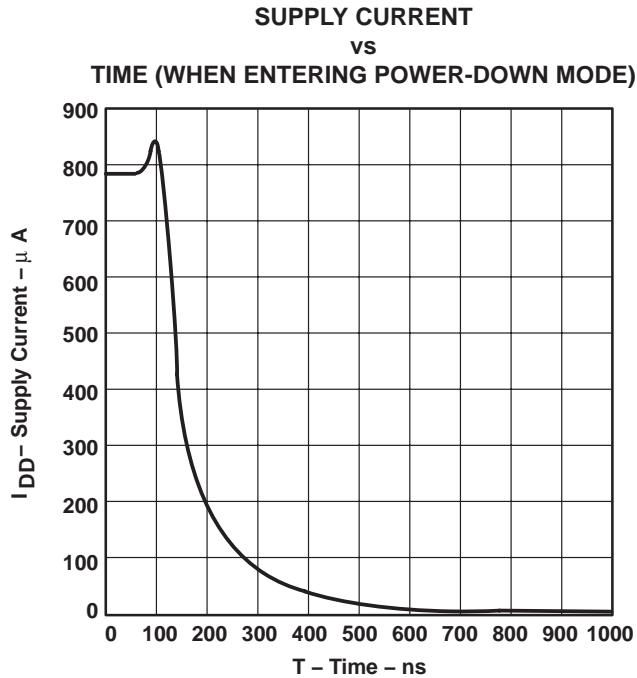
Figure 12

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY ERROR
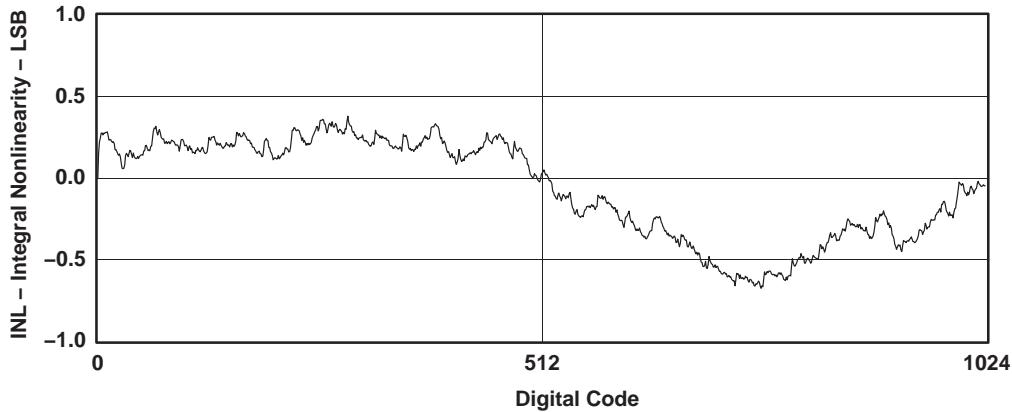
Figure 13

DIFFERENTIAL NONLINEARITY ERROR

Figure 14

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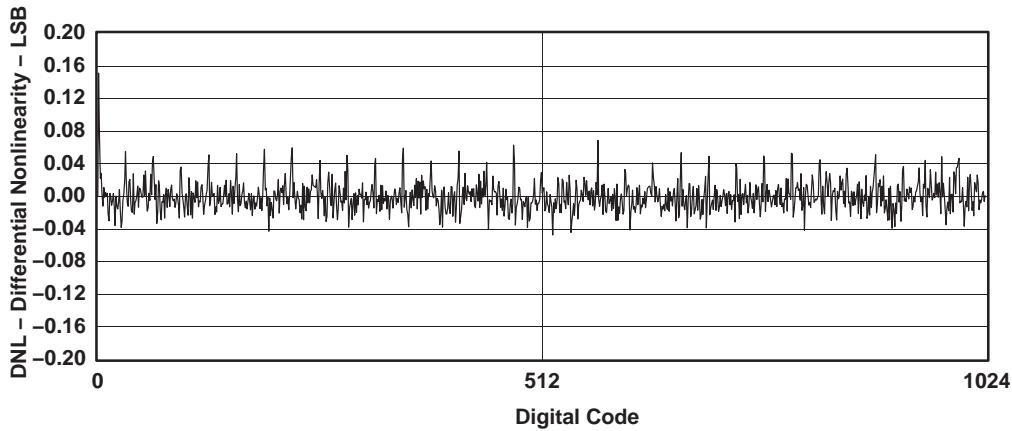
APPLICATION INFORMATION

general function

The TLV5606 is a 10-bit single supply DAC based on a resistor string architecture. The device consists of a serial interface, speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) is given by:

$$2\ \text{REF}\ \frac{\text{CODE}}{2^n}\ [\text{V}]$$

where REF is the reference voltage and CODE is the digital input value within the range of 0_{10} to 2^{n-1}, where n = 10 (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data format* section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

Explanation of data transfer: First, the device has to be enabled with $\overline{\text{CS}}$ set to low. Then, a falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or FS rises, the content of the shift register is moved to the DAC latch which updates the voltage output to the new level.

The serial interface of the TLV5606 can be used in two basic modes:

- Four wire (with chip select)
- Three wire (without chip select)

Using chip select (four wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). The interface is compatible with the TMS320 family. Figure 15 shows an example with two TLV5606s connected directly to a TMS320 DSP.
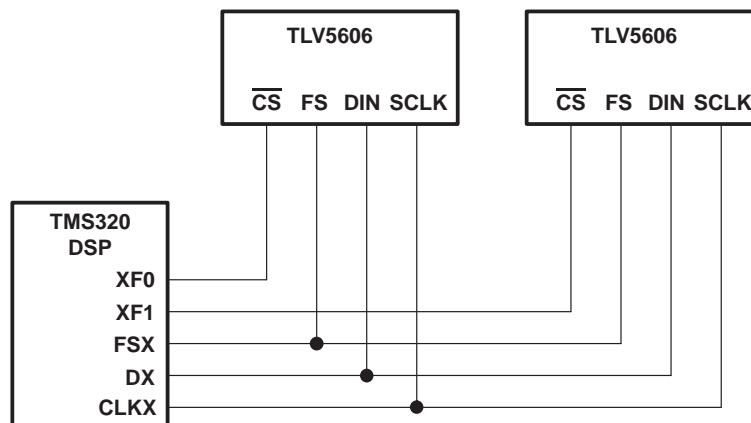

Figure 15. TMS320 Interface

APPLICATION INFORMATION

serial interface (continued)

If there is no need to have more than one device on the serial bus, then $\overline{\text{CS}}$ can be tied low. Figure 16 shows an example of how to connect the TLV5606 to a TMS320, SPI, or Microwire port using only three pins.

TMS320 DSP		TLV5606
FSX		FS
DX		DIN
CLKX		SCLK
		$\overline{\text{CS}}$

SPI		TLV5606
SS		FS
MOSI		DIN
SCLK		SCLK
		$\overline{\text{CS}}$

Microwire		TLV5606
I/O		FS
SO		DIN
SK		SCLK
		$\overline{\text{CS}}$
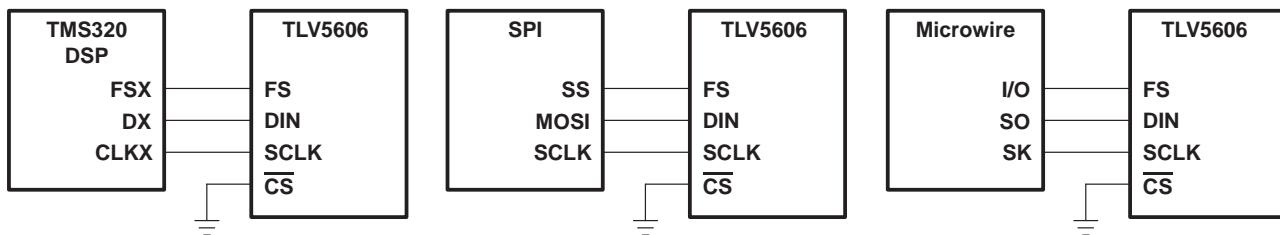
Figure 16. Three-Wire Interface

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to FS. If the word width is 8 bits (SPI and Microwire), two write operations must be performed to program the TLV5606. After the write operation(s), the DAC output is updated automatically on the next positive clock edge following the sixteenth falling clock edge.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{SCLKmax} = \frac{1}{t_{wH(min)} + t_{wL(min)}} = 20 \text{ MHz}$$

The maximum update rate is:

$$f_{UPDATEmax} = \frac{1}{16\left(t_{wH(min)} + t_{wL(min)}\right)} = 1.25 \text{ MHz}$$

The maximum update rate is a theoretical value for the serial interface, since the settling time of the TLV5606 has to be considered also.

data format

The 16-bit data word for the TLV5606 consists of two parts:

• Control bits   (D15 . . . D12)

• New DAC value   (D11 . . . D2)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	SPD	PWR	X	New DAC value (10 bits)										0	0

X: don't care
SPD: Speed control bit. $1 \rightarrow$ fast mode $0 \rightarrow$ slow mode
PWR: Power control bit. $1 \rightarrow$ power down $0 \rightarrow$ normal operation

In power-down mode, all amplifiers within the TLV5606 are disabled.

![Texas Instruments logo]

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APPLICATION INFORMATION

TLV5606 interfaced to TMS320C203 DSP

hardware interfacing

Figure 17 shows an example how to connect the TLV5606 to a TMS320C203 DSP. The serial interface of the TLV5606 is ideally suited to this configuration, using a maximum of four wires to make the necessary connections. In applications where only one synchronous serial peripheral is used, the interface can be simplified even further by pulling $\overline{CS}$ low all the time as shown in the figure.
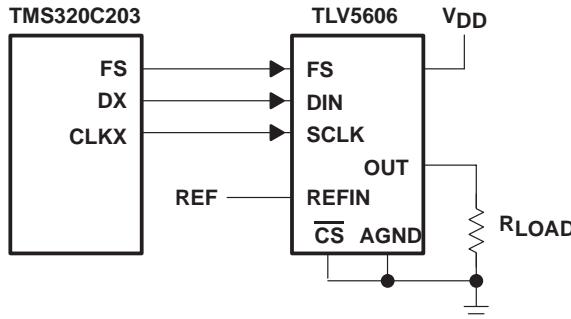

Figure 17. TLV5606 to DSP Interface

software

No setup procedure is needed to access the TLV5606. The output voltage can be set using just a single command.

```
out    data_addr, SDTR
```

where data_addr points to an address location holding the control bits and the 12 data bits providing the output voltage data. SDTR is the address of the transmit FIFO of the synchronous serial port.

The following code shows how to use the timer of the TMS320C203 as a time base to generate a voltage ramp with the TLV5606.

A timer interrupt is generated every 205 µs. The corresponding interrupt service routine increments the output code (stored at 0x0064) for the DAC, adds the DAC control bits to the four most significant bits, and writes the new code to the TLV5606. The resulting period of the saw waveform is:

$$\pi = 4096 \times 205 \text{ E-6 s} = 0.84 \text{ s}$$

```
;*******************************************************************************
;* Title   : Ramp generation with TLV5606                                      *
;* Version : 1.0                                                               *
;* DSP     : TI TMS320C203                                                     *
;* © (1998) Texas Instruments Incorporated                                     *
;*******************************************************************************

;----------- I/O and memory mapped regs ------------
       .include "regs.asm"
;----------- vectors -----------------------------
       .ps       0h
       b         start
       b         INT1
       b         INT23
       b         TIM_ISR
```

APPLICATION INFORMATION

```
;*******************************************************************************
;* Main Program
;*******************************************************************************
        .ps     1000h
        .entry
start:
; disable interrupts
        setc    INTM        ; disable maskable interrupts
        splk    #0ffffh, IFR
        splk    #0004h, IMR

; set up the timer to interrupt ever 205uS
        splk    #0000h, 60h
        splk    #00FFh, 61h
        out     61h, PRD
        out     60h, TIM
        splk    #0c2fh, 62h
        out     62h, TCR
; Configure SSP to use internal clock, internal frame sync and burst mode
        splk    #0CC0Eh, 63h
        out     63h, SSPCR
        splk    #0CC3Eh, 63h
        out     63h, SSPCR

        splk    #0000h, 64h ; set initial DAC value

; enable interrupts
        clrc    INTM        ; enable maskable interrupts

; loop forever!
next:   idle                ;wait for interrupt
        b       next

; all else fails stop here
done:   b       done        ;hang there

;*******************************************************************************
;* Interrupt Service Routines
;*******************************************************************************
INT1:   ret                 ;do nothing and return

INT23:  ret                 ;do nothing and return

TIM_ISR:
        lacl    64h         ; restore counter value to ACC
        add     #4h         ; increment DAC value
        and     #0FFCh      ; mask 4 MSBs
        sacl    64h         ; store 12 bit counter value
        or      #4000h      ; set DAC control bits
        sacl    65h         ; store DAC value
        out     65h, SDTR   ; send data

        clrc    intm        ; re-enable interrupts
        ret
        .END
```

APPLICATION INFORMATION

TLV5606 interfaced to MCS51® microcontroller

hardware interfacing

Figure 18 shows an example of how to connect the TLV5606 to an MCS51® compatible microcontroller. The serial DAC input data and external control signals are sent via I/O port 3 of the controller. The serial data is sent on the RxD line, with the serial clock output on the TxD line. P3.4 and P3.5 are configured as outputs to provide the chip select and frame sync signals for the TLV5606.
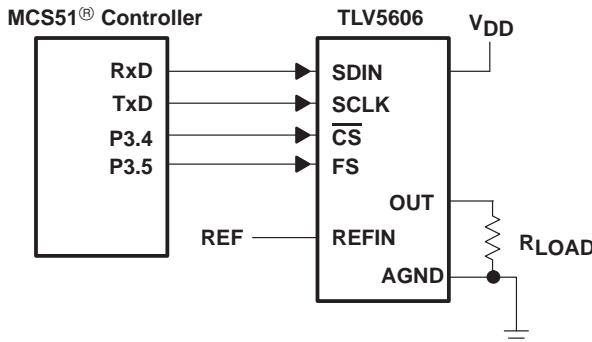

Figure 18. TLV5606 to MCS51® Controller Interface

software

The example program puts out a sine wave on the OUT pin.

The on-chip timer is used to generate interrupts at a fixed frequency. The related interrupt service routine fetches and writes the next sample to the DAC. The samples are stored in a lookup table, which describes one full period of a sine wave.

The serial port of the controller is used in mode 0, which transmits 8 bits of data on RxD, accompanied by a synchronous clock on TxD. Two writes concatenated together are required to write a complete word to the TLV5606. The CS and FS signals are provided in the required fashion through control of I/O port 3, which has bit addressable outputs.

```
;********************************************************************************
;* Title   : Ramp generation with TLV5606                                      *
;* Version : 1.0                                                               *
;* MCU     : INTEL MCS51®                                                       *
;* © (1998) Texas Instruments Incorporated                                     *
;********************************************************************************

;-------------------------------------------------------------------------------
; Program function declaration
;-------------------------------------------------------------------------------

NAME    GENSINE

MAIN    SEGMENT    CODE
ISR     SEGMENT    CODE
SINTBL  SEGMENT    CODE
VAR1    SEGMENT    DATA
STACK   SEGMENT    IDATA

;-------------------------------------------------------------------------------
; Code start at address 0, jump to start
;-------------------------------------------------------------------------------

    CSEG AT  0
```

MCS is a registered trademark of Intel Corporation

APPLICATION INFORMATION

```
        LJMP        start      ; Execution starts at address 0 on power-up.
;-------------------------------------------------------------------------
; Code in the timer0 interrupt vector
;-------------------------------------------------------------------------
    CSEG AT  0BH

    LJMP        timer0isr ; Jump vector for timer 0 interrupt is 000Bh

;-------------------------------------------------------------------------
; Define program variables
;-------------------------------------------------------------------------
    RSEG        VAR1

rolling_ptr: DS 1
;-------------------------------------------------------------------------
; Interrupt service routine for timer 0 interrupts
;-------------------------------------------------------------------------
    RSEG        ISR

timer0isr:

    PUSH        PSW
    PUSH        ACC

    CLR         T0              ; set CSB low
    CLR         T1              ; set FS low

    ; The signal to be output on the dac is a sine function. One cycle of a sine wave is
    ; held in a table @ sinevals as 32 samples of msb, lsb pairs (64 bytes). The pointer,
    ; rolling_ptr, rolls round the table of samples incrementing by 2 bytes (1 sample) on
    ; each interrupt (at the end of this routine).

    MOV         DPTR,#sinevals  ; set DPTR to the start of the table of sine signal values
    MOV         A,rolling_ptr   ; ACC loaded with the pointer into the sine table

    MOVC        A,@A+DPTR       ; get msb from the table
    ORL         A, #00H         ; set control bits
    MOV         SBUF,A          ; send out msb of data word

    MOV A,rolling_ptr ; move rolling pointer in to ACC
    INC         A               ; increment ACC holding the rolling pointer
    MOVC        A,@A+DPTR       ; which is the lsb of this sample, now in ACC
MSB_TX:
    JNB         TI, MSB_TX      ; wait for transmit to complete
    CLR         TI              ; clear for new transmit
    MOV         SBUF,A          ; and send out the lsb

LSB_TX:
    JNB         TI, LSB_TX      ; wait for lsb transmit to complete
    SETB        T1              ; set FS = 1
    CLR         TI              ; clear for new transmit

    MOV    A,rolling_ptr        ; load ACC with rolling pointer
    INC    A                    ; increment the ACC twice, to get next sample
    INC    A
    ANL    A,#03FH              ; wrap back round to 0 if >64
    MOV    rolling_ptr,A        ; move value held in ACC back to the rolling pointer

    SETB   T0                   ; CSB high

    POP    ACC
    POP    PSW

    RETI
;-------------------------------------------------------------------------
; Set up stack
;-------------------------------------------------------------------------
```

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APPLICATION INFORMATION

```
    RSEG    STACK
    DS      10h                 ; 16 Byte Stack!
;----------------------------------------------------------------------------
; Main Program
;----------------------------------------------------------------------------
    RSEG    MAIN

start:
    MOV     SP,#STACK-1  ; first set Stack Pointer

    CLR     A
    MOV     SCON,A          ; set serial port 0 to mode 0
    MOV     TMOD,#02H       ; set timer 0 to mode 2 - auto-reload
    MOV     TH0,#0C8H       ; set TH0 for 16.67 kHs interrupts
    SETB    T1              ; set FS = 1
    SETB    T0              ; set CSB = 1

    SETB    ET0             ; enable timer 0 interrupts
    SETB    EA              ; enable all interrupts

    MOV     rolling_ptr,A   ; set rolling pointer to 0
    SETB    TR0             ; start timer 0
always:
    SJMP    always          ; while(1) !
    RET

;----------------------------------------------------------------------------
; Table of 32 sine wave samples used as DAC data
;----------------------------------------------------------------------------
    RSEG    SINTBL
sinevals:
    DW      01000H
    DW      0903CH
    DW      05094H
    DW      0305CH
    DW      0B084H
    DW      070C8H
    DW      0F0E0H
    DW      0F066H
    DW      0F038H
    DW      0F06CH
    DW      0F0E0H
    DW      070C8H
    DW      0B084H
    DW      0305CH
    DW      05094H
    DW      0903CH
    DW      01000H
    DW      06020H
    DW      0A0E8H
    DW      0C060H
    DW      040F8H
    DW      080B4H
    DW      0009CH
    DW      00050H
    DW      00024H
    DW      00050H
    DW      0009CH
    DW      080B4H
    DW      040F8H
    DW      0C060H
    DW      0A0E8H
    DW      06020H
    END
```

APPLICATION INFORMATION

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 19.
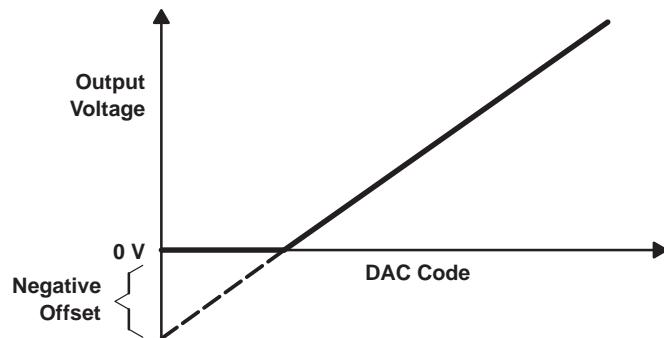

Figure 19. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane, making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1-μF ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 20 shows the ground plane layout and bypassing technique.
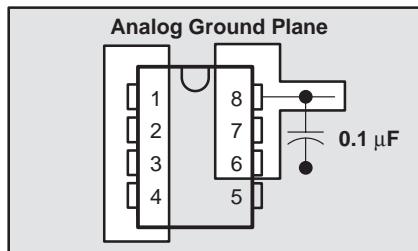
Figure 20. Power-Supply Bypassing

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APPLICATION INFORMATION

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_G)

Gain error is the error in slope of the DAC transfer function.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV5606CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5606C
TLV5606CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5606C
TLV5606CDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AGX
TLV5606CDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AGX
TLV5606CDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AGX
TLV5606CDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AGX
TLV5606CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5606C
TLV5606CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5606C
TLV5606ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5606I
TLV5606ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5606I
TLV5606IDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5606I
TLV5606IDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AGY
TLV5606IDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AGY
TLV5606IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AGY
TLV5606IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AGY
TLV5606IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5606I
TLV5606IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5606I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
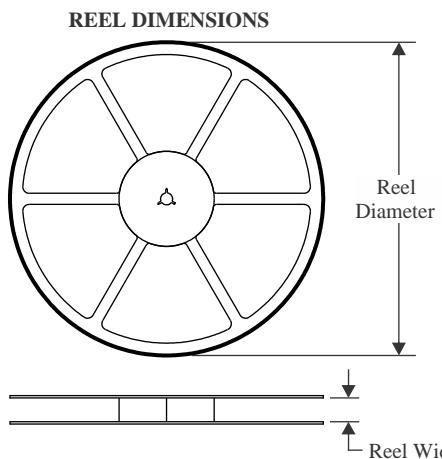
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
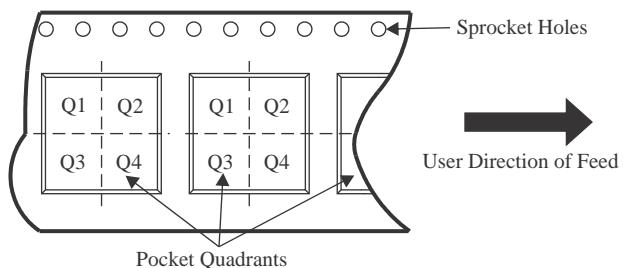
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5606CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV5606CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV5606IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV5606IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
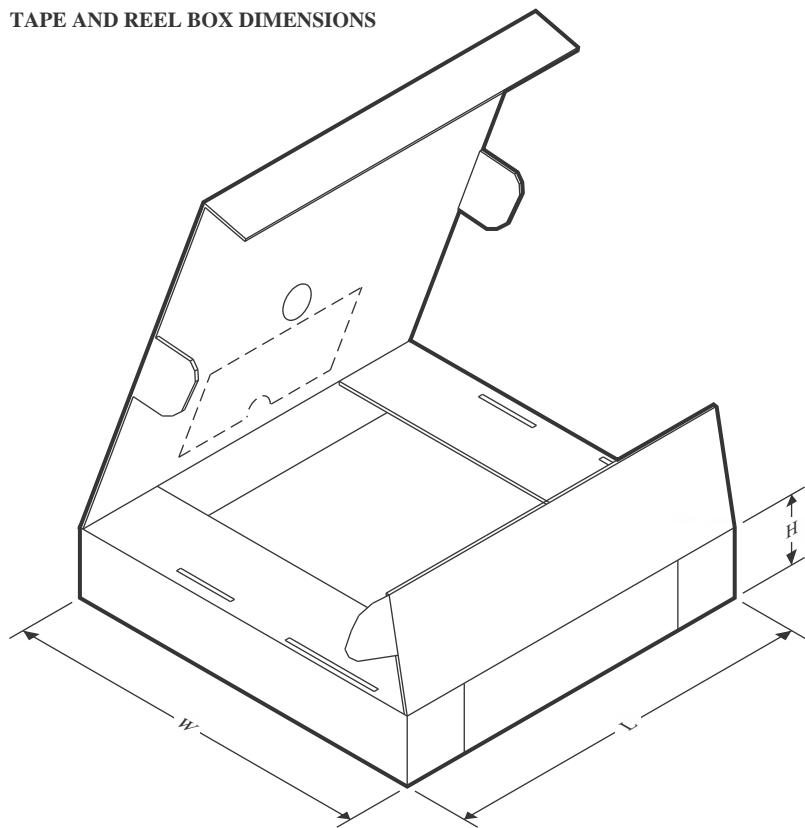
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5606CDGKR	VSSOP	DGK	8	2500	350.0	350.0	43.0
TLV5606CDR	SOIC	D	8	2500	350.0	350.0	43.0
TLV5606IDGKR	VSSOP	DGK	8	2500	350.0	350.0	43.0
TLV5606IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
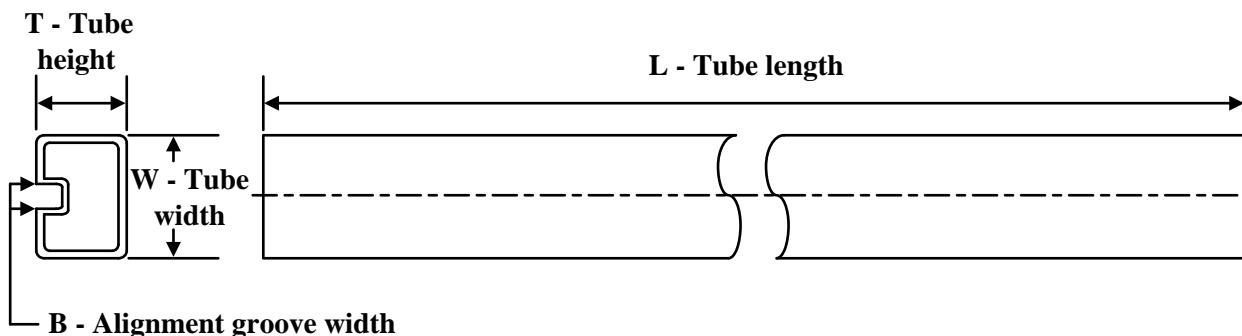
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV5606CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV5606CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLV5606CDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLV5606CDGK.A	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLV5606ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV5606ID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLV5606IDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLV5606IDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLV5606IDGK.A	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
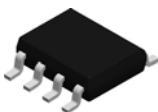
.228-.244   TYP
[5.80-6.19]

PIN 1 ID AREA

A

6X .050
[1.27]

8

2X
.150
[3.81]

.189-.197
[4.81-5.00]
NOTE 3

1

4

5

B

.150-.157
[3.81-3.98]
NOTE 4

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25]Ⓜ C A B

C

SEATING PLANE

⌒ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010   TYP
[0.13-0.25]

.010
[0.25]

0°- 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C   02/2019
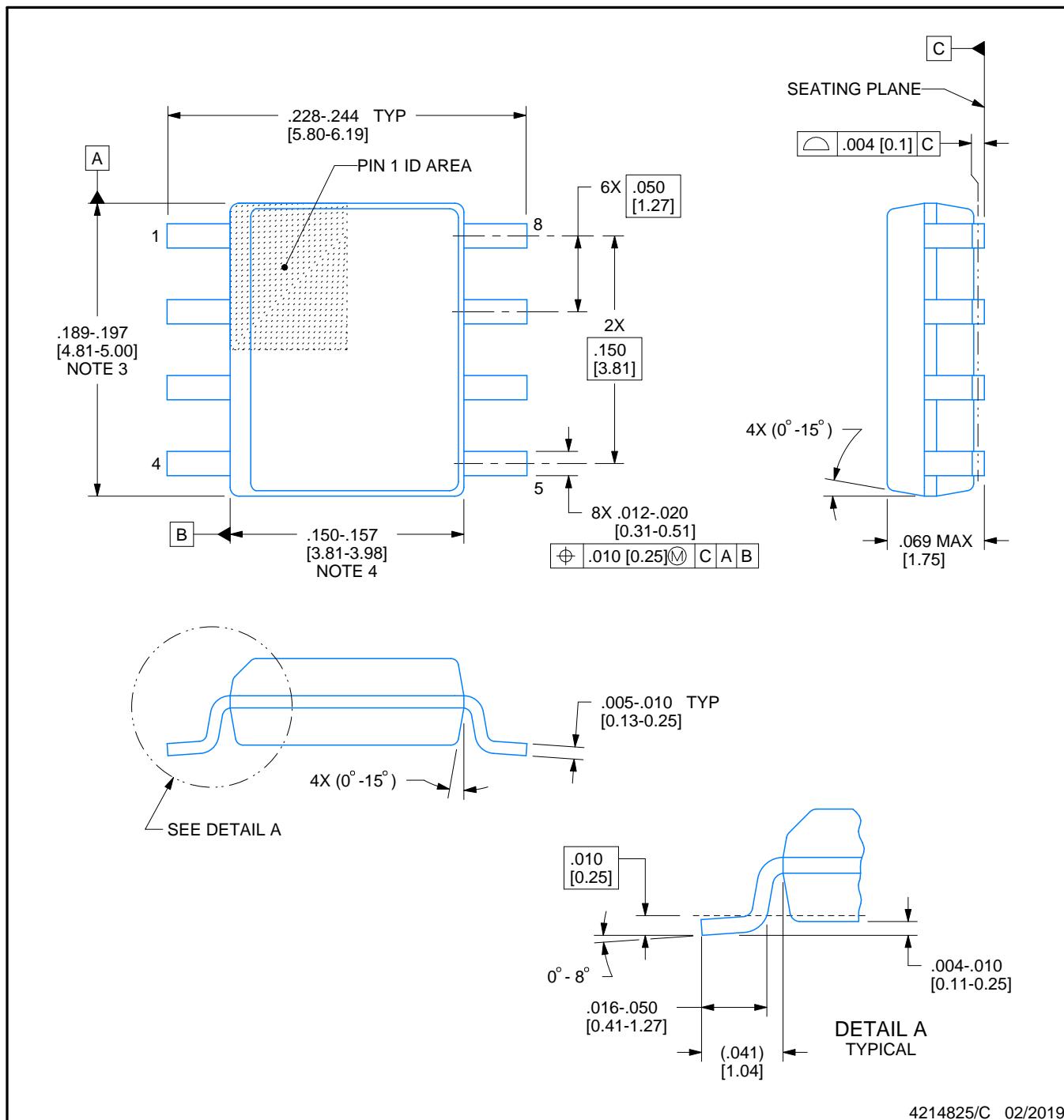
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

SYMM
℄

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM
℄

(R.002) TYP
[0.05]

4

5

6X (.050)
[1.27]

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND
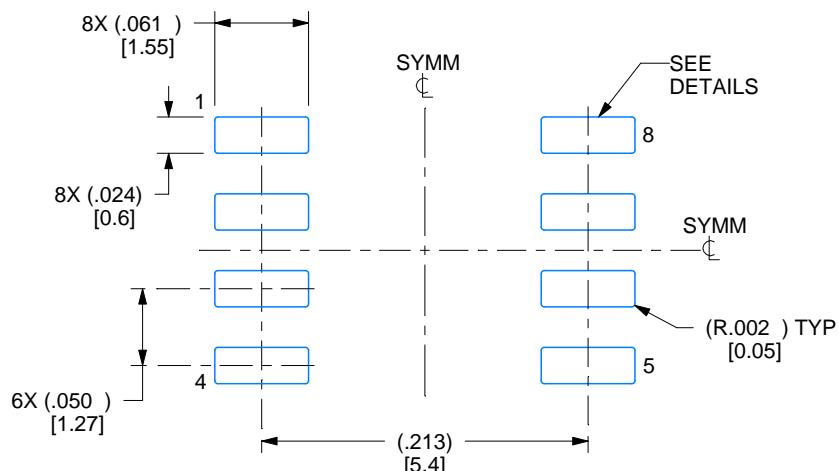
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

SYMM

1

8X (.024)
[0.6]

SYMM

8

(R.002) TYP
[0.05]

6X (.050)
[1.27]

4

5

(.213)
[5.4]
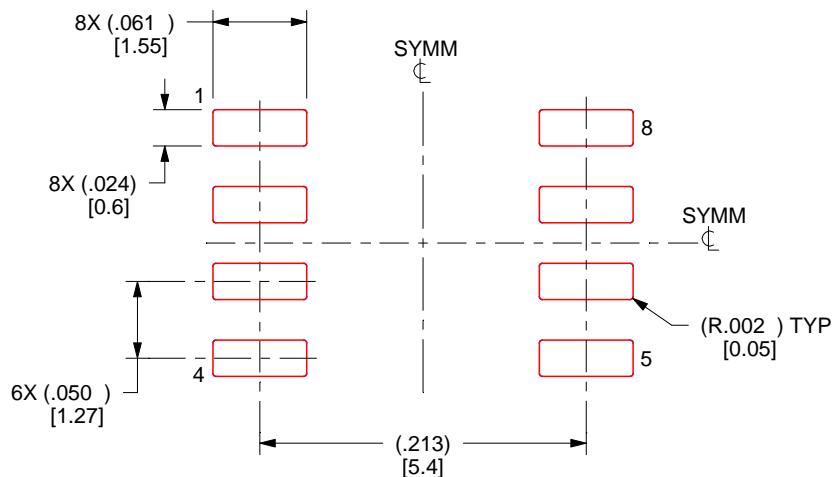
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

A

5.05 / 4.75 TYP

PIN 1 INDEX AREA

8

6X 0.65

2X

1.95

1

3.1 / 2.9
NOTE 3

4

5

8X 0.38 / 0.25

⊕ 0.13 Ⓜ C A B

B

3.1 / 2.9
NOTE 4

C

⌒ 0.1 C

SEATING PLANE

SEE DETAIL A

0.23 / 0.13

0.25
GAGE PLANE

1.1 MAX

0° -8°

0.7 / 0.4

0.15 / 0.05

DETAIL A
TYPICAL

4214862/A   04/2023
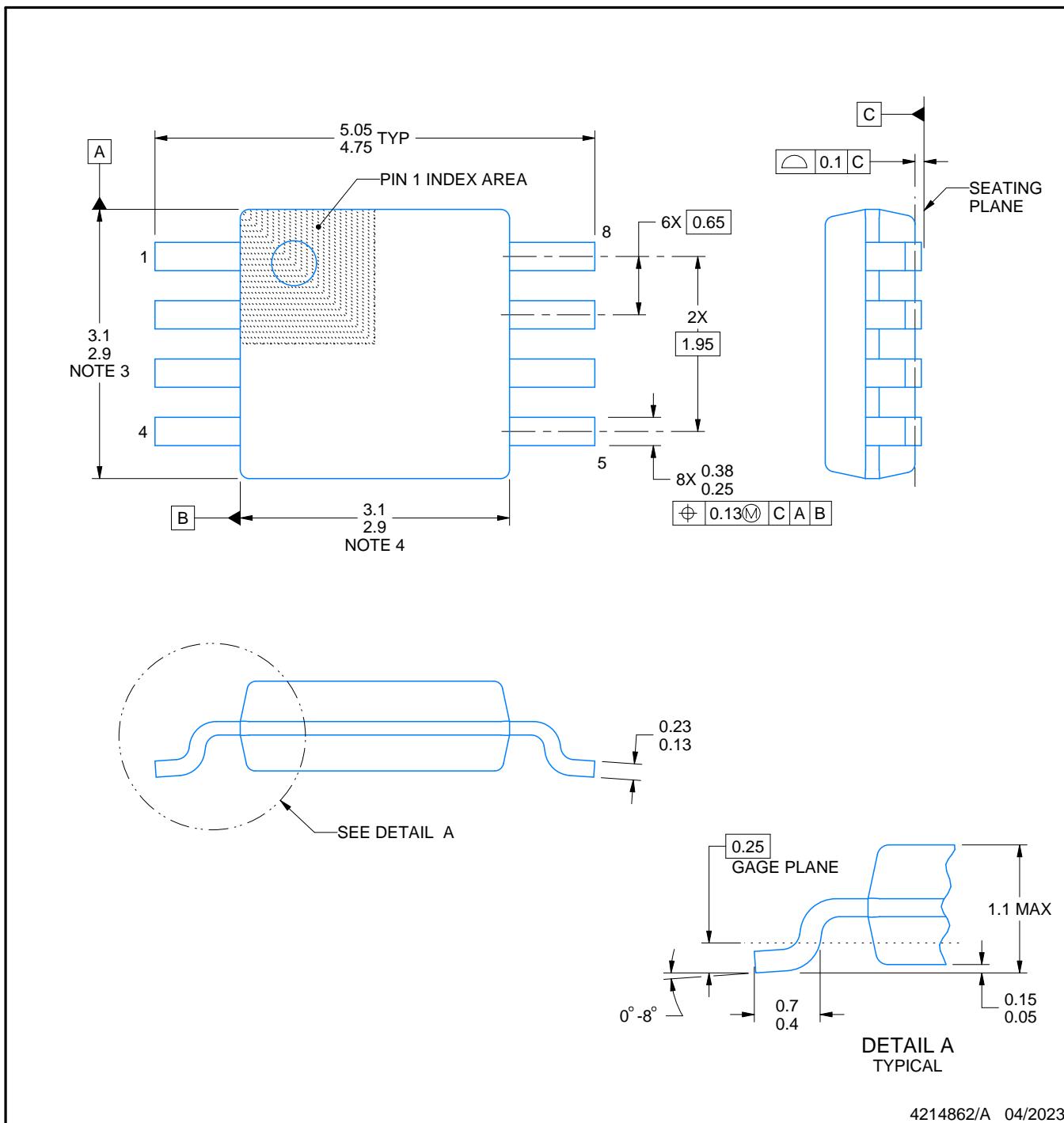
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

SYMM

8X (1.4)

(R0.05) TYP

8X (0.45) 1   8

SYMM

6X (0.65)

4   5

SEE DETAILS

(4.4)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

SOLDER MASK
OPENING   METAL   METAL UNDER   SOLDER MASK
                             SOLDER MASK   OPENING

EXPOSED METAL   EXPOSED METAL

0.05 MAX   0.05 MIN
ALL AROUND   ALL AROUND

NON-SOLDER MASK   SOLDER MASK
DEFINED   DEFINED
(PREFERRED)   SOLDER MASK DETAILS
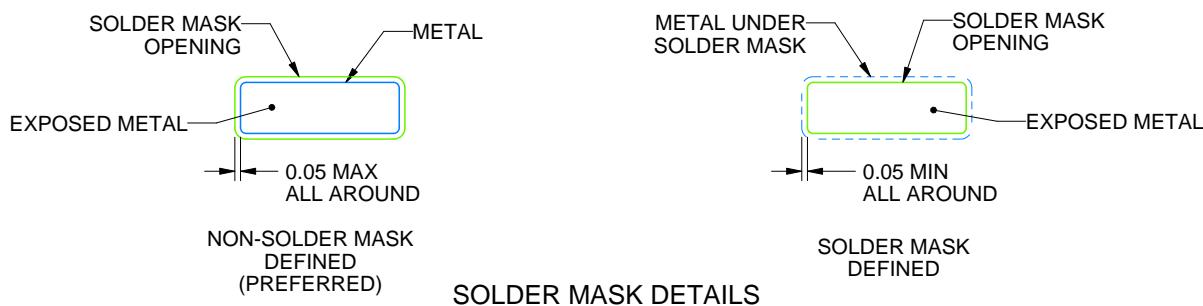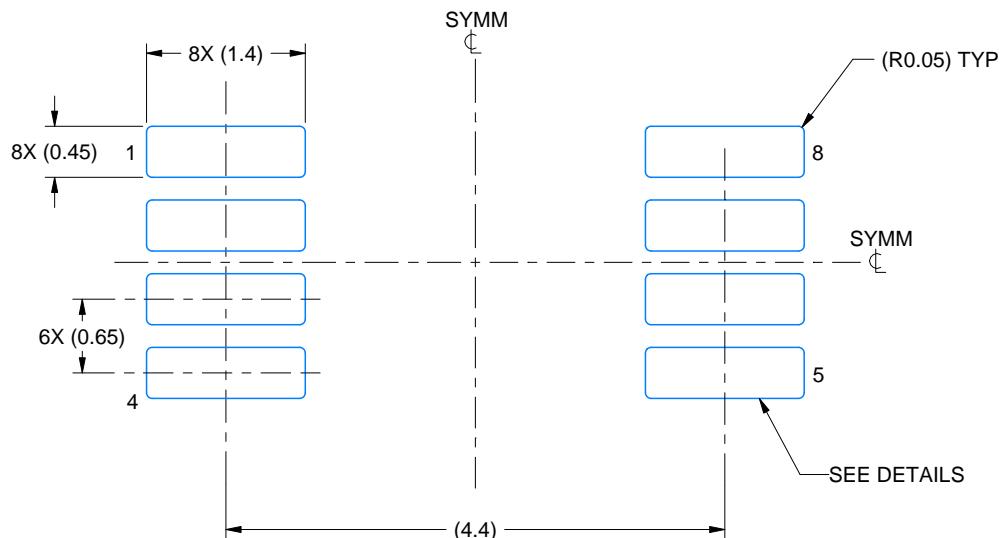
4214862/A   04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
   on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

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SYMM

8X (1.4)

8X (0.45)   1

(R0.05) TYP

8

SYMM

6X (0.65)

4

5

(4.4)
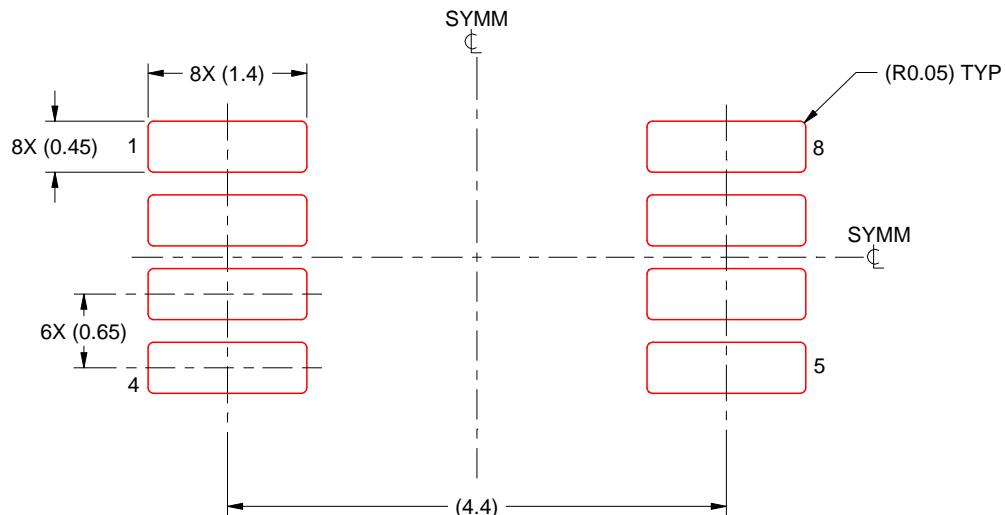
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A   04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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