

## Features

- Very high speed: 45 ns
- Wide voltage range: 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 7  $\mu$ A
- Ultra low active power
  - Typical active current: 2 mA at  $f = 1$  MHz
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) Type II package

## Functional Description

The CY62146E is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down

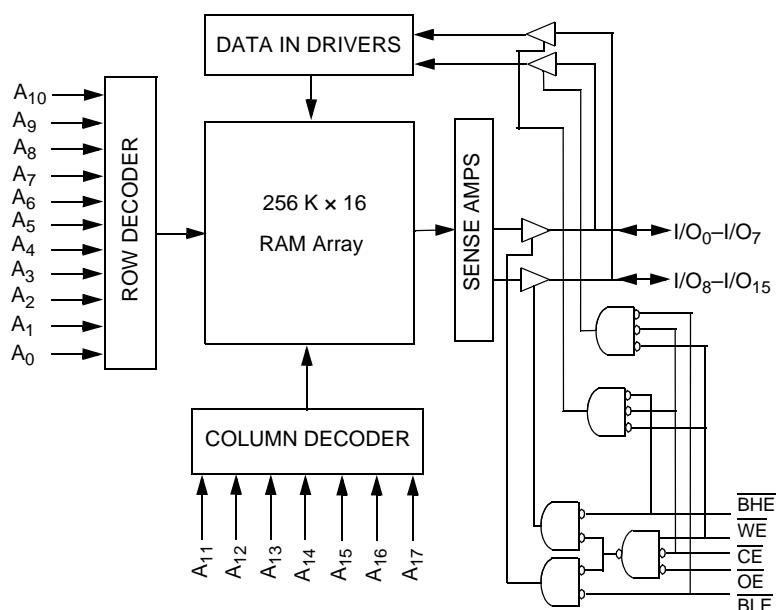
feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ( $CE$  HIGH). The input and output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when the device is deselected ( $CE$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $BHE$ ,  $BLE$  HIGH) or during a write operation ( $CE$  LOW and  $WE$  LOW).

To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $WE$ ) inputs LOW. If Byte Low Enable ( $BLE$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ). If Byte High Enable ( $BHE$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $OE$ ) LOW while forcing the Write Enable ( $WE$ ) HIGH. If Byte Low Enable ( $BLE$ ) is LOW, then data from the memory location specified by the address pins appears on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $BHE$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See [Truth Table on page 11](#) for a complete description of read and write modes.

The CY62146E device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

## Logic Block Diagram

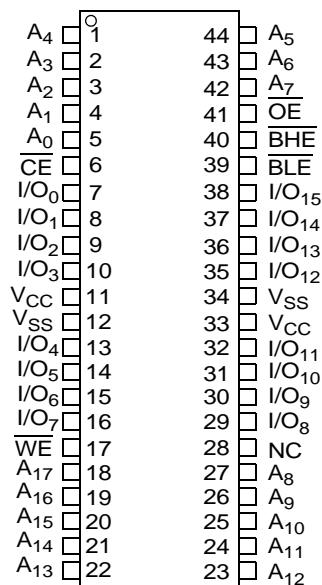


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## Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View) <sup>[1]</sup>



## Product Portfolio

| Product    | Range                     | V <sub>CC</sub> Range (V) |                    |     | Speed (ns) | Power Dissipation                |     |                      |    |                                |     |
|------------|---------------------------|---------------------------|--------------------|-----|------------|----------------------------------|-----|----------------------|----|--------------------------------|-----|
|            |                           |                           |                    |     |            | Operating I <sub>CC</sub> , (mA) |     |                      |    | Standby, I <sub>SB2</sub> (µA) |     |
|            |                           | Min                       | Typ <sup>[2]</sup> | Max |            | f = 1 MHz                        |     | f = f <sub>max</sub> |    | Typ <sup>[2]</sup>             | Max |
| CY62146ELL | Industrial / Automotive-A | 4.5                       | 5.0                | 5.5 | 45         | 2                                | 2.5 | 15                   | 20 | 1                              | 7   |

### Notes

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(typ), T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient temperature with power applied .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Supply voltage to ground potential .....  $-0.5\text{ V}$  to  $6.0\text{ V}$

DC voltage applied to outputs in high Z state<sup>[3, 4]</sup> .....  $-0.5\text{ V}$  to  $6.0\text{ V}$

DC input voltage<sup>[3, 4]</sup> .....  $-0.5\text{ V}$  to  $6.0\text{ V}$

Output current into outputs (LOW) .....  $20\text{ mA}$   
 Static discharge voltage (MIL-STD-883, Method 3015) .....  $>2001\text{ V}$   
 Latch-up current .....  $>200\text{ mA}$

## Operating Range

| Device     | Range                     | Ambient Temperature                            | $V_{CC}^{[5]}$                  |
|------------|---------------------------|--|---------------------------------|
| CY62146ELL | Industrial / Automotive-A | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | $4.5\text{ V}$ – $5.5\text{ V}$ |

## Electrical Characteristics

Over the Operating Range

| Parameter       | Description                                   | Test Conditions   |                                       | 45 ns (Industrial/Automotive-A) |    |                    | Unit          |
|-----------------|---|---|---------------------------------------|---------------------------------|----|--------------------|---------------|
|                 |   | Min   | Typ <sup>[6]</sup>                    | Max                             |    |                    |               |
| $V_{OH}$        | Output high voltage                           | $V_{CC} = 4.5\text{ V}$   | $I_{OH} = -1.0\text{ mA}$             | 2.4                             | –  | –                  | V             |
|                 |   | $V_{CC} = 5.5\text{ V}$   | $I_{OH} = -0.1\text{ mA}$             | –                               | –  | 3.4 <sup>[7]</sup> |               |
| $V_{OL}$        | Output low voltage                            | $I_{OL} = 2.1\text{ mA}$  |                                       | –                               | –  | 0.4                | V             |
| $V_{IH}$        | Input high voltage                            | $4.5 \leq V_{CC} \leq 5.5$  |                                       | 2.2                             | –  | $V_{CC} + 0.5$     | V             |
| $V_{IL}$        | Input low voltage                             | $4.5 \leq V_{CC} \leq 5.5$  |                                       | –0.5                            | –  | 0.8                | V             |
| $I_{IX}$        | Input leakage current                         | $GND \leq V_I \leq V_{CC}$  |                                       | –1                              | –  | +1                 | $\mu\text{A}$ |
| $I_{OZ}$        | Output leakage current                        | $GND \leq V_O \leq V_{CC}$ , output disabled  |                                       | –1                              | –  | +1                 | $\mu\text{A}$ |
| $I_{CC}$        | $V_{CC}$ operating supply current             | $f = f_{max} = 1/t_{RC}$  | $V_{CC} = V_{CCmax}$                  | –                               | 15 | 20                 | mA            |
|                 |   | $f = 1\text{ MHz}$  | $I_{OUT} = 0\text{ mA}$ , CMOS levels | –                               | 2  | 2.5                |               |
| $I_{SB2}^{[8]}$ | Automatic CE power down current – CMOS inputs | $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ , $f = 0$ , $V_{CC} = V_{CC(max)}$ |                                       | –                               | 1  | 7                  | $\mu\text{A}$ |

### Notes

3.  $V_{IL}(\text{min}) = -2.0\text{ V}$  for pulse durations less than 20 ns for  $I < 30\text{ mA}$ .
4.  $V_{IH}(\text{max}) = V_{CC} + 0.75\text{ V}$  for pulse durations less than 20 ns.
5. Full Device AC operation assumes a minimum of 100  $\mu\text{s}$  ramp time from 0 to  $V_{CC}$  (min) and 200  $\mu\text{s}$  wait time after  $V_{CC}$  stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(\text{typ})}$ ,  $T_A = 25^{\circ}\text{C}$ .
7. Please note that the maximum  $V_{OH}$  limit does not exceed minimum CMOS  $V_{IH}$  of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum  $V_{IH}$  of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider.
8. Chip enable ( $\overline{CE}$ ) and byte enables (BHE and  $\overline{BLE}$ ) need to be tied to CMOS levels to meet the  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs are left floating.

## Capacitance

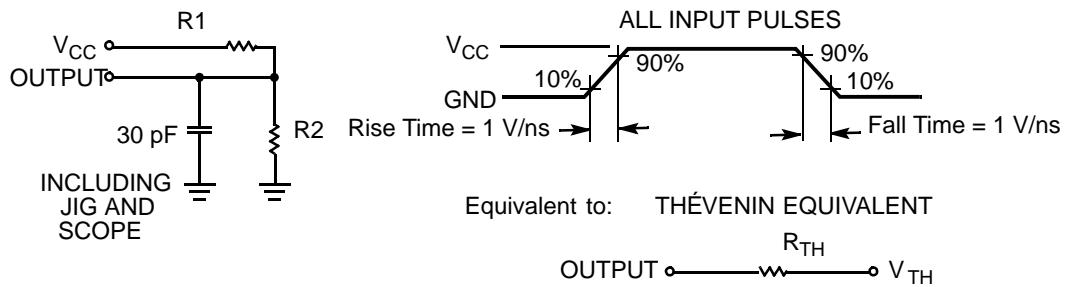
| Parameter [9] | Description        | Test Conditions  | Max | Unit |
|---------------|--------------------|--|-----|------|
| $C_{IN}$      | Input capacitance  | $T_A = 25^\circ C, f = 1 \text{ MHz}, V_{CC} = V_{CC(\text{typ})}$ | 10  | pF   |
| $C_{OUT}$     | Output capacitance |  | 10  | pF   |

## Thermal Resistance

| Parameter [9] | Description                              | Test Conditions  | 44-pin TSOP II | Unit               |
|---------------|--|--|----------------|--------------------|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 x 4.5 inch, two layer printed circuit board | 77             | $^\circ\text{C/W}$ |
| $\Theta_{JC}$ | Thermal resistance (junction to case)    |  | 13             | $^\circ\text{C/W}$ |

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



| Parameters | 5.0 V | Unit     |
|------------|-------|----------|
| R1         | 1800  | $\Omega$ |
| R2         | 990   | $\Omega$ |
| $R_{TH}$   | 639   | $\Omega$ |
| $V_{TH}$   | 1.77  | V        |

**Note**

9. Tested initially after any design or process changes that may affect these parameters.

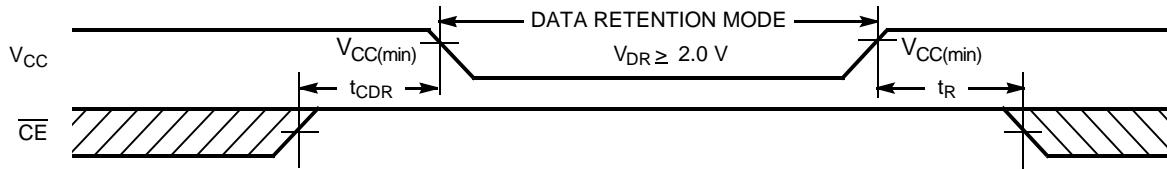
## Data Retention Characteristics

Over the Operating Range

| Parameter       | Description                          | Conditions  | Min | Typ [10] | Max | Unit          |
|-----------------|--------------------------------------|---|-----|----------|-----|---------------|
| $V_{DR}$        | $V_{CC}$ for data retention          |   | 2   | —        | —   | V             |
| $I_{CCDR}$ [11] | Data retention current               | $V_{CC} = 2\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | —   | 1        | 7   | $\mu\text{A}$ |
| $t_{CDR}$ [12]  | Chip deselect to data retention time |   | 0   | —        | —   | ns            |
| $t_R$ [13]      | Operation recovery time              |   | 45  | —        | —   | ns            |

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(\text{typ})}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
11. Chip enable ( $\overline{CE}$ ) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs are left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ .

## Switching Characteristics

Over the Operating Range

| Parameter [14, 15]      | Description                                  | 45 ns (Industrial / Automotive-A) |     | Unit |
|-------------------------|--|-----------------------------------|-----|------|
|                         |  | Min                               | Max |      |
| <b>Read Cycle</b>       |  |                                   |     |      |
| $t_{RC}$                | Read cycle time                              | 45                                | –   | ns   |
| $t_{AA}$                | Address to data valid                        | –                                 | 45  | ns   |
| $t_{OHA}$               | Data hold from address change                | 10                                | –   | ns   |
| $t_{ACE}$               | $\overline{CE}$ LOW to data valid            | –                                 | 45  | ns   |
| $t_{DOE}$               | $\overline{OE}$ LOW to data valid            | –                                 | 22  | ns   |
| $t_{LZOE}$              | $\overline{OE}$ LOW to Low Z [16]            | 5                                 | –   | ns   |
| $t_{HZOE}$              | $\overline{OE}$ HIGH to High Z [16, 17]      | –                                 | 18  | ns   |
| $t_{LZCE}$              | $\overline{CE}$ LOW to Low Z [16]            | 10                                | –   | ns   |
| $t_{HZCE}$              | $\overline{CE}$ HIGH to High Z [16, 17]      | –                                 | 18  | ns   |
| $t_{PU}$                | $\overline{CE}$ LOW to power-up              | 0                                 | –   | ns   |
| $t_{PD}$                | $\overline{CE}$ HIGH to power-down           | –                                 | 45  | ns   |
| $t_{DBE}$               | $\overline{BLE/BHE}$ LOW to data valid       | –                                 | 22  | ns   |
| $t_{LZBE}$              | $\overline{BLE/BHE}$ LOW to Low Z [16]       | 5                                 | –   | ns   |
| $t_{HZBE}$              | $\overline{BLE/BHE}$ HIGH to High Z [16, 17] | –                                 | 18  | ns   |
| <b>Write Cycle [18]</b> |  |                                   |     |      |
| $t_{WC}$                | Write cycle time                             | 45                                | –   | ns   |
| $t_{SCE}$               | $\overline{CE}$ LOW to write end             | 35                                | –   | ns   |
| $t_{AW}$                | Address setup to write end                   | 35                                | –   | ns   |
| $t_{HA}$                | Address hold from write end                  | 0                                 | –   | ns   |
| $t_{SA}$                | Address setup to write start                 | 0                                 | –   | ns   |
| $t_{PWE}$               | $\overline{WE}$ pulse width                  | 35                                | –   | ns   |
| $t_{BW}$                | $\overline{BLE/BHE}$ LOW to write end        | 35                                | –   | ns   |
| $t_{SD}$                | Data setup to write end                      | 25                                | –   | ns   |
| $t_{HD}$                | Data hold from write end                     | 0                                 | –   | ns   |
| $t_{HZWE}$              | $\overline{WE}$ LOW to High Z [16, 17]       | –                                 | 18  | ns   |
| $t_{LZWE}$              | $\overline{WE}$ HIGH to Low Z [16]           | 10                                | –   | ns   |

### Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified  $I_{OL}/I_{OH}$  as shown in [Figure 2 on page 5](#).
15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes [AN13842](#) and [AN66311](#). However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
16. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
17.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
18. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

Figure 4. Read Cycle No.1: Address Transition Controlled [19, 20]

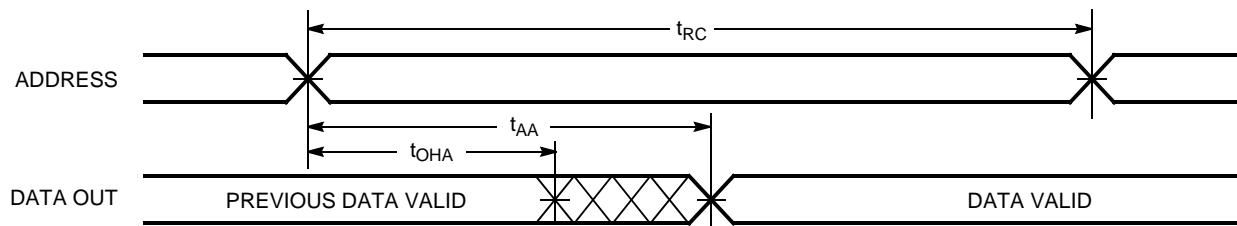
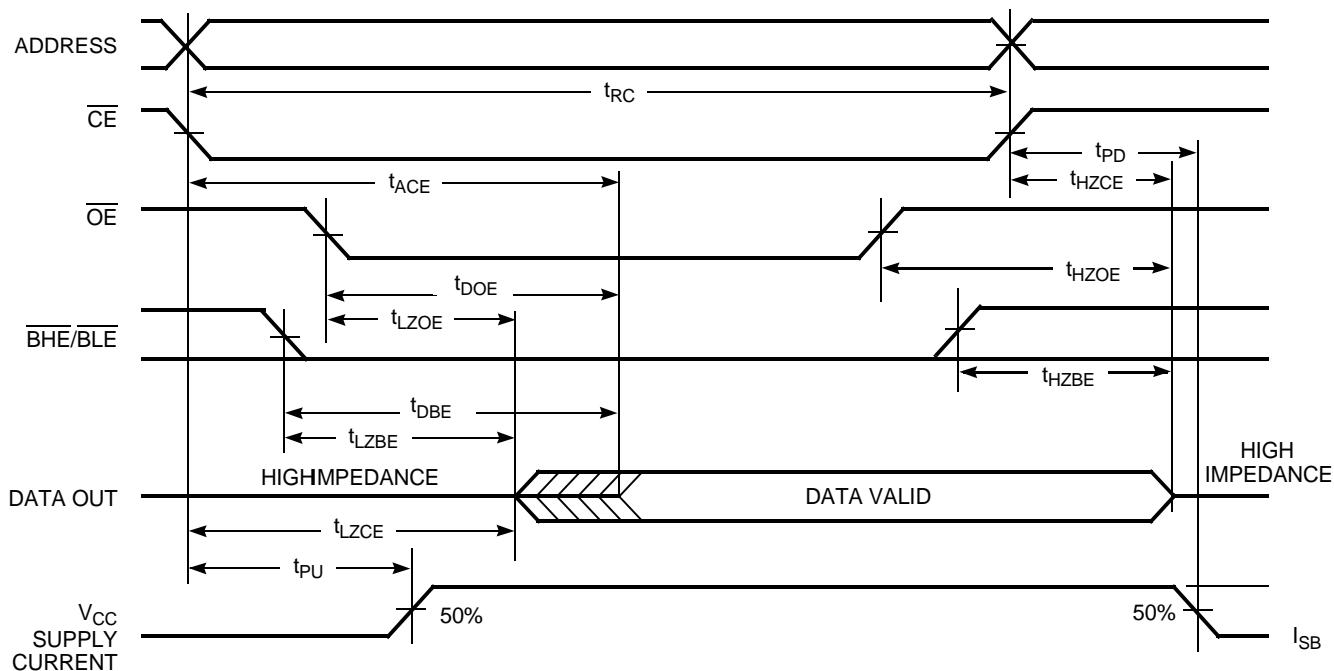


Figure 5. Read Cycle No. 2:  $\overline{OE}$  Controlled [20, 21]

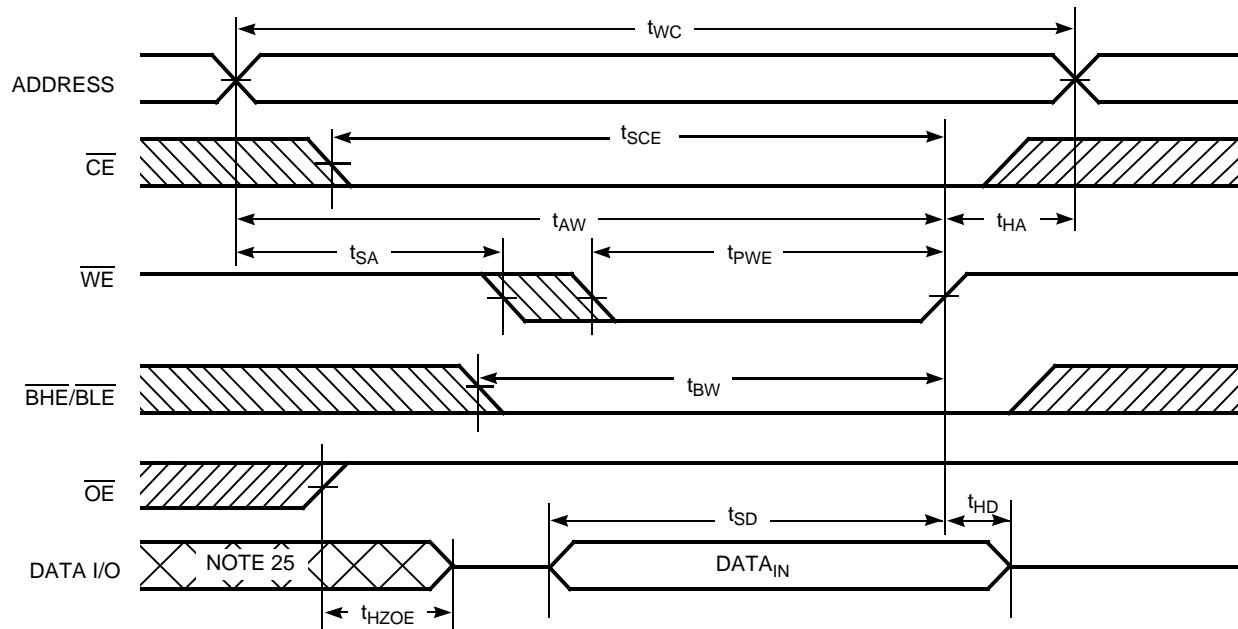


### Notes

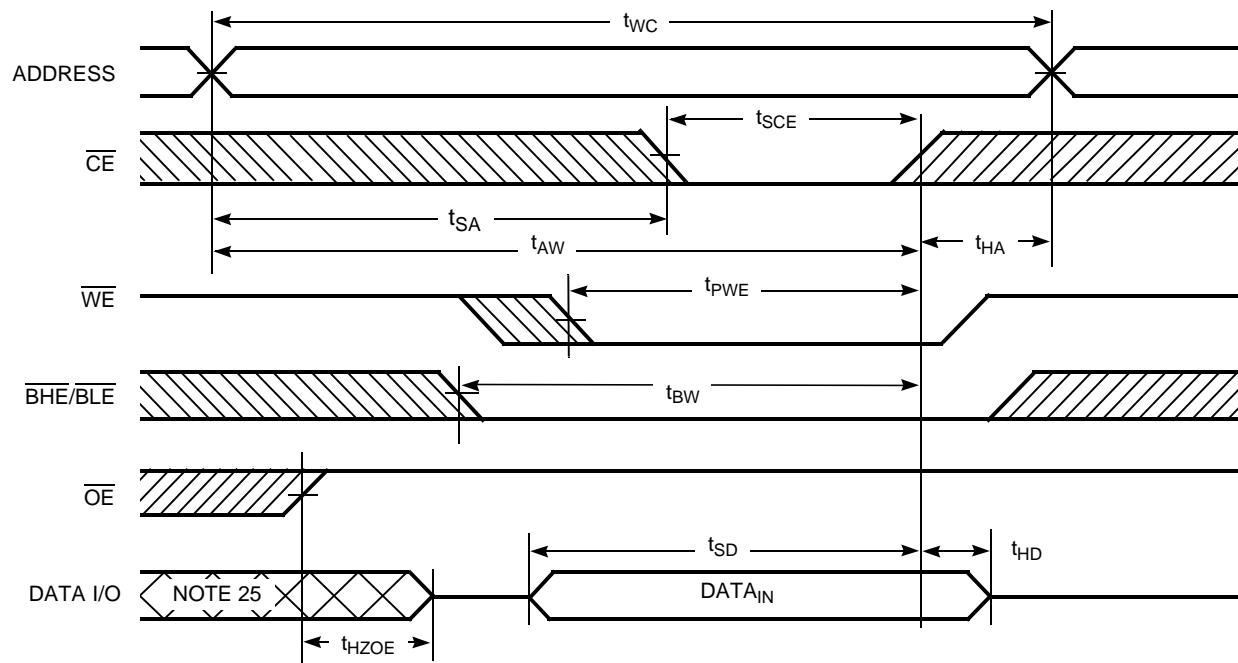
19. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ .
20.  $\overline{WE}$  is HIGH for read cycle.
21. Address valid before or similar to  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

## Switching Waveforms (continued)

**Figure 6. Write Cycle 1:  $\overline{\text{WE}}$  Controlled** [22, 23, 24]



**Figure 7. Write Cycle 2:  $\overline{\text{CE}}$  Controlled** [22, 23, 24]

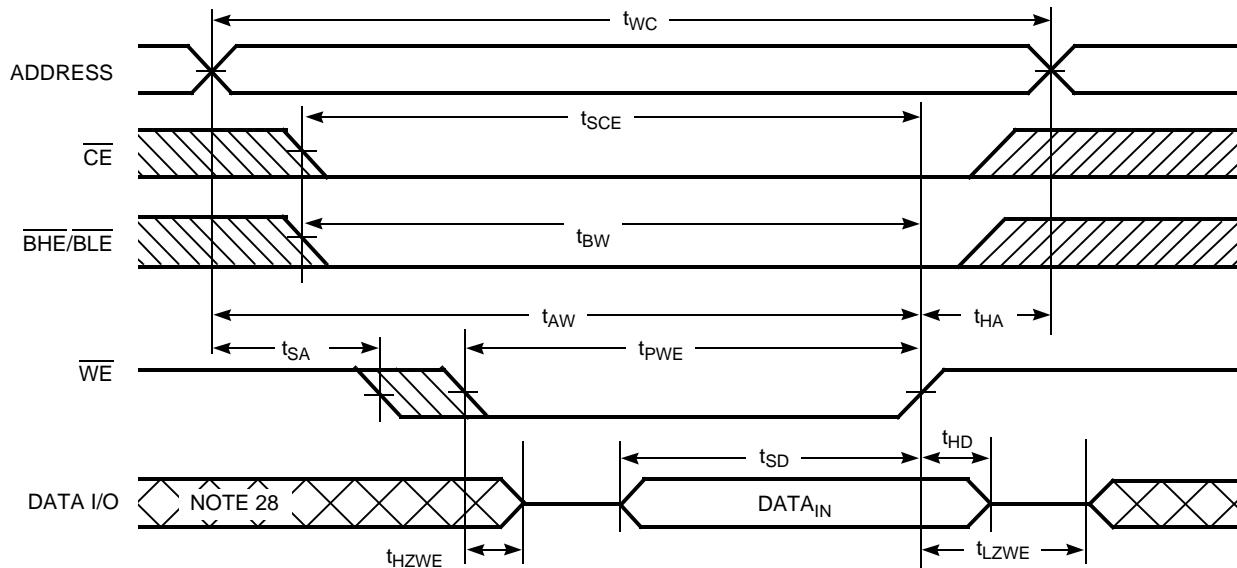


### Notes

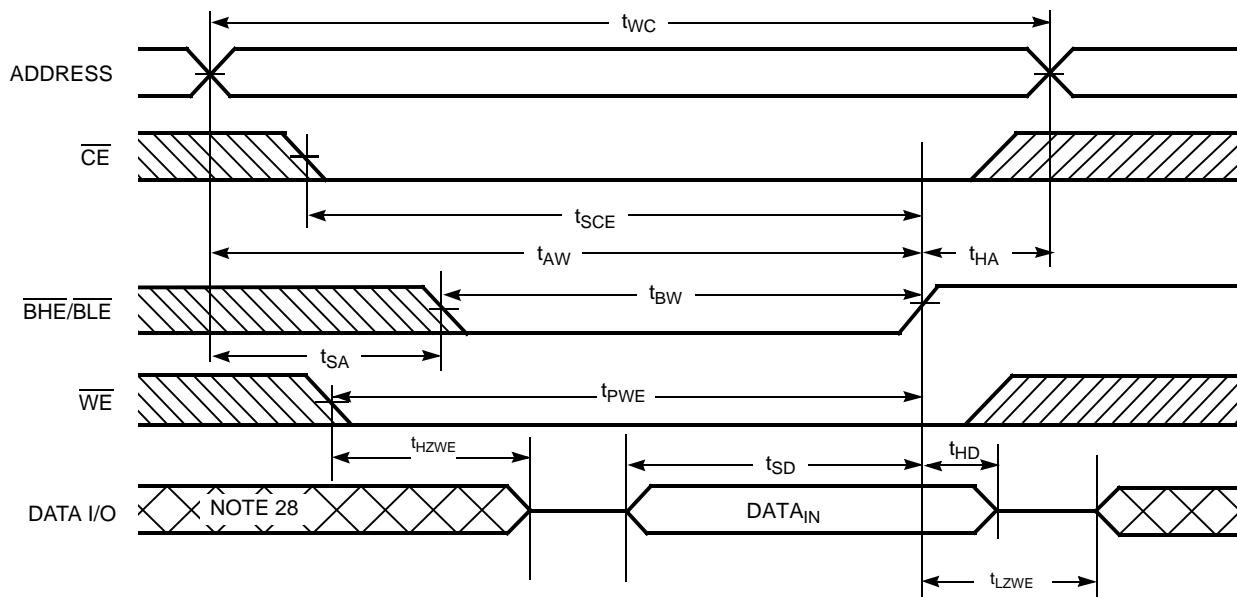
22. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
23. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{IH}$ , the output remains in a high impedance state.
24. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{IL}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate the write by going inactive. The input setup and hold timing must be referenced to the edge of the signal that terminates the write.
25. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 8. Write Cycle 3:  $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW** [26, 27]



**Figure 9. Write Cycle 4:  $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW** [26, 27]



### Notes

26. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high impedance state.

27. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ . All signals must be active to initiate a write and any of these signals can terminate the write by going inactive. The input setup and hold timing must be referenced to the edge of the signal that terminates the write.

28. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

| <b>CE</b> [29] | <b>WE</b> | <b>OE</b> | <b>BHE</b> | <b>BLE</b> | <b>Inputs/Outputs</b>  | <b>Mode</b>         | <b>Power</b>               |
|----------------|-----------|-----------|------------|------------|--|---------------------|----------------------------|
| H              | X         | X         | X [29]     | X [29]     | High Z   | Deselect/power down | Standby (I <sub>SB</sub> ) |
| L              | X         | X         | H          | H          | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L              | H         | L         | L          | L          | Data out (I/O <sub>0</sub> –I/O <sub>15</sub> )  | Read                | Active (I <sub>CC</sub> )  |
| L              | H         | L         | H          | L          | Data out (I/O <sub>0</sub> –I/O <sub>7</sub> );<br>I/O <sub>8</sub> –I/O <sub>15</sub> in High-Z | Read                | Active (I <sub>CC</sub> )  |
| L              | H         | L         | L          | H          | Data out (I/O <sub>8</sub> –I/O <sub>15</sub> );<br>I/O <sub>0</sub> –I/O <sub>7</sub> in High-Z | Read                | Active (I <sub>CC</sub> )  |
| L              | H         | H         | L          | L          | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L              | H         | H         | H          | L          | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L              | H         | H         | L          | H          | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L              | L         | X         | L          | L          | Data in (I/O <sub>0</sub> –I/O <sub>15</sub> )   | Write               | Active (I <sub>CC</sub> )  |
| L              | L         | X         | H          | L          | Data in (I/O <sub>0</sub> –I/O <sub>7</sub> );<br>I/O <sub>8</sub> –I/O <sub>15</sub> in High Z  | Write               | Active (I <sub>CC</sub> )  |
| L              | L         | X         | L          | H          | Data in (I/O <sub>8</sub> –I/O <sub>15</sub> );<br>I/O <sub>0</sub> –I/O <sub>7</sub> in High Z  | Write               | Active (I <sub>CC</sub> )  |

### Note

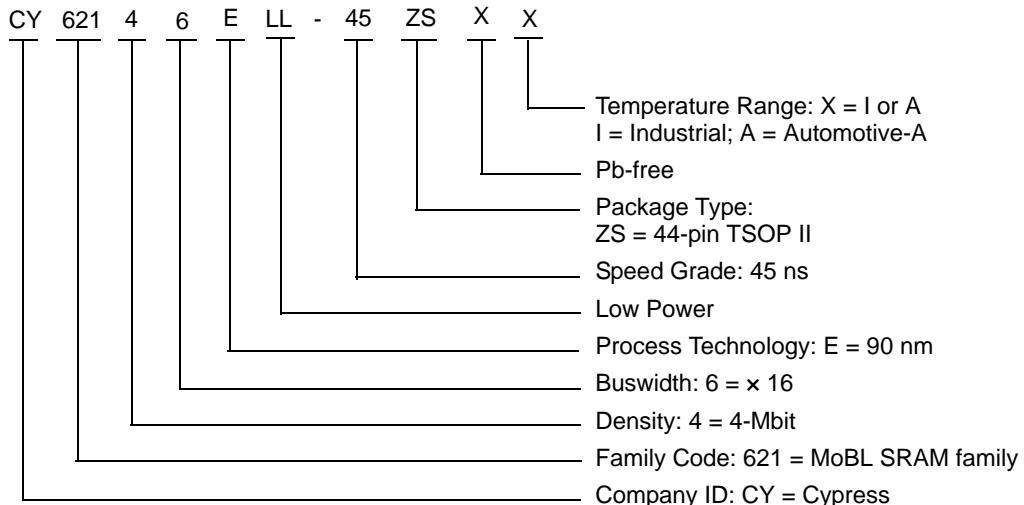
29. Chip enable (**CE**) and byte enables (**BHE** and **BLE**) must be at CMOS levels (not floating) to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Intermediate voltage levels on these pins is not permitted.

## Ordering Information

| Speed<br>(ns) | Ordering Code     | Package<br>Diagram | Package Type             | Operating<br>Range |
|---------------|-------------------|--------------------|--------------------------|--------------------|
| 45            | CY62146ELL-45ZSXI | 51-85087           | 44-pin TSOP II (Pb-free) | Industrial         |
|               | CY62146ELL-45ZSXA | 51-85087           | 44-pin TSOP II (Pb-free) | Automotive-A       |

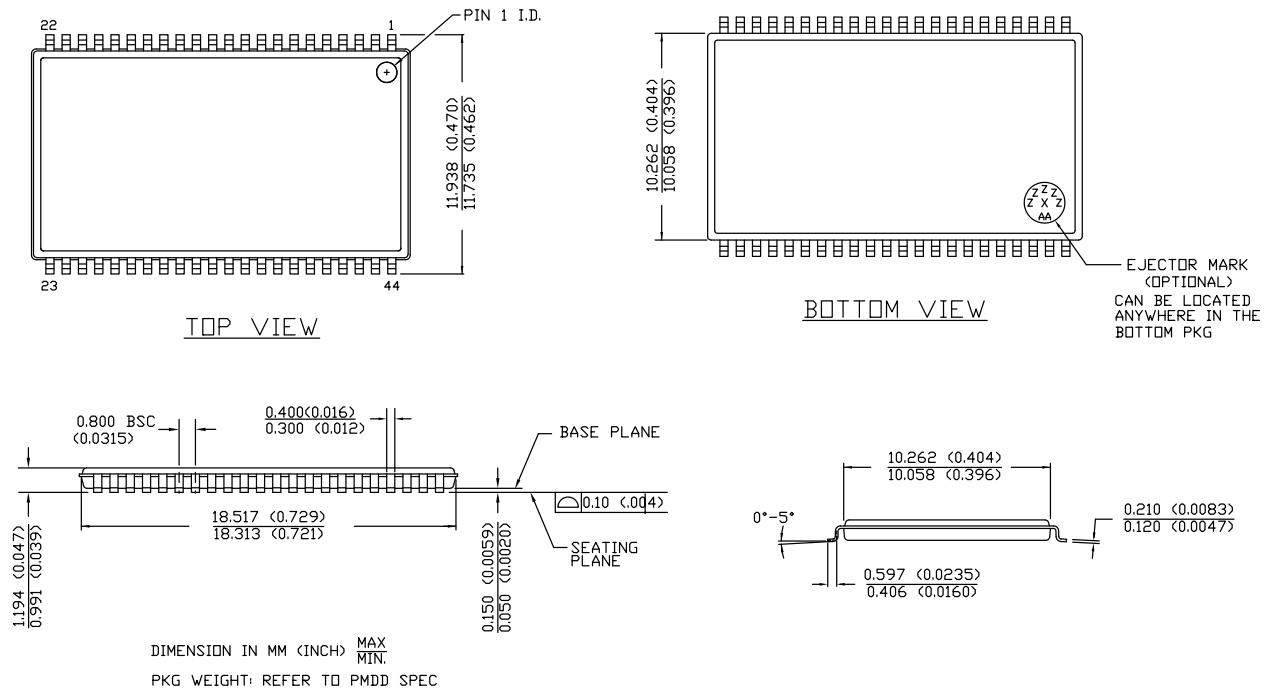
Contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions



## Package Diagram

**Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087**



## Acronyms

| Acronym | Description                             |
|---------|---|
| BHE     | Byte High Enable                        |
| BLE     | Byte Low Enable                         |
| CE      | Chip Enable                             |
| CMOS    | Complementary Metal Oxide Semiconductor |
| I/O     | Input/Output                            |
| OE      | Output Enable                           |
| SRAM    | Static Random Access Memory             |
| TSOP    | Thin Small Outline Package              |
| VFBGA   | Very Fine-Pitch Ball Grid Array         |
| WE      | Write Enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| µA     | microampere     |
| mA     | milliampere     |
| ns     | nanosecond      |
| Ω      | ohm             |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History Page

**Document Title: CY62146E MoBL®, 4-Mbit (256 K × 16) Static RAM**  
**Document Number: 001-07970**

| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change  |
|------|---------|------------|-----------------|--|
| **   | 463213  | See ECN    | NXR             | New data sheet.  |
| *A   | 684343  | See ECN    | VKN             | Added Preliminary Automotive-A Information<br>Updated Ordering Information Table   |
| *B   | 925501  | See ECN    | VKN             | Added footnote #8 related to $I_{SB2}$ and $I_{CCDR}$<br>Added footnote #13 related AC timing parameters   |
| *C   | 1045260 | See ECN    | VKN             | Converted Automotive-A specs from preliminary to final   |
| *D   | 2073548 | See ECN    | VKN / AESA      | Corrected typo in the Data Retention Waveform and removed its irrelevant footnote  |
| *E   | 2943752 | 06/03/2010 | VKN             | Added <a href="#">Contents</a><br>Added footnote related to chip enable in <a href="#">Truth Table</a><br>Updated <a href="#">Package Diagram</a><br>Added <a href="#">Sales, Solutions, and Legal Information</a>   |
| *F   | 3109050 | 12/13/2010 | PRAS            | Changed Table Footnotes to Footnotes.<br>Added Ordering Code Definitions.  |
| *G   | 3149059 | 01/20/2011 | RAME            | Updated as per latest template<br>Corrected Errors in Ordering Code Definitions<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .   |
| *H   | 3296704 | 06/29/11   | RAME            | Removed reference to AN1064 SRAM system guidelines   |
| *I   | 3921993 | 03/05/2013 | MEMJ            | Updated <a href="#">Switching Waveforms</a> :<br>Added Note 24 and referred the same note in <a href="#">Figure 6</a> , <a href="#">Figure 7</a> .<br>Removed Note "WE is HIGH for read cycle." and its references in <a href="#">Figure 6</a> , <a href="#">Figure 7</a> .<br>Added Note 27 and referred the same note in <a href="#">Figure 8</a> , <a href="#">Figure 9</a> .<br><br>Updated <a href="#">Package Diagram</a> :<br>spec 51-85087 – Changed revision from *C to *E. |
| *J   | 4013949 | 06/04/2013 | MEMJ            | Updated <a href="#">Functional Description</a> .<br><br>Updated <a href="#">Electrical Characteristics</a> :<br>Added one more Test Condition " $V_{CC} = 5.5$ V, $I_{OH} = -0.1$ mA" for $V_{OH}$ parameter and added maximum value corresponding to that Test Condition.<br>Added Note 7 and referred the same note in maximum value for $V_{OH}$ parameter corresponding to Test Condition " $V_{CC} = 5.5$ V, $I_{OH} = -0.1$ mA".   |
| *K   | 4102022 | 08/14/2013 | VINI            | Updated <a href="#">Switching Characteristics</a> :<br>Updated Note 15.<br><br>Updated in new template.  |

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