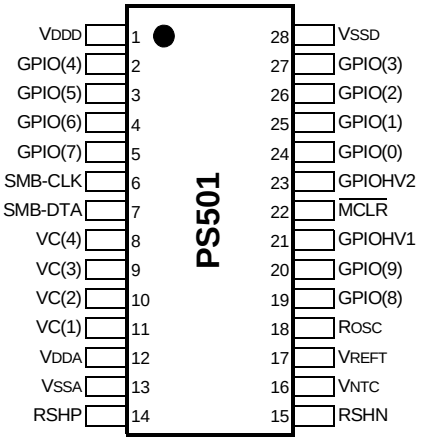
PS501

Single Chip Field Reprogrammable Battery Manager

Features

- Single chip solution for rechargeable battery management
- Footprint compatible with PS401
- SMBus 1.1 and SBData 1.1 compatible
- Precise capacity reporting for Lithium Ion and Lithium Polymer battery chemistries
- Embedded PowerSmart® patented algorithms contained in customizable on-chip 16-Kbyte Flash memory
- User configurable and “learned” parameters stored in on-chip 256 x 8 EEPROM
- Algorithms and parameters fully field reprogrammable via SMBus interface
- Integrating sigma-delta A/D converter with 9 to 16-bit programmable resolution which accurately measures:
  - Current through sense resistor
  - High-voltage (18V) battery cells directly connected to VCELL inputs
  - Temperature measurement from on-chip sensor or optional external thermistor
- Integrated precision silicon time base
- Twelve individually programmable input/output pins that can be assigned as charge control I/O, secondary safety function I/O, SOC LED output or general purpose I/O
  - Two of the twelve I/Os are high voltage, capable for direct drive of Charge and Safety FETs
- On-chip regulator generates precision digital and analog supply voltages directly from pack voltage
- Supports direct connection to 2 to 4-cell Lithium packs
- Flexible power operating modes:
  - Run: Continuous operation
  - Sample: Periodic measurements at programmable intervals
  - Sleep: Shutdown mode due to low voltage. Power consumption less than 25 µA.
  - Shelf-Sleep: Shuts off PS501 power consumption for pack storage with automatic wake-up on pack insertion. Power consumption is less than 1 µA.
- Integrated Reset Control
  - Power-on Reset
  - Watchdog Timer Reset
  - Brown-out Detection Reset

Pin Description



28-pin SSOP Package - 209 mil

Pin Summary

Pin Name	Type	Description
VDDD, VSSD	Supply	Digital supply voltage input, ground
GPIO(0..9)	I/O	Programmable digital I/O
GPIOHV1,2	I/O	Open-drain programmable digital I/O for direct drive of FETs
$\overline{\text{MCLR}}$	I	Master Clear. Pull-up in normal operation
SMB-CLK, SMB-DTA	I/O	SMBus interface
VC(1..4)	I	Cell voltage inputs
VDDA, VSSA	Supply	Voltage regulator output (internally connected to analog supply input), ground
RSHP, RSHN	I	Current sense resistor input
VNTC	I	External thermistor input
VREFT	O	Thermistor reference voltage
ROSC	I	Internal oscillator bias resistor

1.0 PRODUCT OVERVIEW

The PS501 combines a high-performance, low-power Microchip PIC18 microcontroller core together with PowerSmart proprietary monitoring/control algorithms and 3D cell models stored in 16 Kbytes of on-chip reprogrammable Flash memory.

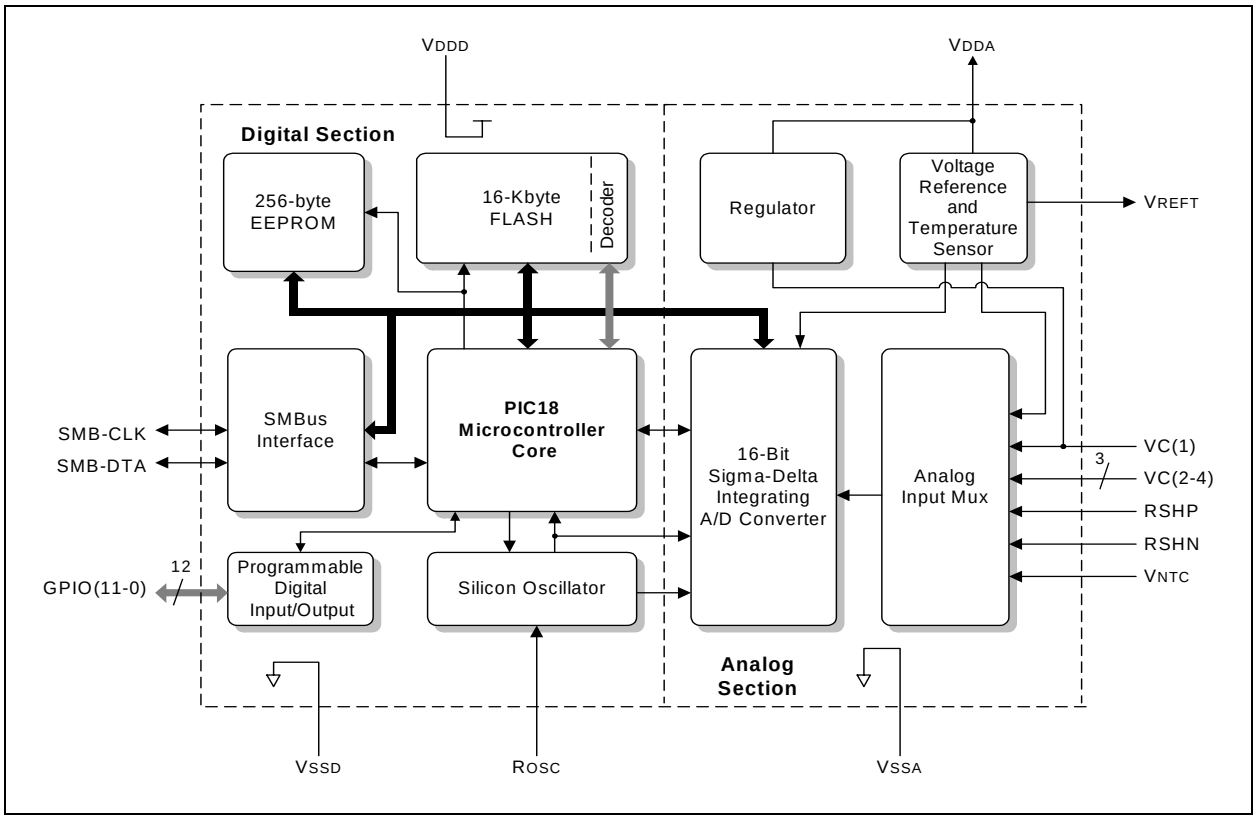
Analog resources include a 16-bit sigma-delta integrating A/D and mixed signal circuitry for precision measurement of battery current, temperature and voltage and for direct connection to 4-cell series Lithium Ion packs. On-chip EEPROM is provided for storage of user customizable and “learned” battery parameters.

An industry standard 2-wire SMBus interface supports host communication using standard SBData commands and status.

Additional integrated features include a high accuracy on-chip oscillator and temperature sensor. Twelve general purpose pins support charge or safety control or user programmable digital I/O. Eight of them can be used as LED drivers and two are open drain for direct FET drive.

The PS501 can be configured to accommodate all Lithium rechargeable battery chemistries, including Li Ion graphite, Li Ion hard carbon and Li Ion polymer, with direct connection to 2 to 4 series cell configurations.

FIGURE 1-1: PS501 INTERNAL BLOCK DIAGRAM



1.1 Architectural Description

The PS501 is a a fully field reprogrammable single chip solution for rechargeable battery management. Figure 1-1 is an internal block diagram highlighting the major architectural elements described below.

1.2 Microcontroller/Memory

The PS501 incorporates an advanced, low-power Microchip PIC18 8-bit RISC microcontroller core. Memory resources include 16 Kbytes of reprogrammable Flash memory for program/data storage and 256 bytes of EEPROM for parameter storage. Both memory arrays may be reprogrammed through the SMBus interface.

1.3 A/D Converter

The PS501 performs precise measurements of current, voltage and temperature, using a highly accurate 16-bit integrating sigma-delta A/D converter. The A/D can be calibrated to eliminate gain and offset errors and incorporates an auto-zero offset correction feature that can be performed while in the end system application.

1.4 PowerSmart® Firmware/Battery Models

Contained within the 16-Kbyte Flash memory is the PowerSmart developed battery management firmware that incorporates proprietary algorithms and sophisticated 3-dimensional cell models. Developed by battery chemists, the patented, self-learning 3D cell models contain over 250 parameters and compensate for self-discharge, temperature and other factors. In addition, multiple capacity correction and error reducing functions are performed during charge/discharge cycles to enhance accuracy and improve fuel gauge and charge control performance. As a result, accurate battery capacity reporting and run-time predictions with less than 1% error are achievable.

The reprogrammability of the Flash allows firmware upgrades and customized versions to be rapidly created without the need for silicon revisions.

The PS501 can be easily customized for a particular application's battery cell chemistry. Standard configuration files are provided by PowerSmart for a wide variety of popular rechargeable cells and battery pack configurations.

1.5 SMBus Interface/SBData Commands

Communication with the host is fully compliant with the industry standard Smart Battery System (SBS) specification. Included is an advanced SMBus communications engine that is compliant with the SMBus v1.1 protocols. The integrated firmware processes all the revised Smart Battery Data (SBData) v1.1 values.

1.6 Accurate Integrated Time Base

The PS501 integrates a highly accurate silicon oscillator that provides accurate timing for self-discharge and capacity calculations and eliminates the need for an external crystal.

1.7 Temperature Sensing

An integrated temperature sensor is provided to minimize component count when the PS501 IC is located in close physical proximity to the battery cells being monitored. As an option, a connection is provided for an external thermistor that can also be monitored.

1.8 General Purpose I/O

Twelve programmable digital input/output pins are provided by the PS501. Eight of these pins can be used as LED outputs to display State-Of-Charge (SOC), used for direct control of external charge circuitry or to provide additional levels of safety in Li Ion packs. Alternatively, they can be used as general purpose input/outputs. Two of the I/Os are open-drain outputs and can thus be used to directly drive FETs or other high-voltage applications.

TABLE 1-1: PIN DESCRIPTIONS

Pin	Name	Description
1	V_{DDD}	(Input) Filter capacitor input for digital supply voltage.
2	GPIO(4)	(Bidirectional) Programmable general purpose digital input/output pin (4) or LED driver.
3	GPIO(5)	(Bidirectional) Programmable general purpose digital input/output pin (5) or LED driver.
4	GPIO(6)	(Bidirectional) Programmable general purpose digital input/output pin (6) or LED driver.
5	GPIO(7)	(Bidirectional) Programmable general purpose digital input/output pin (7) or LED driver.
6	SMB-CLK	SMBus clock pin connection.
7	SMB-DTA	SMBus data pin connection.
8	VC(4)	(Input) Cell voltage input for the fourth highest voltage cell in a series string.
9	VC(3)	(Input) Cell voltage input for the third highest voltage cell in a series string.
10	VC(2)	(Input) Cell voltage input for the second highest voltage cell in a series string.
11	VC(1)	(Input) Cell voltage input for the first or highest voltage cell in a series string.
12	V_{DDA}	(Input) Analog supply voltage input.
13	V_{SSA}	Analog ground reference point.
14	RSHP	(Input) Current measurement A/D input from positive side of the current sense resistor.
15	RSHN	(Input) Current measurement A/D input from negative side of the current sense resistor.
16	V_{NTC}	(Input) A/D input for use with an external temperature circuit. This is the midpoint connection of a voltage divider, where the upper leg is a thermistor (103ETB type) and the lower leg is a 3.65 KOhm resistor. This input should not go above 150 mV.
17	V_{REFT}	(Output) Reference voltage output for use with temperature measuring A/D circuit. This 150 mV output is the top leg of the voltage divider and connects to an external thermistor.
18	R_{OSC}	External bias resistor.
19	GPIO(8)	(Bidirectional) Programmable general purpose digital input/output pin (8).
20	GPIO(9)	(Bidirectional) Programmable general purpose digital input/output pin (9).
21	GPIOHV1	(Bidirectional) Programmable general purpose digital input/output pin (10). Open-drain, high-voltage tolerant.
22	$\overline{MCLR}$	(Input) Master Clear. Must be pulled up for normal operation.
23	GPIOHV2	(Bidirectional) Programmable general purpose digital input/output pin (12). Open-drain, high-voltage tolerant.
24	GPIO(0)	(Bidirectional) Programmable general purpose digital input/output pin (0) or LED driver.
25	GPIO(1)	(Bidirectional) Programmable general purpose digital input/output pin (1) or LED driver.
26	GPIO(2)	(Bidirectional) Programmable general purpose digital input/output pin (2) or LED driver.
27	GPIO(3)	(Bidirectional) Programmable general purpose digital input/output pin (3) or LED driver.
28	V_{SSD}	Digital ground reference point.

2.0 A/D OPERATION

The PS501 A/D converter measures current, voltage and temperature and integrates the current over time to predict State-Of-Charge. Pack voltage and individual cell voltages are monitored and can be individually calibrated for the best accuracy. Using an external sense resistor, current is monitored during both charge and discharge and is integrated over time using the on-chip oscillator as the time base. Temperature is measured from the on-chip temperature sensor or an optional external thermistor. Current and temperature are also calibrated for accuracy.

2.1 A/D Converter List

The A/D converter alternately measures pack voltage, cell voltages, current, temperature and auto-offset as explained below. The schedule for the sequence and frequency of these measurements is programmable, as is the number of bits used. The default scheduling uses three lists. At near full (above the voltage point **ADLNearFull**) and near empty (below the voltage point **ADLNearEmpty**), voltage intensive lists are used to accurately end charge or discharge. In between **ADLNearFull** and **ADLNearEmpty**, a current intensive schedule is used to more accurately calculate capacity.

2.2 Current Measurement

The A/D input channels for current measurement are the RSHP and RSHN pins. The current is measured using an integrating method, which averages over time to get the current measurement and integrates over time to get a precise measurement value.

A 5 to 600 milli-Ohm sense resistor is connected to RSHP and RSHN as shown in the example schematic. The maximum input voltage at either RSHP or RSHN is +/-150 mV. The sense resistor should be properly sized to accommodate the lowest and highest expected charge and discharge currents, including suspend and/or standby currents.

Circuit traces from the sense resistor should be as short as practical without significant crossovers or feedthroughs. Failure to use a single ground reference point at the negative side of the sense resistor can significantly degrade current measurement accuracy.

The EEPROM value, **NullCurr**, represents the zero zone current of the battery. This is provided as a calibration guardband for reading zero current. Currents below the +/- **NullCurr** (in mA) limit are read as zero and are not included in the capacity algorithm calculations. A typical value for **NullCurr** is 3 mA, so currents between -3 mA and +3 mA will be reported as zero and not included in the capacity calculations.

The equation for current measurement resolution and sense resistor selection is shown in the following equation.

EQUATION 2-1:

9.15 mV/R_{SENSE} (milli-Ohms) = Current LSB
(Minimum current measurement if > **NullCurr**)

Current LSB x 16384 = Maximum current measurement possible

In-circuit calibration of the current is done using the SMBus interface at time of manufacture to obtain absolute accuracy. The current measurement equation is:

EQUATION 2-2:

$$I(ma) = (I\_A/D - \mathbf{COCurr} - \mathbf{COD}) * \mathbf{CFCurr}/16384$$

where:

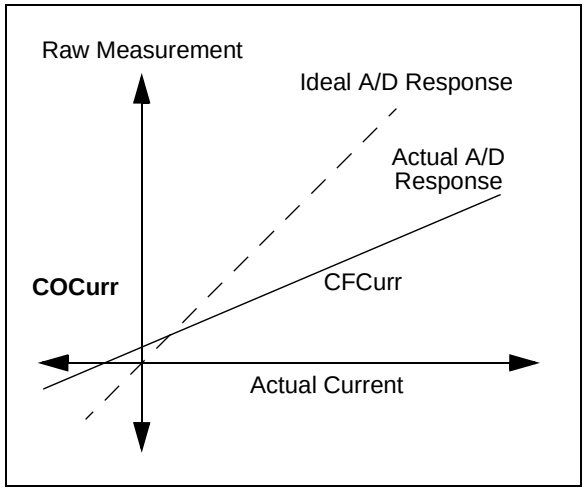
I_A/D is the internal measurement

COCurr is the “Correction Offset for Current” which compensates for any offset error in current measurement stored in EEPROM.

CFCurr is the “Correction Factor for Current” which compensates for any variances in the actual sense resistance over varying currents stored in EEPROM.

Figure 2-1 shows the relationship of the **COCurr** and **CFCurr** values.

FIGURE 2-1: COCurr AND CFCurr VALUE RELATIONSHIP



2.3 Auto-Offset Compensation

Accuracy drift is prevented using an automatic auto-zero self-calibration method, which ‘re-zeroes’ the current measurement circuit every AOMInt * 0.5 seconds when enabled. This feature can correct for drift in temperature during operation. The auto-offset compensation circuit works internally by disconnecting the RSHP and RSHN inputs and internally shorting these inputs to measure the zero input offset. The EEPROM and calibration value COD is the true zero offset value of the particular module.

2.4 Voltage Measurements

The A/D input channels for cell and pack voltage measurements are the VC(1) to VC(4) pins. Measurements are taken each measurement period when the A/D is active. The maximum voltage at any VCELLX input pin is 19V absolute, but voltages above 18V are not suggested. The individual cell voltages are measured with an integration method to reduce any sudden spikes or fluctuations. The A/D uses an 11-bit resolution mode for these measurements.

Cell voltage inputs are read every measurement period, which is approximately every 500 milliseconds. This could be further extended by the use of Sample mode, where A/D measurements are not activated every measurement period, depending on the configuration of **SampleLimit** and **NSample** values. (See **Section 3.0 "Operational Modes"** for additional information.) For Li Ion, Li-based, or even Lead-Acid applications, up to four (4) series cell voltages may be monitored individually. The highest voltage cell of the stack must be connected to VC(1).

For some applications, the actual cell stack arrangement can be altered accordingly. The PS501 voltage input pins (VCELLx pins) are capable of measuring up to 18V each. Therefore, cell arrangements can be combined and the corresponding cell voltage thresholds can be adjusted. For example, a 2-cell Li Ion pack could actually be connected as a single 7.2V cell instead of two 3.6V cells. The values for the cell voltages would all be doubled, for example VCELL1 would equal the sum of two cells and only the VC(1) input pin would be used.

Each VCELLX input circuit contains an internal resistive divider to reduce the external voltage input to a range that the internal A/D circuit can accommodate (150 mV maximum). These dividers are set based on a maximum cell voltage of 4.5 volts. A range of 340 mV with dividers, based on a maximum voltage of 20 volts, is used for pack voltage.

The impedance at each VCELLX input is roughly 100 kOhms, but is only connected to ground (via the VSSA pins) when the actual voltage measurement is occurring. This corresponds to an insignificant amount of capacity drained through this circuit during the brief voltage measurement period, typically 45 ms every 500 ms.

2.4.1 IMPEDANCE COMPENSATION

Since accurate measurement of pack voltage and cell voltages are critical to performance, the voltage measurements can be compensated for any impedance in the power path that might affect the voltage measurements.

The EEPROM value **PackResistance** is used to compensate for additional resistance that should be removed.

The equation for the compensation value (in ohms) is:

EQUATION 2-3:

PackResistance = Trace Resistance * 65535

(This is a 2-byte value so the largest value is 1 ohm.)

This requires modification of overall voltage SBData function to compensate for pack resistance and shunt resistance of the current sense resistor. Thus, the previous voltage equation is modified to:

EQUATION 2-4:

SBData Voltage Value = VC(1) + Measured Current (mA) * **PackResistance**/65535

The voltage measurement equation is:

EQUATION 2-5:

V (mV) = (V_A/D – **COVPack**) x **CFVPack**/2048

where:

V_A/D is the internal measurement output

COVPack is the "Correction Offset for Pack Voltage" which compensates for any offset error in voltage measurement (since the offset of the A/D is less than the voltage measurement resolution of +/- 16.5 mV, the **COVPack** value is typically zero).

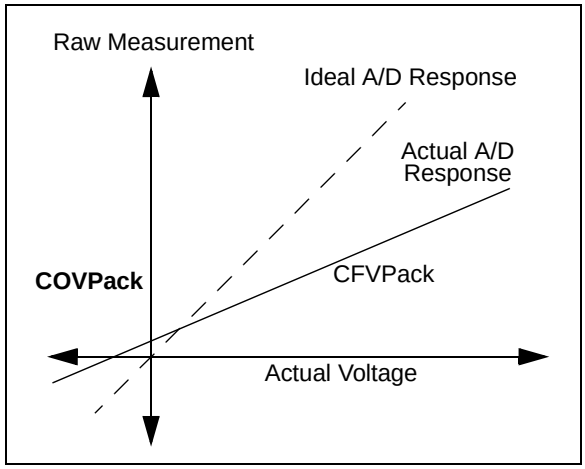
CFVPack is the "Correction Factor for Pack Voltage" which compensates for any variance in the actual A/D response versus an ideal A/D response over varying voltage inputs.

The **COVPack** and **CFVPack** are calibration constants that are stored in EEPROM.

VCELL1 and VCELL4 can also be compensated for impedance in the lines connecting to the PS501. **VC1Res** is the resistance between the PS501 and the highest series cell. **VC4Res** is the resistance between the PS501 and the lowest cell. This allows the PS501 to subtract any voltage drop due to current between the cell and the PS501.

Figure 2-2 shows the relationship of the **COVPack** and **CFVPack** values.

FIGURE 2-2: COVPack AND CFVPack VALUE RELATIONSHIP



In-circuit calibration of the voltage is done at the time of manufacture to obtain absolute accuracy in addition to high resolution. Individual cell voltage measurements can be accurate to within ±20 mV.

The individual cell voltage inputs are also calibrated the same way the pack voltage is. There is one offset value, **COVCell**, for all individual cells and up to four different correction factors, **CFVCell1** through **CFVCell4**, one for each cell input.

2.5 Temperature Measurements

The A/D receives input from the internal temperature sensor to measure the temperature. Optionally, an external thermistor can be connected to the VNTC pin which is also monitored by the A/D converter. An output reference voltage for use with an external thermistor is provided on the VREFT pin. The A/D uses an 11-bit resolution mode for the temperature measurements.

A standard 10 kOhms at 25°C Negative-Temperature-Coefficient (NTC) device of the 103ETB type is suggested for the optional external thermistor. One leg of the NTC should be connected to the VREFT pin and the other to both the VNTC pin and a 3.65 kOhms resistor to analog ground (VSSA). The resistor forms the lower leg of a voltage divider circuit. To maintain high accuracy in temperature measurements, a 1% resistor should be used.

A look-up table is used to convert the voltage measurement seen at the VNTC pin to a temperature value. The external thermistor should be placed as close as possible to the battery cells and should be isolated from any other sources of heat that may affect its operation.

Calibration of the temperature measurements involves a correction factor and an offset exactly like the current and voltage measurements. The internal temperature measurement makes use of correction factor **CFTempI** and offset **COTempI**, while the VNTC and VREFT pins for the optional external thermistor make use of correction factor **CFTempE** and offset **COTempE**.

3.0 OPERATIONAL MODES

The PS501 operates on a continuous cycle. The frequency of the cycles depends on the power mode selected. There are four power modes: Run, Sample, Sleep and Shelf-Sleep. Each mode has specific entry and exit conditions as listed below.

3.1 Run Mode

Whether the PS501 is in Run mode or Sample mode depends on the magnitude of the current. The Run and Sample mode entry-exit threshold is calculated using the EEPROM parameter, **SampleLimit**.

SampleLimit is a programmable EEPROM value and **CFCurr** is an EEPROM value set by calibration.

Entry to Run mode occurs when the current is more than +/- **SampleLimit** mA for two consecutive measurements. Run mode may only be exited to Sample mode, not to Sleep mode, when Sample mode is enabled. Exit from Run mode to Sample mode occurs when the converted measured current is less than the +/- **SampleLimit** mA threshold for two consecutive measurements.

Run mode is the highest power consuming mode. During Run mode, all measurements and calculations occur once per measurement period. Current, voltage and temperature measurements are each typically made sequentially during every measurement period.

3.2 Sample Mode

Entry to Sample mode occurs when the measured current is less than +/- **SampleLimit** (EE parameter) two consecutive measurements. Sample mode may be exited to either Run mode or Sleep mode.

While in Sample mode, measurements of voltage, current and temperature occur only once per **NSample** counts of measurement periods, where **NSample** is a programmable EEPROM value. Calculations of State-Of-Charge, SMBus requests, etc. still continue at the normal Run mode rate, but measurements only occur once every measurement period x **NSample**. The minimum value for **NSample** is two.

The purpose of Sample mode is to reduce power consumption during periods of inactivity (low rate charge or discharge). Since the analog-to-digital converter is not active, except every **NSample** counts of measurement periods, the overall power consumption is significantly reduced.

EXAMPLE 3-1: CONFIGURATION

Measurement period is 500 ms
SampleLimit is set to 20
NSample is set to 16

Result:

Run/Sample mode entry-exit threshold = 20 mA

During Sample mode, measurements will occur every:
16 measurement periods of 500 mS = every 8 seconds

3.3 Low-Voltage Sleep Mode

Entry to Sleep mode can only occur when the measured pack voltage at the VC(1) input is below a preset limit, set by the EEPROM value **SleepVPack** (in mV). Sleep mode may be exited to Run mode, but only when one of the wake-up conditions is satisfied.

While in Sleep mode, no measurements occur and no calculations are made. The fuel gauge display is not operational, no SMBus communications are recognized and only a wake-up condition will permit an exit from Sleep mode. Sleep mode is one of the lowest power consuming modes and is used to conserve battery energy following a complete discharge.

There are two levels of Low-Voltage Sleep mode that can be used, each with a different wake-up criteria. Default Low-Power mode will use 25 µA typical and will wake-up when the voltage exceeds the **WakeUp** voltage level. By setting bit 1 of the **WakeUp** register to '1', the Ultra Low-Power mode can be used. This will be entered by low voltage, but wake-up occurs by pulling the SMBus lines high. Ultra Low-Power mode uses less than 1 µA.

3.4 Shelf-Sleep Mode

Shelf-Sleep mode is used to put the PS501 into Low-Power mode, regardless of voltage level, for long term storage of battery packs. It is entered by an SMBus command. It is exited by the conditions selected in the **WakeUp** register. These can be voltage, current, GPIO or SMBus activity. If any of these four are selected for wake-up, the Shelf-Sleep mode will be Low-Power mode and will draw 25 µA typical. If none of these options are selected and bit 3 of the **WakeUp** register is set, the Shelf-Sleep mode will be Ultra Low-Power mode, which will draw less than 1 µA and wake-up will be by pulling SMBus high.

TABLE 3-1: WakeUp EEPROM VALUE

Bit	Name	Function
7	WakeIO	Wake-up from I/O Activity
6	WakeBus	Wake-up from SMBus Activity
5	WakeCurr	Wake-up from Current
4	WakeVolt	Wake-up from Voltage
3	Enable Shelf-Sleep	Use Ultra Low-Power mode for Shelf-Sleep mode. All other bits must be zero.
1	LV Sleep Mode	Use Ultra Low-Power mode as Low-Voltage Sleep mode
0	Zero Remcap	Set remap to zero when entering Low-Voltage Sleep mode

TABLE 3-2: WakeLevels EEPROM VALUE

WakeUp Voltage (2:0)	Voltage	Purpose
000	6.4V	2 cells Li Ion
001	6.66V	2 cells Li Ion
010	8.88V	2 cells Li Ion
011	9.6V	3 cells Li Ion
100	9.99V	3 cells Li Ion
101	11.1V	3 cells Li Ion
110	12.8V	4 cells Li Ion
111	13.3V	4 cells Li Ion
WakeUp Current (7:3)	**Voltage**	**Purpose**
00000	Minimum	µV across Sense Resistor
11000	Typical Recommended	µV across Sense Resistor
11111	Maximum	µV across Sense Resistor

TABLE 3-3: POWER MODE SUMMARY

Mode	Entry	Exit	Notes
Run	Measured current > preset threshold (set by **SampleLimit**)	Measured current < preset threshold (set by **SampleLimit**)	Highest power consumption and accuracy for rapidly changing current.
Sample	Measured current < preset threshold (set by **SampleLimit**)	Measured current > preset threshold (set by **SampleLimit**)	Saves power for low, steady current consumption. Not as many measurements needed. Measurements made every **NSample** periods.
Sleep	V_{PACK} < **SleepVPack** and in Sample mode	**WakeUp** voltage level exceeded (Low-Power mode) or SMBus pulled high (Ultra Low-Power mode)	No measurements made.
Shelf-Sleep	SMBus command	**WakeUp** register conditions met (Low-Power mode) or SMBus pins pulled high (Ultra Low-Power mode)	No measurements made.

4.0 CAPACITY MONITORING

The PS501 internal CPU uses the voltage, current and temperature data from the A/D converter, along with parameters and cell models, to determine the state of the battery and to process the SBData function instruction set.

By integrating measured current, monitoring voltages and temperature, adjusting for self-discharge and checking for End-Of-Charge and End-Of-Discharge conditions, the PS501 creates an accurate fuel gauge under all battery conditions.

4.1 Capacity Calculations

The PS501 calculates State-Of-Charge and fuel gauging functions using a 'coulomb counting' method, with additional inputs from battery voltage and temperature measurements. By continuously and accurately measuring all the current into and out of the battery cells, along with accurate three-dimensional cell models, the PS501 is able to provide accurate predictions of SOC and run-time.

The capacity calculations consider two separate states: charge acceptance or Capacity Increasing (CI) and discharge or Capacity Decreasing (CD). The CI state only occurs when a charge current larger than the EEPROM **NullCurr** value is measured. Otherwise, while at rest and/or while being discharged, the state is CD. Conditions must persist for at least **NChangeState** measurement periods for a valid state change between CD and CI. A minimum value of 2 is suggested for **NChangeState**.

Regardless of the CI or CD state, self-discharge is also calculated and subtracted from the integrated capacity values. Even when charging, there is still a self-discharge occurring in the battery.

To compensate for known system errors in the capacity calculations, a separate error term is also continuously calculated. This term is the basis for the SBData value of MaxError. Two error values are located in EEPROM. The **CurrError** value is the inherent error in current measurements and should be set based on the selection of a sense resistor and calibration results. The **SelfDischrgErr** value is the error in the parameter tables for self-discharge and depends on the accuracy of the cell chemistry model for self-discharge.

Since the PS501 electronics also drain current from the battery system, another EEPROM value allows even this minor drain to be included in the capacity calculations. The **PwrConsumption** value represents the drain of the IC and associated circuitry, including additional safety monitoring electronics if present. A typical value of 77 represents the module's nominal power consumption, including the PS501 typical consumption.

The total capacity added or subtracted from the battery (change in charge) per measurement period is expressed by the following formula:

EQUATION 4-1:

$\Delta Charge = \Sigma i \Delta t$ (the current integrated over time)

- **CurrError** (Current Measurement Error)
- **PwrConsumption** * Δt (PS501 I_{DD})
- % of Self-Discharge * FCC
- **SelfDischrgErr** (Self-Discharge Error)

The error terms are always subtracted, even though they are +/- errors, so that the fuel gauge value will never be overestimated. Current draw of the PS501 and the self-discharge terms are also always subtracted. The SBData value, MaxError, is the total accumulated error as the gas gauge is running.

The battery current will be precisely measured and integrated in order to calculate total charge removed from or added to the battery. Based on look-up table values, the capacity is adjusted for self-discharge relative to current, temperature and SOC.

4.2 Discharge Termination

Discharge termination is determined based on the End-Of-Discharge (EOD) voltage point. The voltage level at which this point occurs can be chosen to be constant, or to change depending on the temperature and discharge rate, since these factors affect the voltage curve and total capacity of the battery. The EOD voltage parameter table predicts the voltage point at which this EOD will be reached, based on discharge rate and temperature.

The PS501 will monitor temperature and discharge rate continuously and update the **Veodx** in real-time. When the voltage measured on the cell is below EOD voltage for the duration of **EODRecheck** x periods (500 ms), a valid EOD has occurred.

When a valid EOD has been reached, the TERMINATE_DISCHARGE_ALARM bit (bit 11) in BatteryStatus will be set. This will cause an AlarmWarning condition with this bit set.

Additionally, the REMAINING_TIME_ALARM and/or REMAINING_CAPACITY_ALARM bits can be set first to give a user defined early warning prior to the TERMINATE_DISCHARGE_ALARM. The remaining time alarm will trigger in battery status when the remaining time calculation falls below a threshold set by the SMBus command. The remaining capacity alarm will be set in battery status when the capacity falls below a threshold set by the SMBus command. Use an SMBus Write command to Remaining TimeAlarm (command code 0x02) or RemainingCapacityAlarm (command code 0x01) to set these values.

4.3 Capacity Relearn at Discharge Termination

To maintain accurate capacity prediction ability, the **FullCapacity** value is relearned on each discharge, which has reached a valid EOD after a previous valid fully charged condition (EOC). If a partial charge occurs before reaching a valid EOD, then no relearn will occur. If the discharge rate at EOD is greater than the 'C-rate' adjusted value in **RelearnCurrLim,** then no relearn will occur.

When a valid EOD has been reached, then the error calculations represented by the SBData value of MaxError will be cleared to zero. If appropriate, the relearned value of **FullCapacity** (and FullChargeCapacity) will also be updated at this time.

4.4 Discharge Termination Voltage Look-up Table

4.4.1 NEAR EMPTY SHUTDOWN POINT

As the graph in Table 4-1 shows, available capacity in the battery varies with temperature and discharge rate. Since the remaining capacity will vary with temperature and discharge rate, a near empty shutdown point will also vary with temperature and discharge rate.

Knowing the discharge rate that occurs in the system during the shutdown process and knowing the temperature can pinpoint the exact save to disk point that will always leave the perfect shutdown capacity. The PS501 uses this information to tailor the gas gauge to the system and the remaining capacity and RSOC fuel gauge function will always go to zero at the efficient shutdown point. The table will use the voltage points at which this happens as the error correction and **FullCapacity** relearn point. This will ensure a relearn point before shutdown occurs and will correct any error in remaining capacity, also to ensure proper shutdown reserve energy.

The shutdown point has to equal the capacity required to shut down the system under the conditions of the shutdown. That is, looking at the curve that represents the actual discharge C-rate that occurs during the system shutdown function, we must stop discharge and initiate shutdown when the system has used capacity equal to that point on the shutdown C-rate curve. This is because no matter what the C-rate is when the shutdown point is reached, the system will automatically switch to the C-rate curve that represents the actual current draw of the shutdown function. So it doesn't matter if the system is in high discharge or low discharge, it will be in "shutdown" discharge conditions when shutdown begins and there must be enough capacity left. An example is a computer's save to disk function.

Table 4-1 shows that the system will always shutdown at the same capacity point regardless of C-rate conditions (since the C-rate of the save to disk procedure is a constant). Thus, we can automatically have an RSOC that is compensated for C-rate; it will go to zero when the capacity used is equal to the point at which shutdown occurs.

Ignoring the effects of temperature, we could mark the capacity used up to the shutdown point of the shutdown curve. All the shutdown voltage would then represent the same capacity and RSOC would always become zero at this capacity and FCC would always equal this capacity, plus the residual capacity of the save to disk curve.

To compensate for temperature, we can look at the series of curves that represent the shutdown C-rate at different temperatures. The PS501 implementation is to measure the temperature and choose a scaled RSOC value that will go to zero at the save to disk point at this temperature, assuming the temperature does not change. If it does change, then an adjustment to RSOC will be needed to make it go to zero at the shutdown point.

Taking temperature into consideration, the amount of capacity that can be used before shutdown is a constant as C-rate changes, but not constant as temperature changes. Thus, in the Look-up Table (LUT), the individual temperature columns will have voltage points that all represent the same capacity used, but the rows across temperature points (C-rate rows) will represent the different capacity used.

To compensate RSOC and RM, interpolation will be used and the compensation adjustment will happen in real-time to avoid sudden drops or jumps. Every time the temperature decreases by one degree, a new interpolated value will be subtracted from RSOC and RM. Every time the temperature increases by one degree, RSOC and RM will be held constant until discharged capacity equals the interpolated value that should have been added to RSOC and RM (to avoid capacity increases during discharge). With this interpolation happening in real-time, there will be no big jumps or extended flat periods as we cross over boundaries in the LUT. This compensation will not begin until after the fully charged status is reset, allowing RSOC to be 100% always when the battery is full.

4.5 Age Compensation

The voltage EOD points will be compensated due to the age of the cells. A linear factor, **AgeFactor**, will be applied to the voltage points as a function of CycleCount. The voltage levels will decrease as the battery pack ages to model the flattening of the voltage vs. capacity curve that naturally happens to battery cells.

TABLE 4-1: V_EOD LOOK-UP TABLE

	< -10°	< 0°	< 10°	< 20°	< 30°	< 40°	< 50°	> 50°
< 0.2C	V1	V2	V3	—				
< 0.5C								
< 0.8C								
< 1.1C								
< 1.4C								
< 1.7C								
< 2.0C								
> 2.0C					—	V62	V63	V64
Capacity	20%	10%	5%	3%	0%	0%	0%	0%

The above table is an example of the various voltage values that will signal the shutdown points as a function of temperature and discharge rate.

Also shown is the amount of capacity left after shutdown that will compensate RSOC.

Table 4-2 shows the actual names of the values in the EEPROM.

TABLE 4-2: VALUE NAMES IN THE EEPROM

	TEOD(1)	TEOD(2)	TEOD(3)	TEOD(4)	TEOD(5)	TEOD(6)	TEOD(7)	TEOD(8)
CEOD(1)	VEOD1(1)	VEOD1(2)	VEOD1(3)	VEOD1(4)	VEOD1(5)	VEOD1(6)	VEOD1(7)	VEOD1(8)
CEOD(2)	VEOD2(1)	VEOD2(2)	VEOD2(3)	VEOD2(4)	VEOD2(5)	VEOD2(6)	VEOD2(7)	VEOD2(8)
CEOD(3)	VEOD3(1)	VEOD3(2)	VEOD3(3)	VEOD3(4)	VEOD3(5)	VEOD3(6)	VEOD3(7)	VEOD3(8)
CEOD(4)	VEOD4(1)	VEOD4(2)	VEOD4(3)	VEOD4(4)	VEOD4(5)	VEOD4(6)	VEOD4(7)	VEOD4(8)
CEOD(5)	VEOD5(1)	VEOD5(2)	VEOD5(3)	VEOD5(4)	VEOD5(5)	VEOD5(6)	VEOD5(7)	VEOD5(8)
CEOD(6)	VEOD6(1)	VEOD6(2)	VEOD6(3)	VEOD6(4)	VEOD6(5)	VEOD6(6)	VEOD6(7)	VEOD6(8)
CEOD(7)	VEOD7(1)	VEOD7(2)	VEOD7(3)	VEOD7(4)	VEOD7(5)	VEOD7(6)	VEOD7(7)	VEOD7(8)
CEOD(8)	VEOD8(1)	VEOD8(2)	VEOD8(3)	VEOD8(4)	VEOD8(5)	VEOD8(6)	VEOD8(7)	VEOD8(8)
	FCCP(1)	FCCP(2)	FCCP(3)	FCCP(4)	FCCP(5)	FCCP(6)	FCCP(7)	FCCP(8)

TABLE 4-3: VALUE DEFINITIONS IN THE EEPROM

TEOD 8 coded bytes	typ: 5, 20, 35, 50, 80, 113, 150, 150	Range: 1-255 per byte
EOD Temperature boundaries, 8 increasing values of temperature coded as TEODx = (Tcelsius * 10 + 200)/4		
CEOD 8 coded bytes	typ: 19, 32, 48, 64, 77, 90, 109,1 09	Range: 1-255
EOC C-rate boundaries, 8 increasing values of C-rates coded: CEODx = C-rate * (256/28/R_F), where R_F is the Rate Factor (R_{FACTOR}) OTP EPROM parameter. For R_F = 7, CEODx = C-rate * 64. Thus, a value of 32 is one-half C, etc.		
FCCP coded %	typ: 50, 25, 12, 8, 0, 0, 0	Range: 1-255
Unusable residual capacity before save to disk, corresponding to temperature, 255 = 100%		
VEOD coded	typ: 75	Range: 1-255
End-Of-Discharge voltage, voltage = 2700 + 4 * VEOD. Cell voltage at which save to disk is signaled.		

5.0 CHARGE CONTROL

A SBS configuration normally allows the Smart Battery to broadcast the ChargingVoltage and ChargingCurrent values to the Smart Battery Charger (SMBus address 12 hex) to 'control' when to start charge, stop charge and when to signal a valid 'fully charged' condition. AlarmWarnings are also sent from the Smart Battery (SMBus address 16 hex) to the Smart Battery Charger.

Alternately, the SMBus Host or a "Level 3" Smart Battery Charger may simply read the SBData values for ChargingVoltage and ChargingCurrent from the Smart Battery directly. The Host or "Level 3" Smart Battery Charger is also required to read the SBData value of BatteryStatus to obtain the appropriate alarm and status bit flags. When used in this configuration, the ChargingCurrent and ChargingVoltage broadcasts can be disabled from the Smart Battery by setting the CHARGER_MODE (bit 14) in the BatteryMode register. The PS501 ICs support all of these functions. (Please refer to the SBS Smart Battery Charger Specification for a definition of the "Level 3" Smart Battery Charger.)

The ChargingCurrent and ChargingVoltage registers contain the maximum charging parameters desired by the particular chemistry, configuration and environmental conditions. The environmental conditions include the measured temperature and the measured cell or pack voltages.

For Li-based systems, ChargingVoltage should be set to the product of the **EOCVolt** and **Cells** values from the EEPROM:

EQUATION 5-1:

$$\text{ChargingVoltage} = \textbf{EOCVolt} \times \textbf{Cells}$$

The ChargingCurrent value is set to a maximum using the **ChrgCurr** value from the EEPROM. For Lithium systems, both ChargingCurrent and ChargingVoltage values are maximums. When the current reaches **ChrgCurr**, it will be held constant at this value. Then, when the voltage reaches **ChrgVolt**, the current must be reduced so that the voltage will be constant and not exceed the maximum. This is accomplished by setting ChargingCurrent to **ChrgCurrOff**. For safety reasons, this current change also occurs when the temperature limits are exceeded. When temperature or voltage limits are exceeded, the value of ChargingCurrent changes to the **ChrgCurrOff** value from the EEPROM. When a valid End-Of-Charge (EOC) condition is detected and a fully charged state is reached, the ChargingCurrent value is set equal to the **ChrgCurrOff** value.

When ChargingCurrent is set to the **ChrgCurrOff** value, no broadcasts of either ChargingCurrent or ChargingVoltage will occur unless a charge current greater than **NullCurr** is detected by the A/D measurements. Temperature limits are set using the **ChrgMaxTemp**, **DischrgMaxTemp** and **ChrgMinTemp** values from EEPROM. These values represent the temperature limits within which ChargingCurrent will be set to **ChrgCurr**. Temperatures outside these limits will cause ChargingCurrent to be set to **ChrgCurrOff.**

If ChargingCurrent is set to **ChrgCurrOff** *and* the measured temperature is greater than **DischrgMaxTemp** *and* less than **ChrgMaxTemp** *and* a charge current is measured which is significantly larger than the **ChrgCurrOff** value, *then* ChargingCurrent will be set to **ChrgCurr** unless a fully charged condition has already been reached.

If the CHARGER_MODE bit in the BatteryMode register is cleared (enabling broadcasts of ChargingCurrent and ChargingVoltage), then these broadcasts will occur every **NChrgBroadcast** measurement cycle.

The Smart Battery Data and Smart Battery Charger Specifications require that ChargingCurrent and ChargingVoltage broadcasts occur no faster than once per 5 seconds and no slower than once per 60 seconds when charging is occurring or desired. This requires that the **NChrgBroadcast** value must be set between 10 and 120. The SMBus Specification also requires that no broadcasts occur during the first 10 seconds after SMBus initialization.

EXAMPLE 5-1: CONFIGURATION

Measurement cycle is 500 msec

NChrgBroadcast	=	100 decimal
ChrgCurr	=	2500 decimal
ChrgCurrOff	=	10 decimal
ChrgMaxTemp	=	162 decimal
DischrgMaxTemp	=	137 decimal
ChrgMinTemp	=	50 decimal

Results:

ChargingCurrent and ChargingVoltage broadcasts:

100 cycles of 500 msec = every 50 seconds

Broadcast delay after SMBus initialization:

10 seconds

ChargingCurrent if Temperature > 45°C: 10 mA
ChargingCurrent if Temperature < 0°C: 10 mA
ChargingCurrent if Temperature < 35°C and > 0°C: 2500 mA

5.1 Full Charge Detection Methods

For a typical Lithium Ion constant-current/constant-voltage charge system, the PS501 will monitor the taper current that enters the battery once the battery has reached the final voltage level of the charger. Once the taper current falls to a certain level, indicating that the battery is full, the End-Of-Charge (EOC) will be triggered. Different taper currents will be used for different temperatures. See the parameter explanation in **Section 9.0 "Parameter Setup"** for details.

When a valid fully charged EOC condition is detected, the following actions occur:

- The FULLY_CHARGED status bit (bit 5) in the SBData value of BatteryStatus is set to '1' to indicate a full condition. (This will remain set until RelativeStateOfCharge drops below the **ClrFullyChrg** value in EEPROM.)
- RelativeStateOfCharge is set to 100%.
- ChargingCurrent is set to **ChrgCurrOff** value.
- SBData value for MaxError is cleared to zero percent (0%).
- The TERMINATE_CHARGE_ALARM bit (bit 14) is set in BatteryStatus and an AlarmWarning broadcast is sent to the SMBus Host and Smart Battery Charger addresses.
- The **OverChrg** value is incremented for any charge received above 100% after a valid fully charged EOC condition.
- Control flags for internal operations are set to indicate a valid full charge condition was achieved.
- Other BatteryStatus or AlarmWarning flag bits may also be set depending on the conditions causing the EOC.
  - The charge timer, EOCTimer, is exceeded
  - Cell voltage is higher than **TCAVolt**

5.2 Temperature Algorithms

The PS501 SMBus Smart Battery IC provides multiple temperature alarm set points and charging conditions. The following EEPROM parameters control how the temperature alarms and charging conditions operate.

HighTempAl: When the measured temperature is greater than **HighTempAl**, the OVER_TEMP_ALARM is set. If the battery is charging, then the TERMINATE_CHARGE_ALARM is also set.

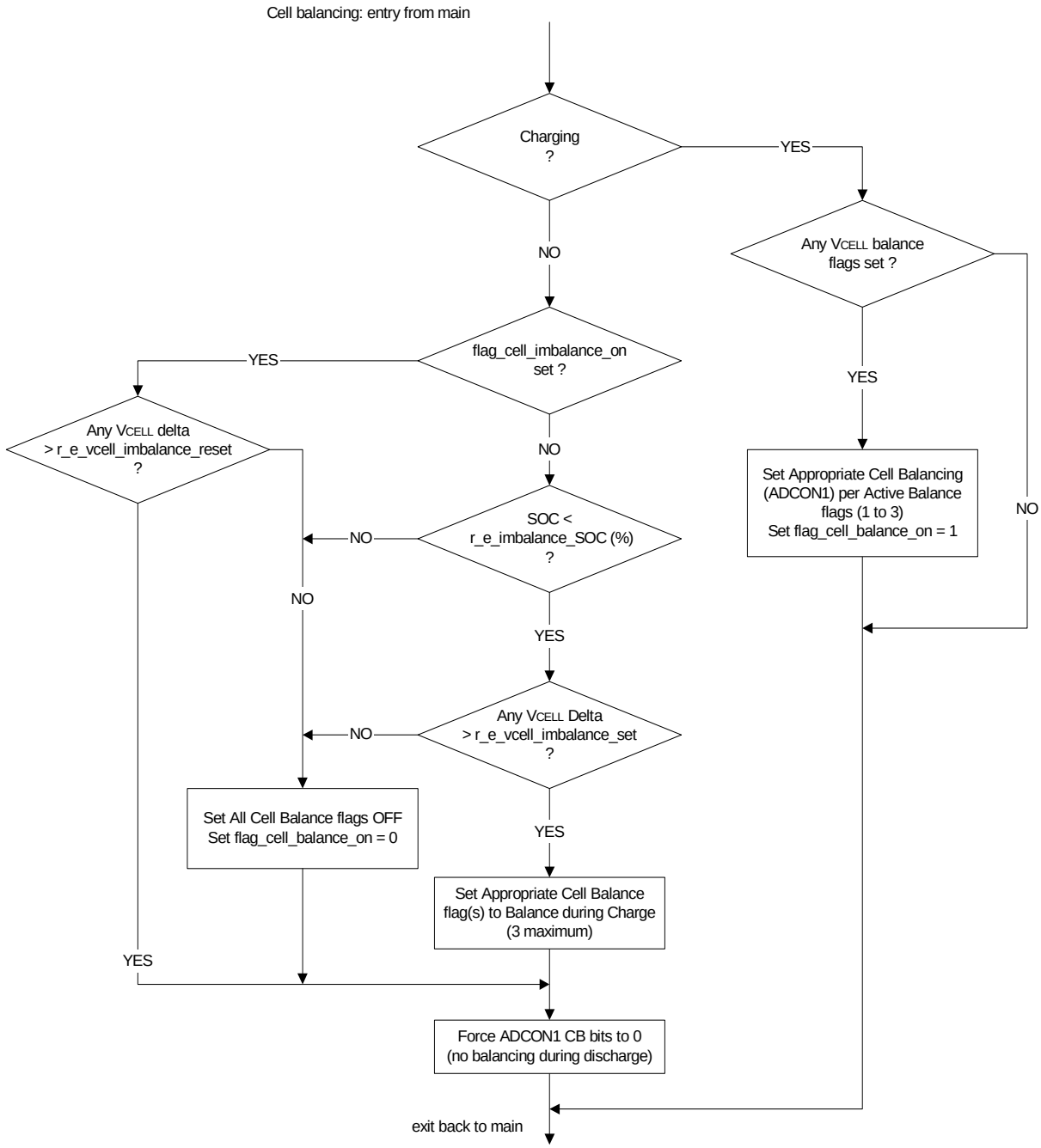
ChrgMinTemp, DischrgMaxTemp and ChrgMaxTemp: If the measured temperature is less than **ChrgMinTemp**, the ChargingCurrent is set to **ChrgCurrOff** and the ChargingVoltage is set to **ChrgVolt** to communicate to the charger that the non-charging state of current and voltage should be given. When measured temperature is greater than **ChrgMaxTemp** and the system is charging, or greater than **DischrgMaxTemp** and the system is discharging, then ChargingCurrent is set to **ChrgCurrOff** and the ChargingVoltage is set to **ChrgVoltOff** also. Otherwise, ChargingCurrent = **ChrgCurr** and ChargingVoltage = **ChrgVolt**.

6.0 CELL BALANCING

The PS501 has internal cell balancing loads with which to draw extra current away from higher voltage cells. There are internal 500 ohm resistors, which will draw up to 8.4 mA of current from each cell, depending on the cell voltage. The cell balancing algorithm will monitor individual cell voltages and the difference between them. When the difference between any cells exceeds the EEPROM parameter, **VcelldiffMax**, the resistor load will be applied to the higher cell until it is within **VcelldiffresetMax** of the lowest. Cell balancing will only be applied during the charging state to maintain run time during discharge.

Determination of cell balance requirement will be made near End-Of-Charge, when the capacity difference results in a cell voltage difference. Once this determination is made, cell balancing will commence on the charge cycle and remain in effect for the entire charge cycle. Upon discharging, cell balancing will be disabled to preserve run time. Once the near empty point is reached again, determination will be made as to whether correct hysteresis has been reached to disable the cell balancing for the next charge cycle.

FIGURE 6-1: CELL BALANCING



This algorithm makes the imbalance determination on the discharge cycle near EOD and uses the entire charge cycle for balancing (good for low balance currents)

7.0 GPIO CONFIGURATION

GPIOs can be set up to act as inputs or outputs that are based on conditions involving SBData parameters or GPIO levels compared to constants. This powerful programming model allows for customizing GPIO to set on any possible fuel gauge conditions and reset on any other possible fuel gauge conditions in any groupings.

TABLE 7-1: GPIO CONFIGURATIONS

Name	Length	Definition
GPIOSTATE	2	Initialized default state (positive logic)
GPIODIRECTION	2	Initialized direction: 1 = input 0 = output

GPIOCONFIG	2	GPIO configuration
		Bit 8:
		1 = pull-ups/downs disabled
		0 = pull-downs enabled
		Bits 7:0:
		if input:
		1 = pulled down
		0 = pulled up
		if output:
		1 = LED drive (GPIO0-7 only)
		0 = standard logic

GPIOPOLARITY	2	“Polarity” mask applied to invert positive logic

GPIOs configured above as standard logic output can be programmed to activate or reset in response to any group of fuel gauge conditions. Each “condition” is defined by 4 bytes.

TABLE 7-2: GPIO CONDITIONS

Byte	Condition	Definition
Byte 1	Flags	bit 7: 1 signifies last condition in group bit 4: Combination function (1:AND, 0:OR) bit 3: Signed (1) or unsigned (0) bits 2:0 Comparison function (0 : >, 1 : <, 2 : =, 3 : AND, 4 : NOR)
Byte 2	Condition selection	x00-x3F – SBData command code x40 – State flags x41 – GPIO flags x42 – VCELL-min x43 – VCELL-max x44 – VCELL-diff x45 – Misc. flags
Byte 3 Byte 4	Condition threshold	Constant

Each condition in the table is processed by applying a "comparison function" to the selected data ("condition selection") and the given constant ("condition threshold"). The result of this operation ("true" or "false") from each condition in the group is combined as dictated by the "AND-OR" "combination function" bit in the flag byte. Because the "AND" function has precedence over the "OR", processing the CG can be described as OR'ing subgroups of ANDs (see Example 7-1 below).

One 8-bit timer (clocked at 500 msec) is associated with all 16 CSF(s). The timer compared to its threshold is an implied "AND" term to the CG (i.e., if processing of the CG to set the CSF results in "true", the timer is incremented and if timer >= threshold, the SF is set; otherwise, the SF is not set even though the GC is satisfied). If processing of the CG to set the CSF results in "false", the timer is set to zero. The timer is not allowed to increment past the threshold.

The conditions in the order they are stored in memory will build the activation equation until bit 7 of byte 1 is set, signifying the last condition of the group. At that point, the next group of conditions is the Reset equation. When the next to last condition bit is set, a new activation group begins.

EXAMPLE 7-1: CONDITION GROUPS

Example Condition Group:
(VCELL-min < 3200) .AND. (CURR > 100) .OR. (TEMP > 60) .AND. (CURR > 200)
because of precedence the equation would be interpreted:
((VCELL-min < 3200) .AND. (CURR > 100)) .OR. ((TEMP > 60) .AND. (CURR > 200))

Example Reset Condition Group:
(VCELL-min > 3200) OR (CURR = 200)

TABLE 7-3: CONDITIONS FOR EXAMPLE 7-1

Condition	Byte 1	Byte 2	Byte 3, 4	Description
1	x01	x42	x0C80	OR VCELL-min < 3200
2	x10	x0A	x0064	AND CURR > 100
3	x00	x08	x0D02	OR TEMP > 60°C (3330 degrees K * 10)
4	x80	x0A	x00C8	AND CURR > 200 (last condition bit set)
1	x00	x42	x0C80	OR VCELL-min > 3200
2	x82	x0A	x00C8	OR CURR = 200 (last condition bit set)

TABLE 7-4: PARAMETERS

Name	Length	Description
SAFE_GPIO_MASK_00	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_01	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_02	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_03	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_04	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_05	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_06	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_07	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_08	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_09	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_10	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_GPIO_MASK_11	2	Mask applied to the CSF, if <> 0, GPIO is set
SAFE_TIMER_LIMIT_0	1	Timer threshold/limit (500 msec tics)
SAFE_TIMER_LIMIT_1	1	

TABLE 7-4: PARAMETERS (CONTINUED)

Name	Length	Description
SAFE_TIMER_LIMIT_2	1	
SAFE_TIMER_LIMIT_3	1	
SAFE_TIMER_LIMIT_4	1	
SAFE_TIMER_LIMIT_5	1	
SAFE_TIMER_LIMIT_6	1	
SAFE_TIMER_LIMIT_7	1	
SAFE_TIMER_LIMIT_8	1	
SAFE_TIMER_LIMIT_9	1	
SAFE_TIMER_LIMIT_10	1	
SAFE_TIMER_LIMIT_11	1	
SAFE_TIMER_LIMIT_12	1	
SAFE_TIMER_LIMIT_13	1	
SAFE_TIMER_LIMIT_14	1	
SAFE_TIMER_LIMIT_15	1	
SAFE_FLAG_COUNT	1	Number of CSF(s) to process, 0-16 (there must be 2 condition groups (CGs) per CSF)
SAFE_CONDITION	4	Condition (start of table)
. . .	4	Condition
SAFE_CONDITION	4	Condition (end of table)

7.1 LED Parameters

When configured as LED drivers, the following parameters determine the State-Of-Charge at which each LED will turn on.

TABLE 7-5: LED PARAMETERS

Name	Length	Definition
LED_MASK	1	Mask defining GPIO(s) used for LED display(s) (1 = LED)
LED_VALUE_0	1	GPIO 0 SOC value (SOC >= LED_VALUE, LED = on)
LED_VALUE_1	1	GPIO 1 SOC value (SOC >= LED_VALUE, LED = on)
LED_VALUE_2	1	GPIO 2 SOC value (SOC >= LED_VALUE, LED = on)
LED_VALUE_3	1	GPIO 3 SOC value (SOC >= LED_VALUE, LED = on)
LED_VALUE_4	1	GPIO 4 SOC value (SOC >= LED_VALUE, LED = on)
LED_VALUE_5	1	GPIO 5 SOC value (SOC >= LED_VALUE, LED = on)
LED_VALUE_6	1	GPIO 6 SOC value (SOC >= LED_VALUE, LED = on)
LED_VALUE_7	1	GPIO 7 SOC value (SOC >= LED_VALUE, LED = on)
LED_ICHG	2	Current threshold for LED display
LED_DUTYCYCLE	1	Duty cycle of LED drivers
GPIO_SWITCHMASK	2	Mask for switch input(s). If switch is active-high, all bits are '0' except switch pin. If switch is active-low, all bits are '1' except switch pin.
LED_DISPLAY_TIME	1	Number of 500 ms periods LEDs are lit after switch press

8.0 SMBus/SBData INTERFACE

The PS501 uses a two-pin System Management Bus (SMBus) protocol to communicate to the Host. One pin is the clock and one pin is the data. The SMBus port responds to all commands in the Smart Battery Data Specification (SBData). To receive information about the battery, the Host sends the appropriate commands to the SMBus port. Certain alarms, warnings and charging information may be sent to the Host by the PS501 automatically. The SMBus protocol is explained in this chapter. The SBData command set is summarized in Table 8-1.

The PS501 SMBus communications port is fully compliant with the System Management Bus Specification, Version 1.1 and supports all previous and new requirements, including bus time-outs (both slave and master), multi-master arbitration and collision detection/recovery. The SMBus port serves as a slave for both read and write functions, as well as a master for write word functions. SMBus slave protocols supported include read word, write word, read block and write block. Master mode supports write word protocols. The PS501 meets and exceeds the Smart Battery Data Specification, Version 1.1/1.1a requirements. The PS501 is compliant with System Management Bus Specification 1.0.

The PS501 fully implements the Smart Battery Data (SBData) Specification v1.1. The SBData Specification defines the interface and data reporting mechanism for an SBS compliant Smart Battery. It defines a consistent set of battery data to be used by a power management system to improve battery life and system run-time, while providing the user with accurate information. This is accomplished by incorporating fixed, measured, calculated and predicted values, along with charging and alarm messages, with a simple communications mechanism between a Host system, Smart Batteries and a Smart Charger.

The PS501 provides full implementation of the SBData set with complete execution of all the data functions, including sub-functions and control bits and flags, compliance to the accuracy and granularity associated with particular data values and proper SMBus protocols and timing.

8.1 SBData Function Description

The following subsections document the detailed operation of all of the individual SBData commands.

8.1.1 ManufacturerAccess (0x00)

Internal use only.

8.1.2 RemainingCapacityAlarm (0x01)

Sets or reads the low capacity alarm value. Whenever the remaining capacity falls below the low capacity alarm value, the Smart Battery sends alarm warning messages to the SMBus Host with the REMAINING_CAPACITY_ALARM bit set. A low capacity alarm value of '0' disables this alarm.

8.1.3 RemainingTimeAlarm (0x02)

Sets or reads the remaining time alarm value. Whenever the AverageTimeToEmpty falls below the remaining time value, the Smart Battery sends alarm warning messages to the SMBus Host with the REMAINING_TIME_ALARM bit set. A remaining time value of '0' disables this alarm.

TABLE 8-1: SMART BATTERY DATA FUNCTIONS

SBData Function Name	Command Code	Access	Parameter Reference	Units
ManufacturerAccess – Write[1]	0x00	R/W		
ManufacturerAccess – Read[1]	0x00	R/W		
RemainingCapacityAlarm	0x01	R/W	**RemCapAl**	mAh or 10 mWh
RemainingTimeAlarm	0x02	R/W	**RemTimeAl**	Minutes
BatteryMode	0x03	R/W		Bit code
AtRate	0x04	Read		mAh or 10 mWh
AtRateTimeToFull	0x05	Read		Minutes
AtRateTimeToEmpty	0x06	Read		Minutes
AtRateOK	0x07	Read		Binary 0/1 (LSB)
Temperature	0x08	Read		0.1°K
Voltage	0x09	Read		mV
Current	0x0a	Read		mA
AverageCurrent	0x0b	Read		mA
MaxError	0x0c	Read		%
RelativeStateOfCharge	0x0d	Read		%
AbsoluteStateOfCharge	0x0e	Read		%
RemainingCapacity	0x0f	Read		mAh or 10 mWh
FullChargeCapacity	0x10	Read		mAh or 10 mWh
RunTimeToEmpty	0x11	Read		Minutes
AverageTimeToEmpty	0x12	Read		Minutes
AverageTimeToFull	0x13	Read		Minutes
ChargingCurrent	0x14	Read	**ChrgCurr** or **ChrgCurrOff**	mA
ChargingVoltage	0x15	Read	**ChrgVolt** or **ChrgVoltOff**	mV
BatteryStatus	0x16	Read	**BatStatus**	Bit code
CycleCount	0x17	Read	**Cycles**	Integer
DesignCapacity	0x18	Read	**DesignCapacity**	mAh or 10 mWh
DesignVoltage	0x19	Read	**DesignVPack**	mV
SpecificationInfo	0x1a	Read	**SBDataVersion**	Coded
ManufactureDate	0x1b	Read	**Date**	Coded
SerialNumber	0x1c	Read	**SerialNumber**	Not specified
Reserved	—	—	—	—
ManufacturerName	0x20	Read	**MFGName**	ASCII text string
DeviceName	0x21	Read	**DeviceName**	ASCII text string
DeviceChemistry	0x22	Read	**Chemistry**	ASCII text string
ManufacturerData	0x23	Read	**MFGData**	Hex string
OptionalMfgFunction4	0x3c	Read	V1 Cell Voltage	mV
OptionalMfgFunction3	0x3d	Read	V2 Cell Voltage	mV
OptionalMfgFunction2	0x3e	Read	V3 Cell Voltage	mV
OptionalMfgFunction1	0x3f	Read	V4 Cell Voltage	mV

Note 1: Reserved.

8.1.4 BatteryMode (0x03)

This function selects the various battery operational modes and reports the battery's capabilities, modes and condition.

Bit 0: INTERNAL_CHARGE_CONTROLLER

Bit set indicates that the battery pack contains its own internal charge controller. When the bit is set, this optional function is supported and the CHARGE_CONTROLLER_ENABLED bit will be activated.

Bit 1: PRIMARY_BATTERY_SUPPORT

Bit set indicates that the battery pack has the ability to act as either the primary or secondary battery in a system. When the bit is set, this optional function is supported and the PRIMARY_BATTERY bit will be activated.

Bit 2-6: Reserved

Bit 7: CONDITION_FLAG

Bit set indicates that the battery is requesting a conditioning cycle. This typically will consist of a full charge to full discharge, back to full charge of the pack. The battery will clear this flag after it detects that a conditioning cycle has been completed.

Bit 8: CHARGE_CONTROLLER_ENABLED

Bit is set to enable the battery pack's internal charge controller. When this bit is cleared, the internal charge controller is disabled (default). This bit is active only when the INTERNAL_CHARGE_CONTROLLER bit is set.

Bit 9: PRIMARY_BATTERY

Bit is set to enable a battery to operate as the primary battery in a system. When this bit is cleared, the battery operates in a secondary role (default). This bit is active only when the PRIMARY_BATTERY_SUPPORT bit is set.

Bit 10-12: Reserved

Bit 13: ALARM_MODE

Disables the Smart Battery's transmission of the BatteryStatus bits on an alarm condition. Will reset to enabled after 60 seconds.

Bit 14: CHARGER_MODE

Enables or disables the Smart Battery's transmission of ChargingCurrent and ChargingVoltage messages to the Smart Battery Charger. When set, the Smart Battery will not transmit ChargingCurrent and ChargingVoltage values to the charger. When cleared, the Smart Battery will transmit the ChargingCurrent and ChargingVoltage values to the charger when charging is desired.

Bit 15: CAPACITY_MODE

Indicates if capacity information will be reported in mA/mAh or 10 mW/10 mWh. When set, the capacity information will be reported in 10 mW/10 mWh. When cleared, the capacity information will be reported in mA/mAh.

8.1.5 AtRate (0x04)

AtRate is a value of current or power that is used by three other functions: AtRateTimeToFull, AtRateTimeToEmpty and AtRateOK:

- AtRateTimeToFull returns the predicted time to full charge at the AtRate value of charge current.
- AtRateTimeToEmpty function returns the predicted operating time at the AtRate value of discharge current.
- AtRateOK function returns a Boolean value that predicts the battery's ability to supply the AtRate value of additional discharge current for 10 seconds.

8.1.6 AtRateTimeToFull (0x05)

Returns the predicted remaining time to fully charge the battery at the AtRate value (mA). The AtRateTimeToFull function is part of a two-function call set used to determine the predicted remaining charge time at the AtRate value in mA. It will be used immediately after the SMBus Host sets the AtRate value.

8.1.7 AtRateTimeToEmpty (0x06)

Returns the predicted remaining operating time if the battery is discharged at the AtRate value. The AtRateTimeToEmpty function is part of a two-function call set used to determine the remaining operating time at the AtRate value. It will be used immediately after the SMBus Host sets the AtRate value.

8.1.8 AtRateOK (0x07)

Returns a Boolean value that indicates whether or not the battery can deliver the AtRate value of additional energy for 10 seconds (Boolean). If the AtRate value is zero or positive, the AtRateOK function will always return true. The AtRateOK function is part of a two-function call set used by power management systems to determine if the battery can safely supply enough energy for an additional load. It will be used immediately after the SMBus Host sets the AtRate value.

8.1.9 Temperature (0x08)

Returns the cell pack's internal temperature in units of 0.1°K.

8.1.10 Voltage (0x09)

Returns the pack voltage (mV).

8.1.11 Current (0x0a)

Returns the current being supplied (or accepted) through the battery's terminals (mA).

8.1.12 AverageCurrent (0x0b)

Returns a one-minute rolling average based on at least 60 samples of the current being supplied (or accepted) through the battery's terminals (mA).

8.1.13 MaxError (0x0c)

Returns the expected margin of error (%) in the State-Of-Charge calculation. For example, when MaxError returns 10% and RelativeStateOfCharge returns 50%, the RelativeStateOfCharge is actually between 50% and 60%. The MaxError of a battery is expected to increase until the Smart Battery identifies a condition that will give it higher confidence in its own accuracy. For example, when a Smart Battery senses that it has been fully charged from a fully discharged state, it may use that information to reset or partially reset MaxError. The Smart Battery can signal when MaxError has become too high by setting the CONDITION_FLAG bit in BatteryMode.

8.1.14 RelativeStateOfCharge (0x0d)

Returns the predicted remaining battery capacity expressed as a percentage of FullChargeCapacity (%).

8.1.15 AbsoluteStateOfCharge (0x0e)

Returns the predicted remaining battery capacity expressed as a percentage of DesignCapacity (%). Note that AbsoluteStateOfCharge can return values greater than 100%.

8.1.16 RemainingCapacity (0x0f)

Returns the predicted remaining battery capacity. The RemainingCapacity value is expressed in either current (mAh) or power (10 mWh), depending on the setting of the BatteryMode's CAPACITY_MODE bit.

8.1.17 FullChargeCapacity (0x10)

Returns the predicted pack capacity when it is fully charged. It is based on either current or power, depending on the setting of the BatteryMode's CAPACITY_MODE bit.

8.1.18 RunTimeToEmpty (0x11)

Returns the predicted remaining battery life at the present rate of discharge (minutes). The RunTimeToEmpty value is calculated based on either current or power, depending on the setting of the BatteryMode's CAPACITY_MODE bit. This is an important distinction because use of the wrong calculation mode may result in inaccurate return values.

8.1.19 AverageTimeToEmpty (0x12)

Returns a one-minute rolling average of the predicted remaining battery life (minutes). The AverageTimeToEmpty value is calculated based on either current or power, depending on the setting of the BatteryMode's CAPACITY_MODE bit. This is an important distinction because use of the wrong calculation mode may result in inaccurate return values.

8.1.20 AverageTimeToFull (0x13)

Returns a one-minute rolling average of the predicted remaining time until the Smart Battery reaches full charge (minutes).

8.1.21 ChargingCurrent (0x14)

Sets the maximum charging current for the Smart Charger to charge the battery. This can be written to the Smart Charger from the Smart Battery or requested by the Smart Charger from the battery.

8.1.22 ChargingVoltage (0x15)

Sets the maximum charging voltage for the Smart Charger to charge the battery. This can be written to the Smart Charger from the Smart Battery or requested by the Smart Charger from the battery.

8.1.23 BatteryStatus (0x16)

Returns the Smart Battery's status word (flags). Some of the BatteryStatus flags, like REMAINING_CAPACITY_ALARM and REMAINING_TIME_ALARM, are calculated based on either current or power, depending on the setting of the BatteryMode's CAPACITY_MODE bit. This is important because use of the wrong calculation mode may result in an inaccurate alarm. The BatteryStatus function is used by the power management system to get alarm and status bits, as well as error codes, from the Smart Battery. This is basically the same information returned by the SBData AlarmWarning function except that the AlarmWarning function sets the error code bits all high before sending the data. Also, information broadcasting is disabled in the PS501.

Battery Status Bits:

bit 15: OVER_CHARGED_ALARM
bit 14: TERMINATE_CHARGE_ALARM
bit 13: Reserved
bit 12: OVER_TEMP_ALARM
bit 11: TERMINATE_DISCHARGE_ALARM
bit 10: Reserved
bit 9: REMAINING_CAPACITY_ALARM
bit 8: REMAINING_TIME_ALARM
bit 7: INITIALIZED
bit 6: DISCHARGING
bit 5: FULLY_CHARGED
bit 4: FULLY_DISCHARGED

The Host system assumes responsibility for detecting and responding to Smart Battery alarms by reading the BatteryStatus to determine if any of the alarm bit flags are set. At a minimum, this requires the system to poll the Smart Battery BatteryStatus every 10 seconds at all times the SMBus is active.

8.1.24 CycleCount (0x17)

CycleCount is updated to keep track of the total usage of the battery. CycleCount is increased whenever an amount of charge has been delivered to, or removed from, the battery equivalent to the full capacity.

8.1.25 DesignCapacity (0x18)

Returns the theoretical capacity of a new pack. The DesignCapacity value is expressed in either current or power, depending on the setting of the BatteryMode's CAPACITY_MODE bit.

8.1.26 DesignVoltage (0x19)

Returns the theoretical voltage of a new pack (mV).

8.1.27 SpecificationInfo (0x1a)

Returns the version number of the Smart Battery specification the battery pack supports.

8.1.28 ManufactureDate (0x1b)

This function returns the date the cell pack was manufactured in a packed integer. The date is packed in the following fashion: (year-1980) * 512 + month * 32 + day.

8.1.29 SerialNumber (0x1c)

This function is used to return a serial number. This number, when combined with the ManufacturerName, the DeviceName and the ManufactureDate, will uniquely identify the battery.

8.1.30 ManufacturerName (0x20)

This function returns a character array containing the battery manufacturer's name.

8.1.31 DeviceName (0x21)

This function returns a character string that contains the battery's name.

8.1.32 DeviceChemistry (0x22)

This function returns a character string that contains the battery's chemistry. For example, if the DeviceChemistry function returns "NiMH", the battery pack would contain nickel metal hydride cells. The following is a partial list of chemistries and their expected abbreviations. These abbreviations are not case sensitive.

Lead Acid: PbAc
Lithium Ion: LION
Nickel Cadmium: NiCd
Nickel Metal Hydride: NiMH
Nickel Zinc: NiZn
Rechargeable Alkaline-Manganese: RAM
Zinc Air: ZnAr

8.1.33 ManufacturerData (0x23)

This function allows access to the manufacturer data contained in the battery (data).

8.1.34 OptionalMfgFunction

The PS501 includes new SBData functions using the OptionalMfgFunction command codes. The command codes, 3C hex to 3F hex, report the individual cell voltages as measured by the analog-to-digital converter. These voltages are reported in mV and are calculated to include compensation for calibration and sense resistance voltage drops. Only one cell voltage is measured per measurement cycle (depending on Run or Sample mode operation).

Rapid voltage changes will see some variation in voltages due to the delay of measurement. These voltage values may be used for cell balancing or other functions as the Host system may desire.

TABLE 8-2: PS501 ALARMS AND STATUS SUMMARY

Battery Status	Set Condition	Clear Condition
FULLY_CHARGED bit	Set at End-Of-Charge Condition: Charge FET off AND Any VC(x) input > 4.175V AND IAVG < EOC_IAVG for **ChrgCntrlTimer** number of consecutive counts	RelativeStateOfCharge ( ) < **ClrFullyChrg** (default RSOC = 80%)
OVER_CHARGED_ALARM bit	VCELLX > **TCAVolt** (default 4.5V/Cell)	All VCELLX < **TCAVolt**
TERMINATE_CHARGE_ALARM bit	VCELLX > **TCAVolt** (default 4.5V/Cell) OR Charging Temperature ( ) > **ChrgMaxTemp** (default 60°C) OR FULLY_CHARGED bit = 1	All VCELLX < **TCAVolt** AND Temperature ( ) < **ChrgMaxTemp** AND Current ( ) = < 0
OVER_TEMP_ALARM bit	Temperature ( ) > **HighTempAl** (default 55°C)	Temperature ( ) < **HighTempAl**
TERMINATE_DISCHARGE_ALARM bit	Primary Method: VCELLX < VEOD1 (per look-up table) AND Above condition continues for **NearEODRecheck** time. Secondary Method: VCELLX < VEOD2 (default 3.1V/Cell) AND Above condition continues for **EODRecheck** time.	Primary Method: All VCELLX > VEOD1 OR Current ( ) > 0 Secondary Method: All VCELLX > VEOD2 OR Current ( ) > 0
REMAINING_CAPACITY_ALARM bit	RemainingCapacity ( ) < RemainingCapacityAlarm ( )	RemainingCapacity ( ) > RemainingCapacityAlarm ( )
REMAINING_TIME_ALARM bit	AverageTimeToEmpty ( ) < RemainingTimeAlarm ( )	AverageTimeToEmpty ( ) > RemainingTimeAlarm ( )
FULLY_DISCHARGED bit	RemainingCapacity ( ) = 0	RelativeStateOfCharge ( ) > **ClrFullyDischrg** (default RSOC = 20%)

TABLE 8-3: Temperature, ChargingCurrent ( ) AND ChargingVoltage ( ) SUMMARY

Temperature ( ) > HighTempAl (default 60°C)	
Charging	**Discharging**
TERMINATE_CHARGE_ALARM and OVER_TEMP_ALARM	OVER_TEMP_ALARM
Cleared	Temperature ( ) < **HighTempAl**

Temperature ( ) > ChrgMaxTemp (default 50°C)	**Temperature ( ) > DischrgMaxTemp (default 65°C)**
Charging	**Discharging**
ChargingCurrent ( ) = **ChrgCurrOff** ChargingVoltage ( ) = **ChrgVoltOff**	

Temperature ( ) < ChrgMinTemp
ChargingCurrent ( ) = **ChrgCurrOff** ChargingVoltage ( ) = **ChrgVolt**

For all other temperature conditions: ChargingCurrent ( ) = **ChrgCurr**
ChargingVoltage ( ) = **ChrgVolt**

9.0 PARAMETER SETUP

This section documents all of the programmable parameters that are resident in the EEPROM. The Parameter Set is organized into the following functional groups:

1. Pack Information
2. Capacity Calculations
3. EOD and FCC Relearn
4. Charge Control
5. GPIO
6. PS501 Settings
7. SBData Settings
8. Calibration

TABLE 9-1: PACK INFORMATION

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
BatStatus	1	0	255	b01000000	Lower byte of SBData register for BatteryStatus.
Cells	1	0	255	4	Number of cells in the battery pack.
Chemistry	4	—	—	LION	SBS data for chemistry. Can be any ASCII string. The chemistry name can be programmed here and retrieved with the SBData DeviceChemistry command.
Date	2	0	65535	0x3042	SBData value for ManufactureDate. The date of manufacture of the battery pack can be programmed here and retrieved with the SBData ManufactureDate command. Coding: Date = (Year-1980) x 512 + Month x 32 + Day
DesignCapacity	2	0	65535	4400	SBData value for DesignCapacity. This is the first capacity loaded into the FullChargeCapacity upon power-up.
DesignVPack	2	0	65535	14800	SBData value for DesignVoltage.
DeviceName	8	—	—	PS501	SBData value for DeviceName. Can be any ASCII string. The battery circuit device name can be programmed here and retrieved with the SBData DeviceName command.
MFGData	4	—	—	0x0	SBS string for ManufacturerData.
MFGName	10	—	—	Microchip	SBS string for ManufacturerName. Can be any ASCII string, typically the name of the battery pack manufacturer. Length of string is defined by MfgNameLength.
PackRes	2	0	65535	65	Resistance of pack.
PW1	2	0	65535	AA4D	First password for the battery pack lock.
PW2	2	0	65535	D4AA	Second password for the battery pack lock.
SpecInfo	2	0	65535	33	Specification info according to SBS Spec. 0011, refers to Smart Battery Specification version 1.1.
SerialNumber	2	0	65535	100	SBData value for SerialNumber. The serial number of the battery pack can be programmed here and retrieved with the SBData SerialNumber command.

TABLE 9-2: CAPACITY CALCULATIONS

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
CurrError	1	0	255	1	Current measurement error. This is the error due to the accuracy of the A/D converter to measure and integrate the current, 255 = 24.9%.
Cycles	2	0	65535	0	SBData register for CycleCount. **Cycles** is updated to keep track of the total usage of the battery. **Cycles** is increased whenever an amount of charge has been delivered to or removed from the battery, equivalent to the full capacity. For a 4000 mAh battery, **Cycles** is increased every time 4000 mAh goes through the battery terminals in any direction.
InitialCap	2	0	65535	2048	The initial capacity of the battery. When the PS501 is first powered up and initialized, before a learning cycle takes place to learn the full capacity, the full capacity will take the value programmed into **InitialCap** to compute relative State-Of-Charge percentage.
LowCurrError	1	0	255	25	Current offset for error calculation. Since the error of the A/D converter is proportional to the level of current it is measuring, the error term can be too low when the current is very low. For this reason, the **LowCurrError** will compensate the ERR term for low currents. **LowCurrError** milli-Amps are added to the current when factoring in the error. Thus, the error is: Error = (Current + **LowCurrError**) * **CurrError**.
NChangeState	1	0	255	8	State change delay filter. Delays the change between “charge increasing” state and “charge decreasing” state based on current direction. To avoid problems with current spikes in opposite directions, a delay filter is built-in to control when to change from charging status to discharging status. The current must change directions and stay in the new direction for CST_DELAY * period before the status is changed and capacity is increased or decreased as a result of the new current direction.
NullCurr	1	0	255	3	A zero zone control is built into the PS501 so that any small inaccuracy doesn’t actually drain the gas gauge, when in fact the current is zero. For this reason, current less than **NullCurr** mA in either direction will be measured as zero.
PwrConsumption	1	0	65535	140	Current consumption of the battery module. This is the average current that the battery module typically draws from the battery (255 = 1 mA).
SelfDischrgErr	1	0	255	1	Self-discharge error. This is the error inherent in the ability of the self-discharge look-up tables to meet actual battery characteristics, 255 = 100%.

TABLE 9-3: EOD AND FCC RELEARN

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
ADLNearEmpty	2	0	65535	3600	Cell voltage at which A/D switches to emphasize voltage over current measurement near EOD (mV).
ADLNearFull	2	0	65535	4000	Cell voltage at which A/D switches to emphasize voltage over current measurement near EOC (mV).
EOD1Cap	2	0	65535	150	The capacity that remains in the battery at VEOD1. This is typically a small amount used to power a shutdown sequence for the system.
EOD1Voltage	2	0	65535	3100	Voltage for EOD1 fixed voltage point (mV).
EOD2Recheck	1	0	255	6	Delay filter for the EOD2 condition. Number of checks before EOD2 trigger. The End-Of-Discharge conditions must remain for at least this number of periods before being considered true, to help filter out false empty conditions due to spikes. EOD2 condition is based on the Variable Voltage Look-up Table.
FullCapacity	2	0	65535	4150	Learned value of battery capacity. Used for SBData value of FullChargeCapacity. This is a learned parameter which is the equivalent of all charge counted from fully charged to fully discharged, including self-discharge and error terms. This is reset after a learning cycle and used for remaining capacity and relative State-Of-Charge calculations.
RelearnCurrLim	2	0	65535	10,000	Value of measured current that prevents a capacity relearn from occurring when a terminate discharge alarm condition is reached at End-Of-Discharge (EOD). A learning cycle will happen when the battery discharges from fully charged, all the way to fully discharged, with no charging in between and the discharge current never exceeds **RelearnCurrLim** (Example: 3000). A relearn will only occur if current does not exceed 3000 mA.
RelearnLimit	1	0	255	205	The maximum relearn limit. The maximum percentage that the FULL_CAPACITY can change after a learning cycle, where 255 = 100%.
RelearnMaxErr	2	0	65535	300	Maximum error for learning **FullCapacity**. The FULL_CAPACITY will not be learned after a learning cycle if the error is too great.
RLCycles	1	0	255	2	The number of initial cycles without **RelearnLimit**. The initial number of cycles where **RelearnLimit** is not active. **FullCapacity** can vary more greatly with the first learning cycle since the initial capacity may not be correct, thus this should be set to at least '2'.
Vempty	2	0	65535	3000	Second and final End-Of-Discharge voltage point. At this point, remaining capacity is optionally set to '0'.

TABLE 9-4: CHARGE CONTROL

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
ChrgCurr	2	0	65535	3000	This is the full charging current that the battery requires during normal charging. It can be broadcasted to the charger or read from the PS501.
ChrgCurrOff	2	0	65535	0	Trickle charging current. This is a small amount of current that the charger should deliver when full charging needs to be halted temporarily due to high temperature.
ChrgMaxTemp	1	0	255	235	Temperature threshold when charging, Coded value = (Celsius * 10 + 200)/4. When the temperature exceeds **ChrgMaxTemp** and the battery is charging, then ChargingCurrent is set to **ChrgCurrOff** and ChargingVoltage is set to **ChrgVoltOff**.
ChrgMinTemp	1	0	255	50	Low temperature threshold, Charging coded value = (Celsius * 10 + 200)/4. When charging, if the temperature is less than **ChrgMinTemp**, then ChargingCurrent is set to **ChrgCurrOff** and ChargingVoltage is set to **ChrgVoltOff**.
ChrgVolt	2	0	65535	16800	This is the voltage required by the battery during normal charging.
ChrgVoltOff	2	0	65535	16800	Voltage required when charging should be halted.
ClrFullyChrg	1	0	255	90	Reset FULLY_CHARGED bit at this level, 100 = 100%. Once the FULLY_CHARGED bit is set, taper or pulse current will not be monitored any more. When discharging begins, the FULLY_CHARGED bit must remain set until the cell voltages are below EOC_VOLT so that a small current will not trigger a false End-Of-Charge trigger. Thus, **ClrFullyChrg** is set at about 90%. FULLY_CHARGED bit will be on until the battery has discharged to less than 90%.
ClrFullyDischrg	1	0	255	10	Reset FULLY_DISCHARGED bit, 100 = 100%. Once fully discharged bit is set, it will stay set until capacity rises above this value, typically 10%.
EOCCurAvg	2	0	65535	200	EOC trigger for pulse charging. If the average current during charging, with the CFET turned off, has dropped below the **AvgCurrEOCThresh** threshold for a pass count equal to the EEPROM parameter value **ChrgCntrlTimr** (typically between 8 and 16), the End-Of-Charge state will be reached.
EOCRecheck	1	0	255	6	Delay filter for the EOC condition. Number of checks before EOC trigger. The End-Of-Charge conditions must remain for at least this number of periods before being considered true, to help filter out false full conditions due to spikes.
EOCVolt	2	0	65535	4175	EOC trigger cell voltage. When any cell in the battery pack reaches this voltage, the End-Of-Charge determination will start monitoring the average current to determine when the battery is full. When the average current is in the proper range and the cell voltage is greater than EOC_VOLT, then FULLY_CHARGED bit in BatteryStatus will be set and terminate charge alarm will be active.
MaxTemp	1	0	65535	750	Maximum temperature measured (including external and internal sensor). Coded value = (Celsius * 10 + 200)/4. This is where the PS501 keeps track of the highest temperature it has measured.
PrechargeCurr	2	0	65535	100	Precharge current required. Posted to SBData ChargingCurrent during precharge conditions.

TABLE 9-4: CHARGE CONTROL (CONTINUED)

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
PrechargeMax	2	0	65535	500	Maximum precharge current allowed. When exceeded under precharge conditions, SBData ChargingCurrent is set to zero.
PrechargeTemp	1	0	255	60	Precharge temperature, Coded value = (Celsius * 10 + 200)/4. This is the temperature under which precharging should occur.
PrechargeVCell	2	0	65535	2500	Precharge cell voltage. This is the voltage under which precharging should occur.
SOCThreshold	1	0	255	125	Second EOC trigger based on State-Of-Charge, 100 = 100%. A second End-Of-Charge trigger is built into the PS501, such that if the State-Of-Charge exceeds a certain value, End-Of-Charge will be forced, even if the taper or pulse current was not detected. When State-Of-Charge reaches SOCThreshold, then End-Of-Charge will trigger.
StableCurr	1	0	255	50	EOC trigger current deviation level. In order to prevent current spikes from causing a premature taper current trigger, the average current and the instantaneous current must be within **StableCurr** of each other for the End-Of-Charge to trigger on the taper current.
TaperCRate	6	0	255	50	Upper limit EOC taper current based on temperature, 256/28/**RFactor** = 1C.
TaperLow	1	0	255	10	Lower limit EOC taper current, 256/28/**RFactor** = 1C.
TaperTemp	5	0	255	80	Temperature corresponding to **TaperCRate** byte.

TABLE 9-5: PS501 SETTINGS

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
AOMInt	1	0	255	60	The frequency of the auto-offset calibration cycle.
ConfigEOC	1	0	255	b01101001	Bit coded as follows: Bit Function 7 EOC on charge timer 6 EOC on **TCAVolt** 5 Limit remcap to FCC 4 Set overcharge alarm at EOC 3 Load capacity with FCC at EOC 2 Trigger EOC on RSOC > **MaxSOC** 1 Trigger EOC on average current 0 Trigger EOC on taper current
ConfigEOD	1	0	255	b01111000	Bit coded as follows: Bit Function 7 Evaluate EOD1 on fixed voltage (else table) 6 Set fully discharged bit on EOD1 5 Set capacity to residual capacity value immediately upon VEOD1 4 Set terminate discharge alarm on VEOD1 (default on VEOD2) 3 Learn FCC at VEOD1 2 TDA alarm at EOD2 1 Set capacity to zero at VEOD2 0 Do not allow capacity to drop below SCAP
ConfigCAP	1	0	255	11010100	Bit Function 7 Compensate remcap – the displayed remcap actually equals FCC minus capacity used, minus residual capacity due to temperature. remcap is compensated for temperature. 6 Remcap decrease only – when compensating, if temperature changed causing a decrease in residual capacity, do not let remcap rise to reflect this. Instead, hold it steady until discharge catches up. This is so user does not see capacity increase while discharging (though usable capacity may increase if the temperature changes, user would be confused). 5 Use compensated FCC – use compensated FCC to compute RSOC. Allows compensated RSOC to equal 100% at full charge (delete). 4 Limit RSOC to 99% until EOC. 3 Report compensated FCC – the compensated FCC is reported in SBData to allow for externally calculated RSOC (delete). 2 Set capacity to positive immediately upon charging. If discharged below zero, this allows capacity to count up immediately upon charging. 1 Learn unconditionally – relearn FCC no matter what. Typically we have a max. current and a max. error limitation on relearn. This would take away the limitations. Typically used for testing only. 0 Self-discharge disable.

TABLE 9-5: PS501 SETTINGS (CONTINUED)

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
ConfigLED	1	0	255	b10000010	Bit coded as follows: Bit Function 7 Disable Master mode 6 (free) 5 Enable fast LED time base 4 LED display while charging 3 Display the most significant LED only 2 LED using absolute SOC, else relative SOC 1 Flash LEDs on remaining time or remaining cap alarm 0 Flash LEDs while charging
FLAGS1	1	0	255	b11101011	Bit coded as follows: Bit Function 7 Enable precharge max current check 6 Hold charge current = 0 until next discharge 5 Int/Ext temperature 4 Disable Sleep in main Idle mode 3 Require null current for Low-Voltage Sleep mode 2 Disable safety GPIO 1 Pack resistance enable 0 Enable Sample mode detect
mWhConv	2	0	65535	2000	Constant for conversion from mAh to mWh.
NSample	1	0	255	10	Frequency of ADC activity in Sample mode. The A/D converter will take measurements every **NSample** period while in Sample mode. In Run mode, new measurements are taken every period.
OSCTrim	1	0	255	200	RC oscillator trimming.
SampleLimit	2	0	65535	15	Value used to determine the current threshold for entry/exit for Sample and Run modes in mA.
SMBMstrBaud	1	0	127	1	Master broadcast baud rate (512 kHz/4)/(**SMBMstrBaud** + 1).
SMBChrgrAddr	1	0	255	0x12	Address to broadcast charger messages to.
SMBHostAddr	1	0	255	0x10	Address to broadcast host messages to.
SMBAlrmInterval	1	0	255	120	Delay between alarm broadcasts, units 0.5 seconds.
Config1	1	0	255	100	Bootload configuration.
SleepVPack	2	0	65535	8800	The pack voltage at which the PS501 will enter Low-Voltage Sleep mode.
WakeUp	1	0	255	b00001011	When in the Low-Voltage Sleep mode (entry due to low voltage and Sample mode), there are four methods for waking up. They are voltage level, current level, SMBus activity and I/O pin activity. This value defines which wake-up functions are enabled and also the voltage wake-up level. The table below indicates the appropriate setting. Note that the setting is independent of the number of cells or their configuration. Wake-up: Bit Name Function 7 WakeIO Wake-up from I/O activity 6 WakeBus Wake-up from SMBus activity 5 WakeCurr Wake-up from current 4 WakeVolt Wake-up from voltage 3 Shelf-Sleep Use Ultra Low-Power mode for Shelf-Sleep mode 1 LV Sleep Mode Use Ultra Low-Power mode as Low-Voltage Sleep mode 0 Zero Remcap Set remcap to zero when entering Low-Voltage Sleep mode

TABLE 9-5: PS501 SETTINGS (CONTINUED)

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
WakeLevels	1	0	255	b11000110	Wake-up Voltage: WakeUp (2:0) — Voltage — Purpose 000 — 6.4V — 2 cells Li Ion 001 — 6.66V — 2 cells Li Ion 010 — 8.88V — 2 cells Li Ion 011 — 9.6V — 3 cells Li Ion 100 — 9.99V — 3 cells Li Ion 101 — 11.1V — 3 cells Li Ion 110 — 12.8V — 4 cells Li Ion 111 — 13.3V — 4 cells Li Ion Wake-up Current: WakeUp (7:3) 00000: Minimum 11000: Typical recommended 11111: Maximum

TABLE 9-6: SBData SETTINGS

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
HighTempAl	1	0	255	200	OVER_TEMP_ALARM threshold bit in AlarmWarning register, 0.1°C increments, Coded value = (Celsius * 10 + 200)/4. When the temperature exceeds **HighTempAl**, the OVER_TEMP_ALARM becomes active. If charging, the TERMINATE_CHARGE_ALARM also becomes active.
NChrgBroadcast	1	0	255	20	Frequency of charging condition broadcasts.
RemCapAl	2	0	65535	440	SBData value for **RemCapAl**. The SBData specification requires a default of DesignCapacity/10 for this value. When the remaining capacity calculation reaches the value of **RemCapAl**, the REMAINING_CAPACITY_ALARM bit will be set in the BatteryStatus register and an alarm broadcast to the Host will occur if alarm broadcasts are enabled.
RemTimeAl	2	0	65535	10	SBData value for **RemTimeAl**. SBData requires a default of 10 minutes for this value. When the RunTimeToEmpty calculation reaches the value of **RemTimeAl**, the REMAINING_TIME_ALARM bit in the BatteryStatus register will be set.
TCAVolt	2	0	65535	4400	Cell voltage when the battery sends TERMINATE_CHARGE_ALARM. This is a voltage higher than the End-Of-Charge voltage that will trigger a TERMINATE_CHARGE_ALARM in case EOC is not responded to by the charger.

TABLE 9-7: CALIBRATION

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
CalStatus	1	0	255	b10000000	Bit coded as follows: Bit Function 7 Factory calibrated 6 EE/Flash downloaded 5 RC oscillator 4 External temperature 3 Internal temperature 2 Current 1 Pack voltage 0 Cell voltages 0 = Not Calibrated 1 = Calibrated
CFCurr	2	0	65535	6844	Correction Factor for Current. Adjusts the scaling of the sense resistor current measurements. Used to calibrate the measurement of current at the RSHP and RSHN input pins. This is set for the size of the current sense resistor.
CFTempE	2	0	65535	1300	Correction Factor for Temperature. Adjusts the scaling of temperature measured across an external thermistor at the VNTC input pin.
CFTempI	2	0	65535	9102	Correction Factor for Temperature. Adjusts the scaling of temperature measured from the internal temperature sensor. Calibration: New CF_TEMP = Old CF_TEMP x (Thermometer[°C]/SBData Temperature[°C]) **Note:** SBData Temperature is reported in 0.1°K normally. It must be converted to °C for this equation.
CFVCell1	2	0	65535	22325	Calibration Correction Factor for VCELL1. Used to calibrate the measurement of individual cell voltage between the VCELL1-4 input pins.
CFVCell2	2	0	65535	22393	Calibration Correction Factor for VCELL2. Used to calibrate the measurement of individual cell voltage between the VCELL1-4 input pins.
CFVCell3	2	0	65535	22420	Calibration Correction Factor for VCELL3. Used to calibrate the measurement of individual cell voltage between the VCELL1-4 input pins.
CFVCell4	2	0	65535	22470	Calibration Correction Factor for VCELL4. Used to calibrate the measurement of individual cell voltage between the VCELL1-4 input pins.
CFVPack	2	0	65535	20045	Correction Factor for Pack Voltage. Adjusts the scaling of the pack voltage measurements. Used to calibrate the measurement of pack voltage between VCELL4 input pin and ground.
COCurr	2	-32768	32767	-12	Correction Offset for Current. This is the value the A/D reads when zero current is flowing through the sense resistor.
COD	1	-128	127	-12	Correction Offset Deviation. Offset value for the auto-zero calibration of the current readings. SBData Current[mA] = (I_A/D – CO_CURR – COD) x CF_CURR/16384 Calibration: CF_CURR = ((Ammeter[mA] x 16384) – 8192)/(Current – I_A/D at OCV)

TABLE 9-7: CALIBRATION (CONTINUED)

Parameter Name	# Bytes	Lower Limit	Upper Limit	Typical Value	Operational Description
COTempE	1	-128	127	-2	Correction Offset for Temperature. Offset = 0 used for temperature measurement using internal temperature sensor.
COTempI	2	-32768	32767	21647	Correction Offset for Temperature. Offset = 0 used for temperature measurement using internal temperature sensor.
COVCell	1	-128	127	0	Correction Offset for Cell Voltage. Offset factor used for individual cell voltage readings. SBData Voltage[mV] = (V_A/D – CO_VOLT) x CF_VOLT/2048 Calibration: New CF_VOLT = Old CF_VOLT x (Voltmeter[mV]/SBData Voltage[mV])
COVPack	1	-128	127	0	Correction Offset for Voltage. Offset factor used for pack voltage reading.
BGCal	1	0	255	0	Band gap voltage calibration factor.
RefCal	1	0	255	0	Reference voltage calibration factor.
VCellSafeVolt	2	0	65535	4150	Safe threshold for VCELLS.
SampleModeRechecks	1	0	255	6	# of OPCs current < **SampleLimit** before entering Sample mode.
AgeFactor	1	0	255	0	Scale factor for EOD voltage due to aging.
RemCapDelta	1	0	255	1	Maximum change in remaining capacity per measurement period.
Flags2	1	0	255	10000000	Bit 7: 1 = compensate remcap only on discharge Bit 6: internal test bit (CJ) Bit 5: internal test bit (CL) Bit 4: compensate remcap on null current Bit 3: unused Bit 2: 1 = cell balancing enabled Bit 1: 1 = compensate VC4/VPACK Bit 0: 1 = compensate VC1/VPACK
VcellmbSet	1	0	255	100	Voltage difference to trigger internal cell balancing.
VcellmbReset	1	0	255	80	Voltage difference to turn off cell balancing.
PwrUpTimer	1	0	255	4	Time during which GPIO are inactive after first power-up.
VC1Res	2	0	65535	0	Series resistance for VCELL1 measurement. 1/16384 ohms.
VC4Res	2	0	65535	0	Series resistance for VCELL4 measurement. 1/16384 ohms.
NPermLogCnt	1	0	255	0	Counter for logging Faults.
NPermLogReg	1	0	255	0	Register for logging Faults.
ReInitGPIO	2	0	65535	0	Register for resetting all GPIO during testing.
GPIODelayFlags	2	0	65535	0	Positive logic change of GPIO is delayed when upper byte is set. Lower byte maps to GPIO.
GPIODelayMS	1	0	255	0	GPIO delay in milliseconds, when **GPIODelayFlags** has the delay enabled.
ParamVersion	1	0	255	0	EEPROM version control number.
KeyByte	1	0	255	0xDA	EE keybyte must be 0xDA before P5 will exit Bootloader mode.
EOD1Recheck	1	0	255	8	Recheck period for EOD.
EOCTimeout	2	0	65535	60	EOC time-out timer.
CapErrReset	2	0	65535	0	Value to set MaxError to at EOD.
ImbalanceSOC	1	0	255	20	RSOC below which cell balance is measured.

10.0 ELECTRICAL CHARACTERISTICS

TABLE 10-1: ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_{CX}	Voltage at any VC(x) pin	-0.3	18.5	V
V_{PIN}	Voltage directly at any pin (except V_{CELLX})	-0.5	7.0	V
T_{BIAS}	Temperature under Bias	-20	85	°C
$T_{STORAGE}$	Storage Temperature (package dependent)	-35	125	°C

Note: These are stress ratings only. Stress greater than the listed ratings may cause permanent damage to the device. Exposure to absolute maximum ratings for an extended period may affect device reliability. Functional operation is implied only at the listed operating conditions below.

TABLE 10-2: DC CHARACTERISTICS (T_A = -20°C TO +85°C; V_{REG} (INTERNAL) = +3.3V ± 10%)

Symbol	Characteristic	Min	Typ	Max	Units	Condition
V_{SUPPLY}	Supply Voltage – Applied to VC(1)	5.6	—	18.0	V	
I_{DD}	Instantaneous Supply Current	—	220	—	µA	**(Note 1)**
I_{DDRUN}	Average Supply Current – Run Mode	—	175	—	µA	A/D active **(Note 1)**
I_{DDINS}	Inactive Supply Current – Sample Mode	—	150	—	µA	A/D inactive **(Note 1, 2)**
I_{DDSSLP}	Inactive Supply Current – Low-Power Mode	—	25	—	µA	A/D inactive **(Note 1, 2)**
I_{DDSLP}	Average Supply Current – Ultra Low-Power Mode	—	0.8	1	µA	Sleep mode **(Note 1, 4)**
I_{WAKE}	Wake-up Current Threshold from Sleep Mode – (voltage across sense resistor)	2.50	3.75	5.00	mV	
V_{IL}	Input Low Voltage – GPIO(7-0)	—	—	0.2 * V_{DDD}	V	
V_{IH}	Input High Voltage – GPIO(7-0)	0.8 * V_{DDD}	—	—	V	
$I_{IL-IOPU}$	GPIO Input Low Current – Pull-up Mode	-80	-110	-140	µA	
$I_{IH-IOPD}$	GPIO Input High Current – Pull-down Mode	-80	-110	-140	µA	
I_L	Leakage Current – GPIO pins Programmed as Outputs	—	1	2	µA	
V_{OL}	Output Low Voltage for GPIO(7-0)	—	—	0.6	V	I_{OL} = 0.5 mA
V_{OH-IO}	Output High Voltage for GPIO(7-0) (non-LED mode)	2.0	—	—	V	I_{OH} = 100 µA
V_{OH-LED}	Output High Voltage for GPIO(7-0) (LED mode)	2.0	—	—	V	I_{OH} = 10 mA **(Note 3)**
V_{SR}	Sense Resistor Input Voltage Range	-152	—	152	mV	
V_{NTC}	Thermistor Input Voltage Range	0	—	152	mV	
V_{REFT}	NTC Reference Voltage Output at V_{REFT} pin	—	150	—	mV	
V_{IL-SMB}	Input Low Voltage for SMBus pins	-0.5	—	0.8	V	
V_{IH-SMB}	Input High Voltage for SMBus pins	2.0	—	5.5	V	
V_{OL-SMB}	Output Low Voltage for SMBus pins	—	—	0.4	V	I_{PULLUP} = 350 µA
V_{OH-SMB}	Output High Voltage for SMBus pins	2.1	—	5.5	V	
$I_{PULLUP-SMB}$	Current through Pull-up Resistor or Current Source for SMBus pins	100	—	350	µA	
$I_{LEAK-SMB}$	Input Leakage Current – SMBus pins	—	—	± 5	µA	

Note 1: Does not include current consumption due to external loading on pins. Valid for a maximum voltage of 16.8 volts for the referenced current specification.

2: Sample mode current is specified during an A/D inactive cycle. Sample mode average current can be calculated using the formula: Average Sample Mode Supply Current = (I_{DDRUN} + (n – 1) * I_{DDINS})/n; where 'n' is the programmed sample rate.

3: During LED illumination, currents may peak at 10 mA but average individual LED current is typically 5 mA (using low-current, high-brightness devices).

4: Measured at 25°C.

TABLE 10-3: AC CHARACTERISTICS (T_A = -20°C TO +85°C; V_{REG} (INTERNAL) = +3.3V ± 10%)

Symbol	Characteristic	Min	Typ	Max	Units	Condition
f_{RC}	Internal RC Oscillator Frequency	—	512.000	—	kHz	
f_{AD}	Internal A/D Clock Frequency	—	$f_{RC}/16$	—	kHz	
t_{CONV}	A/D Conversion Measurement Time, n-bit + sign	—	$2^n/f_{AD}$	—	ms	

TABLE 10-4: AC CHARACTERISTICS – SMBus (T_A = -20°C TO +85°C; V_{REG} (INTERNAL) = +3.3V ± 10%)

Symbol	Characteristic	Min	Typ	Max	Units	Condition
f_{SMB}	SMBus Clock Operating Frequency	<1.0	—	100	kHz	Slave mode
$f_{SMB-MAS}$	SMBus Clock Operating Frequency	50	$f_{RC}/8$	68	kHz	Master mode **(Note 1)**
t_{BUF}	Bus Free Time between START and STOP	4.7	—	—	µs	
t_{SHLD}	Bus Hold Time after Repeated START	4.0	—	—	µs	
$t_{SU:STA}$	Setup Time before Repeated START	4.7	—	—	µs	
$t_{SU:STOP}$	STOP Setup Time	4.0	—	—	µs	
t_{HLD}	Data Hold Time	300	—	—	µs	
t_{SETUP}	Data Setup Time	250	—	—	µs	
$t_{TIMEOUT}$	Clock Low Time-out Period	10	—	35	ms	**(Note 2)**
t_{LOW}	Clock Low Period	4.7	—	—	µs	
t_{HIGH}	Clock High Period	4.0	—	50	µs	**(Note 3)**
$t_{LOW:SEXT}$	Message Buffering Time	—	—	10	ms	**(Note 4)**
$t_{LOW:MEXT}$	Message Buffering Time	—	—	10	ms	**(Note 5)**
t_F	Clock/Data Fall Time	—	—	300	ns	**(Note 6)**
t_R	Clock/Data Rise Time	—	—	1000	ns	**(Note 6)**

Note 1: Used when broadcasting AlarmWarning, ChargingCurrent and/or ChargingVoltage values to either a SMBus Host or a SMBus Smart Battery Charger. This is only used when the PS501 becomes a SMBus master for these functions. The receiving (slave) device may slow the transfer frequency. See SMBus Tutorial in P4 User's Guide for additional information.

2: The PS501 will time-out when the cumulative message time defined from Start-to-Ack, Ack-to-Ack or Ack-to-Stop exceeds the value of $t_{TIMEOUT}$, min. of 25 ms. The PS501 will reset the communication no later than $t_{TIMEOUT}$, max. of 35 ms.

3: t_{HIGH} max. provides a simple method for devices to detect bus idle conditions.

4: $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop.

5: $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from Start-to-Ack, Ack-to-Ack or Ack-to-Stop.

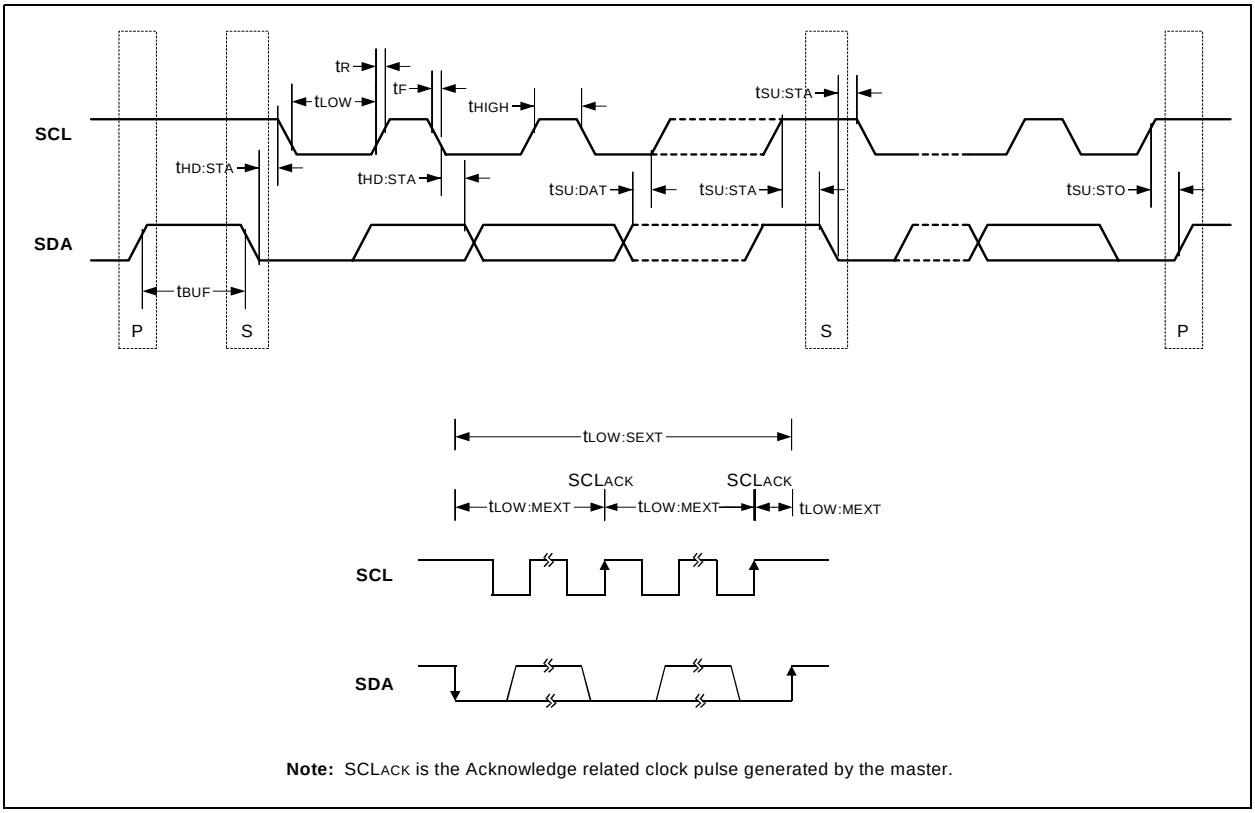
6: Rise and fall time is defined as follows:
$t_R = (V_{IL_{MAX}} -0.15)$ to $(V_{IH_{MIN}} +0.15)$
$t_F = 0.9\ V_{DD}$ to $(V_{IL_{MAX}} -0.15)$

TABLE 10-5: A/D CONVERTER CHARACTERISTICS (T_A = -20°C TO +85°C; V_{REG} (INTERNAL) = +3.3V ± 10%)

Symbol	Characteristic	Min	Typ	Max	Units	Condition
ADRES	A/D Converter Resolution	9	—	16	bits	**(Note 1)**
VADIN	A/D Converter Input Voltage Range (internal)	170	—	170	mV	Differential mode
		0	—	340	mV	Single-Ended mode
EVGAIN	Supply Voltage Gain Error	—	—	0.100	%	
EVOFFSET	Compensated Offset Error	—	—	0.100	%	
ETEMP	Temperature Gain Error	—	—	0.100	%	
EINL	Integrated Nonlinearity Error	—	—	0.004	%	

Note 1: Voltage is internal at A/D converter inputs. VSR and VNTC are measured directly. VC(x) inputs are measured using internal level translation circuitry that scales the input voltage range appropriately for the converter.

FIGURE 10-1: SMBus AC TIMING DIAGRAMS



Note: SCLACK is the Acknowledge related clock pulse generated by the master.

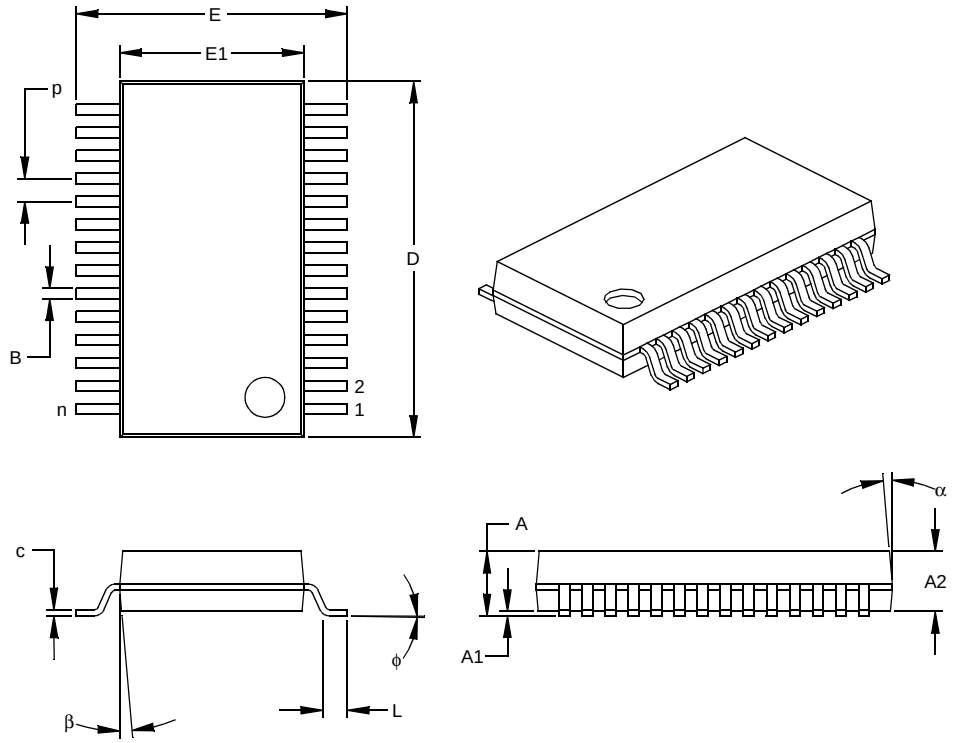
TABLE 10-6: SILICON TIME BASE CHARACTERISTICS (T_A = -20°C TO +85°C; V_{REG} (INTERNAL) = +5.0V ± 10%)

Symbol	Characteristic	Min	Typ	Max	Units	Condition
ETIME	Silicon Time Base Error	—	—	0.35	%	Bias resistor ROSC tolerance = 1%, TL = ± 100 PPM

11.0 PACKAGING INFORMATION

11.1 Mechanical Packaging Information

28-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.026			0.65	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.319	7.59	7.85	8.10
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.396	.402	.407	10.06	10.20	10.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	c	.004	.007	.010	0.10	0.18	0.25
Foot Angle	ϕ	0	4	8	0.00	101.60	203.20
Lead Width	B	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-150
Drawing No. C04-073

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