

NTE3092 Optoisolator Open Collector, NPN Transistor Output

Features:

- High Isolation Voltage
- High Speed: $t_{PHL} = 0.2\mu s$, $t_{PLH} = 1.0\mu s$ (Typ)
- Current Transfer Ratio: 19% Min

Applications:

- Digital Logic Isolation
- Line Receiver Feedback Control
- Power Supply Control
- Switching Power Supply
- Transistor Invertor

Absolute Maximum Ratings: ($T_A = +25^\circ C$ unless otherwise specified)

Input LED

Forward Current, I_F	25mA
Derate Above $70^\circ C$	0.8mA/ $^\circ C$
Pulsed Forward Current (Pulse Width = 1ms, Duty Cycle = 50%), I_{FP}	50mA
Derate Above $70^\circ C$	1.6mA/ $^\circ C$
Total Pulsed Forward Current (Pulse Width = 1s, 300pps), I_{FPT}	1A
Reverse Voltage, V_R	5V
Diode Power Dissipation, P_D	45mW
Derate Above $70^\circ C$	0.9mW/ $^\circ C$

Detector

Output Current, I_O	8mA
Peak Output Current, I_{OP}	16mA
Emitter-Base Reverse Voltage, V_{EB}	5V
Supply Voltage, V_{CC}	-0.5 to 15V
Output Voltage, V_O	-0.5 to 15V
Base Current, I_B	5mA
Output Power Dissipation, P_D	100mW
Derate Above $70^\circ C$	2mW/ $^\circ C$

Coupled

Operating Temperature Range, T_{opr}	-55° to $+100^\circ C$
Storage Temperature Range, T_{stg}	-55° to $+125^\circ C$

Electrical Characteristics: ($T_A = 0^\circ$ to $+70^\circ\text{C}$, Note 1 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Transfer Ratio	CTR	$V_{CC} = 4.5\text{V}$, $I_F = 16\text{mA}$, $V_O = 0.4\text{V}$, $T_A = +25^\circ\text{C}$, Note 2	19	24	–	%
		$V_{CC} = 4.5\text{V}$, $I_F = 16\text{mA}$, $V_O = 0.5\text{V}$, Note 2	15	21	–	%
Logic Low Output Voltage	V_{OL}	$V_{CC} = 4.5\text{V}$, $I_F = 16\text{mA}$, $I_O = 2.4\text{mA}$	–	0.1	0.4	V
Logic High Output Current	I_{OH}	$I_F = 0\text{mA}$, $V_O = V_{CC} = 5.5\text{V}$, $T_A = +25^\circ\text{C}$	–	3	500	nA
		$I_F = 0\text{mA}$, $V_O = V_{CC} = 15\text{V}$, $T_A = +25^\circ\text{C}$	–	0.1	100	μA
		$I_F = 0\text{mA}$, $V_O = V_{CC} = 15\text{V}$	–	–	250	μA
Logic Low Supply Current	I_{CCL}	$I_F = 16\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{V}$	–	40	–	μA
Logic High Supply Current	I_{CCH}	$I_F = 0\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{V}$, $T_A = +25^\circ\text{C}$	–	0.01	1.0	μA
		$I_F = 0\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{V}$	–	–	2.0	μA
Input Forward Voltage	V_F	$I_F = 16\text{mA}$, $T_A = +25^\circ\text{C}$	–	1.65	1.7	V
Temperature Coefficient of Forward Voltage		$I_F = 16\text{mA}$	–	–1.9	–	$\text{mV}/^\circ\text{C}$
Input Reverse Breakdown Voltage	$V_{(BR)R}$	$I_R = 10\mu\text{A}$, $T_A = +25^\circ\text{C}$	5	–	–	V
Input Capacitance	C_{IN}	$V_F = 0$, $f = 1\text{MHz}$	–	60	–	pF
Input–Output Insulation Leakage Current	I_{I-O}	45% Relative Humidity, $t = 5\text{s}$, $V_{I-O} = 3000\text{V}_{dc}$, $T_A = +25^\circ\text{C}$, Note 3	–	–	1.0	μA
Resistance (Input–Output)	R_{I-O}	$V_{I-O} = 500\text{V}_{dc}$, Note 3	–	10^{12}	–	Ω
Capacitance (Input–Output)	C_{I-O}	$f = 1\text{MHz}$, Note 3	–	0.6	–	pF
Transistor DC Current Gain	h_{FE}	$V_O = 5\text{V}$, $I_O = 3\text{mA}$	–	80	–	

Note 1. All typicals are at $T_A = +25^\circ\text{C}$.

Note 2. DC Current Transfer Ratio is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.

Note 3. Device is considered a two-terminal device: Pin1, Pin2, Pin3, and Pin4 shorted together and Pin8 shorted together.

Switching Characteristics: ($T_A = +25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $I_F = 16\text{mA}$, $R_L = 1.9\text{k}\Omega$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time to Logic Low at Output	t_{PHL}	$R_L = 1.9\text{k}\Omega$	–	0.2	0.8	μs
Propagation Delay Time to Logic High at Output	t_{PLH}	$R_L = 1.9\text{k}\Omega$	–	0.5	0.8	μs
Common Mode Transient Immunity at Logic High Level Output	CM_H	$I_F = 0\text{mA}$, $V_{CM} = 10\text{V}_{P-P}$, Note 4	–	1000	–	$\text{V}/\mu\text{s}$
Common Mode Transient Immunity at Logic Low Level Output	CM_L	$V_{CM} = 10\text{V}_{P-P}$, Note 4	–	–1000	–	$\text{V}/\mu\text{s}$
Bandwidth	BW	$R_L = 100\Omega$, Note 5	–	2	–	MHz

Note 4. Common mode transient immunity in High Logic level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm} , to assure that the output will remain in a Logic High state (i.e., $V_O > 2\text{V}$). Common mode mode transient immunity in the Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm} , to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8\text{V}$).

Note 5. The frequency at which the AC output voltage is 3dB below the low frequency asymptote.

Pin Connection Diagram

