

Features

- Temperature Range
 - Automotive: -40 °C to 125 °C
- High speed
 - t_{AA} = 15 ns
- Optimized voltage range: 2.5 V to 2.7 V
- Low active power: 220 mW (Max)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- CMOS for optimum speed/power
- Available in Pb-free and non Pb-free 44-pin TSOP II, 44-pin (400-Mil) Molded SOJ and Pb-free 48-ball FPBGA packages

Functional Description

The CY7C1021CV26 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has

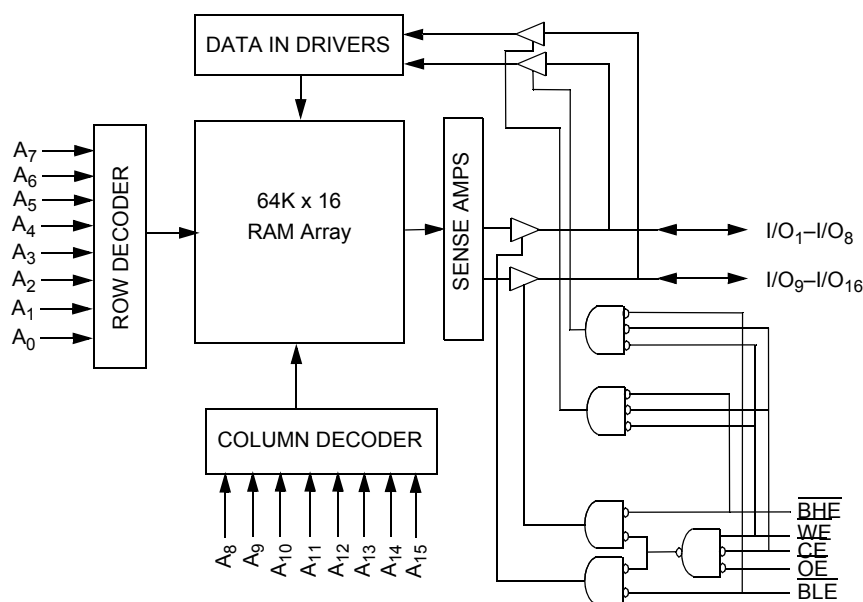
an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_9 to I/O_{16} . See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a Write operation (\overline{CE} LOW, and \overline{WE} LOW).

Logic Block Diagram



Contents

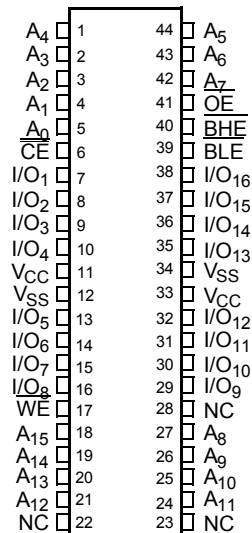
Selection Guide	3	Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)	8
Pin Configuration	3	Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, LOW)	9
Pin Definitions	3	Truth Table	9
Maximum Ratings	4	Ordering Information	10
Operating Range	4	Ordering Code Definitions	10
Electrical Characteristics	4	Package Diagrams	11
Capacitance	4	Acronyms	13
Thermal Resistance	4	Document Conventions	13
AC Test Loads and Waveforms	5	Units of Measure	13
Switching Characteristics	5	Document History Page	14
Switching Waveforms	7	Sales, Solutions, and Legal Information	15
Read Cycle No. 1	7	Worldwide Sales and Design Support	15
Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)	7	Products	15
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)	8	PSoC Solutions	15

Selection Guide^[1]

	-15	Unit
Maximum Access Time	15	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	10	mA

Pin Configuration^[2]

TSOP II -Top View



Pin Definitions

Pin Name	Pin Number	I/O Type	Description
A ₀ –A ₁₅	1–5, 18–21, 24–27, 42–44	Input	Address Inputs used to select one of the address locations.
I/O ₁ –I/O ₁₆	7–10, 13–16, 29–32, 35–38	Input/Output	Bidirectional Data I/O lines. Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	No Connects. This pin is not connected to the die.
$\overline{\text{WE}}$	17	Input/Control	Write Enable Input, active LOW. When selected LOW, a Write is conducted. When selected HIGH, a Read is conducted.
$\overline{\text{CE}}$	6	Input/Control	Chip Enable Input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}, \overline{\text{BLE}}$	40, 39	Input/Control	Byte Write Select Inputs, active LOW. $\overline{\text{BHE}}$ controls I/O ₁₆ –I/O ₉ , $\overline{\text{BLE}}$ controls I/O ₈ –I/O ₁ .
$\overline{\text{OE}}$	41	Input/Control	Output Enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V _{SS}	12, 34	Ground	Ground for the device. Should be connected to ground of the system.
V _{CC}	11, 33	Power Supply	Power Supply inputs to the device.

Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.
- NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage on V_{CC} to relative GND^[3] -0.5 V to +4.6 V

DC voltage applied to outputs in high Z state^[3] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage^[3] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static discharge voltage > 2001 V (per MIL-STD-883, method 3015)

Latch-up current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive	-40 °C to +125 °C	2.5 V–2.7 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.3	–	V
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min}, I_{OL} = 1.0 \text{ mA}$	–	0.4	V
V_{IH}	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW voltage ^[3]		-0.3	0.8	V
I_{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$	-3	+3	μA
I_{OZ}	Output leakage current	$GND \leq V_I \leq V_{CC}$, output disabled	-3	+3	μA
I_{CC}	V_{CC} operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	–	80	mA
I_{SB1}	Automatic CE Power-Down Current — TTL inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	–	15	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$, $V_{IN} \geq V_{CC} - 0.3 \text{ V}$, or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$	–	10	mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 2.6 \text{ V}$	8	pF
C_{OUT}	Output capacitance		8	pF

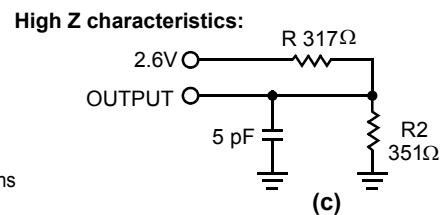
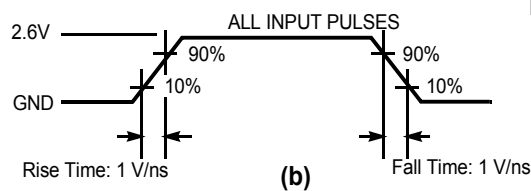
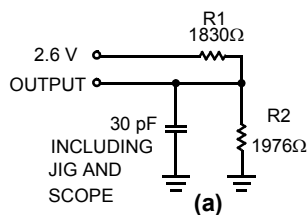
Thermal Resistance^[4]

Parameter	Description	Test Conditions	TSOP-II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	76.92	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		15.86	°C/W

Notes

- $V_{IL}(\text{min.}) = -2.0 \text{ V}$ and $V_{IH}(\text{max.}) = V_{CC} + 0.5 \text{ V}$ for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[5]



Switching Characteristics

Over the Operating Range^[6]

Parameter	Description	–15		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	15	–	ns
t _{AA}	Address to data valid	–	15	ns
t _{OHA}	Data hold from address change	3	–	ns
t _{ACE}	\overline{CE} LOW to data valid	–	15	ns
t _{DOE}	\overline{OE} LOW to data valid	–	7	ns
t _{LZOE}	\overline{OE} LOW to low Z ^[7]	0	–	ns
t _{HZOE}	\overline{OE} HIGH to high Z ^[7, 8]	–	7	ns
t _{LZCE}	\overline{CE} LOW to low Z ^[7]	3	–	ns
t _{HZCE}	\overline{CE} HIGH to high Z ^[7, 8]	–	7	ns
t _{PU} ^[9]	\overline{CE} LOW to power-up	0	–	ns
t _{PD} ^[9]	\overline{CE} HIGH to power-down	–	15	ns
t _{DBE}	Byte enable to data valid	–	7	ns
t _{LZBE}	Byte enable to low Z	0	–	ns
t _{HZBE}	Byte disable to high Z	–	7	ns

Notes

- AC characteristics (except high Z) are tested using the Thevenin load shown in Figure (a). High Z characteristics are tested for all speeds using the test load shown in Figure (c).
- Test conditions assume signal transition time of 2.6 ns or less, timing reference levels of 1.3 V, input pulse levels of 0 to 2.6 V.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- This parameter is guaranteed by design and is not tested.

Switching Characteristics

Over the Operating Range^[6] (continued)

Parameter	Description	−15		Unit
		Min	Max	
Write Cycle ^[10]				
t _{WC}	Write cycle time	15	—	ns
t _{SCE}	\overline{CE} LOW to write end	10	—	ns
t _{AW}	Address set-up to write end	10	—	ns
t _{HA}	Address hold from write end	0	—	ns
t _{SA}	Address set-up to write start	0	—	ns
t _{PWE}	\overline{WE} pulse width	10	—	ns
t _{SD}	Data set-up to write end	8	—	ns
t _{HD}	Data hold from write end	0	—	ns
t _{LZWE}	\overline{WE} HIGH to low Z ^[11]	3	—	ns
t _{HZWE}	\overline{WE} LOW to high Z ^[11, 12]	—	7	ns
t _{BW}	Byte enable to end of write	9	—	ns

Notes

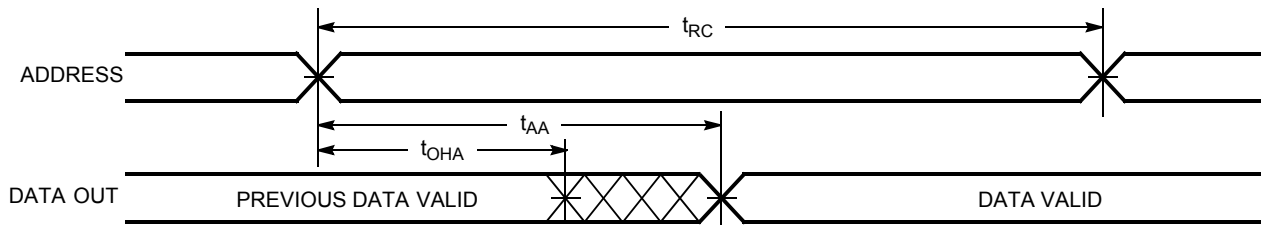
10. The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and $\overline{BHE}/\overline{BLE}$ LOW. \overline{CE} , \overline{WE} and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.

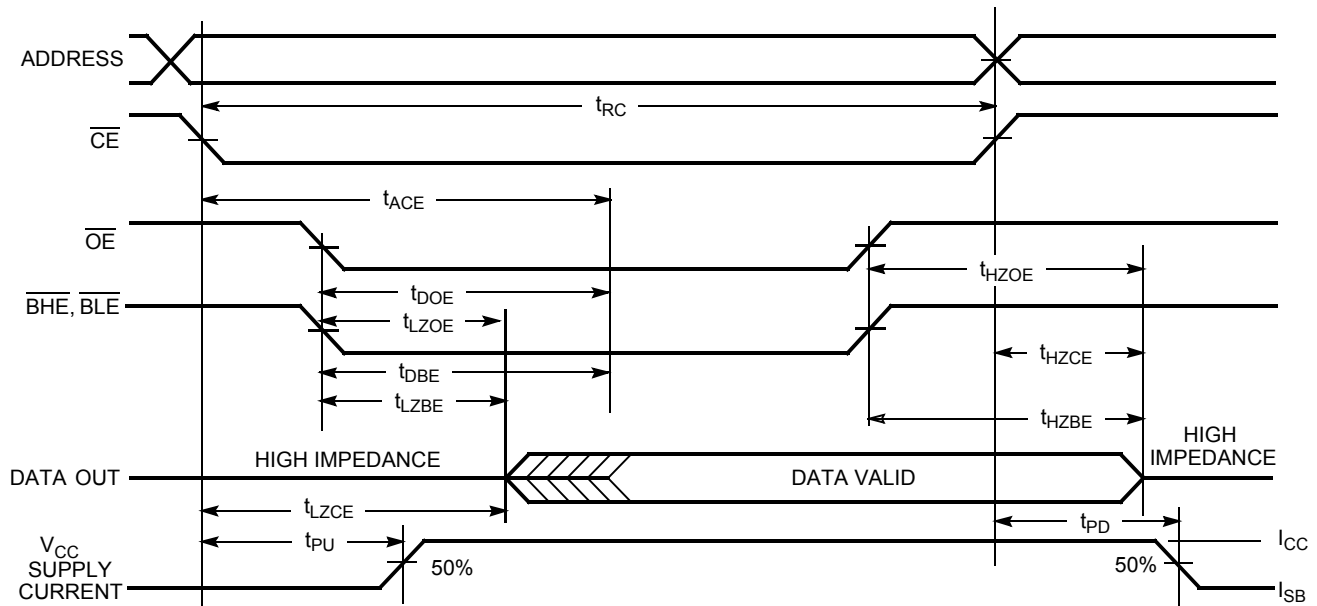
12. t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.

Switching Waveforms

Read Cycle No. 1^[13, 14]



Read Cycle No. 2 (\overline{OE} Controlled)^[14, 15]

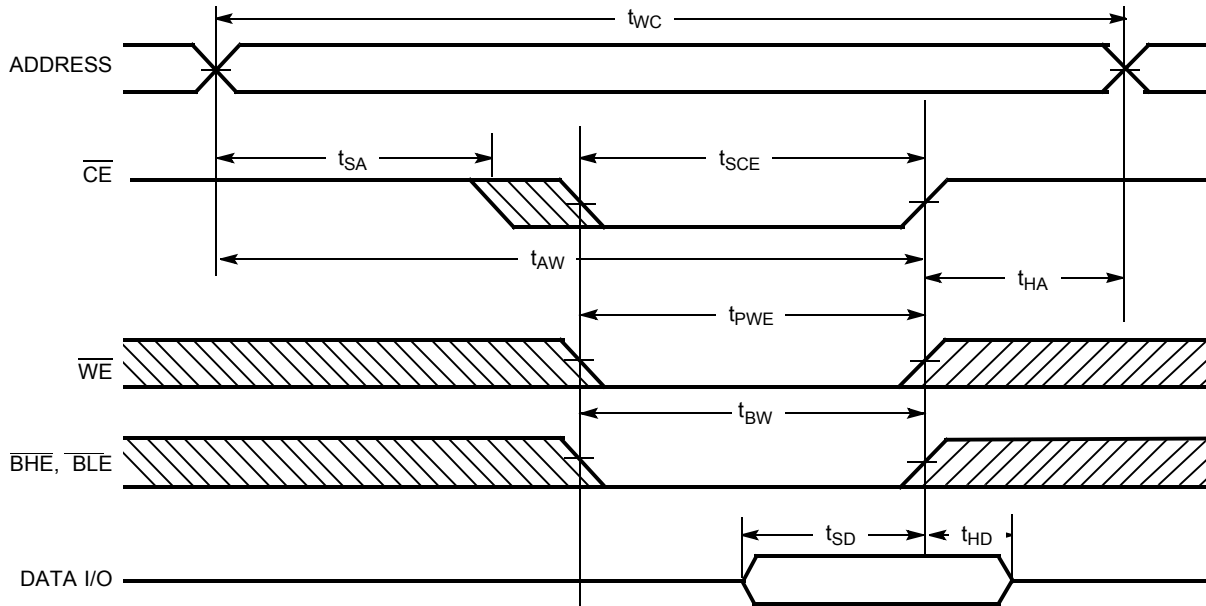


Notes

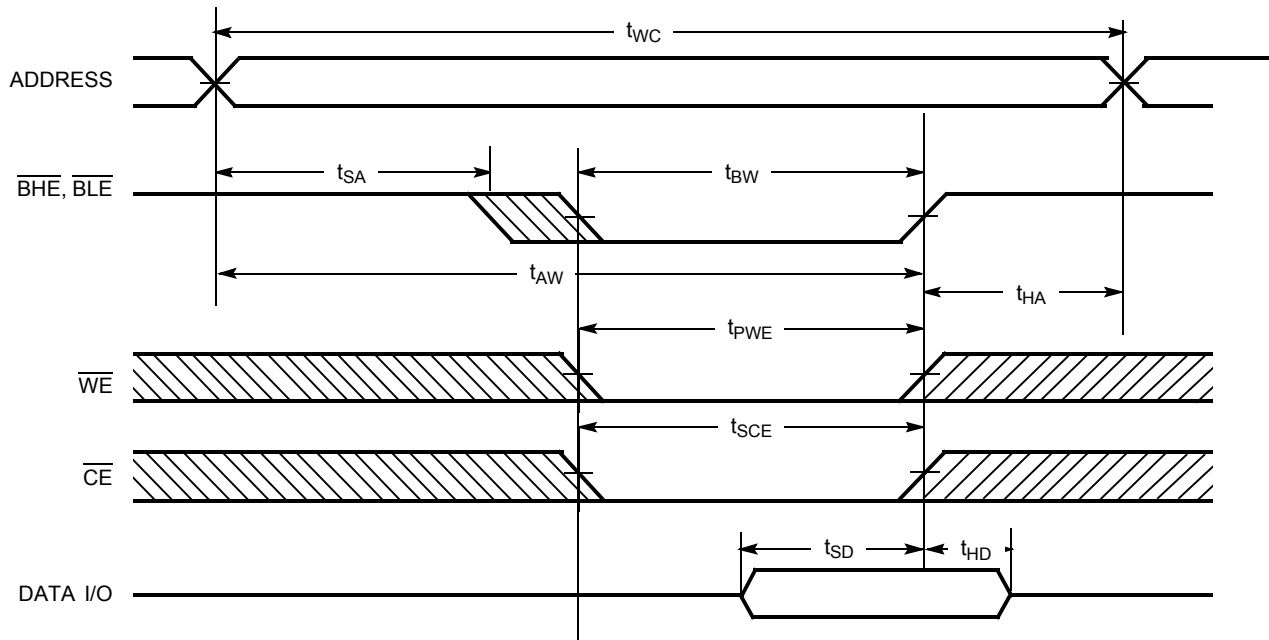
13. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
14. \overline{WE} is HIGH for Read cycle.
15. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms *(continued)*

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[16, 17]

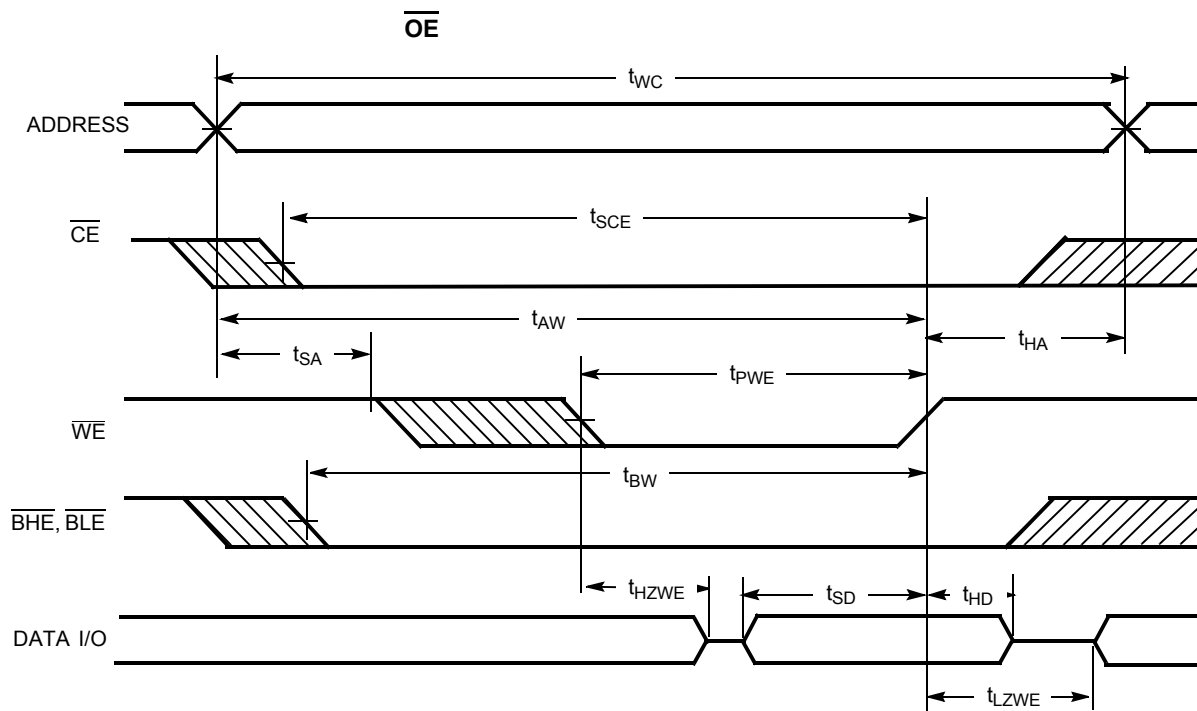


Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Notes

16. Data I/O is high-impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
17. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms *(continued)*
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, LOW)

Truth Table

CE	OE	WE	BLE	BHE	I/O ₁ –I/O ₈	I/O ₉ –I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

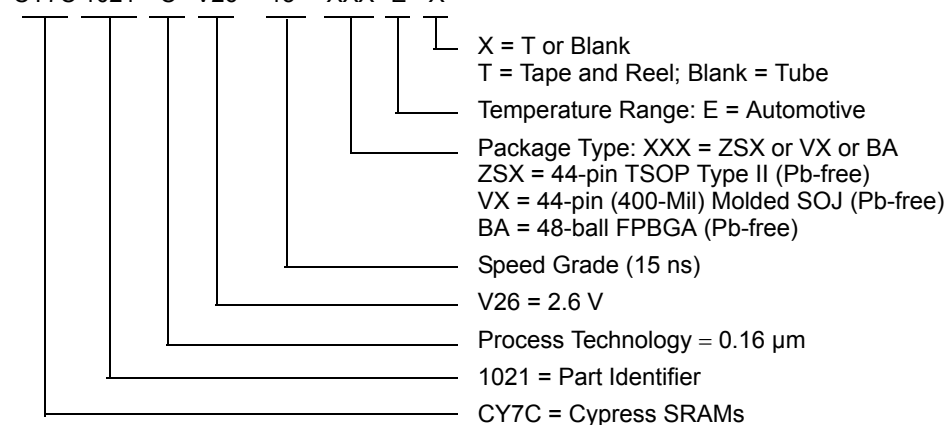
Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at <http://www.cypress.com> and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1021CV26-15ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive
	CY7C1021CV26-15VXE	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021CV26-15BAE	51-85150	48-ball FPBGA (6 × 8 × 1 mm) (Pb-free)	
	CY7C1021CV26-15BAET	51-85150	48-ball FPBGA (6 × 8 × 1 mm) (Pb-free)	
	CY7C1021CV26-15VXET	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021CV26-15ZSXET	51-85087	44-pin TSOP Type II (Pb-free)	

Ordering Code Definitions

CY7C 1021 C V26 - 15 XXX E X



Package Diagrams

Figure 1. 44-pin TSOP II, 51-85087

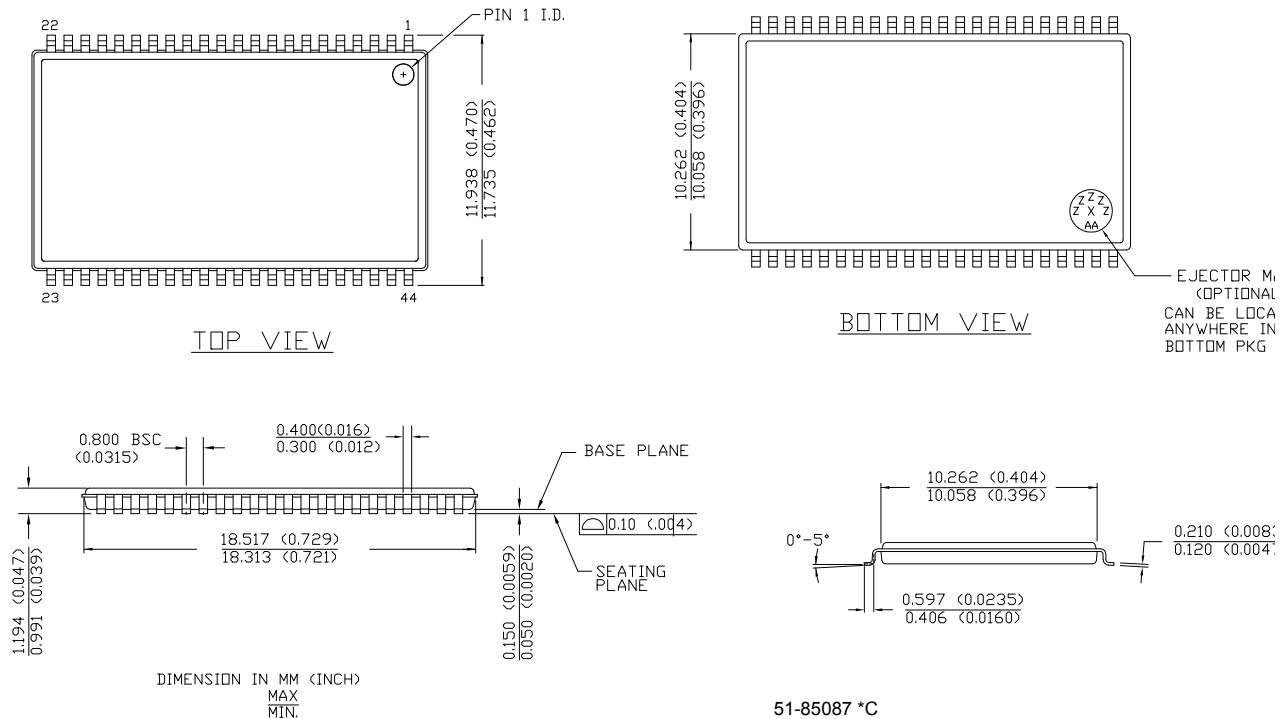
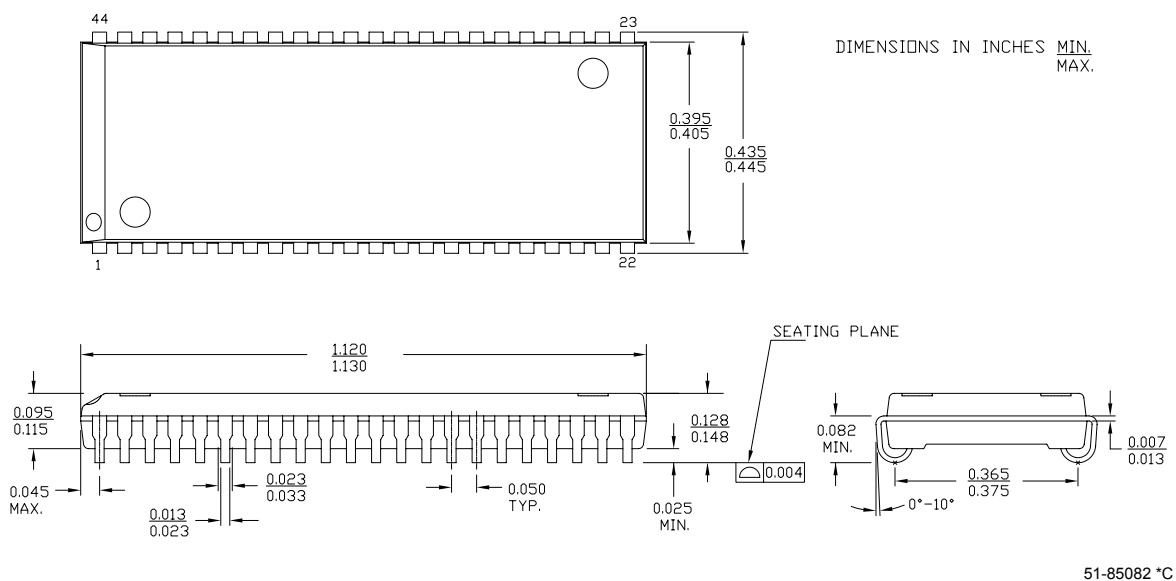
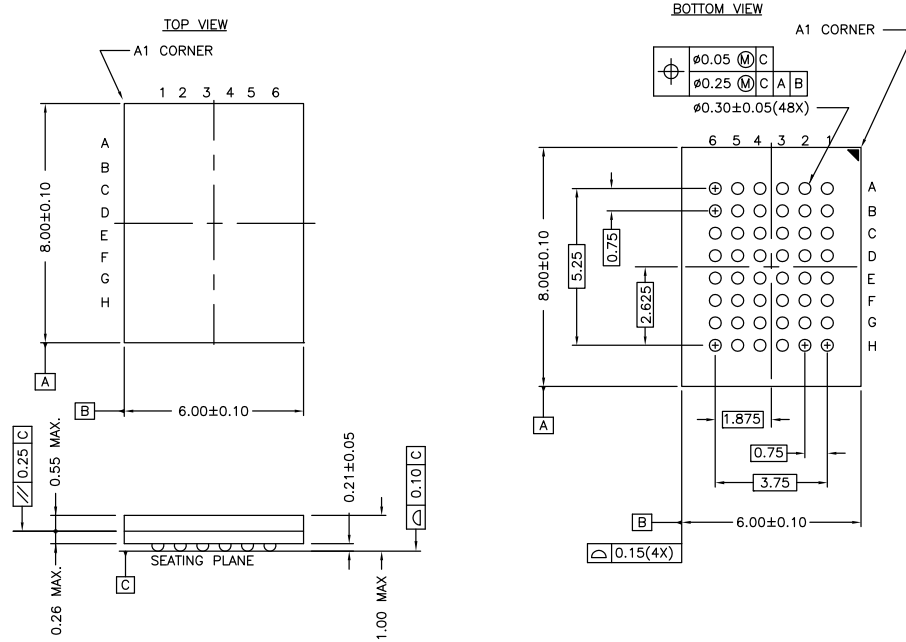


Figure 2. 44-pin (400-Mil) Molded SOJ, 51-85082



Package Diagrams (continued)

Figure 3. 48-ball FBGA (6 × 8 × 1 mm), 51-85150



51-85150 *F

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	chip enable
I/O	input/output
OE	output enable
SOJ	small outline J-lead
SRAM	static random access memory
TSOP	thin small-outline package
TTL	transistor-transistor logic
FPBGA	fine-pitch ball grid array
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μA	micro Amperes
mA	milli Amperes
mW	milli Watts
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts
%	percent

Document History Page

Document Title: CY7C1021CV26 1-Mbit (64 K × 16) Static RAM Document Number: 38-05589				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	238454	See ECN	RKF	New data sheet for Automotive
*A	335861	See ECN	SYT	Added Lead-Free Product Information Included the 44-Lead (400-Mil) Molded SOJ V34 Package
*B	493543	See ECN	NXR	Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated Ordering Information Table
*C	2897087	03/22/10	AJU	Removed obsolete parts from ordering information table Updated package diagrams
*D	3057593	10/13/2010	PRAS	Updated Ordering Information and added Ordering Code Definitions . Updated Package Diagrams.
*E	3098812	12/01/2010	PRAS	Added Acronyms and Units of Measure . Minor edits and updated in new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2004-2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.