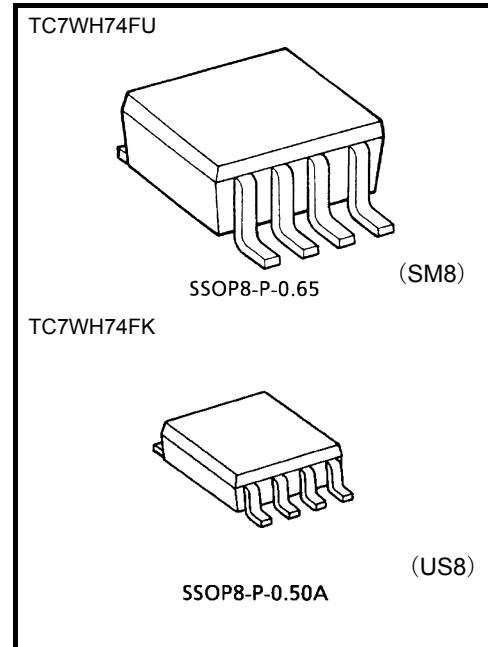
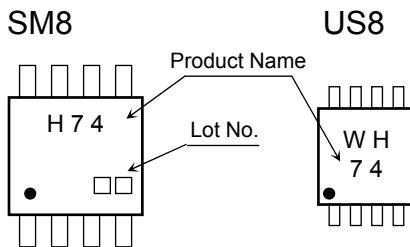


TC7WH74FU, TC7WH74FK

D-Type flip flop with preset and clear

Features

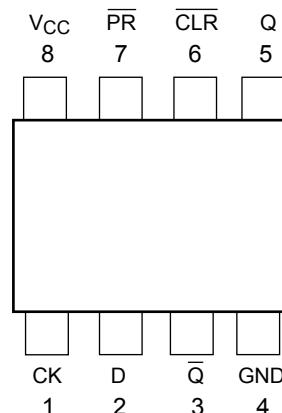
- High speed: $f_{MAX} = 170$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 2\mu A$ (max) at $T_a = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- 5.5-V tolerant inputs
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: $V_{CC} = 2$ to 5.5 V

Marking

Weight
 SSOP8-P-0.65: 0.02 g (typ.)
 SSOP8-P-0.50A: 0.01 g (typ.)

Absolute Maximum Ratings ($T_a = 25^\circ C$)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20 (Note 1)	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	300 (SM8)	mW
		200 (US8)	
Storage temperature	T_{STG}	-65 to 150	°C
Lead temperature (10 s)	T_L	260	°C

Pin Assignment (top view)

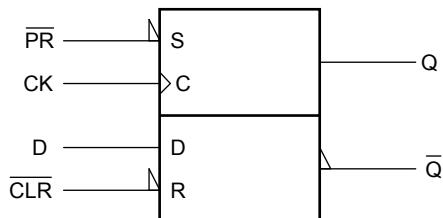
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: $V_{OUT} < GND$ 、 $V_{OUT} > V_{CC}$

Start of commercial production
1994-07

IEC Logic Symbol



Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	\bar{Q}	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q n	\bar{Q} n	No Change

X: Don't care

Operating Ranges

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V)	ns/V
		0 to 20 ($V_{CC} = 5.0 \pm 0.5$ V)	

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	V _{CC} (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
High-level input voltage	V _{IH}	—	2.0	1.5	—	—	1.5	—	V
			3.0 to 5.5	V _{CC} × 0.7	—	—	V _{CC} × 0.7	—	
Low-level input voltage	V _{IL}	—	2.0	—	—	0.5	—	0.5	V
			3.0 to 5.5	—	—	V _{CC} × 0.3	—	V _{CC} × 0.3	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 µA	2.0	1.9	2.0	—	1.9	V
				3.0	2.9	3.0	—	2.9	
				4.5	4.4	4.5	—	4.4	
			I _{OH} = -4 mA	3.0	2.58	—	—	2.48	
			I _{OH} = -8 mA	4.5	3.94	—	—	3.80	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 µA	2.0	—	0.0	0.1	—	V
				3.0	—	0.0	0.1	—	
				4.5	—	0.0	0.1	—	
			I _{OL} = 4 mA	3.0	—	—	0.36	—	
			I _{OL} = 8 mA	4.5	—	—	0.36	—	
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND	0 to 5.5	—	—	±0.1	—	±1.0	µA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	2.0	—	20.0	µA

TIMING REQUIREMENTS (unless otherwise specified, Input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Ta = 25°C		Ta = -40 to 85°C		Unit
				Limit	Limit	Limit	Limit	
Minimum pulse width (CK)	t _w (L)		3.3 ± 0.3	6.0	—	7.0	—	ns
			5.0 ± 0.5	—	5.0	—	5.0	
Minimum pulse width (CLR, PR)	t _w (L)		3.3 ± 0.3	6.0	—	7.0	—	ns
			5.0 ± 0.5	—	5.0	—	5.0	
Minimum setup time	t _s		3.3 ± 0.3	6.0	—	7.0	—	ns
			5.0 ± 0.5	—	5.0	—	5.0	
Minimum hold time	t _h		3.3 ± 0.3	0.5	—	0.5	—	
			5.0 ± 0.5	—	0.5	—	0.5	
Minimum removal time (CLR, PR)	t _{rem}		3.3 ± 0.3	5.0	—	5.0	—	
			5.0 ± 0.5	—	3.0	—	3.0	

AC Characteristics (unless otherwise specified, Input: $t_r = t_f = 3 \text{ ns}$)

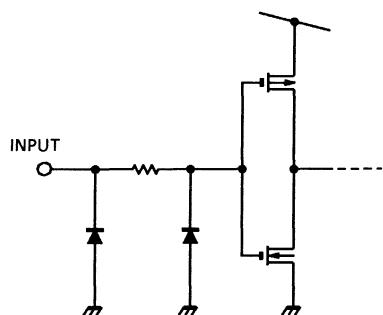
Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit	
			V _{CC} (V)	C _L (pF)	Min	Typ.	Max		
Propagation delay time (CK-Q, \bar{Q})	t_{pLH}	3.3 ± 0.3 5.0 ± 0.5	15	—	6.7	11.9	1.0	14.0	
			50	—	9.2	15.4	1.0	17.5	
	t_{pHL}		15	—	4.6	7.3	1.0	8.5	
			50	—	6.1	9.3	1.0	10.5	
Propagation delay time (\bar{CLR} , \bar{PR} -Q, \bar{Q})	t_{pLH}	3.3 ± 0.3 5.0 ± 0.5	15	—	7.6	12.3	1.0	14.5	
			50	—	10.1	15.8	1.0	18.0	
	t_{pHL}		15	—	4.8	7.7	1.0	9.0	
			50	—	6.3	9.7	1.0	11.0	
Maximum clock frequency	f_{MAX}	3.3 ± 0.3 5.0 ± 0.5	15	80	125	—	70	—	
			50	50	75	—	45	—	
			15	130	170	—	110	—	
			50	90	115	—	75	—	
Input capacitance	C_{IN}				—	4	10	10	pF
Power dissipation capacitance	C_{PD}	(Note 2)			—	22	—	—	pF

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

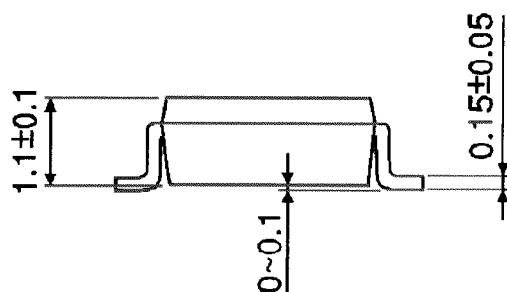
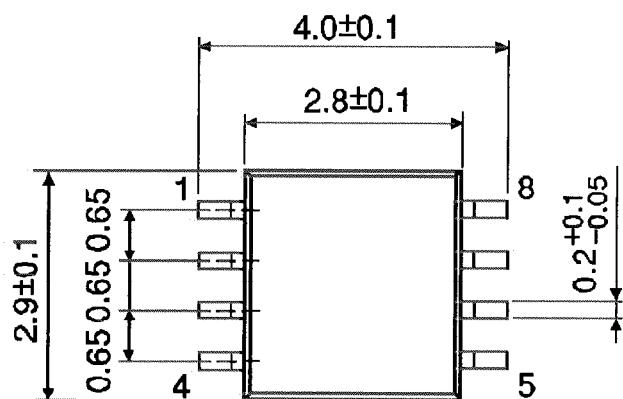
Input Equivalent Circuit



Package Dimensions

SSOP8-P-0.65

Unit : mm

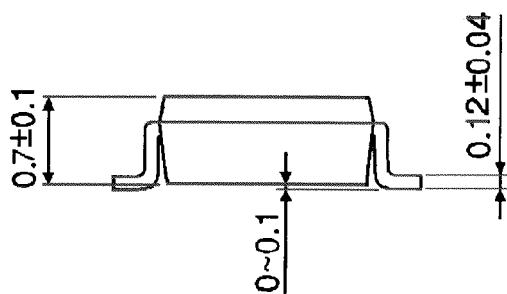
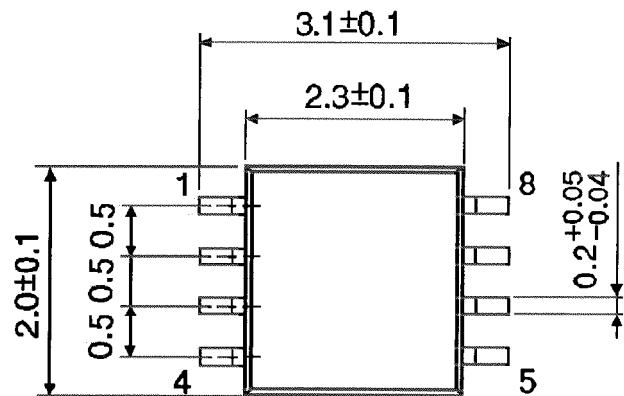


Mass: 0.02 g (typ.)

Package Dimensions

SSOP8-P-0.50A

Unit : mm



Mass: 0.01 g (typ.)

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