

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

1. DESCRIPTION

The M37280MF-XXXSP and M37280MK-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. They have a OSD function and a data slicer function, so it is useful for a channel selection system for TV with a closed caption decoder. The features of the M37280EKSP is similar to those of the M37280MK-XXXSP except that the chip has a built-in PROM which can be written electrically. The difference between M37280MK-XXXSP and M37280MF-XXXSP are the ROM size and RAM size. Accordingly, the following descriptions will be for the M37280MK-XXXSP.

2. FEATURES

- Number of basic instructions 71
- Memory size
 - ROM 60K bytes (M37280MF-XXXSP)
 - 80K bytes (M37280MK-XXXSP,
M37280EKSP)
 - RAM 1024 bytes (M37280MF-XXXSP)
 - 1472 bytes (M37280MK-XXXSP,
M37280EKSP)
 - ROM correction memory 64 bytes
- Minimum instruction execution time 0.5 μ s (at 8 MHz oscillation frequency)
- Power source voltage 5 V \pm 10 %
- Subroutine nesting 128 levels (Max.)
- Interrupts 19 types, 16 vectors
- 8-bit timers 6
- Programmable I/O ports (Ports P0, P1, P2, P30, P31) 26
- Input ports (Ports P40-P46, P63, P64, P70-P72) 12
- Output ports (Ports P32, P47, P5, P60-P62, P65-P67) 16
- 12 V withstand ports 8
- LED drive ports 2
- Serial I/O 8-bit \times 1 channel
- Multi-master I²C-BUS interface 1 (2 systems)
- A-D converter (8-bit resolution) 8 channels
- PWM output circuit 8-bit \times 8
- Power dissipation
 - In high-speed mode 165 mW
(at V_{CC} = 5.5V, 8 MHz oscillation frequency, CRT on, and Data slicer on)
 - In low-speed mode 0.33 mW
(at V_{CC} = 5.5V, 32 kHz oscillation frequency)
- ROM correction function

● Closed caption data slicer

● OSD function

Display characters 32 characters \times 16 lines + RAM font (1 character)

(CC/OSD mode)(CDOSD mode)(RAM font)

Kinds of characters 510 kinds + 62 kinds + 1 kind
(Coloring unit) (a character) (a dot) (a dot)

Triple layer function

2 layers selected from CC/CDOSD/OSD mode + RAM font layer

Character display area CC/CDOSD mode: 16 \times 26 dots

OSD mode/RAM font: 16 \times 20 dots

Kinds of character sizes CC mode/RAM font: 4 kinds

OSD/CDOSD mode: 14 kinds

Kinds of character colors

64 colors (4 adjustment levels for each R, G, B)

Coloring unit dot, character, character background, raster

Blanking output OUT1, OUT2

Display position

Horizontal: 256 levels Vertical: 1024 levels
(RAM font can be set independently)

Attribute

CC mode: smooth italic, underline, flash, automatic solid space

OSD mode: border, shadow

Window/Blank function

3. APPLICATION

TV with a closed caption decoder

4. PIN CONFIGURATION

Refer to page 3.

5. BLOCK DIAGRAM

Refer to page 4.

6. PERFORMANCE OVERVIEW

Refer to pages 5 and 6.

7. PIN DESCRIPTION

Refer to pages 7 to 11.

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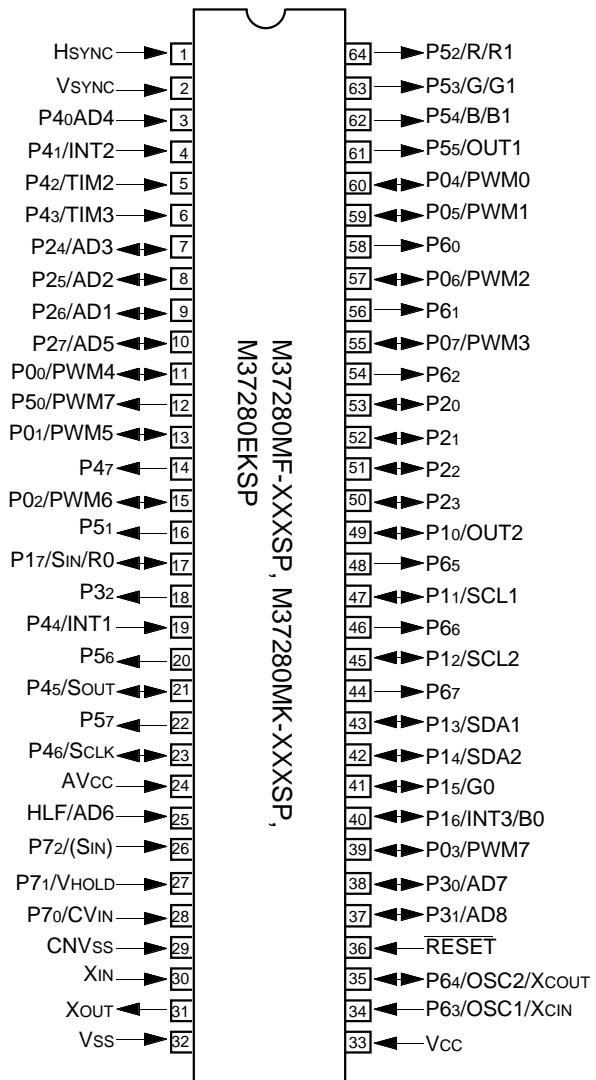
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8. PIN CONFIGURATION



Outline 64P4B

Fig. 8.1 Pin Configuration (Top View)

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9. FUNCTIONAL BLOCK DIAGRAM

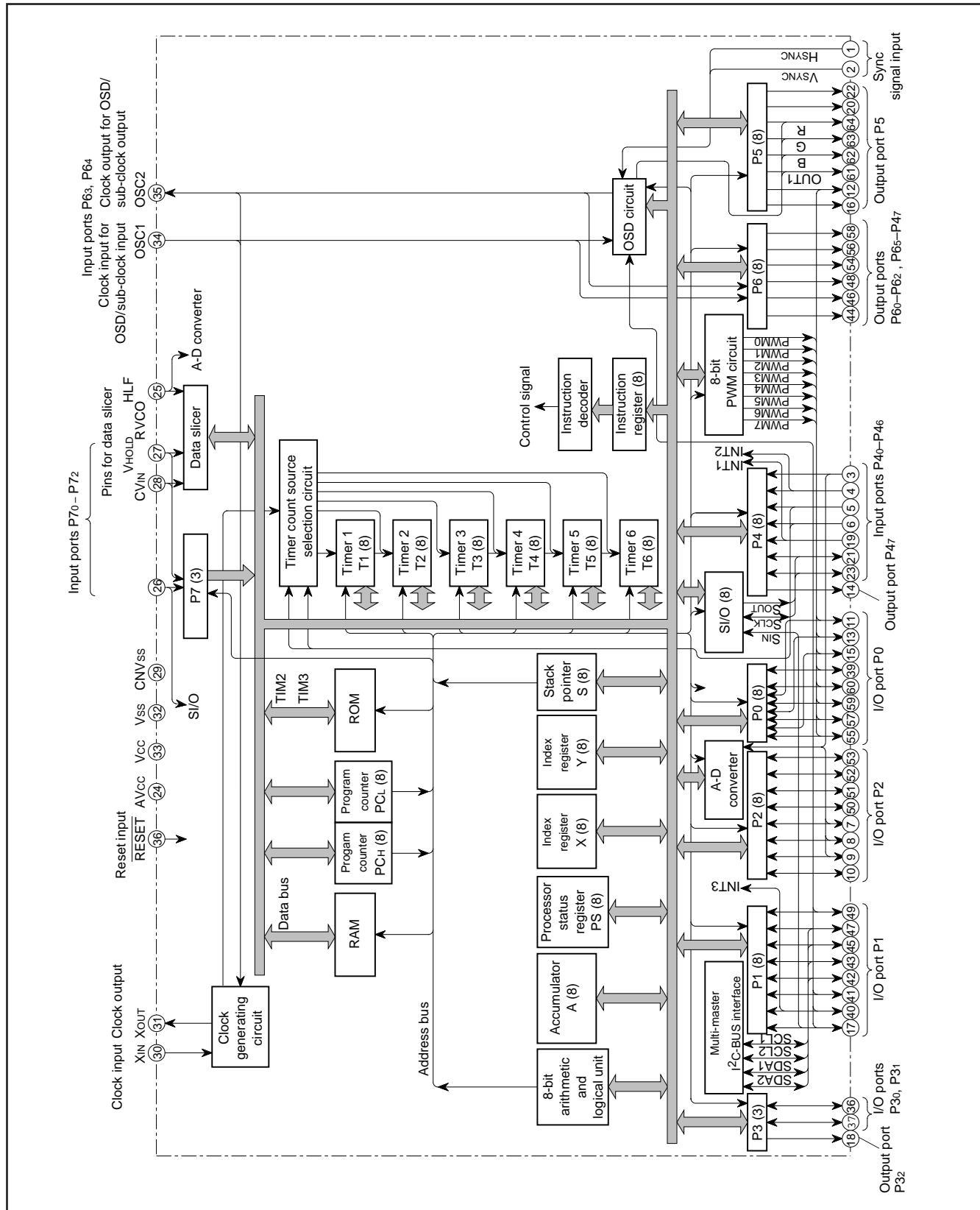


Fig. 9.1 Functional Block Diagram of M37280

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10. PERFORMANCE OVERVIEW

Table 10.1 Performance Overview

Parameter			Functions
Number of basic instructions			71
Instruction execution time			0.5 μ s (the minimum instruction execution time, at 8 MHz oscillation frequency)
Clock frequency			8 MHz (maximum)
Memory size	ROM	M37280MF-XXXSP	60K bytes
		M37280MK-XXXSP, M37280EKSP	80K bytes
	RAM	M37280MF-XXXSP	1024 bytes
		M37280MK-XXXSP, M37280EKSP	1472 bytes
	ROM correction memory		64 bytes
	OSD ROM (character font)		20400 bytes
	OSD ROM (color dot font)		9672 bytes
	OSD RAM (SPRITE)		120 bytes
	OSD RAM (character)		1536 bytes
Input/Output ports	P00–P02, P04–P07	I/O	7-bit X 1 (N-channel open-drain output structure, can be used as 8-bit PWM output pins)
	P03	I/O	1-bit X 1 (CMOS input/output structure, can be used as 14-bit PWM output pin)
	P10, P15–P17	I/O	4-bit X 1 (CMOS input/output structure, can be used as OSD output pin, INT input pin, serial input pin)
	P11–P14	I/O	4-bit X 1 (N-channel open-drain output structure, can be used as multi-master I ² C-BUS interface)
	P2	I/O	8-bit X 1 (CMOS input/output structure, can be used as A-D input pins)
	P30, P31	I/O	2-bit X 1 (CMOS input/output structure, can be used as A-D input pins)
	P32	Output	1-bit X 1 (N-channel open-drain output structure)
	P40–P44	Input	5-bit X 1 (can be used as A-D input pins, INT input pins, external clock input pins)
	P45, P46	Input	2-bit X 1 (N-channel open-drain output structure when serial I/O is used, can be used as serial I/O pins)
	P47	Output	1-bit X 1 (N-channel open-drain output structure)
	P50, P51, P56, P57	Output	4-bit X 1 (N-channel open-drain output structure, can be used as PWM output pin)
	P52–P55	Output	4-bit X 1 (CMOS output structure, can be used as OSD output pins)
	P60–P62, P65–P67	Output	6-bit X 1 (N-channel open-drain output structure)
	P63	Input	1-bit X 1 (can be used as sub-clock input pin, OSD clock input pin)
	P64	Input	1-bit X 1 (CMOS output structure when LC is oscillating, can be used as sub-clock output pin, OSD clock output pin)
	P70–P72	Input	3-bit X 1 (can be used as data slicer input/output, serial input pin)
Serial I/O			8-bit X 1
Multi-master I ² C-BUS interface			1 (2 systems)
A-D converter			8 channels (8-bit resolution)
PWM output circuit			8-bit X 8
Timers			8-bit timer X 6
Subroutine nesting			128 levels (maximum)
Interrupt			<19 types> External interrupt X 3, Internal timer interrupt X 6, Serial I/O interrupt X 1, OSD interrupt X 1, Multi-master I ² C-BUS interface interrupt X 1, Data slicer interrupt X 1, f(XIN)/4096 interrupt X 1, SPRITE OSD interrupt X 1, VSYNC interrupt X 1, A-D conversion interrupt X 1, BRK instruction interrupt X 1
Clock generating circuit			2 built-in circuits (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Data slicer			Built in

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Table 10.2 Performance Overview

Parameter		Functions	
OSD function	Number of display characters	32 characters X 16 lines	
	Character display area	CC mode: 16 X 26 dots (dot structure: 16 X 20 dots) OSD mode: 16 X 20 dots EXOSD mode: 16 X 26 dots SPRITE display: 16 X 20 dots	
	Kinds of characters	CC/OSD mode: 510 kinds CDOSD mode: 62 kinds SPRITE display: 1 kind	
	Kinds of character sizes	CC mode: 2 kinds OSD/CDOSD mode: 14 kinds SPRITE display: 8 kinds	
	Kinds of character colors	CC/CDOSD mode: 8 kinds (R, G, B, OUT1, OUT2) OSD mode: 15 kinds (R, G, B, OUT1, OUT2) SPRITE display: 8 kinds (R, G, B, OUT1)	
	Display position (horizontal, vertical)	256 levels (horizontal) X 1024 levels (vertical) SPRITE display: 2048 X 1024	
Power source voltage		5V ± 10%	
Power dissipation	In high-speed mode	OSD ON (Analog output)	Data slicer ON
		OSD ON (Digital output)	Data slicer OFF
		OSD OFF	Data slicer OFF
	In low-speed mode	OSD OFF	Data slicer OFF
	In stop mode		
Operating temperature range		-10 °C to 70 °C	
Device structure		CMOS silicon gate process	
Package		64-pin shrink plastic molded DIP	

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11. PIN DESCRIPTION

Table 11.1 Pin Description

Pin	Name	Input/ Output	Functions
Vcc, AVcc, Vss	Power source		Apply voltage of 5 V ± 10 % (typical) to Vcc and AVcc, and 0 V to Vss.
CNVss	CNVss	Input	Connected to Vss.
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a LOW for 2 μ s or more (under normal Vcc conditions). If more time is needed for the quartz-crystal oscillator to stabilize, this LOW condition should be maintained for the required time.
XIN	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins XIN and XOUT.
XOUT	Clock output	Output	If an external clock is used, the clock source should be connected to the XIN pin and the XOUT pin should be left open.
P00/ PWM4– P02/PWM6, P03/PWM7, P04/ PWM0– P07/PWM3	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure of P03 is CMOS output, that of P00–P02 and P04–P07 are N-channel open-drain output. See notes at end of Table for full details of port P0 functions.
	8-bit PWM output	Output	Pins P00–P03 and P04–P07 are also used as 8-bit PWM output pins PWM4–PWM7 and PWM0–PWM3 respectively. The output structure of PWM0–PWM6 is N-channel open-drain output. And the output structure of PWM7 is CMOS output.
P10/OUT2, P11/SCL1, P12/SCL2, P13/SDA1, P14/SDA2, P15/G0, P16/INT3/ B0, P17/SIN/R0	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure of P10 and P15–P17 is CMOS output, that of P11–P14 is N-channel open-drain output.
	OSD output	Output	Pin P10, P15–P17 are also used as OSD output pins OUT2, G0, B0, R0, respectively. The output structure is CMOS output.
	Multi-master I ² C-BUS interface	Output	Pin P11–P14 are used as SCL1, SCL2, SDA1 and SDA2 respectively, when multi-master I ² C-BUS interface is used. The output structure is N-channel open-drain output.
	External interrupt input	Input	Pin P16 is also used as external interrupt input pin INT3.
	Serial I/O data input	Input	Pin P17 is also used as serial I/O data input pin SIN.
P20–P23 P24/AD3– P26/AD1, P27/AD5	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
	Analog input	Input	Pins P24–P26, P27 are also used as analog input pins AD3–AD1, AD5 respectively.
P30/AD7, P31/AD8	I/O port P3	I/O	Ports P30 and P31 are 2-bit I/O ports and have basically the same functions as port P0. The output structure is CMOS output.
	Analog input	Input	Pins P30, P31 are also used as analog input pins AD7, AD8 respectively.
P32	Output port P3	Output	Ports P32 is a 1-bit output port. The output structure is N-channel open-drain output.
P40/AD4, P41/INT2, P42/TIM2, P43/TIM3, P44/INT1, P45/SOUT, P46/SCLK	Input port P4	Input	Ports P40–P46 are a 7-bit input port.
	Analog input	Input	Pin P40 is also used as analog input pin AD4.
	External interrupt input	Input	Pins P41, P44 are also used as external interrupt input pins INT2, INT1.
	External clock input	Input	Pins P42 and P43 are also used as external clock input pins TIM2, TIM3 respectively.
	Serial I/O data output	Output	Pin P45 is used as serial I/O data output pin SOUT. The output structure is N-channel open-drain output.
	Serial I/O synchronous clock input/output	I/O	Pin P46 is used as serial I/O synchronous clock input/output pin SCLK. The output structure is N-channel open-drain output.
P47	Output port P4	Output	Port P47 is a 1-bit output port. The output structure is N-channel open-drain output.

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Table 11.2 Pin Description (continued)

Pin	Name	Input/ Output	Functions
P50/PWM7, P51, P52/R/R1, P53/G/G1, P54/B/B1, P55/OUT1, P56, P57	Output port P5	Output	Port P5 is a 4-bit output port. The output structure of P50, P51, P56 and P57 is N-channel open-drain output, that of P52–P55 is CMOS output.
	PWM output	Output	Pin P50 is also used as 8-bit PWM output pin PWM7. The output structure is N-channel open-drain output.
	OSD output	Output	Pins P52–P55 are also used as OSD output pins R/R1, G/G1, B/B1, OUT1 respectively. At R, G, B output, the output structure is analog output. At R1, G1, B1 and OUT1 output, the output structure is CMOS output.
P60–P62, P65–P67	Output port P6	Output	Ports P60–P62 and P65–P67 are 6-bit output ports. The output structure is N-channel open-drain output.
P63/OSC1/ XCIN, P64/OSC2/ XCOUT	Input port P6	Input	Ports P63 and P64 are 2-bit input port.
	Clock input for OSD	Input	Pin P63 is also used as OSD clock input pin OSC1.
	Clock output for OSD	Output	Pin P64 is also used as OSD clock output pin OSC2. The output structure is CMOS output.
	Sub-clock output	Output	Pin P64 is also used as sub-clock output pin XCOUT. The output structure is CMOS output.
	Sub-clock input	Input	Pin P63 is also used as sub-clock input pin XCIN.
P70/CVIN, P71/VHOLD, P72/(SIN)	Input port P7	Input	Ports P70–P72 are 3-bit input port.
	Input for data slicer	Input	Pins P70, P71 are also used as data slicer input pins CVIN, VHOLD respectively. When using data slicer, input composite video signal through a capacitor. Connect a capacitor between VHOLD and VSS.
	Serial I/O data input	Input	Pins P72 is also used as serial I/O data input pin SIN.
HLF/AD6			When using data slicer, connect a filter using of a capacitor and a resistor between HLF and VSS.
	Analog input	Input	This is an analog input pin AD6.
HSYNC	Hsync input	Input	This is a horizontal synchronous signal input for OSD.
VSYNC	Vsync input	Input	This is a vertical synchronous signal input for OSD.

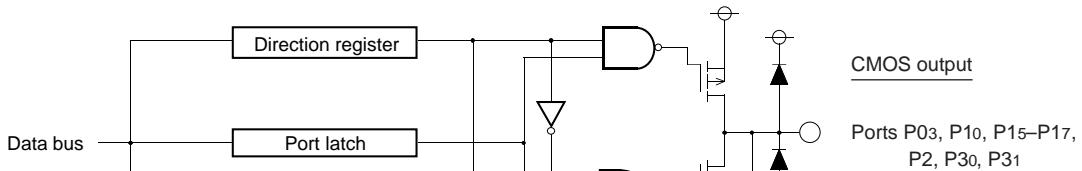
Note : As shown in the memory map (Figure 12.2.1), port P0 is accessed as a memory at address 00C016 of zero page. Port P0 has the port P0 direction register (address 00C116 of zero page) which can be used to program each bit as an input ("0") or an output ("1"). The pins programmed as "1" in the direction register are output pins. When pins are programmed as "0," they are input pins. When pins are programmed as output pins, the output data are written into the port latch and then output. When data is read from the output pins, the output pin level is not read but the data of the port latch is read. This allows a previously-output value to be read correctly even if the output "L" voltage has risen, for example, because a light emitting diode was directly driven. The input pins float, so the values of the pins can be read. When data is written into the input pin, it is written only into the port latch, while the pin remains in the floating state.

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Ports P03, P10, P15–P17, P2, P30, P31



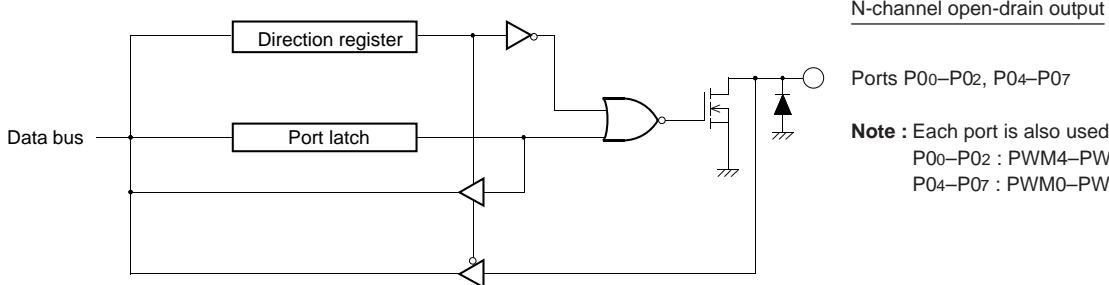
CMOS output

Ports P03, P10, P15–P17,
P2, P30, P31

Note : Each port is also used as follows :

P00 : PWM7
P10 : OUT2
P15 : G0
P16 : INT3/B0
P17 : SIN/R0
P24–P26 : AD3–AD1
P27 : AD5
P30 : AD7
P31 : AD8

Ports P00–P02, P04–P07

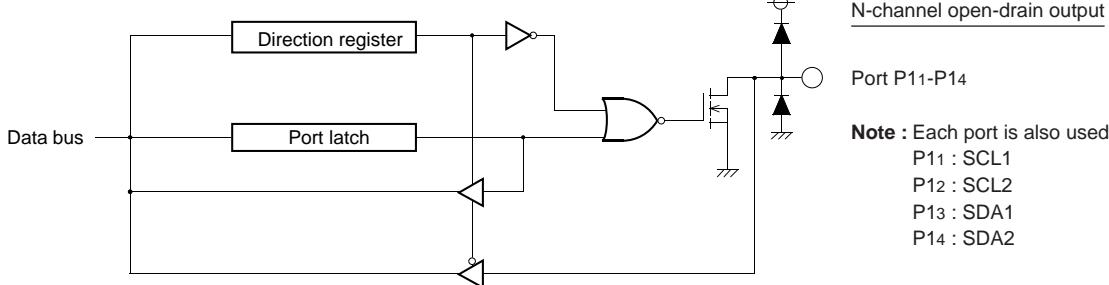


N-channel open-drain output

Ports P00–P02, P04–P07

Note : Each port is also used as follows :
P00–P02 : PWM4–PWM6
P04–P07 : PWM0–PWM3

Ports P11–P14



N-channel open-drain output

Port P11–P14

Note : Each port is also used as follows :
P11 : SCL1
P12 : SCL2
P13 : SDA1
P14 : SDA2

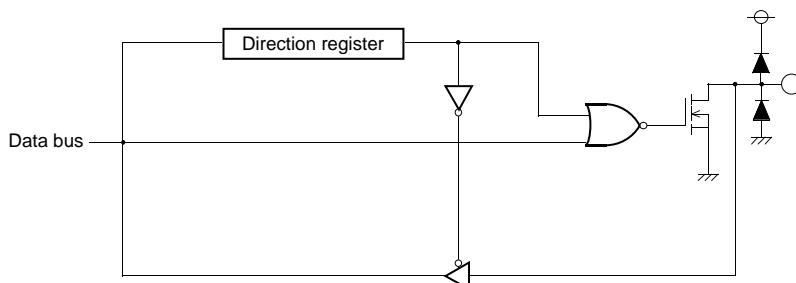
Fig. 11.1 I/O Pin Block Diagram (1)

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

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SOUT, SCLK

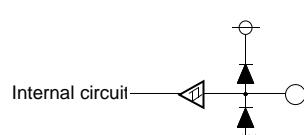


N-channel open-drain output

Ports P45, P46

Note : Each pin is also used as follows:
P45 : SOUT
P46 : SCLK

HSYNC, VSYNC



Schmidt input

HSYNC, VSYNC

Port P55

Input

Ports P40-P44

Note : Each port is also used as below:

P40 : AD4

P41 : INT2

P42 : TIM2

P43 : TIM3

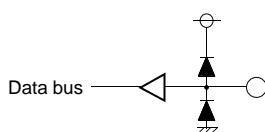
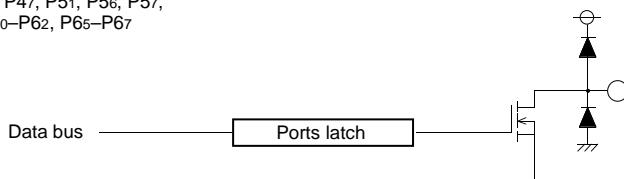
P44 : INT1

CMOS output

Port P55

Note : Port P55 is also used as pin OUT1.

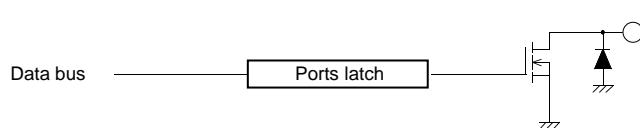
Ports P40-P44

Ports P32, P47, P51, P56, P57,
P60-P62, P65-P67

N-channel open drain output

Ports P32, P47, P51, P56, P57,
P60-P62, P65-P67

Port P50



N-channel open drain output

Port P50

Note : Port P50 is also used as pin PWM7.

Fig. 11.2 I/O Pin Block Diagram (2)

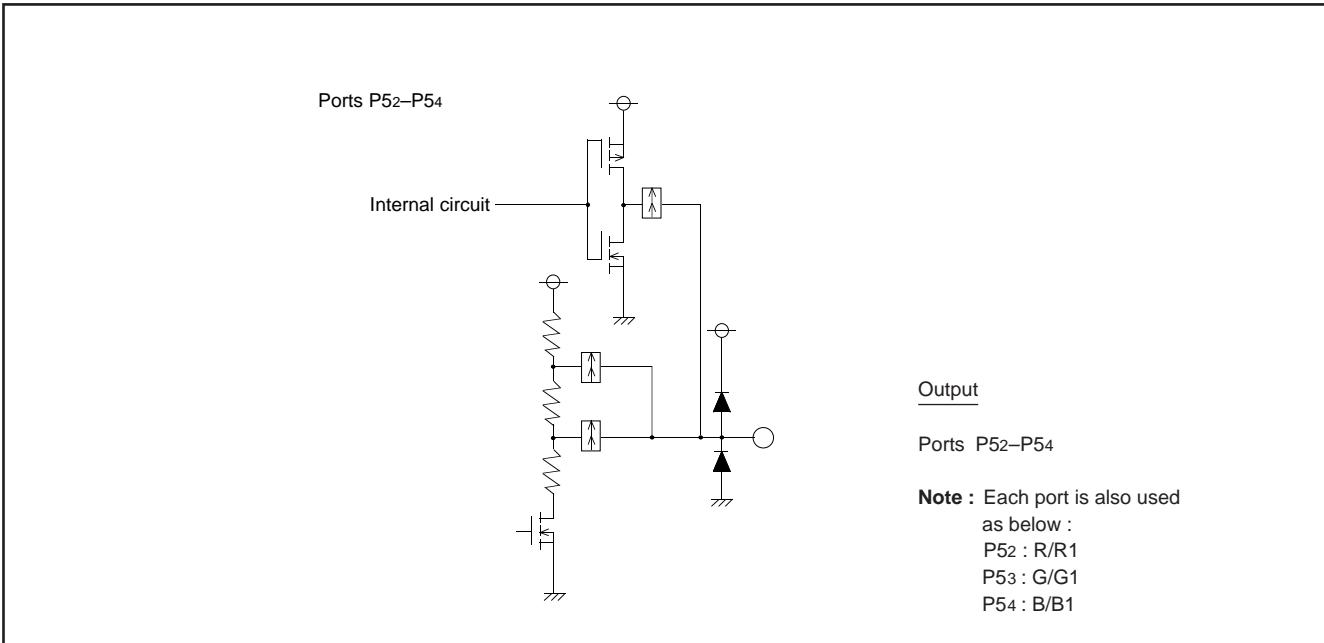
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Fig. 11.3 I/O Pin Block Diagram (3)

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12. FUNCTIONAL DESCRIPTION

12.1. CENTRAL PROCESSING UNIT (CPU)

This microcomputer uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

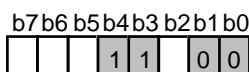
The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instructions can be used.

12.1.1 CPU Mode Register

The CPU mode register contains the stack page selection bit and internal system clock selection bit. The CPU mode register is allocated at address 00FB16.

CPU Mode Register



CPU mode register (CM) [Address 00FB16]

B	Name	Functions	After reset	R/W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: } 1 0: } Not available 1 1: }	0	R/W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R/W
3, 4	Fix these bits to "1."		1	R/W
5	XCOUT drivability selection bit (CM5)	0: LOW drive 1: HIGH drive	1	R/W
6	Main Clock (XIN-XOUT) stop bit (CM6)	0: Oscillating 1: Stopped	0	R/W
7	Internal system clock selection bit (CM7)	0: XIN-XOUT selected (high-speed mode) 1: XCIN-XCOUT selected (low-speed mode)	0	R/W

Note: This bit is set to "1" after the reset release.

Fig. 12.1.1 CPU Mode Register

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

12.2 MEMORY

12.2.1 Special Function Register (SFR) Area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

12.2.2 RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

12.2.3 ROM

The M37280MF-XXXSP has 60K-byte program area. The M37280MK-XXXSP has 56K-byte program area and 24K-byte data-dedicated area. For the M37280EKSP, the two area (60K, 24K + 56K) can be switched each other by setting the bank control register.

12.2.4 OSD RAM

RAM for display is used for specifying the character codes and colors to display.

12.2.5 OSD ROM

ROM for display is used for storing character data.

12.2.6 Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

12.2.7 Zero Page

The 256 bytes from addresses 000016 to 00FF16 are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

12.2.8 Special Page

The 256 bytes from addresses FF0016 to FFFF16 are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

12.2.9 ROM Correction Memory (RAM)

This is used as the program area for ROM correction.

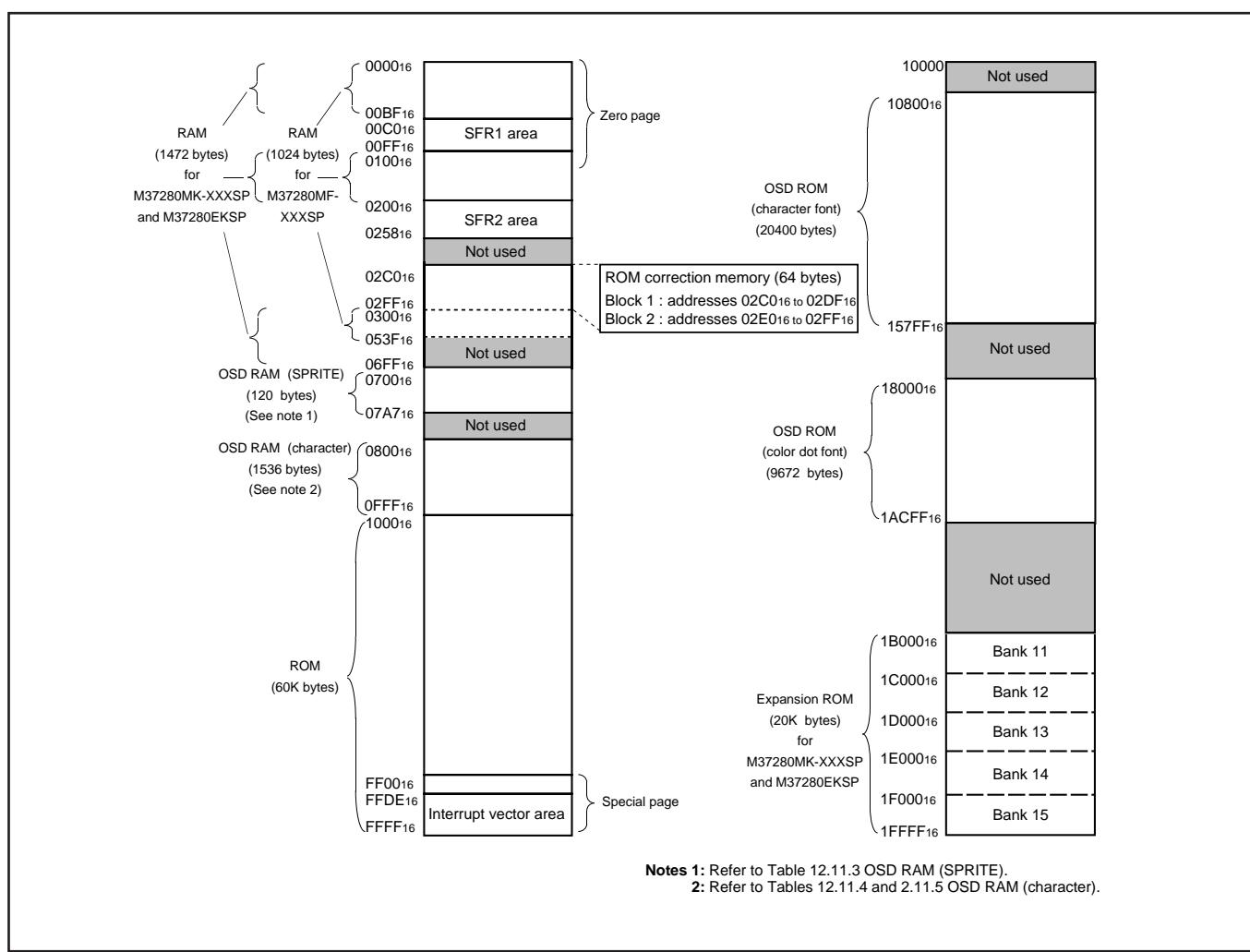


Fig. 12.2.1 Memory Map

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

12.2.10 Expansion ROM (only M37280MK-XXXSP/M37280EKSP)

The M37280MK-XXXSP/M37280EKSP can use 5-bank (total 20K bytes) expansion ROM (4K bytes each bank) by setting the bank register.

The expansion ROM is assigned to address 1B00016 to 1FFFF16. The contents of each bank in the expansion ROM are read by setting the bank register and accessing addresses 100016 to 1FFFF16. As the expansion ROM is not programmable, use it as data-dedicated area. When using the expansion ROM area, the internal ROM at addresses 100016 to 1FFFF16 (extra area) is not also programmable.

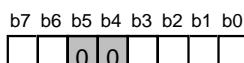
Notes 1: When using the expansion ROM (BK7 = "1"), the ROM correction function do not operate for addresses 100016 to 1FFFF16.

2: When using the emulator MCU (M37280ERSS), as addresses 100016 to 1FFFF16 can be emulated by setting bit 7 of the bank control register to "0," the expansion ROM cannot be used. Addresses 200016 to 1FFFF16 can be emulated by setting it to "1." The data in specified area by the bank selection bits can be read by accessing addresses 100016 to 1FFFF16.

3: When using the emulator MCU, the expansion ROM and the extra area cannot be emulated by setting bit 7 of the bank control register to "1." Therefore, write the data to this area before using.

4: For the M37280MK-XXXSP, fix bit 7 of the bank control register to "1." For M37280MF-XXXSP, fix the address 00ED16 to "0016."

Bank Control Register



Bank control register (BK) [Address 00ED16]

B	Name	Functions				After reset	R	W
0 to 3	Bank selection bits (BK0 to BK3)	Bank number is selected (bank 11 to 15)				0	R	W
4, 5	Fix these bits to "0".				0	R	W	
6, 7	Bank control bits (BK6, BK7)	b7	b6	Bank ROM	Address 100016 level access	0	R	W
		0	X	Not used	Read out from extra area (programmable)			
		1	0	Used	Read out the data from area specified by the bank selection bits			
		1	1	Used	Read out from extra area (data-dedicated)			

Fig. 12.2.2 Bank Control Register

■ SFR1 area (addresses C0₁₆ to DF₁₆)

Bit allocation		State immediately after reset	
<input type="checkbox"/>	: } Function bit	<input type="checkbox"/> 0 : "0" immediately after reset	<input type="checkbox"/> 1 : "1" immediately after reset
<input type="checkbox"/>	: No function bit	<input type="checkbox"/> ? : Indeterminate immediately after reset	
<input type="checkbox"/> 0	: Fix to this bit to "0" (do not write to "1")		
<input type="checkbox"/> 1	: Fix to this bit to "1" (do not write to "0")		
Address	Register	Bit allocation	
C016	Port P0 (P0)	b7	b0
C116	Port P0 direction register (D0)		
C216	Port P1 (P1)		
C316	Port P1 direction register (D1)		
C416	Port P2 (P2)		
C516	Port P2 direction register (D2)		
C616	Port P3 (P3)		
C716	Port P3 direction register (D3)		
C816	Port P4 (P4)		
C916	Port P4 direction register (D4)		
CA16	Port P5 (P5)		
CB16	OSD port control register (PF)		
CC16	Port P6 (P6)		
CD16	Port P7 (P7)		
CE16	OSD control register 1 (OC 1)		
CF16	Horizontal position register (HP)		
DO16	Block control register 1 (BC ₁)		
DI16	Block control register 2 (BC ₂)		
DI216	Block control register 3 (BC ₃)		
DI316	Block control register 4 (BC ₄)		
DI416	Block control register 5 (BC ₅)		
DI516	Block control register 6 (BC ₆)		
DI616	Block control register 7 (BC ₇)		
DI716	Block control register 8 (BC ₈)		
DI816	Block control register 9 (BC ₉)		
DI916	Block control register 10 (BC ₁₀)		
DA16	Block control register 11 (BC ₁₁)		
DB16	Block control register 12 (BC ₁₂)		
DC16	Block control register 13 (BC ₁₃)		
DD16	Block control register 14 (BC ₁₄)		
DE16	Block control register 15 (BC ₁₅)		
DF16	Block control register 16 (BC ₁₆)		

Fig. 12.2.3 Memory Map of Special Function Register 1 (SFR1) (1)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

■ SFR1 area (addresses E0₁₆ to FF₁₆)

Bit allocation

| : } Function bit
 | : }
Name : }

 : No function bit

- 0 : Fix to this bit to “0”
(do not write to “1”)
- 1 : Fix to this bit to “1”
(do not write to “0”)

State immediately after reset

0 : “0” immediately after reset

1 : “1” immediately after reset

? : Indeterminate immediately after reset

Address Register

Bit allocation

State immediately after reset

E016	Data slicer control register 1 (DSC1)	b7	0 0 0 0 0	DSC12 DSC11 DSC10	b0	0016
E116	Data slicer control register 2 (DSC2)		0 DSC25 DSC24 DSC23	0 DSC20		0016
E216	Caption data register 1 (CD1)		CDL17 CDL16 CDL15 CDL14 CDL13 CDL12 CDL11 CDL10			0016
E316	Caption data register 2 (CD2)		CDH17 CDH16 CDH15 CDH14 CDH13 CDH12 CDH11 CDH10			0016
E416	Caption data register 3 (CD3)		CDL27 CDL26 CDL25 CDL24 CDL23 CDL22 CDL21 CDL20			0016
E516	Caption data register 4 (CD4)		CDH27 CDH26 CDH25 CDH24 CDH23 CDH22 CDH21 CDH20			0016
E616	Caption Position register (CPS)		CPS7 CPS6 CPS5 CPS4 CPS3 CPS2 CPS1 CPS0		0 0 ? 0 0 0 0 0	0016
E716	Data slicer test register 2			0016		0016
E816	Data slicer test register 1			0016		0016
E916	Sync signal counter register (HC)				0 0 ? ? ? ? ? ?	0016
EA16	Clock run-in detect register (CRD)		CRD7 CRD6 CRD5 CRD4 CRD3			0016
EB16	Data clock position register (DPS)		DPS7 DPS6 DPS5 DPS4 DPS3	0 0 1		0916
EC16						?
ED16	Bank control register (BK)		BK7 BK6 0 0	BK3 BK2 BK1 BK0		0016
EE16	A-D conversion register (AD)					?
EF16	A-D control register (ADCON)		0 0 ADVREF	ADSTR ADIN2 ADIN1 ADINO		0016
F016	Timer 1 (T1)					FF16
F116	Timer 2 (T2)					0716
F216	Timer 3 (T3)					FF16
F316	Timer 4 (T4)					0716
F416	Timer mode register 1 (TM1)		TM17 TM16 TM15 TM14 TM13 TM12 TM11 TM10			0016
F516	Timer mode register 2 (TM2)		TM27 TM26 TM25 TM24 TM23 TM22 TM21 TM20			0016
F616	I ² C data shift register (S0)		D7 D6 D5 D4 D3 D2 D1 D0			?
F716	I ² C address register (S0D)		SAD6 SAD5 SAD4 SAD3 SAD2 SAD1 SAD0	RBW		0016
F816	I ² C status register (S1)		MST TRX BB PIN AL AAS AD0 LRB			
F916	I ² C control register (S1D)		BSEL1 BSEL0 10BIT SAD	ALS ESO BC2 BC1 BC0		0016
FA16	I ² C clock control register (S2)		ACK ACK BIT FAST MODE	CCR4 CCR3 CCR2 CCR1 CCR0		0016
FB16	CPU mode register (CM)		CM7 CM6 CM5 1 1	CM2 0 0		3C16
FC16	Interrupt request register 1 (IREQ1)		ADR VSCR OSDR	TM4R TM3R TM2R TM1R		0016
FD16	Interrupt request register 2 (IREQ2)		0 TM56R	IICR IN2R CKR SIOR DSR IN1R		0016
FE16	Interrupt control register 1 (ICON1)			ADE VSCE OSDE	TM4E TM3E TM2E TM1E	0016
FF16	Interrupt control register 2 (ICON2)		TM56S TM56E	IIC1 IN2E CKE SIOE DSE	IN1E	0016

Fig. 12.2.4 Memory Map of Special Function Register 1 (SFR2) (2)

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

■ SFR2 area (addresses 20016 to 21F16)

Bit allocation

 : } Function bit
Name :

 : No function bit

 : Fix to this bit to "0"
(do not write to "1")
 : Fix to this bit to "1"
(do not write to "0")

State immediately after reset

 : "0" immediately after reset

 : "1" immediately after reset

 : Indeterminate immediately
after reset

Address Register

Address	Register
20016	PWM0 register (PWM0)
20116	PWM1 register (PWM1)
20216	PWM2 register (PWM2)
20316	PWM3 register (PWM3)
20416	PWM4 register (PWM4)
20516	PWM5 register (PWM5)
20616	PWM6 register (PWM6)
20716	PWM7 register (PWM7)
20816	
20916	
20A16	PWM mode register 1 (PN)
20B16	PWM mode register 2 (PW)
20C16	ROM correction address 1 (high-order)
20D16	ROM correction address 1 (low-order)
20E16	ROM correction address 2 (high-order)
20F16	ROM correction address 2 (low-order)
21016	ROM correction enable register (RCR)
21116	Test register
21216	Interrupt input polarity register (IP)
21316	Serial I/O mode register (SM)
21416	Serial I/O register (SIO)
21516	OSD control register 2(OC2)
21616	Clock control register (CS)
21716	I/O polarity control register (PC)
21816	Raster color register (RC)
21916	OSD control register 3(OC3)
21A16	Timer 5 (TM5)
21B16	Timer 6 (TM6)
21C16	Top border control register 1 (TB1)
21D16	Bottom border control register 1 (BB1)
21E16	Top border control register 1 (TB2)
21F16	Bottom border control register 1 (BB2)

Address	Register	Bit allocation	State immediately after reset
20016	PWM0 register (PWM0)	b7 b0	?
20116	PWM1 register (PWM1)	b7 b0	?
20216	PWM2 register (PWM2)	b7 b0	?
20316	PWM3 register (PWM3)	b7 b0	?
20416	PWM4 register (PWM4)	b7 b0	?
20516	PWM5 register (PWM5)	b7 b0	?
20616	PWM6 register (PWM6)	b7 b0	?
20716	PWM7 register (PWM7)	b7 b0	?
20816		b7 b0	?
20916		b7 b0	?
20A16	PWM mode register 1 (PN)	b7 b0	0016
20B16	PWM mode register 2 (PW)	b7 b0	0016
20C16	ROM correction address 1 (high-order)	b7 b0	0016
20D16	ROM correction address 1 (low-order)	b7 b0	0016
20E16	ROM correction address 2 (high-order)	b7 b0	0016
20F16	ROM correction address 2 (low-order)	b7 b0	0016
21016	ROM correction enable register (RCR)	b7 b0	0016
21116	Test register	b7 b0	0016
21216	Interrupt input polarity register (IP)	b7 b0	0016
21316	Serial I/O mode register (SM)	b7 b0	0016
21416	Serial I/O register (SIO)	b7 b0	?
21516	OSD control register 2(OC2)	b7 b0	0016
21616	Clock control register (CS)	b7 b0	0016
21716	I/O polarity control register (PC)	b7 b0	8016
21816	Raster color register (RC)	b7 b0	0016
21916	OSD control register 3(OC3)	b7 b0	0016
21A16	Timer 5 (TM5)	b7 b0	0016
21B16	Timer 6 (TM6)	b7 b0	0716
21C16	Top border control register 1 (TB1)	b7 b0	FF16
21D16	Bottom border control register 1 (BB1)	b7 b0	?
21E16	Top border control register 1 (TB2)	b7 b0	?
21F16	Bottom border control register 1 (BB2)	b7 b0	?

Fig. 12.2.5 Memory Map of Special Function Register 2 (SFR2) (1)

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

■ SFR2 area (addresses 22016 to 23F16)

Bit allocation

: } Function bit
Name : }

: No function bit

0 : Fix to this bit to "0"
(do not write to "1")

1 : Fix to this bit to "1"
(do not write to "0")

State immediately after reset

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Indeterminate immediately
after reset

Address Register

22016	Vertical position register 1 ₁ (VP1 ₁)
22116	Vertical position register 1 ₂ (VP1 ₂)
22216	Vertical position register 1 ₃ (VP1 ₃)
22316	Vertical position register 1 ₄ (VP1 ₄)
22416	Vertical position register 1 ₅ (VP1 ₅)
22516	Vertical position register 1 ₆ (VP1 ₆)
22616	Vertical position register 1 ₇ (VP1 ₇)
22716	Vertical position register 1 ₈ (VP1 ₈)
22816	Vertical position register 1 ₉ (VP1 ₉)
22916	Vertical position register 1 ₁₀ (VP1 ₁₀)
22A16	Vertical position register 1 ₁₁ (VP1 ₁₁)
22B16	Vertical position register 1 ₁₂ (VP1 ₁₂)
22C16	Vertical position register 1 ₁₃ (VP1 ₁₃)
22D16	Vertical position register 1 ₁₄ (VP1 ₁₄)
22E16	Vertical position register 1 ₁₅ (VP1 ₁₅)
22F16	Vertical position register 1 ₁₆ (VP1 ₁₆)
23016	Vertical position register 2 ₁ (VP2 ₁)
23116	Vertical position register 2 ₂ (VP2 ₂)
23216	Vertical position register 2 ₃ (VP2 ₃)
23316	Vertical position register 2 ₄ (VP2 ₄)
23416	Vertical position register 2 ₅ (VP2 ₅)
23516	Vertical position register 2 ₆ (VP2 ₆)
23616	Vertical position register 2 ₇ (VP2 ₇)
23716	Vertical position register 2 ₈ (VP2 ₈)
23816	Vertical position register 2 ₉ (VP2 ₉)
23916	Vertical position register 2 ₁₀ (VP2 ₁₀)
23A16	Vertical position register 2 ₁₁ (VP2 ₁₁)
23B16	Vertical position register 2 ₁₂ (VP2 ₁₂)
23C16	Vertical position register 2 ₁₃ (VP2 ₁₃)
23D16	Vertical position register 2 ₁₄ (VP2 ₁₄)
23E16	Vertical position register 2 ₁₅ (VP2 ₁₅)
23F16	Vertical position register 2 ₁₆ (VP2 ₁₆)

Bit allocation

b7 b0

VP1 ₁	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀	b7 b0	?
VP1 ₂	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₃	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₄	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₅	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₆	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₇	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₈	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₉	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₁₀	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₁₁	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₁₂	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₁₃	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₁₄	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₁₅	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP1 ₁₆	VP1 ₆	VP1 ₅	VP1 ₄	VP1 ₃	VP1 ₂	VP1 ₁	VP1 ₀		?
VP2 ₁						VP2 ₁	VP2 ₀		?
VP2 ₂						VP2 ₂	VP2 ₀		?
VP2 ₃						VP2 ₃	VP2 ₀		?
VP2 ₄						VP2 ₄	VP2 ₀		?
VP2 ₅						VP2 ₅	VP2 ₀		?
VP2 ₆						VP2 ₆	VP2 ₀		?
VP2 ₇						VP2 ₇	VP2 ₀		?
VP2 ₈						VP2 ₈	VP2 ₀		?
VP2 ₉						VP2 ₉	VP2 ₀		?
VP2 ₁₀						VP2 ₁₀	VP2 ₀		?
VP2 ₁₁						VP2 ₁₁	VP2 ₀		?
VP2 ₁₂						VP2 ₁₂	VP2 ₀		?
VP2 ₁₃						VP2 ₁₃	VP2 ₀		?
VP2 ₁₄						VP2 ₁₄	VP2 ₀		?
VP2 ₁₅						VP2 ₁₅	VP2 ₀		?
VP2 ₁₆						VP2 ₁₆	VP2 ₀		?

Fig. 12.2.6 Memory Map of Special Function Register 2 (SFR2) (2)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

■ SFR2 area (addresses 240₁₆ to 258₁₆)

Bit allocation

: } Function bit
Name :
 : }

 : No function bit

- 0** : Fix to this bit to “0”
(do not write to “1”)
- 1** : Fix to this bit to “1”
(do not write to “0”)

State immediately after reset

0 : “0” immediately after reset

1 : “1” immediately after reset

: Indeterminate immediately after reset

Address Register

Bit allocation

State immediately after reset

Fig. 12.2.7 Memory Map of Special Function Register 2 (SFR2) (3)

M37280MF-XXXSP, M37280MK-XXXSP

M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

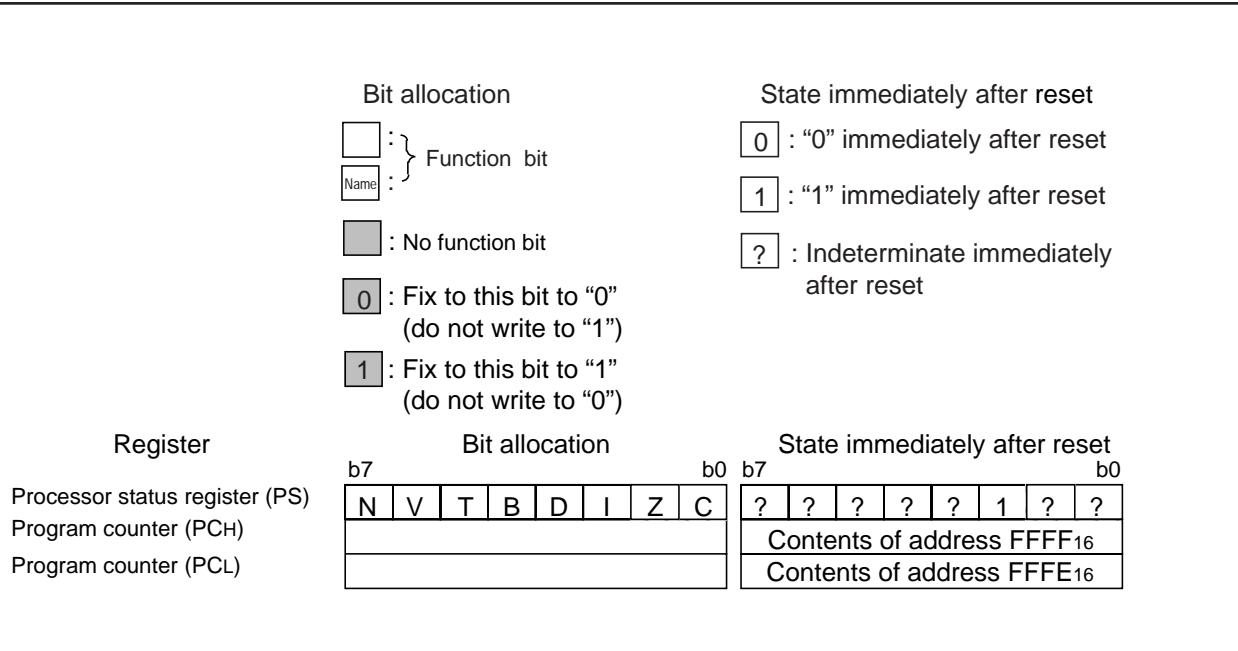


Fig. 12.2.8 Internal State of Processor Status Register and Program Counter at Reset

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

12.3 INTERRUPTS

Interrupts can be caused by 19 different sources consisting of 3 external, 14 internal, 1 software, and reset. Interrupts are vectored interrupts with priorities as shown in Table 12.3.1. Reset is also included in the table because its operation is similar to an interrupt. When an interrupt is accepted,

- ① The contents of the program counter and processor status register are automatically stored into the stack.
- ② The interrupt disable flag I is set to "1" and the corresponding interrupt request bit is set to "0."
- ③ The jump destination address stored in the vector address enters the program counter.

Other interrupts are disabled when the interrupt disable flag is set to "1."

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figures 12.3.2 to 12.3.6 show the interrupt-related registers.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1," interrupt request bit is "1," and the interrupt disable flag is "0." The interrupt request bit can be set to "0" by a program, but not set to "1." The interrupt enable bit can be set to "0" and "1" by a program.

Reset is treated as a non-maskable interrupt with the highest priority.

Figure 12.3.1 shows interrupt control.

Table 12.3.1 Interrupt Vector Addresses and Priority

Priority	Interrupt Source	Vector Addresses	Remarks
1	Reset	FFFF16, FFFE16	Non-maskable
2	OSD interrupt	FFFD16, FFFC16	
3	INT1 interrupt	FFFB16, FFFA16	Active edge selectable
4	Data slicer interrupt	FFF916, FFF816	
5	Serial I/O interrupt	FFF716, FFF616	
6	Timer 4 • SPRITE OSD interrupt	FFF516, FFF416	
7	f(XIN)/4096 interrupt	FFF316, FFF216	Software switch by software (See note)
8	VSYNC interrupt	FFF116, FFF016	Active edge selectable
9	Timer 3 interrupt	FFEF16, FFEE16	
10	Timer 2 interrupt	FFED16, FFEC16	
11	Timer 1 interrupt	FFEB16, FFEA16	
12	A-D conversion • INT3 interrupt	FFE916, FFE816	Software switch by software (See note)/ When selecting INT3 interrupt, active edge selectable.
13	INT2 interrupt	FFE716, FFE616	Active edge selectable
14	Multi-master I ² C-BUS interface interrupt	FFE516, FFE416	
15	Timer 5 • 6 interrupt	FFE316, FFE216	Software switch by software (See note)
16	BRK instruction interrupt	FFDF16, FFDE16	Non-maskable (software interrupt)

Note : Switching a source during a program causes an unnecessary interrupt occurs. Accordingly, set a source at initializing of program.

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(4) Serial I/O Interrupt

This is an interrupt request from the clock synchronous serial I/O function.

(5) f(XIN)/4096 • SPRITE OSD Interrupt

The f(XIN)/4096 interrupt occurs regularly with a f(XIN)/4096 period. Set bit 0 of the PWM mode register 1 to "0."

The SPRITE OSD interrupt occurs at the completion of SPRITE display.

Since f(XIN)/4096 interrupt and SPRITE OSD interrupt share the same vector, an interrupt source is selected by bit 5 of the SPRITE OSD control register (address 025816).

(6) Data Slicer Interrupt

An interrupt occurs when slicing data is completed.

(7) Multi-master I²C-BUS Interface Interrupt

This is an interrupt request related to the multi-master I²C-BUS interface.

(8) A-D Conversion • INT3 Interrupt

The A-D conversion interrupt occurs at the completion of A-D conversion.

The INT3 is an external input, the system detects that the level of a pin changes from LOW to HIGH or from HIGH to LOW, and generates an interrupt request. The input active edge can be selected by bit 6 of the interrupt input polarity register (address 021216) : when this bit is "0," a change from LOW to HIGH is detected; when it is "1," a change from HIGH to LOW is detected. Note that this bit is cleared to "0" at reset.

Since A-D conversion interrupt and the INT3 interrupt share the same vector, an interrupt source is selected by bit 7 of the interrupt interval determination control register (address 021216).

(9) Timer 5 • 6 Interrupt

An interrupt is generated by an overflow of timer 5 or 6. Their priorities are same, and can be switched by software.

(10) BRK Instruction Interrupt

This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

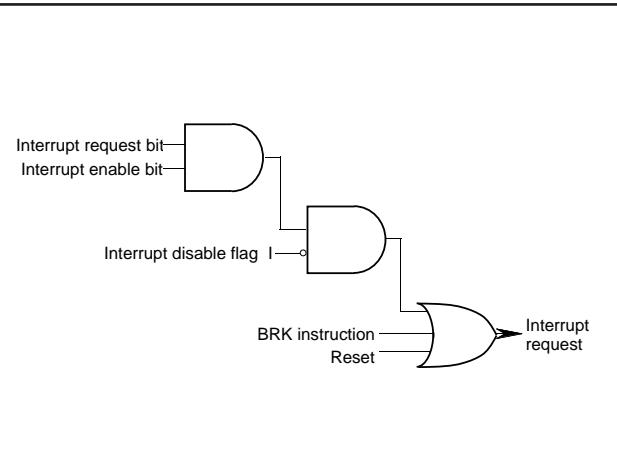


Fig. 12.3.1 Interrupt Control

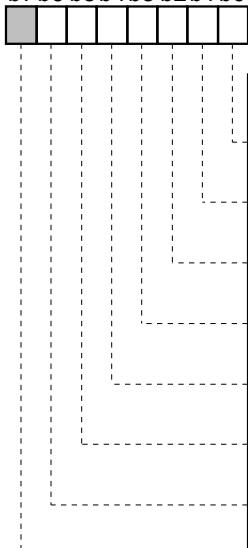
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Interrupt Request Register 1

b7 b6 b5 b4 b3 b2 b1 b0



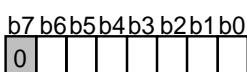
Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	A-D conversion • INT3 interrupt request bit (ADR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

*: "0" can be set by software, but "1" cannot be set.

Fig. 12.3.2 Interrupt Request Register 1

Interrupt Request Register 2



Interrupt request register 2 (IREQ2) [Address 00FD16]

B	Name	Functions	After reset	R	W
0	INT1 interrupt request bit (IN1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Data slicer interrupt request bit (DSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Serial I/O interrupt request bit (SIOR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	f(XIN)/4096 • SPRITE OSD interrupt request bit (CKR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	INT2 interrupt request bit (IN2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	Multi-master I ² C-BUS interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	Timer 5 • 6 interrupt request bit (TM56R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Fix this bit to "0."		0	R	W

*: "0" can be set by software, but "1" cannot be set.

Fig. 12.3.3 Interrupt Request Register 2

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Interrupt Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0



Interrupt control register 1 (ICON1) [Address 00FE16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	OSD interrupt enable bit (OSDE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	A-D conversion • INT3 interrupt enable bit (ADE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Fig. 12.3.4 Interrupt Control Register 1

Interrupt Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0



Interrupt control register 2 (ICON2) [Address 00FF16]

B	Name	Functions	After reset	R	W
0	INT1 interrupt enable bit (IN1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Data slicer interrupt enable bit (DSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (SIOE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	f(XIN)/4096 • SPRITE OSD interrupt enable bit (CKE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	INT2 interrupt enable bit (IN2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	Multi-master I ² C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Timer 5 • 6 interrupt enable bit (TM56E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Timer 5 • 6 interrupt switch bit (TM56S)	0 : Timer 5 1 : Timer 6	0	R	W

Fig. 12.3.5 Interrupt Control Register 2

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Interrupt Input Polarity Register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt input polarity register (IP) [Address 0212₁₆]

B	Name	Functions	After reset	R : W
0 to 2	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R : —
3	INT1 polarity switch bit (POL1)	0 : Positive polarity 1 : Negative polarity	0	R : W
4	INT2 polarity switch bit (POL2)	0 : Positive polarity 1 : Negative polarity	0	R : W
5	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is "0."		0	R : —
6	INT3 polarity switch bit (POL3)	0 : Positive polarity 1 : Negative polarity	0	R : W
7	A-D conversion • INT3 interrupt source selection bit (AD/INT3SEL)	0 : INT3 interrupt 1 : A-D conversion interrupt	0	R : W

Fig. 12.3.6 Interrupt Input Polarity Register

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12.4 TIMERS

This microcomputer has 6 timers: timer 1, timer 2, timer 3, timer 4, timer 5, and timer 6. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 12.4.3.

All of the timers count down and their divide ratio is $1/(n+1)$, where n is the value of timer latch. By writing a count value to the corresponding timer latch (addresses 00F016 to 00F316 : timers 1 to 4, addresses 021A16 and 021B16 : timers 5 and 6), the value is also set to a timer, simultaneously.

The count value is decremented by 1. The timer interrupt request bit is set to "1" by a timer overflow at the next count pulse, after the count value reaches "0016".

12.4.1 Timer 1

Timer 1 can select one of the following count sources:

- $f(XIN)/16$ or $f(XCIN)/16$
- $f(XIN)/4096$ or $f(XCIN)/4096$
- External clock from the P42/TIM2 pin

The count source of timer 1 is selected by setting bits 5 and 0 of timer mode register 1 (address 00F416). Either $f(XIN)$ or $f(XCIN)$ is selected by bit 7 of the CPU mode register.

Timer 1 interrupt request occurs at timer 1 overflow.

12.4.2 Timer 2

Timer 2 can select one of the following count sources:

- $f(XIN)/16$ or $f(XCIN)/16$
- Timer 1 overflow signal
- External clock from the TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of timer mode register 1 (address 00F416). Either $f(XIN)$ or $f(XCIN)$ is selected by bit 7 of the CPU mode register. When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

12.4.3 Timer 3

Timer 3 can select one of the following count sources:

- $f(XIN)/16$ or $f(XCIN)/16$
- $f(XCIN)$
- External clock from the TIM3 pin

The count source of timer 3 is selected by setting bit 0 of timer mode register 2 (address 00F516) and bit 6 at address 00C716. Either $f(XIN)$ or $f(XCIN)$ is selected by bit 7 of the CPU mode register.

Timer 3 interrupt request occurs at timer 3 overflow.

12.4.4 Timer 4

Timer 4 can select one of the following count sources:

- $f(XIN)/16$ or $f(XCIN)/16$
- $f(XIN)/2$ or $f(XCIN)/2$
- $f(XCIN)$

The count source of timer 3 is selected by setting bits 1 and 4 of timer mode register 2 (address 00F516). Either $f(XIN)$ or $f(XCIN)$ is selected by bit 7 of the CPU mode register. When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow.

12.4.5 Timer 5

Timer 5 can select one of the following count sources:

- $f(XIN)/16$ or $f(XCIN)/16$
- Timer 2 overflow signal
- Timer 4 overflow signal

The count source of timer 3 is selected by setting bit 6 of timer mode register 1 (address 00F416) and bit 7 of timer mode register 2 (address 00F516). When overflow of timer 2 or 4 is a count source for timer 5, either timer 2 or 4 functions as an 8-bit prescaler. Either $f(XIN)$ or $f(XCIN)$ is selected by bit 7 of the CPU mode register.

Timer 5 interrupt request occurs at timer 5 overflow.

12.4.6 Timer 6

Timer 6 can select one of the following count sources:

- $f(XIN)/16$ or $f(XCIN)/16$
- Timer 5 overflow signal

The count source of timer 6 is selected by setting bit 7 of timer mode register 1 (address 00F416). Either $f(XIN)$ or $f(XCIN)$ is selected by bit 7 of the CPU mode register. When timer 5 overflow signal is a count source for timer 6, timer 5 functions as an 8-bit prescaler.

Timer 6 interrupt request occurs at timer 6 overflow.

At reset, timers 3 and 4 are connected by hardware and "FF16" is automatically set in timer 3; "0716" in timer 4. The $f(XIN)^*/16$ is selected as the timer 3 count source. The internal reset is released by timer 4 overflow in this state and the internal clock is connected.

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF16" is automatically set in timer 3; "0716" in timer 4. However, the $f(XIN)^*/16$ is not selected as the timer 3 count source. So set both bit 0 of timer mode register 2 (address 00F516) and bit 6 at address 00C716 to "0" before execution of the STP instruction ($f(XIN)^*/16$ is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow in this state and the internal clock is connected.

As a result of the above procedure, the program can start under a stable clock.

*: When bit 7 of the CPU mode register (CM7) is "1," $f(XIN)$ becomes $f(XCIN)$.

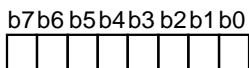
The structure of timer-related registers is shown in Figures 12.4.1 and 12.4.2.

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Timer Mode Register 1



Timer mode register 1 (TM1) [Address 00F416]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (TM10)	0: $f(X_{IN})/16$ or $f(X_{CIN})/16$ (Note) 1: Count source selected by bit 5 of TM1	0	R	W
1	Timer 2 count source selection bit 1 (TM11)	0: Count source selected by bit 4 of TM1 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (TM12)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (TM13)	0: Count start 1: Count stop	0	R	W
4	Timer 2 count source selection bit 2 (TM14)	0: $f(X_{IN})/16$ or $f(X_{CIN})/16$ (See note) 1: Timer 1 overflow	0	R	W
5	Timer 1 count source selection bit 2 (TM15)	0: $f(X_{IN})/4096$ or $f(X_{CIN})/4096$ (See note) 1: External clock from TIM2 pin	0	R	W
6	Timer 5 count source selection bit 2 (TM16)	0: Timer 2 overflow 1: Timer 4 overflow	0	R	W
7	Timer 6 internal count source selection bit (TM17)	0: $f(X_{IN})/16$ or $f(X_{CIN})/16$ (See note) 1: Timer 5 overflow	0	R	W

Note: Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register.

Fig. 12.4.1 Timer Mode Register 1

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Timer Mode Register 2

b7 b6 b5 b4 b3 b2 b1 b0

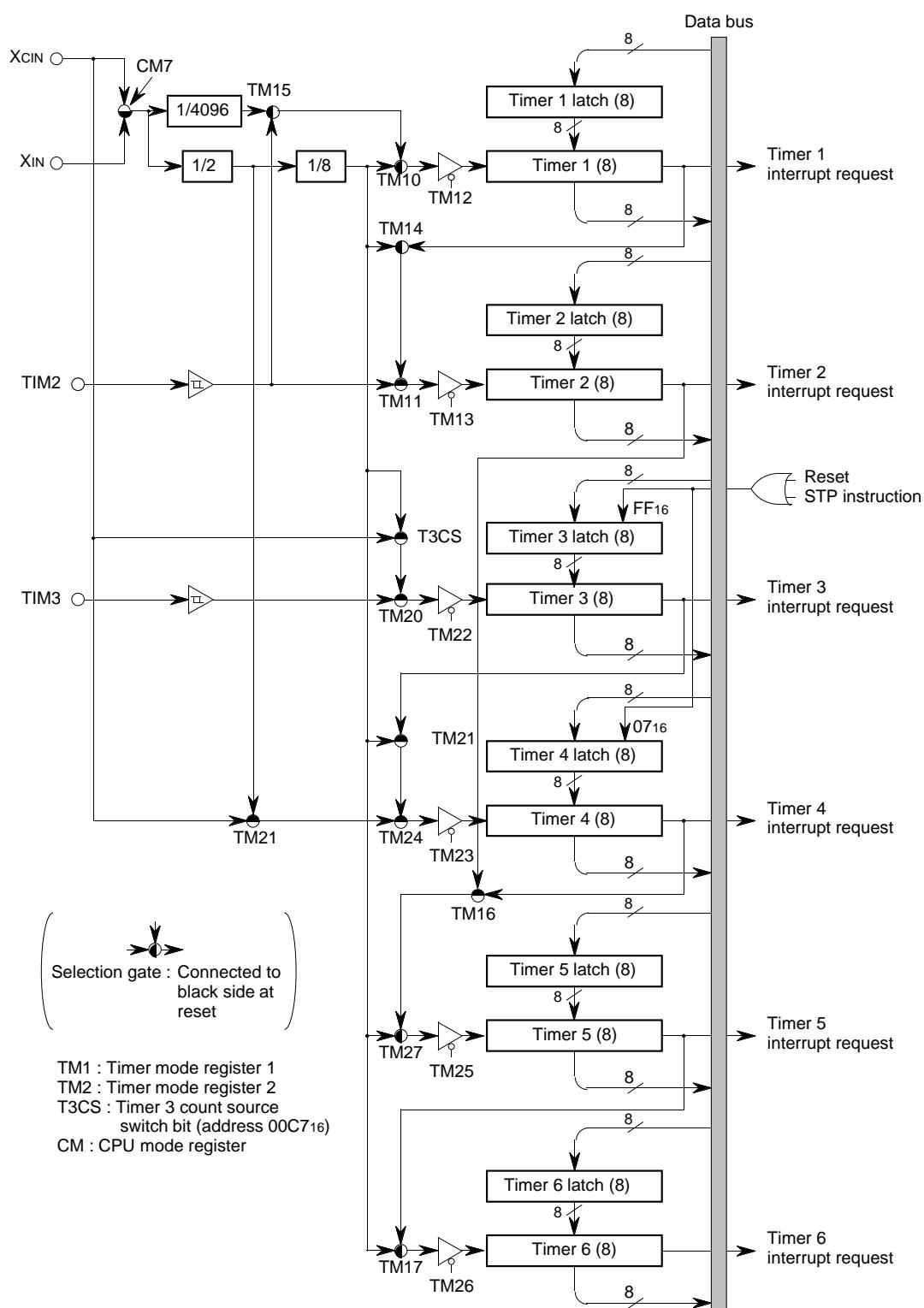
Timer mode register 2 (TM2) [Address 00F516]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (TM20)	(b6 at address 00C716) ↓ b0 0 0 : f(XIN)/16 or f(XCIN)/16 (See note) 1 0 : f(XCIN) 0 1 : } 1 1 : } External clock from TIM3 pin	0	R	W
1, 4	Timer 4 count source selection bits (TM21, TM24)	b4 b1 0 0 : Timer 3 overflow signal 0 1 : f(XIN)/16 or f(XCIN)/16 (See note) 1 0 : f(XIN)/2 or f(XCIN)/2 (See note) 1 1 : f(XCIN)	0	R	W
2	Timer 3 count stop bit (TM22)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (TM23)	0: Count start 1: Count stop	0	R	W
5	Timer 5 count stop bit (TM25)	0: Count start 1: Count stop	0	R	W
6	Timer 6 count stop bit (TM26)	0: Count start 1: Count stop	0	R	W
7	Timer 5 count source selection bit 1 (TM27)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Count source selected by bit 6 of TM1	0	R	W

Note: Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

Fig. 12.4.2 Timer Mode Register 2

PRELIMINARY
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Notes 1: HIGH pulse width of external clock inputs TIM2 and TIM3 needs 4 machine cycles or more.

2: When the external clock source is selected, timers 1, 2, and 3 are counted at a rising edge of input signal.

3: In the stop mode or the wait mode, external clock inputs TIM2 and TIM3 cannot be used.

Fig. 12.4.3 Timer Block Diagram

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12.5 SERIAL I/O

This microcomputer has a built-in serial I/O which can either transmit or receive 8-bit data serially in the clock synchronous mode.

The serial I/O block diagram is shown in Figure 12.5.1. The synchronous clock I/O pin (SCLK), and data output pin (SOUT) also function as port P4, data input pin (SIN) also functions as ports P1 and P7.

Bit 2 of the serial I/O mode register (address 021316) selects whether the synchronous clock is supplied internally or externally (from the SCLK pin). When an internal clock is selected, bits 1 and 0 select whether $f(XIN)$ or $f(XCIN)$ is divided by 8, 16, 32, or 64. To use SOUT and SCLK pins for serial I/O, set the corresponding bits of the port P4 direction register (address 00C916) to "0." To use SIN pin for serial I/O, set the corresponding bit of the port P1 direction register (address 00C316) to "0."

The operation of the serial I/O is described below. The operation of the serial I/O differs depending on the clock source; external clock or internal clock.

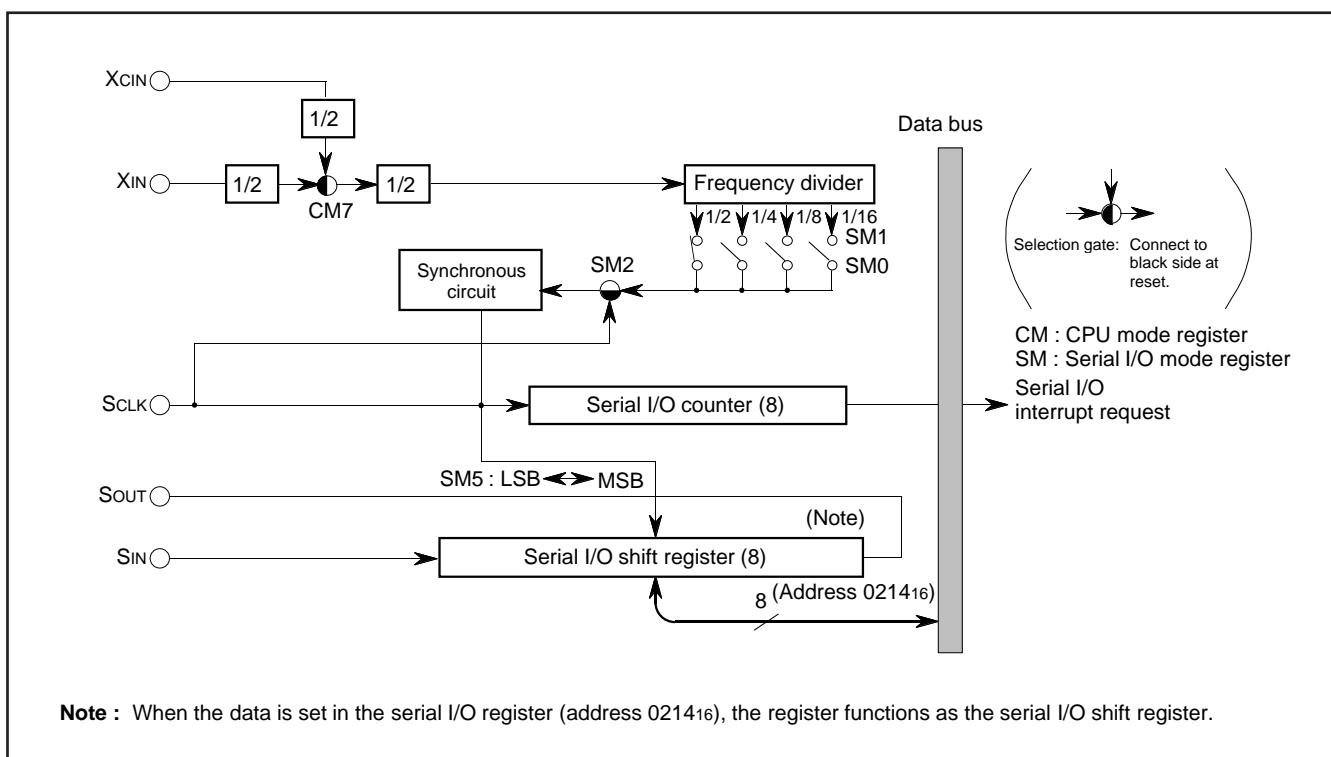


Fig. 12.5.1 Serial I/O Block Diagram

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Internal clock : The serial I/O counter is set to "7" during the write cycle into the serial I/O register (address 021416), and the transfer clock goes "H" forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the SOUT pin. Transfer direction can be selected by bit 5 of the serial I/O mode register. At each rising edge of the transfer clock, data is input from the SIN pin and data in the serial I/O register is shifted 1 bit.

After the transfer clock has counted 8 times, the serial I/O counter becomes "0" and the transfer clock stops at HIGH. At this time the interrupt request bit is set to "1."

External clock : The an external clock is selected as the clock source, the interrupt request is set to "1" after the transfer clock has been counted 8 counts. However, transfer operation does not stop, so the clock should be controlled externally. Use the external clock of 500kHz or less with a duty cycle of 50%.

The serial I/O timing is shown in Figure 12.5.2. When using an external clock for transfer, the external clock must be held at HIGH for initializing the serial I/O counter. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O counter after switching.

Notes 1: On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions, such as SEB and CLB.

2: When an external clock is used as the synchronous clock, write transmit data to the serial I/O register when the transfer clock input level is HIGH.

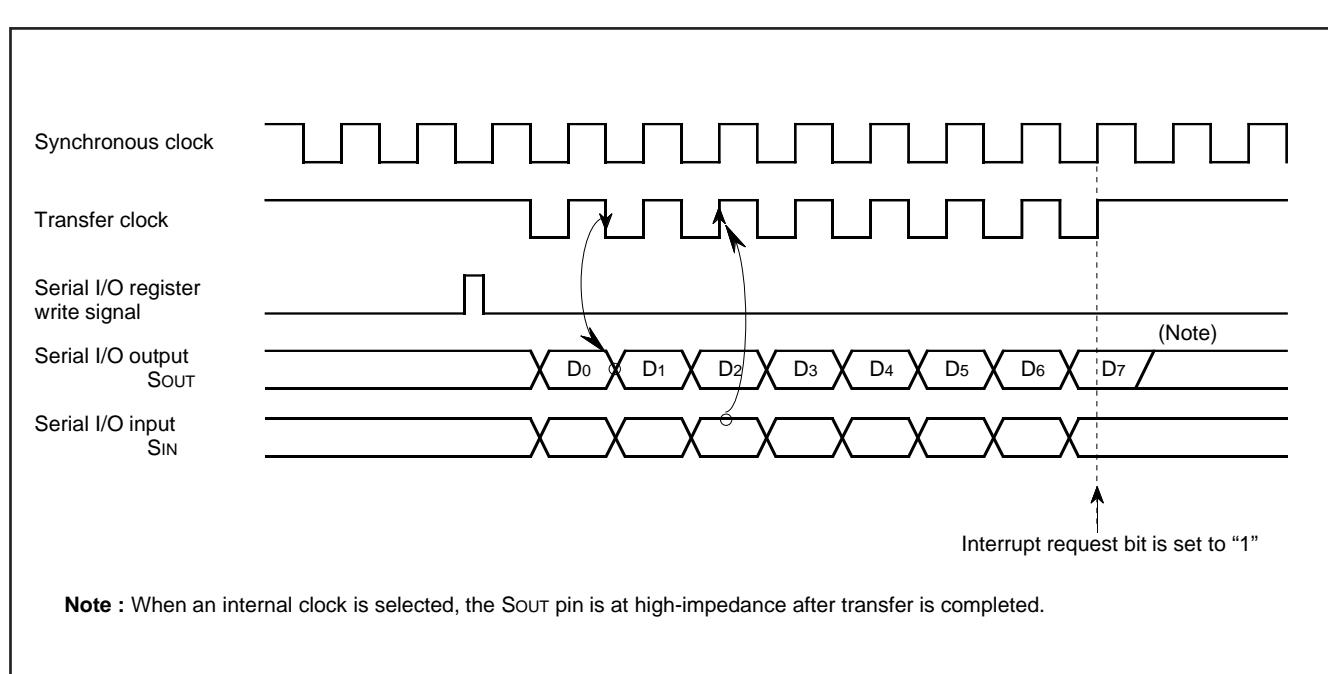


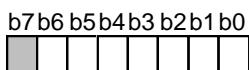
Fig. 12.5.2 Serial I/O Timing (for LSB first)

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Serial I/O Mode Register



Serial I/O mode register (SM) [Address 021316]

B	Name	Functions	After reset	R : W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: $f(XIN)/8$ or $f(XCIN)/8$ 0 1: $f(XIN)/16$ or $f(XCIN)/16$ 1 0: $f(XIN)/32$ or $f(XCIN)/32$ 1 1: $f(XIN)/64$ or $f(XCIN)/64$	0	R : W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R : W
3	Port function selection bit (SM3)	0: P11, P13 1: SCL1, SDA1	0	R : W
4	Port function selection bit (SM4)	0: P12, P14 1: SCL2, SDA2	0	R : W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R : W
6	SIN pin switch bit (SM6)	0: P17 is SIN pin. 1: P72 is SIN pin.	0	R : W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R —

Fig. 12.5.3 Serial I/O Mode Register

PRELIMINARY

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12.6 MULTI-MASTER I²C-BUS INTERFACE

The multi-master I²C-BUS interface is a serial communications circuit, conforming to the Philips I²C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.

Figure 12.6.1 shows a block diagram of the multi-master I²C-BUS interface and Table 12.6.1 shows multi-master I²C-BUS interface functions.

This multi-master I²C-BUS interface consists of the I²C address register, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register and other control circuits.

Table 12.6.1 Multi-master I²C-BUS Interface Functions

Item	Function
Format	In conformity with Philips I ² C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I ² C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at $\phi = 4$ MHz)

ϕ : System clock = $f(XIN)/2$

Note : We are not responsible for any third party's infringement of patent rights or other rights attributable to the use of the control function (bits 6 and 7 of the I²C control register at address 00F916) for connections between the I²C-BUS interface and ports (SCL1, SCL2, SDA1, SDA2).

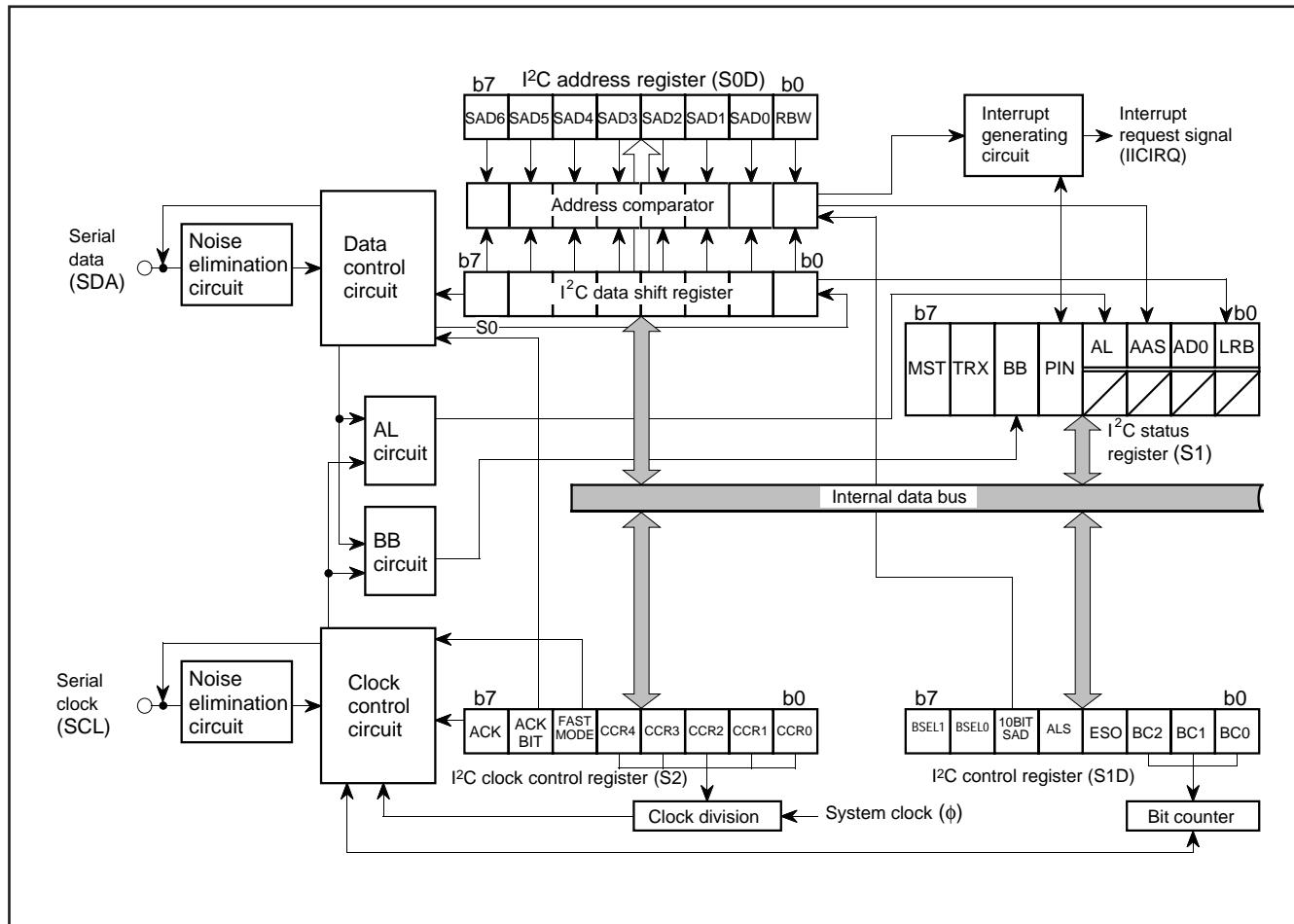


Fig. 12.6.1 Block Diagram of Multi-master I²C-BUS Interface

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12.6.1 I²C Data Shift Register

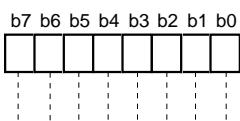
The I²C data shift register (S0 : address 00F616) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted one bit to the left.

The I²C data shift register is in a write enable status only when the ESO bit of the I²C control register (address 00F916) is "1." The bit counter is reset by a write instruction to the I²C data shift register. When both the ESO bit and the MST bit of the I²C status register (address 00F816) are "1," the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ESO bit value.

Note: To write data into the I²C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

I²C Data Shift Register



I²C data shift register 1 (S0) [Address 00F616]

B	Name	Functions	After reset	R	W
0 to 7	D0 to D7	This is an 8-bit shift register to store receive data and write transmit data.	Indeterminate	R	W

Note: To write data into the I²C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

Fig. 12.6.2 Data Shift Register

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12.6.2 I²C Address Register

The I²C address register (address 00F716) consists of a 7-bit slave address and a read/write bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition are detected.

(1) Bit 0: Read/Write Bit (RBW)

Not used when comparing addresses, in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RBW) of the I²C address register.

The RBW bit is cleared to "0" automatically when the stop condition is detected.

(2) Bits 1 to 7: Slave Address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

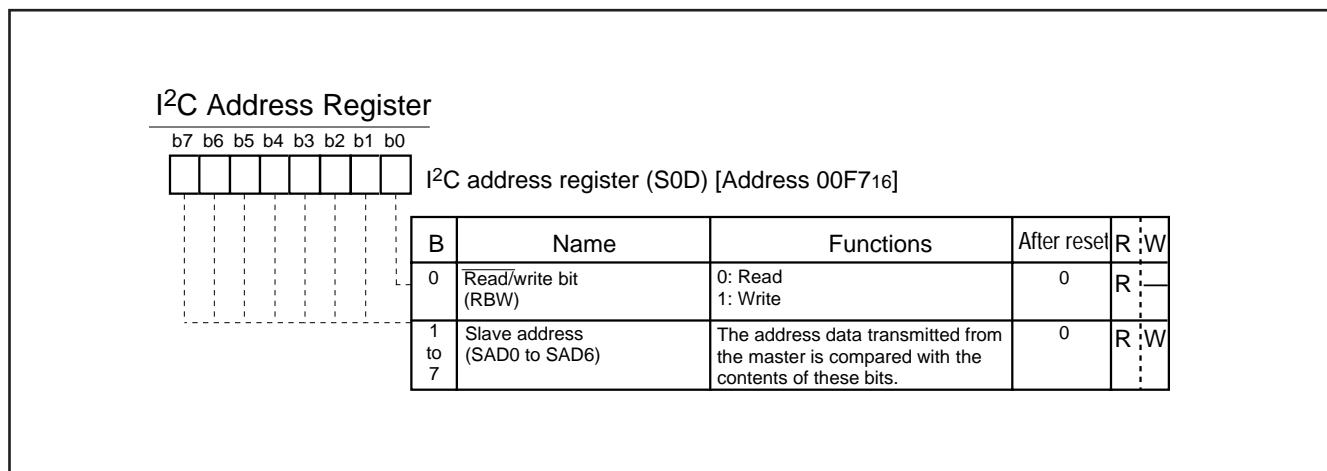


Fig. 12.6.3 I²C Address Register

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12.6.3 I²C Clock Control Register

The I²C clock control register (address 00FA₁₆) is used to set ACK control, SCL mode and SCL frequency.

(1) Bits 0 to 4: SCL Frequency Control Bits (CCR0–CCR4)

These bits control the SCL frequency.

(2) Bit 5: SCL Mode Specification Bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0," the standard clock mode is set. When the bit is set to "1," the high-speed clock mode is set.

(3) Bit 6: ACK Bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to "0," the ACK return mode is set and SDA goes to LOW at the occurrence of an ACK clock. When the bit is set to "1," the ACK non-return mode is set. The SDA is held in the HIGH status at the occurrence of an ACK clock.

However, when the slave address matches the address data in the reception of address data at ACK BIT = "0," the SDA is automatically made LOW (ACK is returned). If there is a mismatch between the slave address and the address data, the SDA is automatically made HIGH (ACK is not returned).

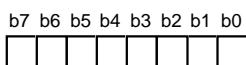
*ACK clock: Clock for acknowledgement

(4) Bit 7: ACK Clock Bit (ACK)

This bit specifies a mode of acknowledgment which is an acknowledgment response of data transmission. When this bit is set to "0," the no ACK clock mode is set. In this case, no ACK clock occurs after data transmission. When the bit is set to "1," the ACK clock mode is set and the master generates an ACK clock upon completion of each 1-byte data transmission. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (make SDA HIGH) and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transmission. If data is written during transmission, the I²C clock generator is reset, so that data cannot be transmitted normally.

I²C Clock Control Register



I²C clock control register (S2) [Address 00FA₁₆]

B	Name	Functions			After reset	R : W
0 to 4	SCL frequency control bits (CCR0 to CCR4)	Setup value of CCR4–CCR0	Standard clock mode	High speed clock mode	0	R : W
		00 to 02	Setup disabled	Setup disabled		
		03	Setup disabled	333		
		04	Setup disabled	250		
		05	100	400 (See note)		
		06	83.3	166		
		⋮	500/CCR value	1000/CCR value		
		1D	17.2	34.5		
		1E	16.6	33.3		
		1F	16.1	32.3		
		(at $\phi = 4$ MHz, unit : kHz)				
5	SCL mode specification bit (FAST MODE)	0: Standard clock mode 1: High-speed clock mode			0	R : W
6	ACK bit (ACK BIT)	0: ACK is returned. 1: ACK is not returned.			0	R : W
7	ACK clock bit (ACK)	0: No ACK clock 1: ACK clock			0	R : W

Note: At 400 kHz in the high-speed clock mode, the duty is as below.

"0" period : "1" period = 3 : 2

In the other cases, the duty is as below.

"0" period : "1" period = 1 : 1

Fig. 12.6.4 I²C Address Register

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12.6.4 I²C Control Register

The I²C control register (address 00F916) controls the data communication format.

(1) Bits 0 to 2: Bit Counter (BC0-BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. An interrupt request signal occurs immediately after the number of bits specified with these bits are transmitted.

When a START condition is received, these bits become "0002" and the address data is always transmitted and received in 8 bits.

(2) Bit 3: I²C Interface Use Enable Bit (ESO)

This bit enables usage of the multimaster I²C BUS interface. When this bit is set to "0," the use disable status is provided, so the SDA and the SCL become high-impedance. When the bit is set to "1," use of the interface is enabled.

When ESO = "0," the following is performed.

- PIN = "1," BB = "0" and AL = "0" are set (they are bits of the I²C status register at address 00F816).
- Writing data to the I²C data shift register (address 00F616) is disabled.

(3) Bit 4: Data Format Selection Bit (ALS)

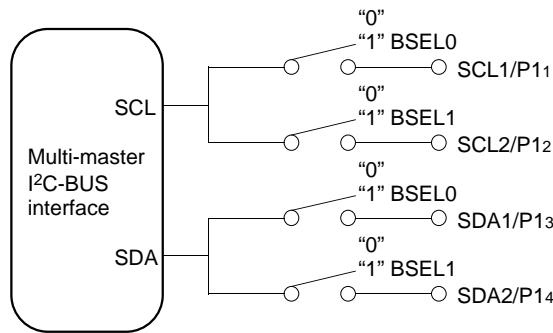
This bit decides whether or not to recognize slave addresses. When this bit is set to "0," the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to "12.6.5 I²C Status Register," bit 1) is received, transmission processing can be performed. When this bit is set to "1," the free data format is selected, so that slave addresses are not recognized.

(4) Bit 5: Addressing Format Selection Bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to "0," the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C address register (address 00F716) are compared with address data. When this bit is set to "1," the 10-bit addressing format is selected, all the bits of the I²C address register are compared with address data.

(5) Bits 6 and 7: Connection Control Bits between I²C-BUS Interface and Ports (BSEL0, BSEL1)

These bits controls the connection between SCL and ports or SDA and ports (refer to Figure 12.6.5).



Note: When using multi-master I²C-BUS interface, set bits 3 and 4 of the serial I/O mode register (address 021316) to "1." Moreover, set the corresponding direction register to "1" to use the port as multi-master I²C-BUS interface.

Fig. 12.6.5 Connection Port Control by BSEL0 and BSEL1

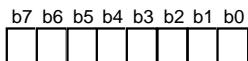
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I²C Control Register



I²C control register (S1D) [Address 00F9₁₆]

B	Name	Functions	After reset	R	W
0 to 2	Bit counter (Number of transmit/recieve bits) (BC0 to BC2)	b2 b1 b0 0 0 0: 8 0 0 1: 7 0 1 0: 6 0 1 1: 5 1 0 0: 4 1 0 1: 3 1 1 0: 2 1 1 1: 1	0	R	W
3	I ² C-BUS interface use enable bit (ESO)	0: Disabled 1: Enabled	0	R	W
4	Data format selection bit(ALS)	0: Addressing format 1: Free data format	0	R	W
5	Addressing format selection bit (10BIT SAD)	0: 7-bit addressing format 1: 10-bit addressing format	0	R	W
6, 7	Connection control bits between I ² C-BUS interface and ports (BSEL0, BSEL1)	b7 b6 Connection port (See note) 0 0: None 0 1: SCL1, SDA1 1 0: SCL2, SDA2 1 1: SCL1, SDA1, SCL2, SDA2	0	R	W

Fig. 12.6.6 I²C Control Register

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12.6.5 I²C Status Register

The I²C status register (address 00F816) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

(1) Bit 0: Last Receive Bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00F616).

(2) Bit 1: General Call Detecting Flag (AD0)

This bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition.

*General call: The master transmits the general call address "0016" to all slaves.

(3) Bit 2: Slave Address Comparison Flag (AAS)

This flag indicates a comparison result of address data.

- In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions.
 - The address data immediately after occurrence of a START condition matches the slave address stored in the high-order 7 bits of the I²C address register (address 00F716).
 - A general call is received.
- In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition.
 - When the address data is compared with the I²C address register (8 bits consists of slave address and RBW), the first bytes match.
- The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00F616).

(4) Bit 3: Arbitration Lost* detecting flag (AL)

In the master transmission mode, when a device other than the microcomputer sets the SDA to "L," arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to receive and recognize its own slave address transmitted by another master device.

*Arbitration lost: The status in which communication as a master is disabled.

(5) Bit 4: I²C-BUS Interface Interrupt Request Bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the state of the PIN bit changes from "1" to "0." At the same time, an interrupt request signal is sent to the CPU. The PIN bit is set to "0" in synchronization with a falling edge of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling edge of the PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 12.6.8 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in any one of the following conditions.

- Executing a write instruction to the I²C data shift register (address 00F616).
- When the ESO bit is "0"
- At reset

The conditions in which the PIN bit is set to "0" are shown below:

- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

(6) Bit 5: Bus Busy Flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. When this bit is set to "1," this bus system is busy and the occurrence of a START condition is disabled by the START condition duplication prevention function (Note).

This flag can be written by software only in the master transmission mode. In the other modes, this bit is set to "1" by detecting a START condition and set to "0" by detecting a STOP condition. When the ESO bit of the I²C control register (address 00F916) is "0" and at reset, the BB flag is kept in the "0" state.

(7) Bit 6: Communication Mode Specification Bit (transfer direction specification bit: TRX)

This bit decides the direction of transfer for data communication. When this bit is "0," the reception mode is selected and the data of a transmitting device is received. When the bit is "1," the transmission mode is selected and address data and control data are output into the SDA in synchronization with the clock generated on the SCL.

When the ALS bit of the I²C control register (address 00F916) is "0" in the slave reception mode is selected, the TRX bit is set to "1" (transmit) if the least significant bit (R/W bit) of the address data transmitted by the master is "1." When the ALS bit is "0" and the R/W bit is "0," the TRX bit is cleared to "0" (receive).

The TRX bit is cleared to "0" in one of the following conditions.

- When arbitration lost is detected.
- When a STOP condition is detected.
- When occurrence of a START condition is disabled by the START condition duplication prevention function (Note).
- With MST = "0" and when a START condition is detected.
- With MST = "0" and when ACK non-return is detected.
- At reset

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(8) Bit 7: Communication Mode Specification Bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is "0," the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is "1," the master is specified and a START condition and a STOP condition are generated, and also the clocks required for data communication are generated on the SCL.

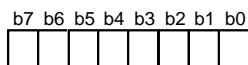
The MST bit is cleared to "0" in one of the following conditions.

- Immediately after completion of 1-byte data transmission when arbitration lost is detected
- When a STOP condition is detected.
- When occurrence of a START condition is disabled by the START condition duplication preventing function (Note).
- At reset

Note: The START condition duplication prevention function disables the START condition generation, reset of bit counter reset, and SCL output, when the following condition is satisfied:

a START condition is set by another master device.

I²C Status Register



I²C status register (S1) [Address 00F816]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0" 1 : Last bit = "1" (See note)	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected (See note)	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address match 1 : Address mismatch (See note)	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected (See note)	0	R	—
4	I ² C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	0	R	W
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave receive mode 0 1 : Slave transmit mode 1 0 : Master receive mode 1 1 : Master transmit mode	0	R	W

Note : These bits and flags can be read out, but cannot be written.

Fig. 12.6.7 I²C Status Register

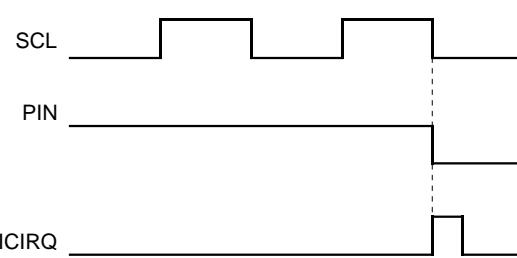


Fig. 12.6.8 Interrupt Request Signal Generation Timing

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12.6.6 START Condition Generation Method

When the ESO bit of the I²C control register (address 00F916) is "1," execute a write instruction to the I²C status register (address 00F816) to set the MST, TRX and BB bits to "1." A START condition will then be generated. After that, the bit counter becomes "0002" and an SCL for 1 byte is output. The START condition generation timing and BB bit set timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 12.6.9 for the START condition generation timing diagram, and Table 12.6.2 for the START condition/STOP condition generation timing table.

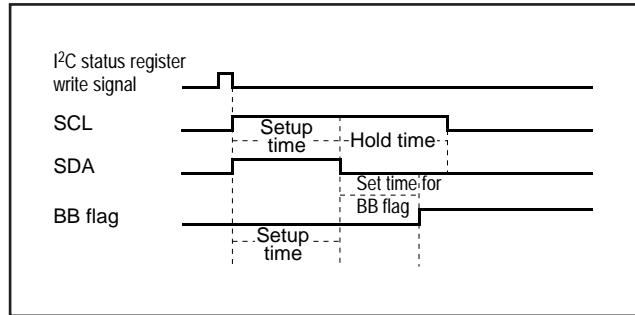


Fig. 12.6.9 START Condition Generation Timing Diagram

12.6.7 STOP Condition Generation Method

When the ESO bit of the I²C control register (address 00F916) is "1," execute a write instruction to the I²C status register (address 00F816) for setting the MST bit and the TRX bit to "1" and the BB bit to "0". A STOP condition will then be generated. The STOP condition generation timing and the BB flag reset timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 12.6.10 for the STOP condition generation timing diagram, and Table 12.6.2 for the START condition/STOP condition generation timing table.

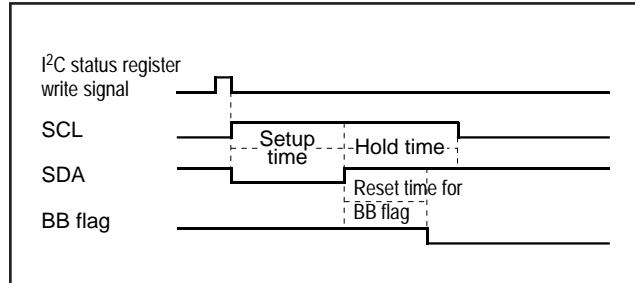


Fig. 12.6.10 STOP Condition Generation Timing Diagram

Table 12.6.2 START Condition/STOP Condition Generation Timing Table

Item	Standard Clock Mode	High-speed Clock Mode
Setup time	4.25 μ s (17 cycles)	1.75 μ s (7 cycles)
Hold time	5.0 μ s (20 cycles)	2.5 μ s (10 cycles)
Set/reset time for BB flag	3.0 μ s (12 cycles)	1.5 μ s (6 cycles)

Note: Absolute time at $\phi = 4$ MHz. The value in parentheses denotes the number of ϕ cycles.

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12.6.8 START/STOP Condition Detect Conditions

The START/STOP condition detect conditions are shown in Figure 12.6.11 and Table 12.6.3. Only when the 3 conditions of Table 12.6.3 are satisfied, a START/STOP condition can be detected.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "IICIRQ" is generated to the CPU.

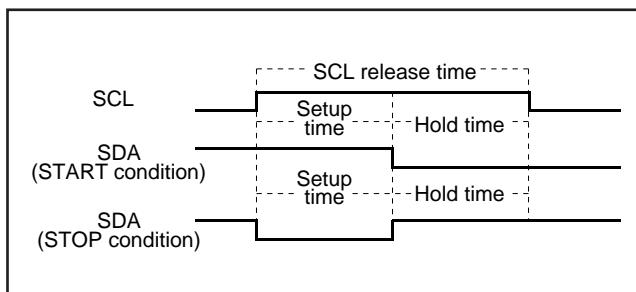


Fig. 12.6.11 START Condition/STOP Condition Detect Timing Diagram

Table 12.6.3 START Condition/STOP Condition Detect Conditions

Standard Clock Mode	High-speed Clock Mode
6.5 μ s (26 cycles) < SCL release time	1.0 μ s (4 cycles) < SCL release time
3.25 μ s (13 cycles) < Setup time	0.5 μ s (2 cycles) < Setup time
3.25 μ s (13 cycles) < Hold time	0.5 μ s (2 cycles) < Hold time

Note: Absolute time at $\phi = 4$ MHz. The value in parentheses denotes the number of ϕ cycles.

12.6.9 Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats is described below.

(1) 7-bit Addressing Format

To meet the 7-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 00F916) to "0." The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I²C address register (address 00F716). At the time of this comparison, address comparison of the RBW bit of the I²C address register (address 00F716) is not made. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 12.6.12, (1) and (2).

(2) 10-bit Addressing Format

To meet the 10-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 00F916) to "1." An address comparison is made between the first-byte address data transmitted from the master and the 7-bit slave address stored in the I²C address register (address 00F716). At the time of this comparison, an address comparison between the RBW bit of the I²C address register (address 00F716) and the R/W bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the R/W bit which is the last bit of the address data not only specifies the direction of communication for control data but also is processed as an address data bit.

When the first-byte address data matches the slave address, the AAS bit of the I²C status register (address 00F816) is set to "1." After the second-byte address data is stored into the I²C data shift register (address 00F616), make an address comparison between the second-byte data and the slave address by software. When the address data of the 2nd bytes matches the slave address, set the RBW bit of the I²C address register (address 00F716) to "1" by software. This processing can match the 7-bit slave address and R/W data, which are received after a RESTART condition is detected, with the value of the I²C address register (address 00F716). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 12.6.12, (3) and (4).

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12.6.10 Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

- ① Set a slave address in the high-order 7 bits of the I²C address register (address 00F716) and "0" in the RBW bit.
- ② Set the ACK return mode and SCL = 100 kHz by setting "8516" in the I²C clock control register (address 00FA16).
- ③ Set "1016" in the I²C status register (address 00F816) and hold the SCL at the HIGH.
- ④ Set a communication enable status by setting "4816" in the I²C control register (address 00F916).
- ⑤ Set the address data of the destination of transmission in the high-order 7 bits of the I²C data shift register (address 00F616) and set "0" in the least significant bit.
- ⑥ Set "F016" in the I²C status register (address 00F816) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occurs.
- ⑦ Set transmit data in the I²C data shift register (address 00F616). At this time, an SCL and an ACK clock automatically occurs.
- ⑧ When transmitting control data of more than 1 byte, repeat step ⑦.
- ⑨ Set "D016" in the I²C status register (address 00F816). After this, if ACK is not returned or transmission ends, a STOP condition will be generated.

12.6.11 Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode, using the addressing format, is shown below.

- ① Set a slave address in the high-order 7 bits of the I²C address register (address 00F716) and "0" in the RBW bit.
- ② Set the no ACK clock mode and SCL = 400 kHz by setting "2516" in the I²C clock control register (address 00FA16).
- ③ Set "1016" in the I²C status register (address 00F816) and hold the SCL at the HIGH.
- ④ Set a communication enable status by setting "4816" in the I²C control register (address 00F916).
- ⑤ When a START condition is received, an address comparison is made.
 - When all transmitted address are "0" (general call):
AD0 of the I²C status register (address 00F816) is set to "1" and an interrupt request signal occurs.
 - When the transmitted addresses match the address set in ①:
ASS of the I²C status register (address 00F816) is set to "1" and an interrupt request signal occurs.
 - In the cases other than the above:
AD0 and AAS of the I²C status register (address 00F816) are set to "0" and no interrupt request signal occurs.
- ⑥ Set dummy data in the I²C data shift register (address 00F616).
- ⑦ When receiving control data of more than 1 byte, repeat step ⑦.
- ⑧ When a STOP condition is detected, the communication ends.

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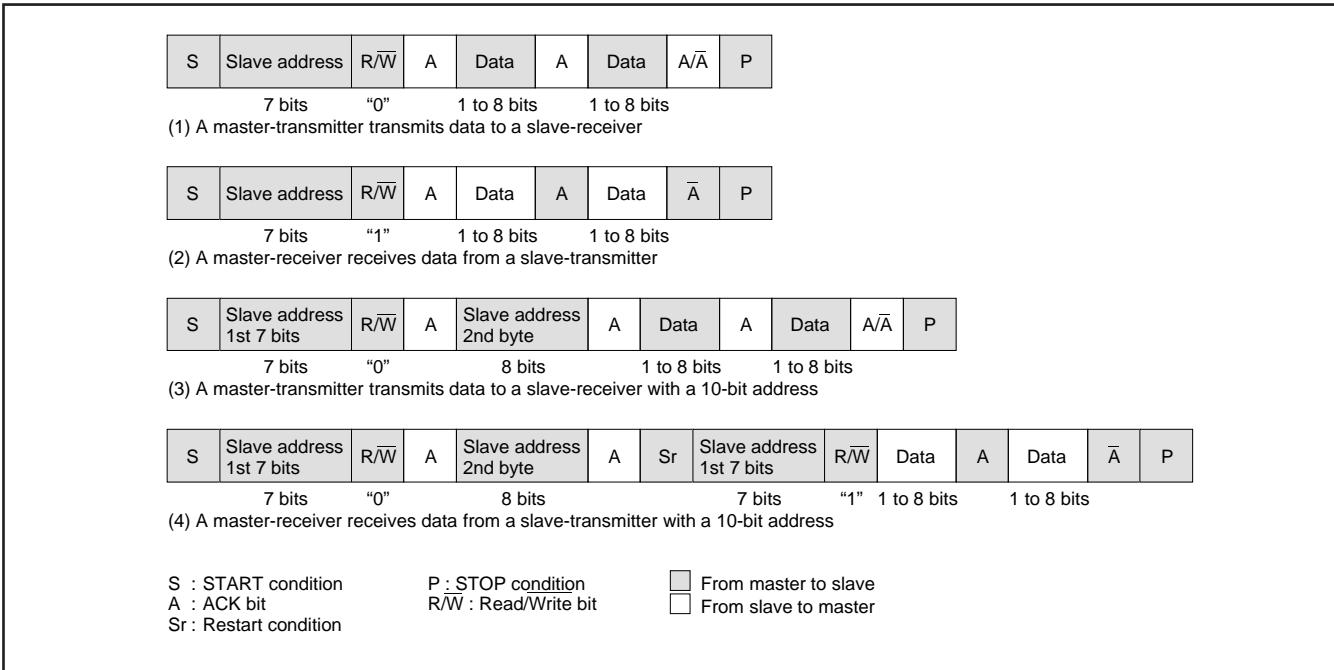


Fig. 12.6.12 Address Data Communication Format

12.6.12 Precautions when using multi-master I²C-BUS interface

(1) Read-modify-write instruction

The precautions when the read-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I²C-BUS interface are described below.

•I²C data shift register (S0)

When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.

•I²C address register (S0D)

When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because hardware changes the read/write bit (RBW) at the above timing.

•I²C status register (S1)

Do not execute the read-modify-write instruction for this register because all bits of this register are changed by hardware.

•I²C control register (S1D)

When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because hardware changes the bit counter (BC0-BC2) at the above timing.

•I²C clock control register (S2)

The read-modify-write instruction can be executed for this register.

(2) START condition generating procedure using multi-master

①Procedure example (The necessary conditions of the generating procedure are described as the following ② to ⑤).

```

    •
    •
    LDA   —      (Taking out of slave address value)
    SEI
    BBS  5,S1,BUSBUSY (BB flag confirming and branch process)
BUSFREE:
    STA  S0      (Writing of slave address value)
    LDM  #$F0, S1 (Trigger of START condition generating)
    CLI
    •
    •
    BUSBUSY:
    CLI      (Interrupt enabled)
    •
    •

```

②Use "STA," "STX" or "STY" of the zero page addressing instruction for writing the slave address value to the I²C data shift register.

③Use "LDM" instruction for setting trigger of START condition generating.

④Write the slave address value of above ② and set trigger of START condition generating of above ③ continuously shown the above procedure example.

⑤Disable interrupts during the following three process steps:

- BB flag confirming
- Writing of slave address value
- Trigger of START condition generating

When the condition of the BB flag is bus busy, enable interrupts immediately.

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(3) RESTART condition generating procedure

① Procedure example (The necessary conditions of the generating procedure are described as the following ② to ⑥.)

Execute the following procedure when the PIN bit is "0."

•		
LDM	#\$00, S1	(Select slave receive mode)
LDA	—	(Taking out of slave address value)
SEI		(Interrupt disabled)
STA	S0	(Writing of slave address value)
LDM	#\$F0, S1	(Trigger of RESTART condition generating)
CLI		(Interrupt enabled)
•		
•		

② Select the slave receive mode when the PIN bit is "0." Do not write "1" to the PIN bit. Neither "0" nor "1" is specified for the writing to the BB bit.

The TRX bit becomes "0" and the SDA pin is released.

③ The SCL pin is released by writing the slave address value to the I²C data shift register. Use "STA," "STX" or "STY" of the zero page addressing instruction for writing.

④ Use "LDM" instruction for setting trigger of RESTART condition generating.

⑤ Write the slave address value of above ③ and set trigger of RESTART condition generating of above ④ continuously shown the above procedure example.

⑥ Disable interrupts during the following two process steps:

- Writing of slave address value
- Trigger of RESTART condition generating

(4) STOP condition generating procedure

① Procedure example (The necessary conditions of the generating procedure are described as the following ② to ④.)

•		
SEI		(Interrupt disabled)
LDM	#\$C0, S1	(Select master transmit mode)
NOP		(Set NOP)
LDM	#\$D0, S1	(Trigger of STOP condition generating)
CLI		(Interrupt enabled)
•		
•		

② Write "0" to the PIN bit when master transmit mode is select.

③ Execute "NOP" instruction after setting of master transmit mode. Also, set trigger of STOP condition generating within 10 cycles after selecting of master transmit mode.

④ Disable interrupts during the following two process steps:

- Select of master transmit mode
- Trigger of STOP condition generating

(5) Writing to I²C status register

Do not execute an instruction to set the PIN bit to "1" from "0" and an instruction to set the MST and TRX bits to "0" from "1" simultaneously. It is because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to "0" from "1" simultaneously when the PIN bit is "1." It is because it may become the same as above.

(6) Process of after STOP condition generating

Do not write data in the I²C data shift register S0 and the I²C status register S1 until the bus busy flag BB becomes "0" after generating the STOP condition in the master mode. It is because the STOP condition waveform might not be normally generated. Reading to the above registers do not have the problem.

12.7 PWM OUTPUT CIRCUIT

This microcomputer is equipped with eight 8-bit PWMs (PWM0–PWM7). PWM0–PWM7 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of 4 μ s and repeat period of 1024 μ s (for $f(XIN) = 8$ MHz).

Figure 12.7.1 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to PWM0–PWM7 using $f(XIN)$ divided by 2 as a reference signal.

12.7.1 Data Setting

When outputting PWM0–PWM7, set 8-bit output data to the PWM_i register (*i* means 0 to 7; addresses 020016 to 020716).

12.7.2 Transmitting Data from Register to PWM circuit

Data transfer from the PWM register to the PWM circuit is executed at writing data to the register.

The signal output from the PWM output pin corresponds to the contents of this register.

12.7.3 PWM Operation

The following explains PWM operation.

First, set the bit 0 of PWM mode register 1 (address 020A16) to "0" (at reset, bit 0 is already set to "0" automatically), so that the PWM count source is supplied.

PWM0–PWM3 are also used as pins P04–P07, PWM4–PWM6 are also used as pins P00–P02, and PWM7 is also used as pin P50 and P03 respectively. Set the corresponding bits of the port P0 direction register to "1" (output mode). And select each output polarity by bit 3 of PWM mode register 1 (address 020A16). Then, set bits 7 to 0 of PWM mode register 2 to "1" (PWM output).

The PWM waveform is output from the PWM output pins by setting these registers.

Figure 12.7.2 shows the PWM timing. One cycle (T) is composed of 256 (2^8) segments. The 8 kinds of pulses, relative to the weight of each bit (bits 0 to 7), are output inside the circuit during 1 cycle. Refer to Figure 12.7.2 (a). The PWM outputs waveform which is the logical sum (OR) of pulses corresponding to the contents of bits 0 to 7 of the PWM register. Several examples are shown in Figure 12.7.2 (b). 256 kinds of output (HIGH area: 0/256 to 255/256) are selected by changing the contents of the PWM register. A length of entirely HIGH cannot be output, i.e. 256/256.

12.7.4 Output after Reset

At reset, the output of port P0 is in the high-impedance state, port P50 outputs Low, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

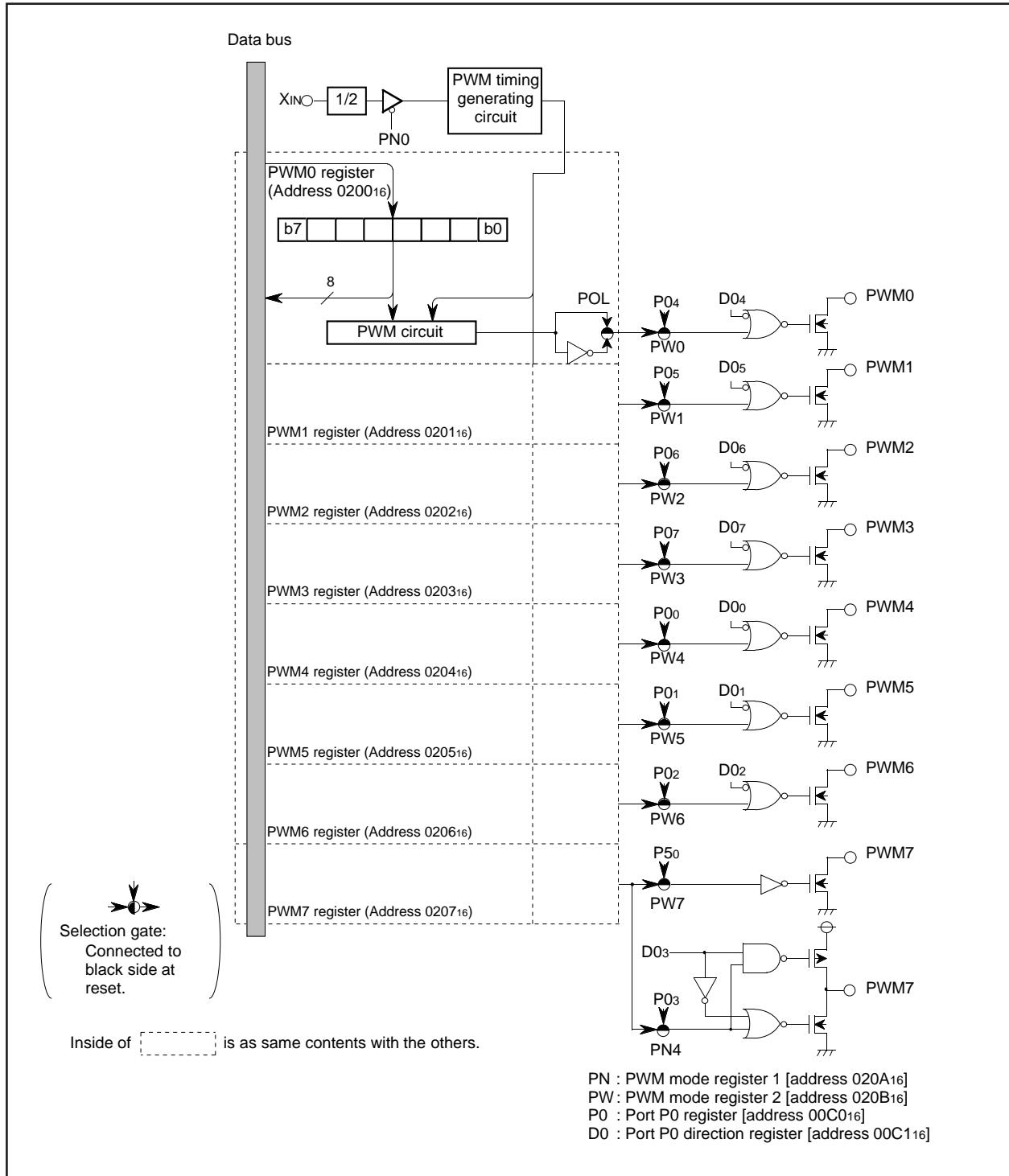


Fig. 12.7.1 PWM Block Diagram

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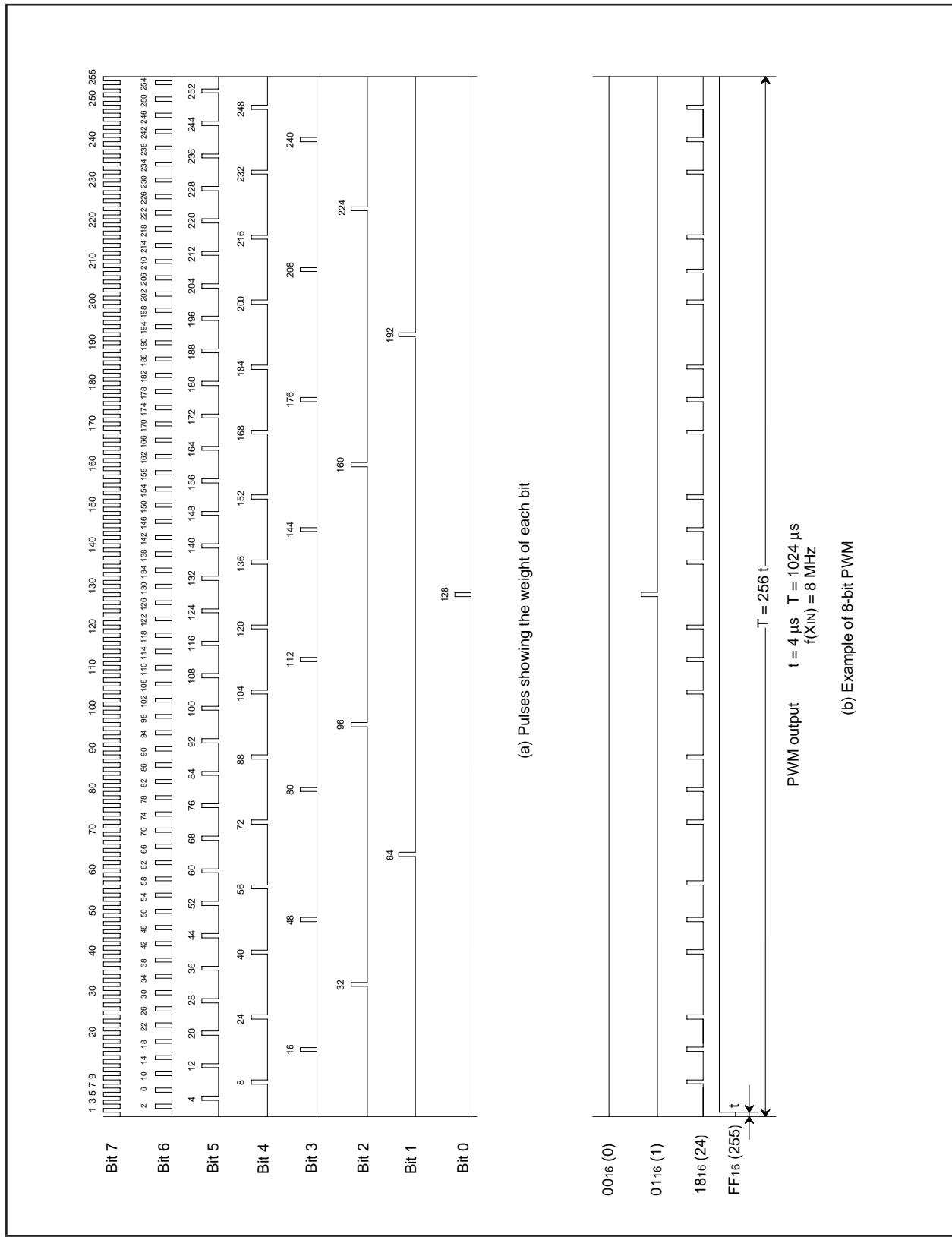


Fig. 12.7.2 PWM Timing

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PWM Mode Register 1

b7 b6 b5 b4 b3 b2 b1 b0



PWM mode register 1 (PN) [Address 020A16]

B	Name	Functions	After reset	R	W
0	PWM counts source selection bit (PN0)	0 : Count source supply 1 : Count source stop	0	R	W
1, 2	Nothing is assigned. These bits are write disable bits. When these bits are read out. the values are "0."		0	R	—
3	PWM output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	P03/PWM7 output selection bit (PN4)	0 : P03 output 1 : PWM7 output	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out. the values are "0."		0	R	—

Fig. 12.7.3 PWM Mode Register 1

PWM Mode Register 2

b7 b6 b5 b4 b3 b2 b1 b0



PWM mode register 2 (PW) [Address 020B16]

B	Name	Functions	After reset	R	W
0	P04/PWM0 output selection bit (PW0)	0 : P04 output 1 : PWM0 output	0	R	W
1	P05/PWM1 output selection bit (PW1)	0 : P05 output 1 : PWM1 output	0	R	W
2	P06/PWM2 output selection bit (PW2)	0 : P06 output 1 : PWM2 output	0	R	W
3	P07/PWM3 output selection bit (PW3)	0 : P07 output 1 : PWM3 output	0	R	W
4	P00/PWM4 output selection bit (PW4)	0 : P00 output 1 : PWM4 output	0	R	W
5	P01/PWM5 output selection bit (PW5)	0 : P01 output 1 : PWM5 output	0	R	W
6	P02/PWM6 output selection bit (PW6)	0 : P02 output 1 : PWM6 output	0	R	W
7	P50/PWM7 output selection bit (PW7)	0 : P50 output 1 : PWM7 output	0	R	W

Fig. 12.7.4 PWM Mode Register 2

12.8 A-D CONVERTER

12.8.1 A-D Conversion Register (AD)

A-D conversion register is a read-only register that stores the result of an A-D conversion. This register should not be read during A-D conversion.

12.8.2 A-D Control Register (ADCON)

The A-D control register controls A-D conversion. Bits 2 to 0 of this register select analog input pins. When these pins are not used as analog input pins, they are used as ordinary I/O pins. Bit 3 is the A-D conversion completion bit, A-D conversion is started by writing "0" to this bit. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Bit 4 controls connection between the resistor ladder and Vcc. When not using the A-D converter, the resistor ladder can be cut off from the internal Vcc by setting this bit to "0," accordingly providing low-power dissipation.

12.8.3 Comparison Voltage Generator (Resistor Ladder)

The voltage generator divides the voltage between Vss and Vcc by 256, and outputs the divided voltages to the comparator as the reference voltage Vref.

12.8.4 Channel Selector

The channel selector connects an analog input pin, selected by bits 2 to 0 of the A-D control register, to the comparator.

12.8.5 Comparator and Control Circuit

The conversion result of the analog input voltage and the reference voltage "Vref" is stored in the A-D conversion register. The A-D conversion completion bit and A-D conversion interrupt request bit are set to "1" at the completion of A-D conversion.

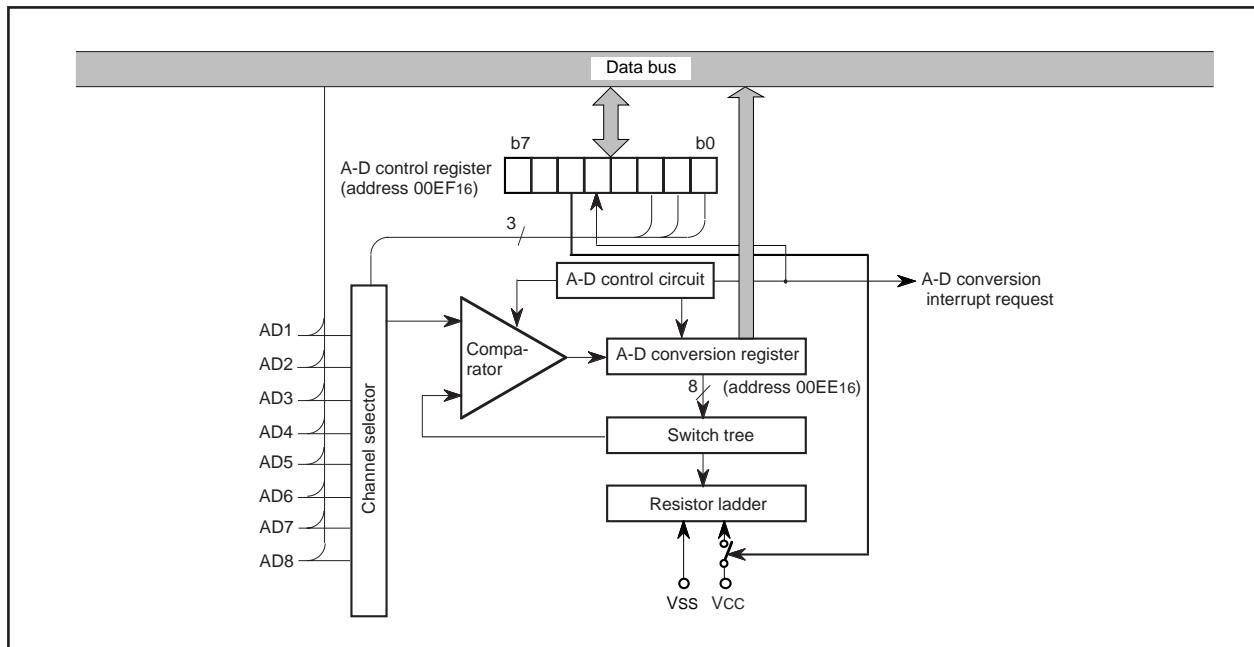


Fig. 12.8.1 A-D Comparator Block Diagram

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A-D Control Register

b7 b6 b5 b4 b3 b2 b1 b0

0

A-D control register (ADCON) [Address 00EF16]

B	Name	Functions	After reset	R \ W
0	Analog input pin selection bits (ADIN0 to ADIN2)	b2 b1 b0 0 0 0 : AD1 0 0 1 : AD2 0 1 0 : AD3 0 1 1 : AD4 1 0 0 : AD5 1 0 1 : AD6 1 1 0 : AD7 1 1 1 : AD8	0	R \ W
3	A-D conversion completion bit (ADSTR)	0: Conversion in progress 1: Conversion completed	1	R \ W
4	Vcc connection selection bit (ADVREF)	0: OFF 1: ON	0	R \ W
5	Fix this bit to "0."		0	R \ W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R —
7	Fix this bit to "0."		0	R \ W

Fig. 12.8.2 A-D Control Register

12.8.6 Conversion Method

- ① Set bit 7 of the interrupt input polarity register (address 021216) to "1" to generate an interrupt request at completion of A-D conversion.
- ② Set the A-D conversion · INT3 interrupt request bit to "0" (even when A-D conversion is started, the A-D conversion · INT3 interrupt request bit is not set to "0" automatically).
- ③ When using A-D conversion interrupt, enable interrupts by setting A-D conversion · INT3 interrupt request bit to "1" and setting the interrupt disable flag to "0."
- ④ Set the Vcc connection selection bit to "1" to connect Vcc to the resistor ladder.
- ⑤ Select analog input pins by the analog input selection bit of the A-D control register.
- ⑥ Set the A-D conversion completion bit to "0." This write operation starts the A-D conversion. Do not read the A-D conversion register during the A-D conversion.
- ⑦ Verify the completion of the conversion by the state ("1") of the A-D conversion completion bit, the state ("1") of A-D conversion · INT3 interrupt request bit, or the occurrence of an A-D conversion interrupt.
- ⑧ Read the A-D conversion register to obtain the conversion results.

Note : When the ladder resistor is disconnect from Vcc, set the Vcc connection selection bit to "0" between steps ⑦ and ⑧.

12.8.7 Internal Operation

When the A-D conversion starts, the following operations are automatically performed.

- ① The A-D conversion register is set to "0016."
- ② The most significant bit of the A-D conversion register becomes "1," and the comparison voltage "Vref" is input to the comparator. At this point, Vref is compared with the analog input voltage "VIN."
- ③ Bit 7 is determined by the comparison results as follows.

When $Vref < VIN$: bit 7 holds "1"
When $Vref > VIN$: bit 7 becomes "0"

With the above operations, the analog value is converted into a digital value. The A-D conversion terminates in a maximum of 50 machine cycles (12.5 μ s at $f(XIN) = 8$ MHz) after it starts, and the conversion result is stored in the A-D conversion register.

An A-D conversion interrupt request occurs at the same time as A-D conversion completion, the A-D conversion · INT3 interrupt request bit becomes "1." The A-D conversion completion bit also becomes "1."

Table 12.8.1 Expression for Vref and VREF

A-D conversion register contents "n" (decimal notation)	Vref (V)
0	0
1 to 255	$\frac{VREF}{256} \sim (n \mid 0.5)$

Note: VREF indicates the reference voltage (= Vcc).

	Contents of A-D conversion register	Reference voltage (Vref) [V]
A-D conversion start	0 0 0 0 0 0 0 0	0
1st comparison start	1 0 0 0 0 0 0 0	$\frac{VREF}{2} - \frac{VREF}{512}$
2nd comparison start	1 1 0 0 0 0 0 0	$\frac{VREF}{2} \pm \frac{VREF}{4} - \frac{VREF}{512}$
3rd comparison start	1 2 1 0 0 0 0 0	$\frac{VREF}{2} \pm \frac{VREF}{4} \pm \frac{VREF}{8} - \frac{VREF}{512}$
8th comparison start	1 2 3 4 5 6 7 1	$\frac{VREF}{2} \pm \frac{VREF}{4} \pm \frac{VREF}{8} \pm \dots$ $\dots \pm \frac{VREF}{256} - \frac{VREF}{512}$
A-D conversion completion (8th comparison completion)	1 2 3 4 5 6 7 8	Digital value corresponding to analog input voltage.
		m : Value determined by mth (m = 1 to 8) result

Fig. 12.8.3 Changes in A-D Conversion Register and Comparison Voltage during A-D Conversion

12.8.8 Definition of A-D Conversion Accuracy

The definition of A-D conversion accuracy is described below (refer to Figure 12.8.4).

(1) Relative Accuracy

• Zero transition error (V_{0T})

The deviation of the input voltage at which A-D conversion output data changes from "0" to "1," from the corresponding ideal A-D conversion characteristics between 0 and V_{REF} .

$$V_{0T} = \frac{(V_0 - 1/2 \times V_{REF}/256)}{1LSB} \quad [LSB]$$

• Full-scale transition error (V_{FST})

The deviation of the input voltage at which A-D conversion output data changes from "255" to "254," from the corresponding ideal A-D conversion characteristics between 0 and V_{REF} .

$$V_{FST} = \frac{(V_{REF} - 3/2 \times V_{REF}/256) - V_{254}}{1LSB} \quad [LSB]$$

• Non-linearity error

The deviation of the actual A-D conversion characteristics, from the ideal A-D conversion characteristics between V_0 and V_{254} .

$$\text{Non-linearity error} = \frac{V_n - (1LSB \times n + V_0)}{1LSB} \quad [LSB]$$

• Differential non-linearity error

The deviation of the input voltage required to change output data by "1," from the corresponding ideal A-D conversion characteristics between 0 and V_{REF} .

$$\text{Differential non-linearity error} = \frac{(V_{n+1} - V_n) - 1LSB}{1LSB} \quad [LSB]$$

(2) Absolute Accuracy

• Absolute accuracy error

The deviation of the actual A-D conversion characteristics, from the ideal A-D conversion characteristics between 0 and V_{REF} .

$$\text{Absolute accuracy error} = \frac{V_n - 1LSBA \times (n + 1/2)}{1LSBA} \quad [LSB]$$

Note: The analog input voltage "V_n" at which A-D conversion output data changes from "n" to "n + 1" (n ; 0 to 254) is as follows (refer to Figure 12.8.4) :

$$1LSB \text{ with respect to relative accuracy} = \frac{V_{254} - V_0}{254} \quad [V]$$

$$1LSBA \text{ with respect to absolute accuracy} = \frac{V_{REF}}{256} \quad [V]$$

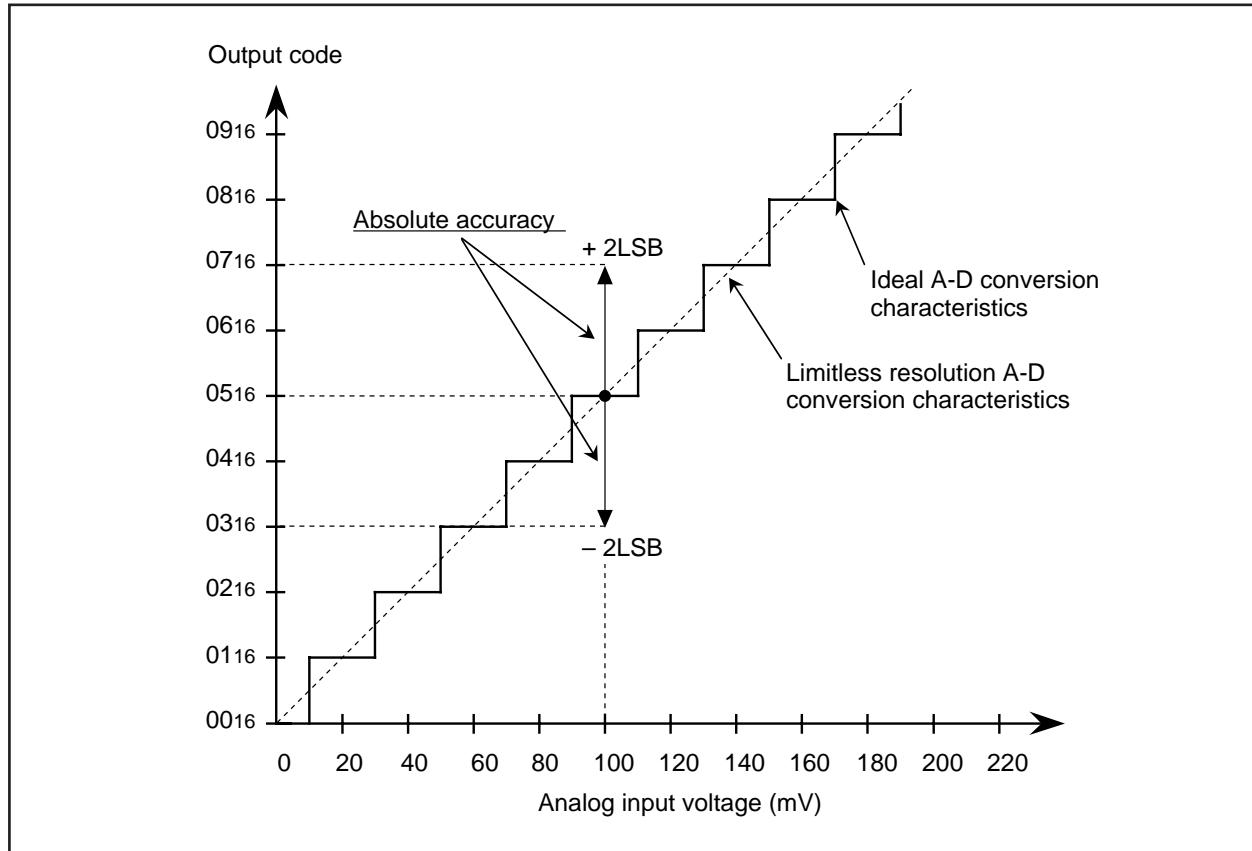


Fig. 12.8.4 Definition of A-D Conversion Accuracy

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12.9 ROM CORRECTION FUNCTION

This can correct program data in ROM. Up to 2 addresses (2 blocks) can be corrected, a program for correction is stored in the ROM correction memory in RAM. The ROM memory for correction is 32 bytes X 2 blocks.

Block 1 : addresses 02C016 to 02DF16

Block 2 : addresses 02E016 to 02FF16

Set the address of the ROM data to be corrected into the ROM correction address register. When the value of the counter matches the ROM data address in the ROM correction address, the main program branches to the correction program stored in the ROM memory for correction. To return from the correction program to the main program, the op code and operand of the JMP instruction (total of 3 bytes) are necessary at the end of the correction program. When the blocks 1 and 2 are used in series, the above instruction is not needed at the end of the block 1.

The ROM correction function is controlled by the ROM correction enable register.

Notes 1: Specify the first address (op code address) of each instruction as the ROM correction address.

- 2:** Use the JMP instruction (total of 3 bytes) to return from the correction program to the main program.
- 3:** Do not set the same ROM correction address to blocks 1 and 2.
- 4:** For the M37280MK-XXXSP and M37280EKSP, when using the expansion ROM (BK7 = "1"), the ROM correction function do not operate used for addresses 100016 to 1FFF16. Note that on programming.

ROM correction address 1 (high-order)	020C16
ROM correction address 1 (low-order)	020D16
ROM correction address 2 (high-order)	020E16
ROM correction address 2 (low-order)	020F16

Fig. 12.9.1 ROM Correction Address Registers

ROM Correction Enable Register

b7 b6 b5 b4 b3 b2 b1 b0		ROM correction enable register (RCR) [Address 021016]			
B	Name	Functions	After reset	R	W
0	Block 1 enable bit (RCR0)	0: Disabled 1: Enabled	0	R	W
1	Block 2 enable bit (RCR1)	0: Disabled 1: Enabled	0	R	W
2, 3	Fix these bits to "0."		0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 12.9.2 ROM Correction Enable Register

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12.10 DATA SLICER

This microcomputer includes the data slicer function for the closed caption decoder (referred to as the CCD). This function takes out the caption data superimposed in the vertical blanking interval of a composite video signal. A composite video signal which makes the sync chip's polarity negative is input to the CVIN pin.

When the data slicer function is not used, the data slicer circuit and the timing signal generating circuit can be cut off by setting bit 0 of the data slicer control register 1 (address 00E016) to "0." These settings can realize the low-power dissipation.

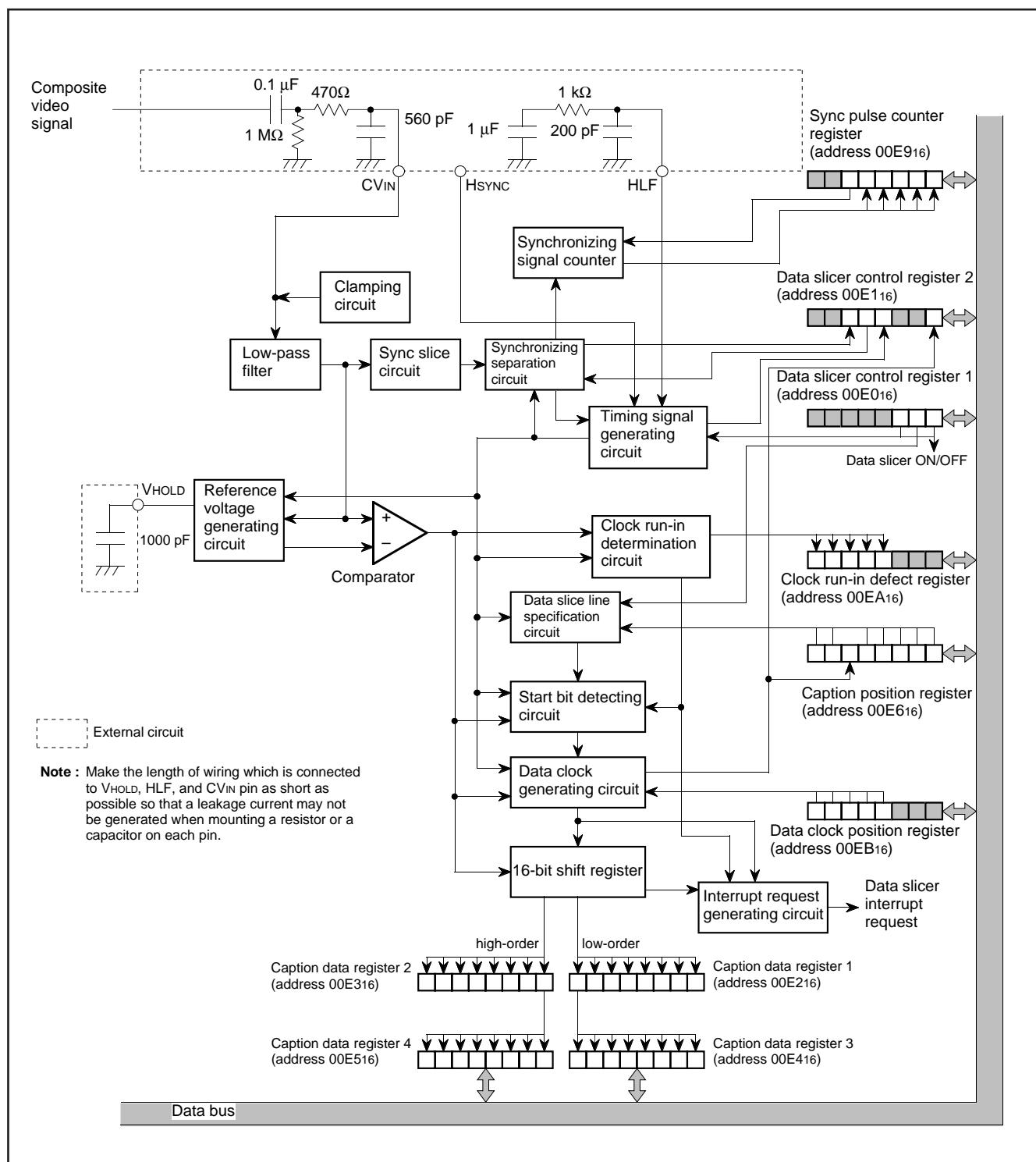


Fig. 12.10.1 Data Slicer Block Diagram

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12.10.1 Notes When not Using Data Slicer

When bit 0 of data slicer control register 1 (address 00E016) is "0," terminate the pins as shown in Figure 12.10.2.

<When data slicer circuit and timing signal generating circuit is in OFF state>

Apply the same voltage as Vcc to AVcc pin.

Apply HLF pin Vcc or Vss level.

Apply VHOLD pin Vcc or Vss level.

Pull-up CVIN pin to Vcc through a resistor of 5 kΩ or more.

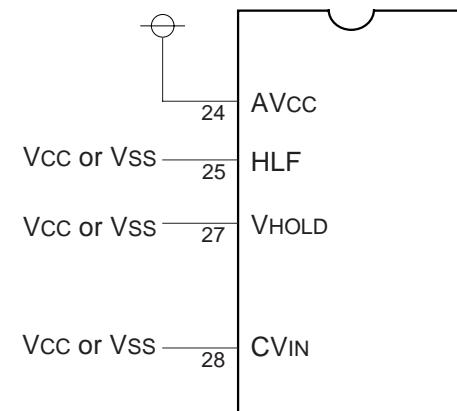


Fig. 12.10.2 Termination of Data Slicer Input/Output Pins when Data Slicer Circuit and Timing Generating Circuit Is in OFF State

When both bits 0 and 2 of data slicer control register 1 (address 00E016) are "1," terminate the pins as shown in Figure 12.10.3.

<When using a reference clock generated in timing signal generating circuit as OSD clock>

Apply the same voltage as Vcc to AVcc pin.

Connect the same external circuit as when using data slicer to HLF pin.

Leave VHOLD pin open.

Pull-up CVIN to Vcc through a resistor of 5 kΩ or more.

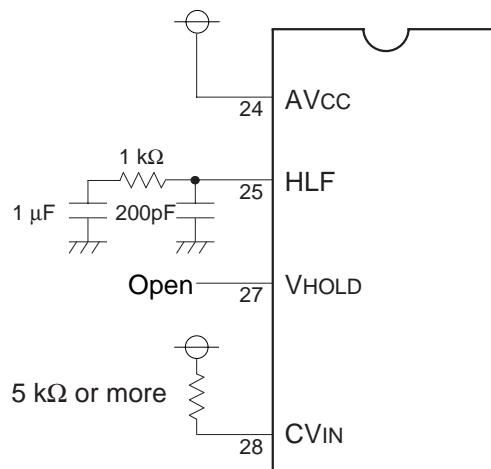


Fig. 12.10.3 Termination of Data Slicer Input/Output Pins when Timing Signal Generating Circuit Is in ON State

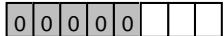
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Figures 12.10.4 and 12.10.5 the data slicer control registers.

Data Slicer Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0



Data slicer control register 1(DSC1) [Address 00E016]

B	Name	Functions	After reset	R	W
0	Data slicer and timing signal generating circuit control bit (DSC10)	0: Stopped 1: Operating	0	R	W
1	Selection bit of data slice reference voltage generating field (DSC11)	0: F2 1: F1	0	R	W
2	Reference clock source selection bit (DSC12)	0: Video signal 1: HSYNC signal	0	R	W
3 to 7	Fix these bits to "0."		0	R	W

Definition of fields 1 (F1) and 2 (F2)

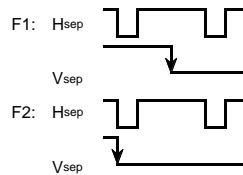
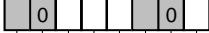


Fig. 12.10.4 Data Slicer Control Register 1

Data Slicer Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0



Data slicer control register 2 (DSC2) [Address 00E116]

B	Name	Functions	After reset	R	W
0	Caption data latch completion flag 1 (DSC20)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	—
1	Fix this bit to "0."		0	R	W
2	Test bit	Read-only	Indeterminate	R	—
3	Field determination flag(DSC23)	0: F2 1: F1	Indeterminate	R	—
4	Vertical synchronous signal (Vsep) generating method selection bit (DSC24)	0: Method (1) 1: Method (2)	0	R	W
5	V-pulse shape determination flag (DSC25)	0: Match 1: Mismatch	Indeterminate	R	—
6	Fix this bit to "0."		0	R	W
7	Test bit	Read-only	Indeterminate	R	—

Definition of fields 1 (F1) and 2 (F2)

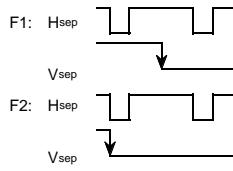


Fig. 12.10.5 Data Slicer Control Register 2

PRELIMINARY

Notice: This is not a final specification.
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12.10.2 Clamping Circuit and Low-pass Filter

The clamp circuit clamps the sync chip part of the composite video signal input from the CVIN pin. The low-pass filter attenuates the noise of clamped composite video signal. The CVIN pin to which composite video signal is input requires a capacitor (0.1 μ F) coupling outside. Pull down the CVIN pin with a resistor of hundreds of kilohms to 1 Ω . In addition, we recommend to install externally a simple low-pass filter using a resistor and a capacitor at the CVIN pin (refer to Figure 12.10.1).

12.10.3 Sync Slice Circuit

This circuit takes out a composite sync signal from the output signal of the low-pass filter.

12.10.4 Synchronous Signal Separation Circuit

This circuit separates a horizontal synchronous signal and a vertical synchronous signal from the composite sync signal taken out in the sync slice circuit.

(1)Horizontal Synchronous Signal (Hsep)

A one-shot horizontal synchronizing signal Hsep is generated at the falling edge of the composite sync signal.

(2)Vertical Synchronous Signal (Vsep)

As a Vsep signal generating method, it is possible to select one of the following 2 methods by using bit 4 of the data slicer control register 2 (address 00E116).

- Method 1 The “L” level width of the composite sync signal is measured. If this width exceeds a certain time, a Vsep signal is generated in synchronization with the rising of the timing signal immediately after this “L” level.

- Method 2 The “L” level width of the composite sync signal is measured. If this width exceeds a certain time, it is detected whether a falling of the composite sync signal exists or not in the “L” level period of the timing signal immediately after this “L” level. If a falling exists, a Vsep signal is generated in synchronization with the rising of the timing signal (refer to Figure 12.10.6).

Figure 12.10.6 shows a Vsep generating timing. The timing signal shown in the figure is generated from the reference clock which the timing generating circuit outputs.

Reading bit 5 of data slicer control register 2 permits determining the shape of the V-pulse portion of the composite sync signal. As shown in Figure 12.10.7, when the A level matches the B level, this bit is “0.” In the case of a mismatch, the bit is “1.”

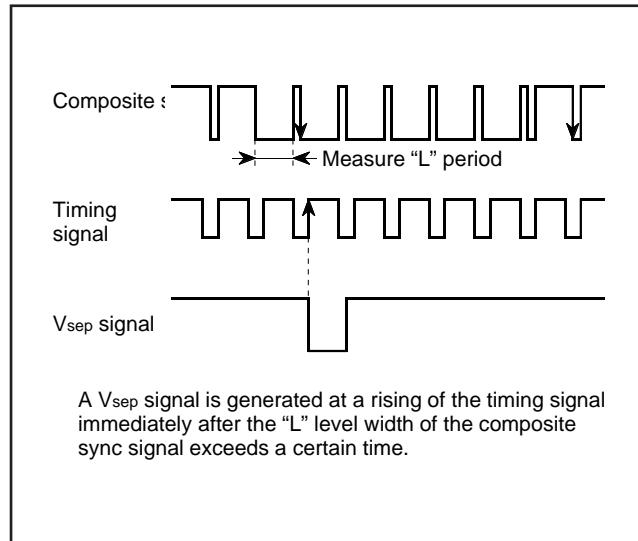


Fig. 12.10.6 Vsep Generating Timing (method 2)

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12.10.5 Timing Signal Generating Circuit

This circuit generates a reference clock which is 832 times as large as the horizontal synchronous signal frequency. It also generates various timing signals on the basis of the reference clock, horizontal synchronous signal and vertical synchronizing signal. The circuit operates by setting bit 0 of data slicer control register 1 (address 00E016) to "1."

The reference clock can be used as a display clock for OSD function in addition to the data slicer. The HSYNC signal can be used as a count source instead of the composite sync signal. However, when the HSYNC signal is selected, the data slicer cannot be used. A count source of the reference clock can be selected by bit 2 of data slicer control register 1 (address 00E016).

For the pins HLF, connect a resistor and a capacitor as shown in Figure 12.10.1. Make the length of wiring which is connected to these pins as short as possible so that a leakage current may not be generated.

Note: It takes a few tens of milliseconds until the reference clock becomes stable after the data slicer and the timing signal generating circuit are started. In this period, various timing signals, H_{sep} signals and V_{sep} signals become unstable. For this reason, take stabilization time into consideration when programming.

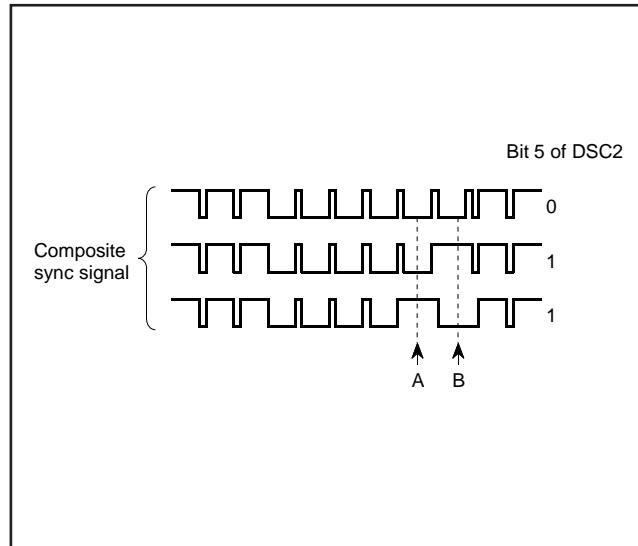


Fig. 12.10.7 Determination of V-pulse Waveform

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

12.10.6 Data Slice Line Specification Circuit

(1) Specification of Data Slice Line

This circuit decides a line on which caption data is superimposed. The line 21 (fixed), 1 appropriate line for a period of 1 field (total 2 line for a period of 1 field), and both fields (F1 and F2) are sliced their data. The caption position register (address 00E616) is used for each setting (refer to Table 12.10.1).

The counter is reset at the falling edge of V_{sep} and is incremented by 1 every H_{sep} pulse. When the counter value matched the value specified by bits 4 to 0 of the caption position register, this H_{sep} is sliced.

The values of "0016" to "1F16" can be set in the caption position register (at setting only 1 appropriate line). Figure 12.10.8 shows the signals in the vertical blanking interval. Figure 12.10.9 shows the structure of the caption position register.

(2) Specification of Line to Set Slice Voltage

The reference voltage for slicing (slice voltage) is generated for the clock run-in pulse in the particular line (refer to Table 7). The field to generate slice voltage is specified by bit 1 of data slicer control register 1. The line to generate slice voltage 1 field is specified by bits 6, 7 of the caption position register (refer to Table 12.10.1).

(3) Field Determination

The field determination flag can be read out by bit 3 of data slicer control register 2. This flag charge at the falling edge of V_{sep} .

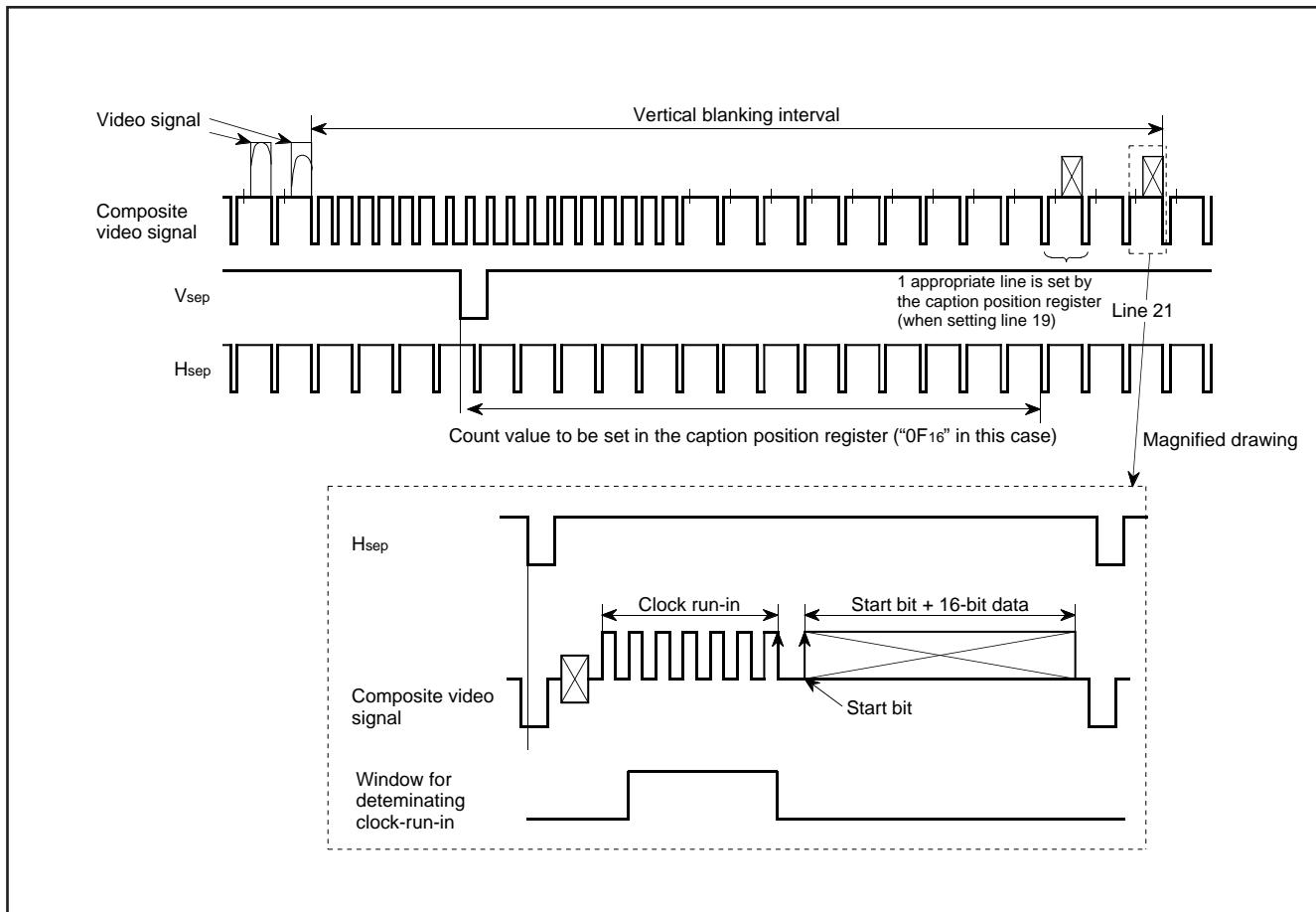


Fig. 12.10.8 Signals in Vertical Blanking Interval

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Caption Position Register

b7 b6 b5 b4 b3 b2 b1 b0



Caption Position Register (CPS) [Address 00E616]

B	Name	Functions	After reset	R	W
0 to 4	Caption position bits(CPS0 to CPS4)		0	R	W
5	Caption data latch completion flag 2 (CPS5)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	—
6, 7	Slice line mode specification bits (in 1 field) (CPS6, CPS7)	Refer to the corresponding Table (Table 12.10.1).	0	R	W

Fig. 12.10.9 Caption Position Register

Table 12.10.1 Specification of Data Slice Line

CPS		Field and Line to Be Sliced Data	Field and Line to Generate Slice Voltage
b7	b6		
0	0	<ul style="list-style-type: none"> Both fields of F1 and F2 Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2) 	<ul style="list-style-type: none"> Field specified by bit 1 of DSC1 Line 21 (total 1 line)
0	1	<ul style="list-style-type: none"> Both fields of F1 and F2 A line specified by bits 4 to 0 of CPS (total 1 line) (See note 3) 	<ul style="list-style-type: none"> Field specified by bit 1 of DSC1 A line specified by bits 4 to 0 of CPS (total 1 line) (See note 3)
1	0	<ul style="list-style-type: none"> Both fields of F1 and F2 Line 21 (total 1 line) 	<ul style="list-style-type: none"> Field specified by bit 1 of DSC1 Line 21 (total 1 line)
1	1	<ul style="list-style-type: none"> Both fields of F1 and F2 Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2) 	<ul style="list-style-type: none"> Field specified by bit 1 of DSC1 Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2)

Notes 1: DSC1 is data slicer control register 1.

CPS is caption position register.

2: Set "0016" to "1016" to bits 4 to 0 of CPS.

3: Set "0016" to "1F16" to bits 4 to 0 of CPS.

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12.10.7 Reference Voltage Generating Circuit and Comparator

The composite video signal clamped by the clamping circuit is input to the reference voltage generating circuit and the comparator.

(1) Reference Voltage Generating Circuit

This circuit generates a reference voltage (slice voltage) by using the amplitude of the clock run-in pulse in line specified by the data slice line specification circuit. Connect a capacitor between the V_{HOLD} pin and the V_{SS} pin, and make the length of wiring as short as possible so that a leakage current may not be generated.

(2) Comparator

The comparator compares the voltage of the composite video signal with the voltage (reference voltage) generated in the reference voltage generating circuit, and converts the composite video signal into a digital value.

12.10.8 Start Bit Detecting Circuit

This circuit detects a start bit at line decided in the data slice line specification circuit.

The detection of a start bit is described below.

- ① A sampling clock is generated by dividing the reference clock output by the timing signal.
- ② A clock run-in pulse is detected by the sampling clock.
- ③ After detection of the pulse, a start bit pattern is detected from the comparator output.

12.10.9 Clock Run-in Determination Circuit

This circuit determinates clock run-in by counting the number of pulses in a window of the composite video signal.

The reference clock count value in one pulse cycle is stored in bits 3 to 7 of the clock run-in detect register (address 00EA16). Read out these bits after the occurrence of a data slicer interrupt (refer to "12.10.12 Interrupt Request Generating Circuit").

Figure 12.10.10 shows the structure of clock run-in detect register.

Clock Run-in Detect Register

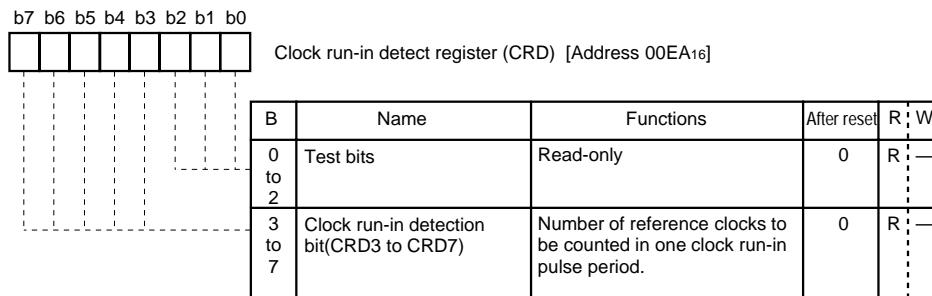


Diagram illustrating the structure of the Clock Run-in Detect Register (CRD). The register is 16 bits wide, labeled b7 to b0. Bits b7 to b2 are labeled "Test bits" and are read-only. Bits b3 to b7 are labeled "Clock run-in detection bit(CRD3 to CRD7)" and are used to count reference clocks. The register is addressed at 00EA16.

B	Name	Functions	After reset	R	W
0 to 2	Test bits	Read-only	0	R	—
3 to 7	Clock run-in detection bit(CRD3 to CRD7)	Number of reference clocks to be counted in one clock run-in pulse period.	0	R	—

Fig. 12.10.10 Clock Run-in Detect Register

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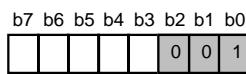
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12.10.10 Data Clock Generating Circuit

This circuit generates a data clock synchronized with the start bit detected in the start bit detecting circuit. The data clock stores caption data to the 16-bit shift register. When the 16-bit data has been stored and the clock run-in determination circuit determines clock run-in, the caption data latch completion flag is set. This flag is reset at a falling of the vertical synchronous signal (V_{sep}).

Data Clock Position Register



Data clock position register (DPS) [Address 00EB₁₆]

B	Name	Functions	After reset	R	W
0	Fix these bits to "1."		1	R	W
1,2	Fix this bit to "0."		0	R	W
3	Data clock position set bits (DPS3 to DPS7)		1	R	W
4 to 7			0		

Fig. 12.10.11 Data Clock Position Register

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12.10.11 16-bit Shift Register

The caption data converted into a digital value by the comparator is stored into the 16-bit shift register in synchronization with the data clock. The contents of the high-order 8 bits of the stored caption data can be obtained by reading out data register 2 (address 00E316) and data register 4 (address 00E516). The contents of the low-order 8 bits can be obtained by reading out data register 1 (address 00E216) and data register 3 (address 00E416), respectively. These registers are reset to "0" at a falling of Vsep. Read out data registers 1 and 2 after the occurrence of a data slicer interrupt (refer to "12.10.12 Interrupt Request Generating Circuit").

12.10.12 Interrupt Request Generating Circuit

The interrupt requests as shown in Table 12.10.3 are generated by combination of the following bits; bits 6 and 7 of the caption position register (address 00E616). Read out the contents of data registers 1 to 4 and the contents of bits 3 to 7 of the clock run-in detect register after the occurrence of a data slicer interrupt request.

Table 12.10.2 Contents of Caption Data Latch Completion Flag and 16-bit Shift Register

Slice Line Specification Mode		Contents of Caption Data Latch Completion Flag		Contents of 16-bit Shift Register	
CPS		Completion Flag 1 (bit 0 of DSC2)	Completion Flag 2 (bit 5 of CPS)	Caption Data Registers 1, 2	Caption Data Registers 3, 4
bit 7	bit 6				
0	0	Line 21	A line specified by bits 4 to 0 of CPS	16-bit data of line 21	16-bit data of a line specified by bits 4 to 0 of CPS
0	1	A line specified by bits 4 to 0 of CPS	Invalid	16-bit data of a line specified by bits 4 to 0 of CPS	Invalid
1	0	Line 21	Invalid	16-bit data of line 21	Invalid
1	1	Line 21	A line specified by bits 4 to 0 of CPS	16-bit data of line 21	16-bit data of a line specified by bits 4 to 0 of CPS

CPS: Caption position register

DSC2: Data slicer control register 2

Table 12.10.3 Occurrence Sources of Interrupt Request

Caption position register		Occurrence Sources of Interrupt Request at End of Data Slice Line
b7	b6	
0	0	After slicing line 21
	1	After a line specified by bits 4 to 0 of CPS
1	0	After slicing line 21
	1	After slicing line 21

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12.10.13 Synchronous Signal Counter

The synchronous signal counter counts the composite sync signal taken out from a video signal in the data slicer circuit or the vertical synchronous signal V_{sep} as a count source.

The count value in a certain time (T time) generated by $f(XIN)/2^{13}$ or $f(XIN)/2^3$ is stored into the 5-bit latch. Accordingly, the latch value changes in the cycle of T time. When the count value exceeds "1F16," "1F16" is stored into the latch.

The latch value can be obtained by reading out the sync pulse counter register (address 00E916). A count source is selected by bit 5 of the sync pulse counter register.

The synchronous signal counter is used when bit 0 of PWM mode register 1 (address 020816).

Figure 12.10.12 shows the structure of the sync pulse counter and Figure 12.10.13 shows the synchronous signal counter block diagram.

Sync Pulse Counter Register

B	Name	Functions	After reset	R	W
0 to 4	Count value (HC0 to HC4)		Indeterminate	R	—
5	Count source (HC5)	0: HSYNC signal 1: Composite sync signal	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 12.10.12 Sync Pulse Counter Register

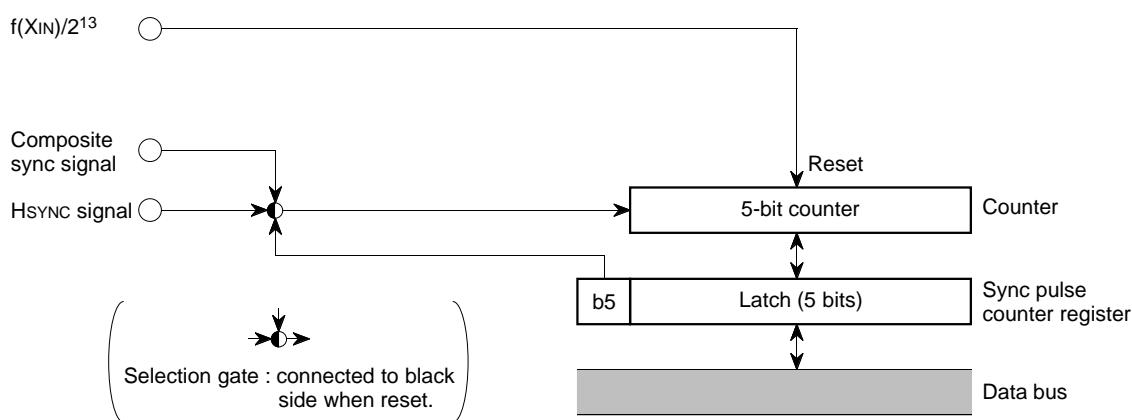


Fig. 12.10.13 Synchronous Signal Counter Block Diagram

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12.11 OSD FUNCTIONS

Table 12.11.1 outlines the OSD functions.

This OSD function can display the following: the block display (32 characters X 16 lines), the SPRITE display. And besides, the function can display the both display at the same time. There are 3 display modes and they are selected by a block unit. The display modes are selected by block control register i (i = 1 to 16).

The features of each mode are described below.

Table.12.11.1 Features of Each Display Style

Parameter	Display style	Block display			SPRITE display			
		CC mode (Closed caption mode)	OSD mode (On-screen display mode)	CDOSD mode (Color dot on-screen display mode)				
Number of display characters		32 characters X 16 lines			1 character			
Dot structure	16 X 20 dots	(Character sidplay area: 16 X 26 dots)		16 X 26 dots	16 X 20 dots			
	(Character sidplay area: 16 X 26 dots)							
Kinds of characters	510 kinds		62 kinds	1 kind				
Font memory	ROM				RAM			
Kinds of character sizes	4 kinds	14 kinds			8 kinds			
Pre-divide ratio (Note)	X 1, X 2	X 1, X 2, X 3			X 1, X 2			
	Dot size	1Tc X 1/2H, 1Tc X 1H	1Tc X 1/2H, 1Tc X 1H, 1.5Tc X 1/2H, 1.5Tc X 1H, 2Tc X 2H, 3Tc X 3H	1Tc X 1/2H, 1Tc X 1H, 2Tc X 2H, 3Tc X 3H				
Attribute	Smooth italic, under line, flash	Border						
Character font coloring	1 screen: 8 kinds (per character unit) Max. 64 kinds	1 screen: 15 kinds (per character unit) Max. 64 kinds	1 screen: 8 kinds (per dot unit) 1 screen: 15 kinds (only specified dots are colored per character unit) Max. 64 kinds	1 screen: 8 kinds (per dot unit) Max. 64 kinds	1 screen: 8 kinds (per dot unit) Max. 64 kinds			
Character background coloring	Possible (a character unit, 1 screen: 4 kinds, Max. 64 kinds)	Possible (a character unit, 1 screen: 15 kinds, Max. 64 kinds)						
Display layer	Layer 1	Layer 1 and layer 2			Layer 3 (with highest priority)			
OSD output	Analog R, G, B output (each 4 adjustment levels : 64 colors), Digital OUT1, OUT2 output							
Raster coloring	Possible (a screen unit, max 64 kinds)							
Function	Auto solid space function	Triple layer OSD function, window function, blank funtion						
Display expansion (multiline display)	Possible							

Notes1: The divide ratio of the frequency divider (the pre-divide circuit) is referred as "pre-divide ratio" hereafter.

2: The character size is specified with dot size and pre-divide ratio (refer to "2.11.3 Dot Size").

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The OSD circuit has an extended display mode. This mode allows multiple lines (16 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 12.11.1 shows the configuration of OSD character display area. Figure 12.11.2 shows the block diagram of the OSD circuit. Figure 12.11.3 shows the OSD control register 1. Figure 12.11.4 shows the block control register i.

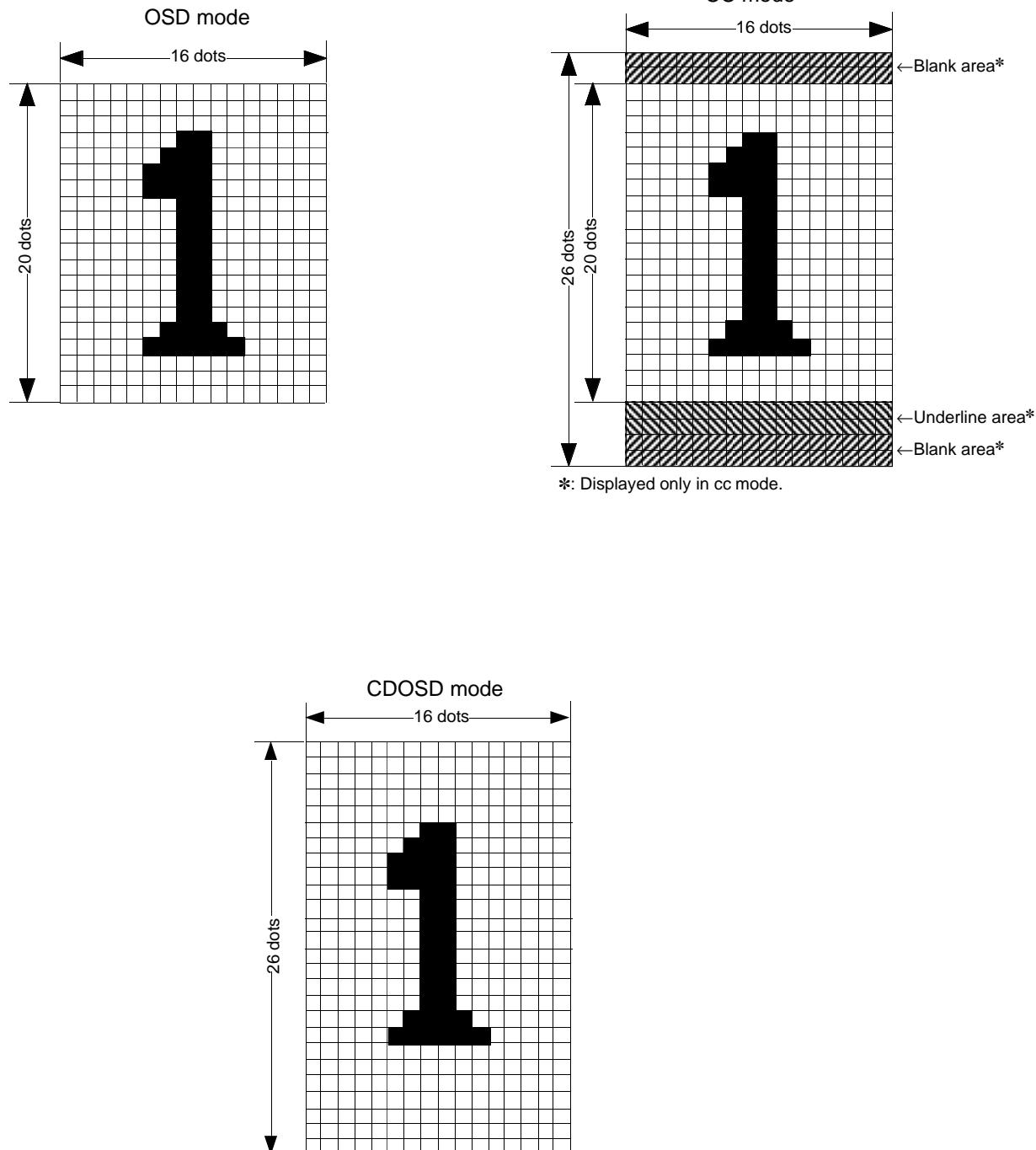


Fig. 12.11.1 Configuration of OSD Character Display Area

PRELIMINARY

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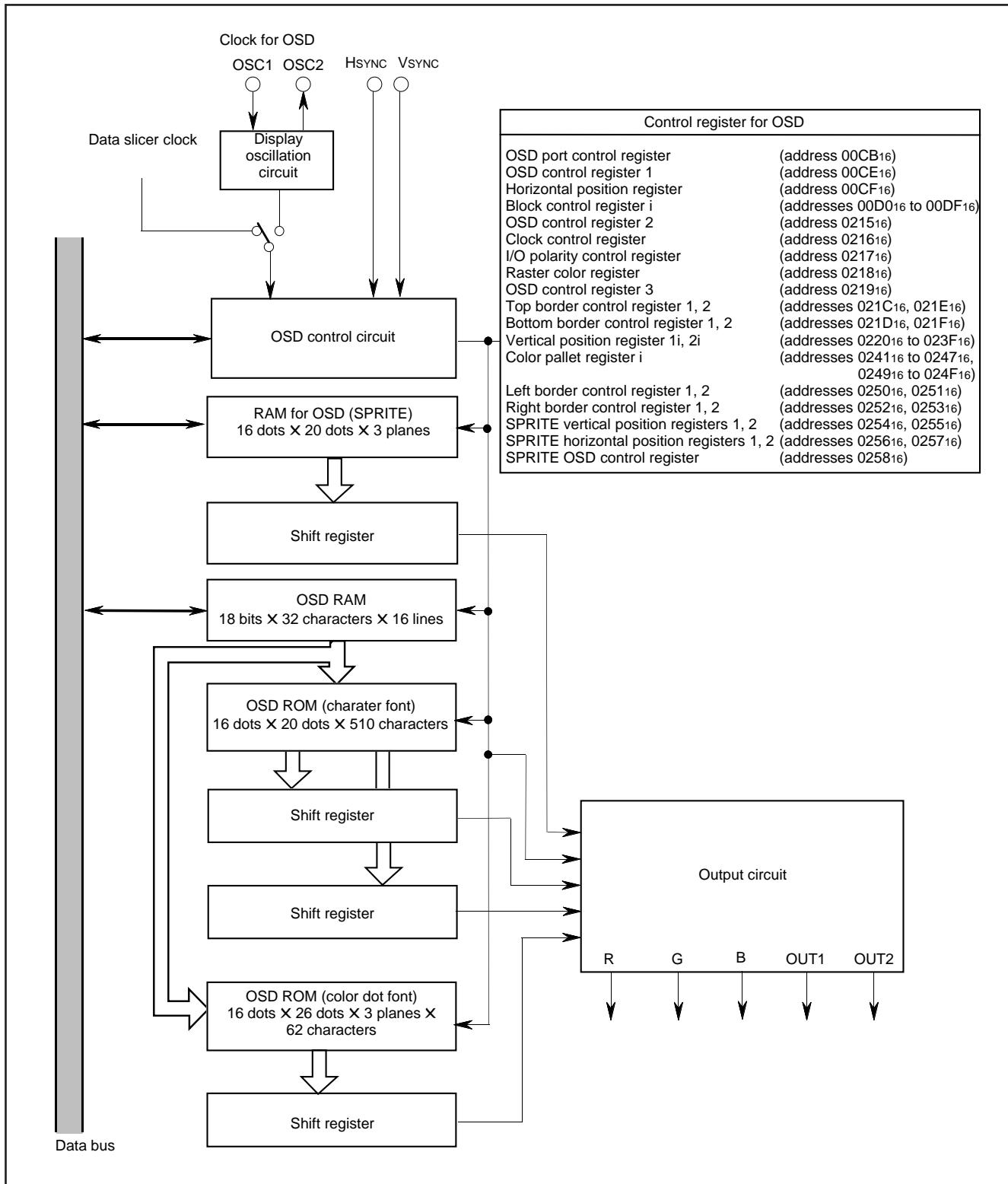


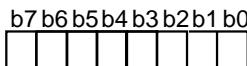
Fig. 12.11.2 Block Diagram of OSD Circuit

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OSD Control Register 1



OSD control register 1 (OC1) [Address 00CE16]

B	Name	Functions	After reset	R:W
0	OSD control bit (OC10) (See note 1)	0 : All-blocks display off 1 : All-blocks display on	0	R:W
1	Scan mode selection bit (OC11)	0 : Normal scan mode 1 : Bi-scan mode	0	R:W
2	Border type selection bit (OC12)	0 : All bordered 1 : Shadow bordered (See note 2)	0	R:W
3	Flash mode selection bit (OC13)	0 : Color signal of character background part does not flash 1 : Color signal of character background part flashes	0	R:W
4	Automatic solid space control bit (OC14)	0 : OFF 1 : ON	0	R:W
5	Vertical window/blank control bit (OC15)	0 : OFF 1 : ON	0	R:W
6, 7	Layer mixing control bits (OC16, OC17) (See note 3)	b7 b6 0 0: Logic sum (OR) of layer 1's color and layer 2's color 0 1: Layer 1's color has priority 1 0: Layer 2's color has priority 1 1: Do not set.	0	R:W

Notes 1 : Even this bit is switched during display, the display screen remains unchanged until a rising (falling) of the next VSYNC.

2 : Shadow border is output at right and bottom side of the font.

3 : OUT2 is always ORed, regardless of values of these bits.

Fig. 12.11.3 OSD Control Register 1

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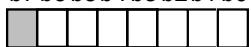
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY

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Block Control Register i

b7 b6 b5 b4 b3 b2 b1 b0



Block control register i (BCi) (i=1 to 16) [Addresses 00D016 to 00DF16]

B	Name	Functions						After reset	R	W			
0, 1	Display mode selection bits (BCi0, BCi1)	b1	b0	Functions				Indeterminate	R	W			
		0	0	Display OFF									
		0	1	OSD mode				Indeterminate	R	W			
		1	0	CC mode									
		1	1	CDOSD mode									
2	Border control bit (BCi2)	0 : Border OFF 1 : Border ON						Indeterminate	R	W			
3, 4	Dot size selection bits (BCi3, BCi4)	b6	b5	b4	b3	Pre-divide ratio	Dot size						
		0	0	0	0	X 1	1Tc X 1/2H	Indeterminate	R	W			
		0	0	1	0		1Tc X 1H						
		1	1	0	0		2Tc X 2H						
							3Tc X 3H						
		0	1	0	0	X 2	1Tc X 1/2H	Indeterminate	R	W			
		0	1	1	0		1Tc X 1H						
		1	1	0	0		2Tc X 2H						
							3Tc X 3H						
5, 6	Pre-divide ratio selection bit (BCi5, BCi6)	1	1	0	0	X 3	1.5Tc X 1/2H (See note 3)	Indeterminate	R	W			
		1	1	0	1		1.5Tc X 1H (See note 3)						
		1	1	0	0		1Tc X 1/2H						
		1	1	1	1		1Tc X 1H						
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.						2Tc X 2H	Indeterminate	R	W			
							3Tc X 3H						

Notes 1: Tc : OSD clock cycle divided in pre-divide circuit

2: H : HSYNC

3: This character size is available only in Layer 2. At this time, set layer 1's pre-divide ratio = X 2, layer 1's horizontal dot size = 1Tc.

Fig. 12.11.4 Block Control Register i (i = 1 to 16)

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Notice: This is not a final specification.
Some parametric limits are subject to change.

12.11.1 Triple Layer OSD

Three built-in layers of display screens accommodate triple display of channels, volume, etc., closed caption, and sprite displays within layers 1 to 3.

The layer to be displayed in each block is selected by bit 0 or 1 of the OSD control register 2 for each display mode (refer to Figure 12.11.7). Layer 3 always displays the sprite display.

When the layer 1 block and the layer 2 block overlay, the screen is composed (refer to Figure 12.11.5) with layer mixing by bit 6 or 7 of the OSD control register 1, as shown in Figure 12.11.3. Layer 3 always takes display priority of layers 1 and 2.

Notes 1: When mixing layer 1 and layer 2, note Table 12.11.2.

2: OUT2 is always ORed, regardless of values of bits 6, 7 of the OSD control register 1. And besides, even when OUT2 (layer 1 or layer 2) overlaps with SPRITE display (layer 3), OUT2 is output.

Table 12.11.2 Mixing Layer 1 and Layer 2

Parameter	Block	Block in Layer 1	Block in Layer 2
Display mode		CC, OSD, CDOSD mode	OSD, CDOSD mode
Pre-divide ratio		X 1, X 2 (CC mode)	Same as layer 1
Dot size		X 1 to X 3 (OSD, CDOSD mode)	
	1Tc X 1/2H, 1Tc X 1H (CC mode)	Pre-divide ratio = X 1 1Tc X 1/2H 1Tc X 1H	Pre-divide ratio = X 2 1Tc X 1/2H, 1.5Tc X 1/2H 1Tc X 1H, 1.5Tc X 1H
	1TC X 1H, 1Tc X 1/2H, 2Tc X 2H, 3Tc X 3H (OSD, CDOSD mode)	<ul style="list-style-type: none"> Same size as layer 1 1.5Tc can be selected only when: layer 1's pre-divide ratio = X 2 AND layer 1's horizontal dot size = 1Tc. As this time, vertical dot size is the same as layer 1. 	
Horizontal display start position	Arbitrary		Same position as layer 1
Vertical display start position		Arbitrary However, when dot size is 2Tc X 2H or 2Tc X 3H, set difference between vertical display position of layer 1 and that of layer 2 as follows. •2Tc X 2H: 2H Units •3Tc X 3H: 3H Units	

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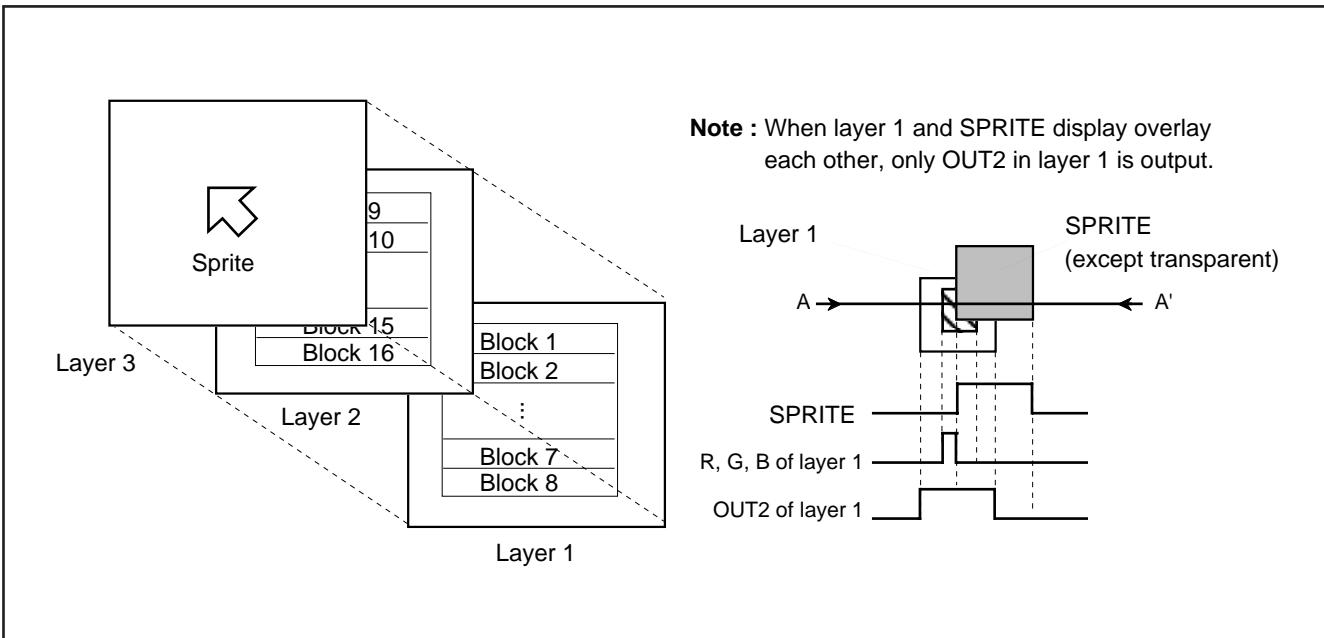


Fig. 12.11.5 Triple Layer OSD

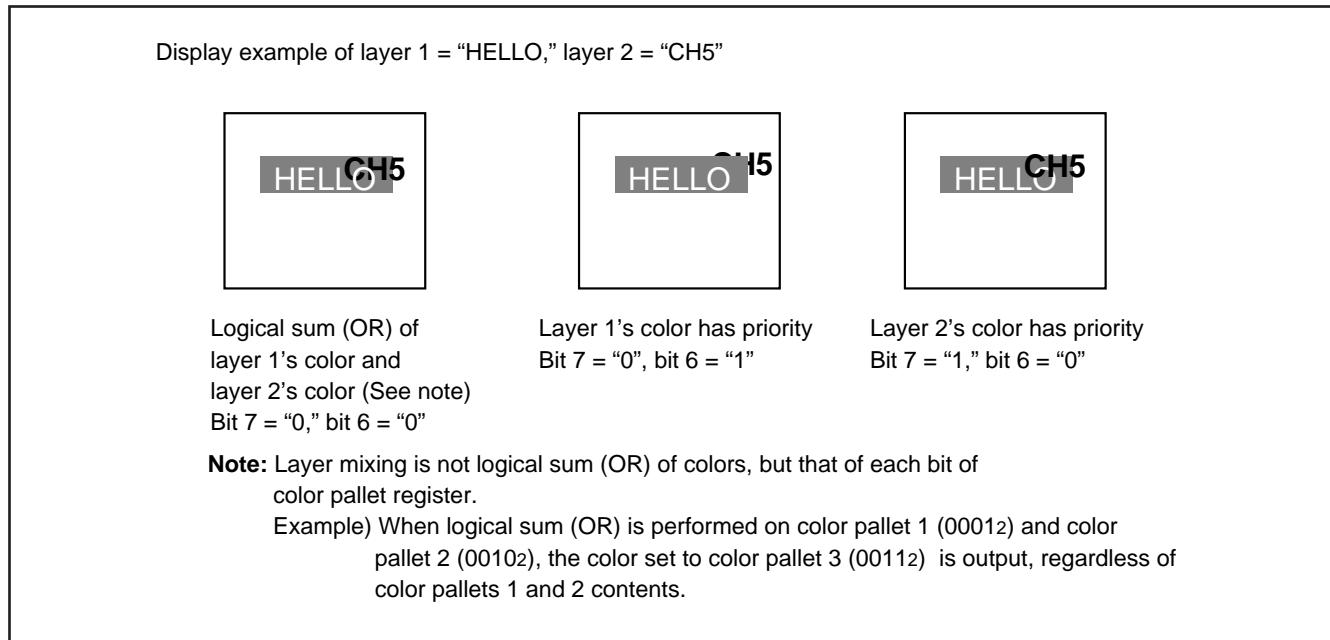


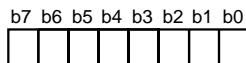
Fig. 12.11.6 Display Example of Triple Layer OSD

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PRELIMINARY
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OSD Control Register 2



OSD control register 2 (OC2) [Address 0215₁₆]

B	Name	Functions	At reset	R	W																				
0, 1	Display layer selection bits (OC20, OC21)	<table border="1"> <tr> <td>b1</td> <td>b0</td> <td>Layer 1</td> <td>Layer 2</td> </tr> <tr> <td>0</td> <td>0</td> <td>CC, OSD, CDOSD</td> <td>—</td> </tr> <tr> <td>0</td> <td>1</td> <td>CC, OSD</td> <td>CDOSD</td> </tr> <tr> <td>1</td> <td>0</td> <td>CC, CDOSD</td> <td>OSD</td> </tr> <tr> <td>1</td> <td>1</td> <td>CC</td> <td>CDOSD OSD</td> </tr> </table>	b1	b0	Layer 1	Layer 2	0	0	CC, OSD, CDOSD	—	0	1	CC, OSD	CDOSD	1	0	CC, CDOSD	OSD	1	1	CC	CDOSD OSD	0	R	W
b1	b0	Layer 1	Layer 2																						
0	0	CC, OSD, CDOSD	—																						
0	1	CC, OSD	CDOSD																						
1	0	CC, CDOSD	OSD																						
1	1	CC	CDOSD OSD																						
2	R, G, B signal output selection bit(OC22)	0: Digital output (See note) 1: Analog output (4 gradations)	0	R	W																				
3	Solid space output bit (OC23)	0: OUT1 output 1: OUT2 output	0	R	W																				
4	Horizontal window/blank control bit (OC24)	0: OFF 1: ON	0	R	W																				
5	Window/blank selection bit 1 (horizontal) (OC25)	0: Horizontal blank function 1: Horizontal window function	0	R	W																				
6	Window/blank selection bit 2 (vertical) (OC26)	0: Vertical blank function 1: Vertical window function	0	R	W																				
7	OSD interrupt request selection bit (OC27)	0: At completion of layer 1 block display 1: At completion of layer 2 block display	0	R	W																				

Note: When setting bit 1 of the OSD port control register to "1," the value which is converted from the 4-adjustment-level analog to the 2-bit digital is output regardless of this bit value as follows : the high-order bit (R1, G1 and B1) is output from pins P5₂, P5₃ and P5₄, and the low-order bit is (R0, G0 and B0) output from pins P1₇, P1₅ and P1₆. And besides, when not using OSD function, the low-power dissipation can realize by setting this bit to "0."

Fig. 12.11.7 OSD Control Register 2

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12.11.2 Display Position

The display positions of characters are specified by a block. There are 16 blocks, blocks 1 to 16. Up to 32 characters can be displayed in each block (refer to "12.11.6 Memory for OSD").

The display position of each block can be set in both horizontal and vertical directions by software.

The display position in the horizontal direction can be selected for all blocks in common from 256-step display positions in units of 4 Tosc (Tosc = OSD oscillation cycle).

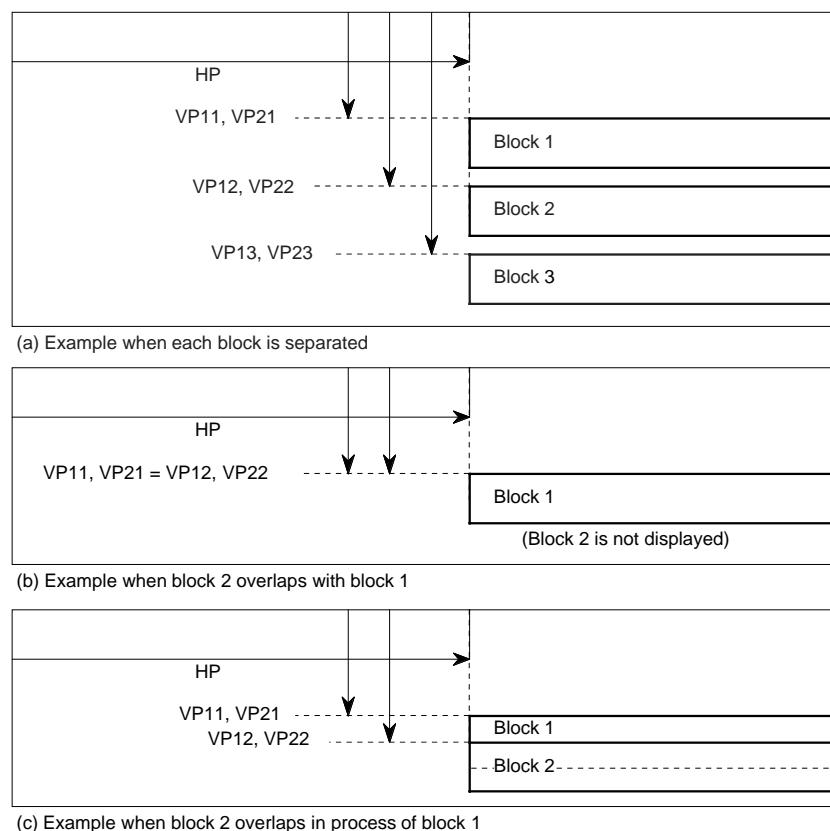
The display position in the vertical direction for each block can be selected from 1024-step display positions in units of 1 TH (TH = HSYNC cycle).

Blocks are displayed in conformance with the following rules:

- When the display position is overlapped with another block (Figure 12.11.8 (b)), a lower block number (1 to 16) is displayed on the front.
- When another block display position appears while one block is displayed (Figure 12.11.8 (c)), the block with a larger set value as the vertical display start position is displayed. However, do not display block with the dot size of 2TC X 2H or 3TC X 3H during display period (*) of another block.

* In the case of OSD mode block: 20 dots in vertical from the vertical display start position.

* In the case of CC or CDOSD mode block: 26 dots in vertical from the vertical display start position.



Note: VP_i or VP2_i (i : 1 to 16) indicates the vertical display start position of display block i.

Fig. 12.11.8 Display Position

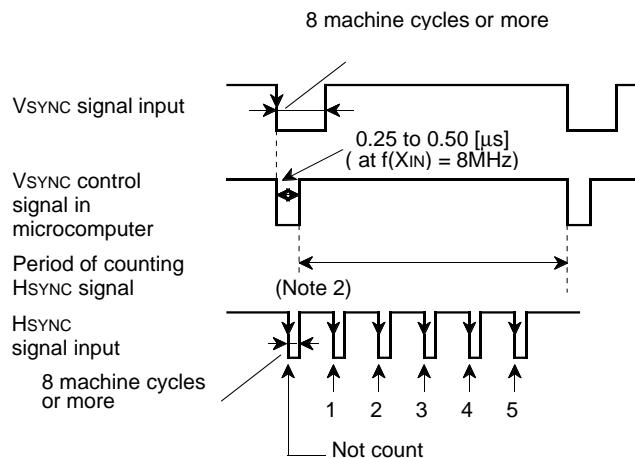
PRELIMINARY

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The display position in the vertical direction is determined by counting the horizontal sync signal (H_{SYNC}). At this time, when V_{SYNC} and H_{SYNC} are positive polarity (negative polarity), it starts to count the rising edge (falling edge) of H_{SYNC} signal from after fixed cycle of rising edge (falling edge) of V_{SYNC} signal. So interval from rising edge (falling edge) of V_{SYNC} signal to rising edge (falling edge) of H_{SYNC} signal needs enough time (2 machine cycles or more) for avoiding jitter. The polarity of H_{SYNC} and V_{SYNC} signals can select with the I/O polarity control register (address 021716).



When bits 0 and 1 of the I/O polarity control register (address 021716) are set to "1" (negative polarity)

Notes 1 : The vertical position is determined by counting falling edge of H_{SYNC} signal after rising edge of V_{SYNC} control signal in the microcomputer.

2 : Do not generate falling edge of H_{SYNC} signal near rising edge of V_{SYNC} control signal in microcomputer to avoid jitter.

3 : The pulse width of V_{SYNC} and H_{SYNC} needs 8 machine cycles or more.

Fig. 12.11.9 Supplement Explanation for Display Position

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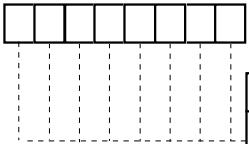
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The vertical position for each block can be set in 1024 steps (where each step is 1TH (TH: HSYNC cycle)) as values "0016" to "FF16" in vertical position register 1i (i = 1 to 16) (addresses 022016 to 022F16) and values "0016" to "0316" in vertical position register 2i (i = 1 to 16) (addresses 023016 to 023F16). The vertical position registers are shown in Figures 12.11.10 and 12.11.11.

Vertical Position Register 1i

b7 b6 b5 b4 b3 b2 b1 b0



Vertical position register 1i (VP1i) (i = 1 to 16) [Addresses 022016 to 022F16]

B	Name	Functions	After reset	R:W
0 to 7	Control bits of vertical display start positions (VP1i0 to VP1i7) (See note 1)	Vertical display start positions (low-order 8 bits) TH \times (setting value of low-order 2 bits of VP2i $\times 16^2$ + setting value of low-order 4 bits of VP1i $\times 16^1$ + setting value of low-order 4 bits of VP1i $\times 16^0$)	Indeterminate	R:W

Notes 1: Do not "0016" and "0116" to VP1i at VP2i = "0016."

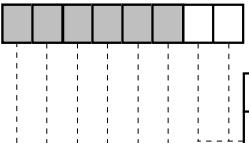
2: TH is cycle of HSYNC.

3: VP2i is vertical position register 2i.

Fig. 12.11.10 Vertical Position Register 1i (i = 1 to 16)

Vertical Position Register 2i

b7 b6 b5 b4 b3 b2 b1 b0



Vertical position register 2i (VP2i) (i = 1 to 16) [Addresses 023016 to 023F16]

B	Name	Functions	After reset	R:W
0, 1	Control bits of vertical display start positions (VP2i0, VP2i1) (See note 1)	Vertical display start positions (high-order 2 bits) TH \times (setting value of low-order 2 bits of VP2i $\times 16^2$ + setting value of low-order 4 bits of VP1i $\times 16^1$ + setting value of low-order 4 bits of VP1i $\times 16^0$)	Indeterminate	R:W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R:-

Notes 1: Do not set "0016" and "0116" to VP1i at VP2i = "0016."

2: TH is cycle of HSYNC.

3: VP1i is vertical position register 1i.

Fig. 12.11.11 Vertical Position Register 2i (i = 1 to 16)

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

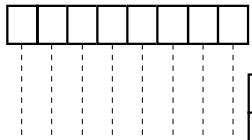
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The horizontal position is common to all blocks, and can be set in 256 steps (where 1 step is 4Tosc, Tosc being the oscillating cycle for display) as values "0016" to "FF16" in bits 0 to 7 of the horizontal position register (address 00CF16). The horizontal position register is shown in Figure 12.11.12.

Horizontal Position Register

b7 b6 b5 b4 b3 b2 b1 b0



Horizontal position register (HP) [Address 00CF16]

B	Name	Functions	After reset	R:W
0 to 7	Control bits of horizontal display start positions (HP0 to HP7)	Horizontal display start positions 4Tosc \times (setting value of high-order 4 bits \times 16 ¹ +setting value of low-order 4 bits \times 16 ⁰)	0	R:W

Notes

1. The setting value synchronizes with the VSYNC.
2. Tosc = OSD oscillation period.

Fig. 12.11.12 Horizontal Position Register

Note : 1Tc (Tc : OSD clock cycle divided in pre-divide circuit) gap occurs between the horizontal display start position set by the horizontal position register and the most left dot of the 1st block. Accordingly, when 2 blocks have different pre-divide ratios, their horizontal display start position will not match.

Ordinaly, this gap is 1Tc regardless of character sizes, however, the gap is 1.5Tc only when the character size is 1.5Tc.

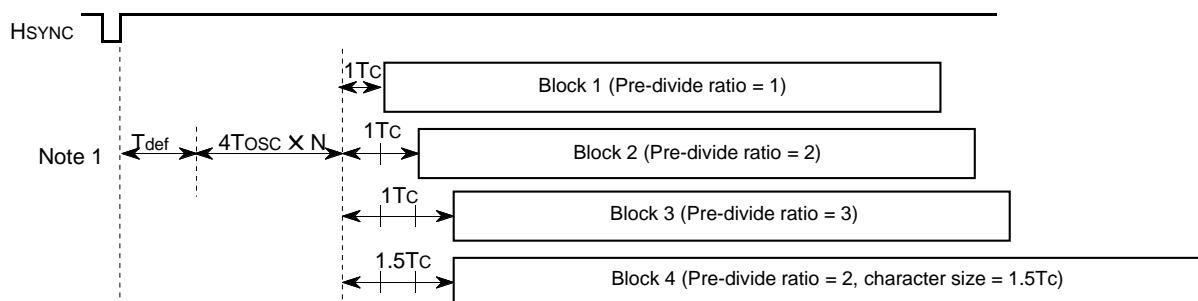


Fig. 12.11.13 Notes on Horizontal Display Start Position

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PRELIMINARY

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12.11.3 Dot Size

The dot size can be selected by a block unit. The dot size in vertical direction is determined by dividing HSYNC in the vertical dot size control circuit. The dot size in horizontal is determined by dividing the following clock in the horizontal dot size control circuit : the clock gained by dividing the OSD clock source (data slicer clock, OSC1, main clock) in the pre-divide circuit. The clock cycle divided in the pre-divide circuit is defined as 1Tc.

The dot size is specified by bits 6 to 3 of the block control register.

Refer to Figure 12.11.4 (the block control register i), refer to Figure 12.11.6 (the clock control register).

The block diagram of dot size control circuit is shown in Figure 12.11.4.

Notes 1: The pre-divide ratio = 3 cannot be used in the CC mode.

2: The pre-divide ratio of the layer 2 must be same as that of the layer 1 by the block control register i.

3: In the bi-scan mode, the dot size in the vertical direction is 2 times as compared with the normal mode. Refer to "12.11.13 Scan Mode" about the scan mode.

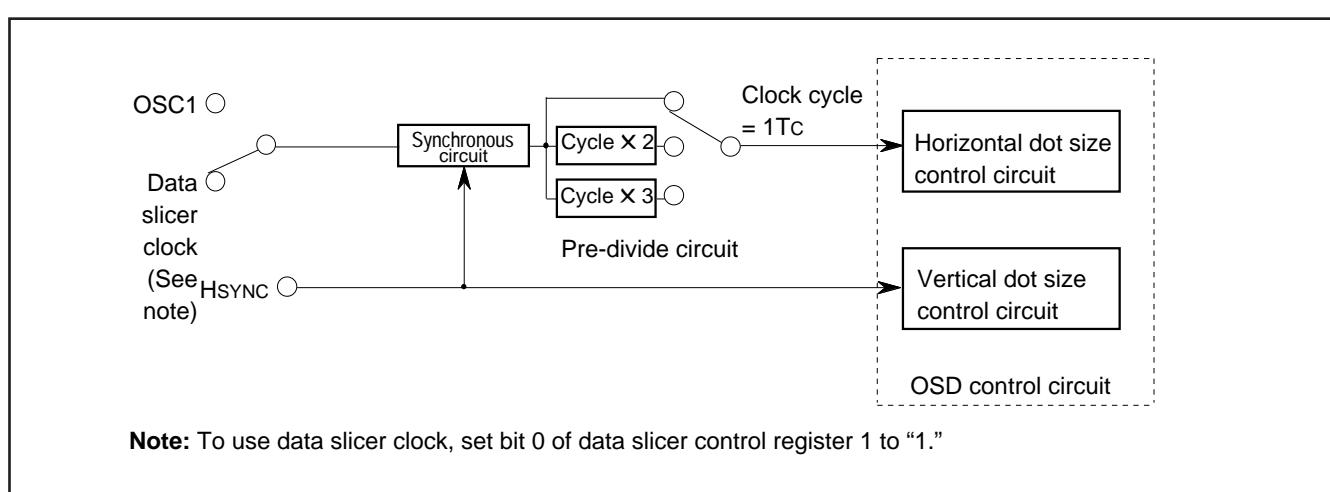


Fig. 12.11.14 Block Diagram of Dot Size Control Circuit

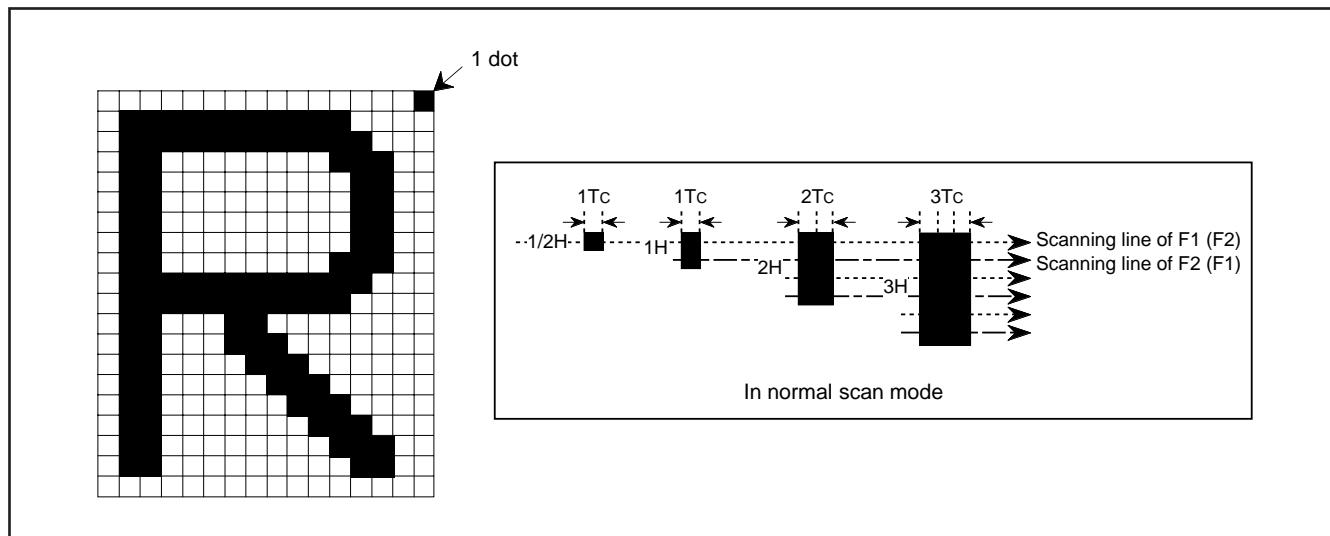


Fig. 12.11.15 Definition of Dot Sizes

PRELIMINARY

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12.11.4 Clock for OSD

As a clock for display to be used for OSD, it is possible to select one of the following 3 types.

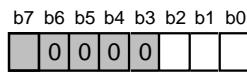
- Data slicer clock output from the data slicer (approximately 26 MHz)
- Clock from the LC oscillator supplied from the pins OSC1 and OSC2
- Clock from the ceramic resonator or the quartz-crystal oscillator from the pins OSC1 and OSC2

The clock for display to be used for OSD can be selected by bit 7 of port P3 direction register, bit 2 and bit 1 of clock source control register (address 021616). If the pins OSC1 and OSC2 are not used as OSD clock input/output, these pins can be used as the sub-clock input/output, or port P6.

Table 12.11.2 Setting of P63/OSC1/XCIN, P64/OSC2/XCOUT

Registers	Function	Clock input/ output pins for OSD		Sub-clock input/ output pins	Input port
Bit 7 of Port P3 Direction Register				0	0
Clock Control Register	Bit 2	1	1	0	0
	Bit 1	0	1	0	1

Clock Control Register



Clock control register (CS) [Address 021616]

B	Name	Functions	After reset	R	W
0	Clock selection bit (CS0)	0: Data slicer clock 1: OSC1 clock	0	R	W
1, 2	OSC1 oscillating mode selection bits (CS1, CS2)	b2 b1 0 0: 32kHz oscillating mode. 0 1: Used as input port of P63 and P64 (See note 1). 1 0: LC oscillating mode 1 1: Ceramic • quartz-crystal oscillating mode	0	R	W
3 to 6	Fix these bits to "0."		0	R	W
7	Test bit (See note 2)		0	R	W

Note 1: Set bit 7 of address 00C7₁₆ to "1", when OSC1 and OSC2 are used as P63 and P64.

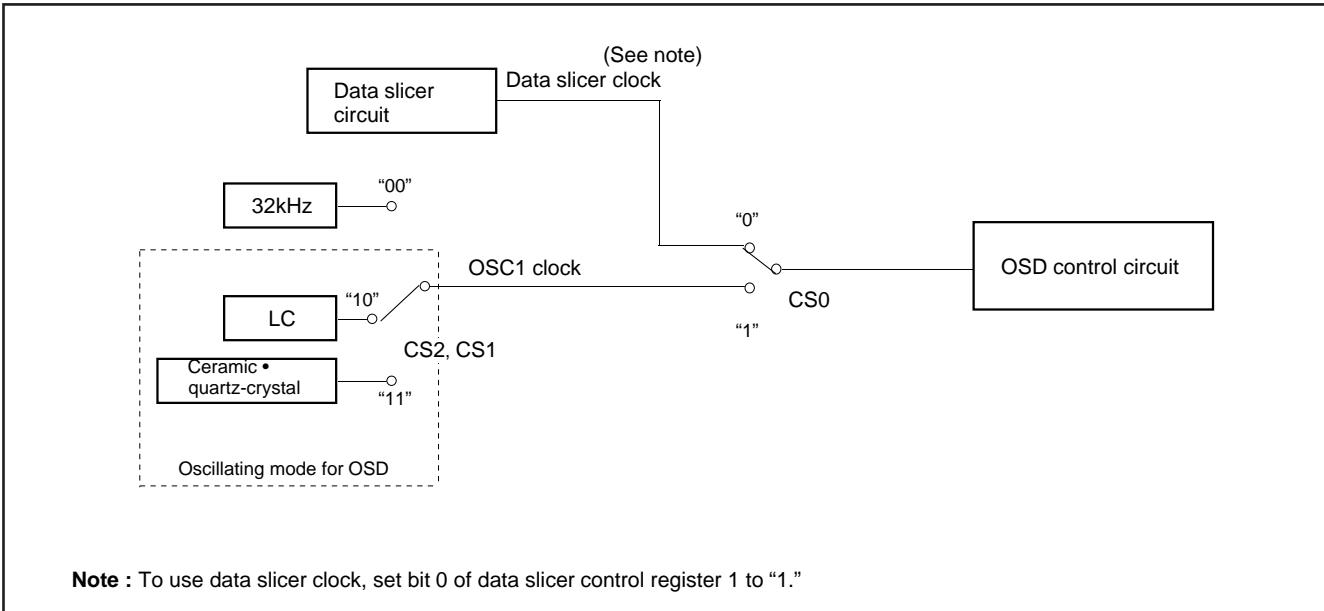
2: Be sure to set bit 7 to "0" for program of the mask and the EPROM versions. For the emulator MCU version (M37280ERSS), be sure to set bit 7 to "1" when using the data slicer clock for software debugging.

Fig. 12.11.16 Clock Control Register

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Note : To use data slicer clock, set bit 0 of data slicer control register 1 to "1."

Fig. 12.11.17 Block Diagram of OSD Selection Circuit

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PRELIMINARY

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12.11.5 Field Determination Display

To display the block with vertical dot size of 1/2H, whether an even field or an odd field is determined through differences in a synchronizing signal waveform of interlacing system. The dot line 0 or 1 (refer to Figure 12.11.19) corresponding to the field is displayed alternately.

In the following, the field determination standard for the case where both the horizontal sync signal and the vertical sync signal are negative-polarity inputs will be explained. A field determination is determined by detecting the time from a falling edge of the horizontal sync signal until a falling edge of the VSYNC control signal (refer to Figure

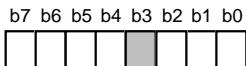
12.11.19) in the microcomputer and then comparing this time with the time of the previous field. When the time is longer than the comparing time, it is regarded as even field. When the time is shorter, it is regarded as odd field.

The field determination flag changes at a rising edge of VSYNC control signal in the microcomputer.

The contents of this field can be read out by the field determination flag (bit 7 of the I/O polarity control register at address 021716). A dot line is specified by bit 6 of the I/O polarity control register (refer to Figure 12.11.19).

However, the field determination flag read out from the CPU is fixed to "0" at even field or "1" at odd field, regardless of bit 6.

I/O Polarity Control Register



I/O polarity control register (PC) [Address 021716]

B	Name	Functions	After reset	R : W
0	Hsync input polarity switch bit (PC0)	0 : Positive polarity input 1 : Negative polarity input	0	R : W
1	Vsync input polarity switch bit (PC1)	0 : Positive polarity input 1 : Negative polarity input	0	R : W
2	R, G, B output polarity switch bit (PC2)	0 : Positive polarity output 1 : Negative polarity output	0	R : W
3	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0".		0	R : —
4	OUT1 output polarity switch bit (PC4)	0 : Positive polarity output 1 : Negative polarity output	0	R : W
5	OUT2 output polarity switch bit (PC5)	0 : Positive polarity output 1 : Negative polarity output	0	R : W
6	Display dot line selection bit (PC6) (See note)	0 : "█" at even field "█" at odd field 1 : "█" at even field "█" at odd field	0	R : W
7	Field determination flag (PC7)	0 : Even field 1 : Odd field	1	R : —

Note: Refer to Fig. 12.11.19.

Fig. 12.11.18 I/O Polarity Control Register

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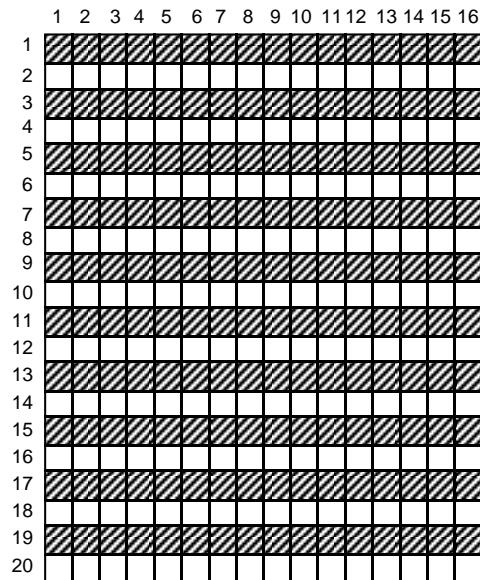
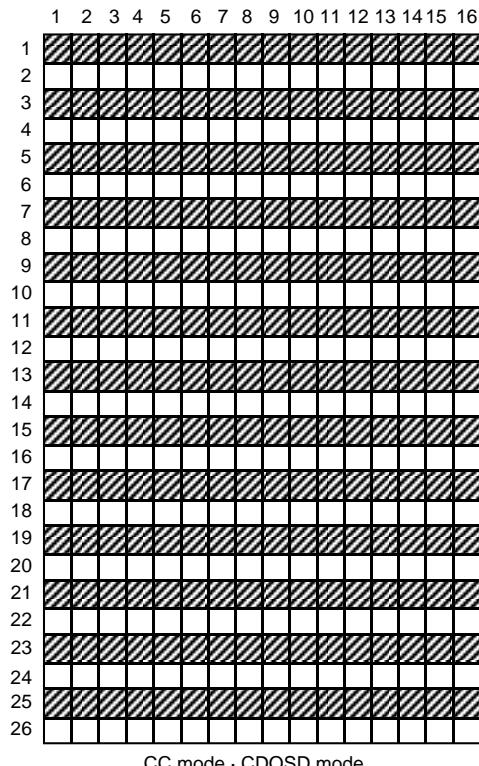
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Both HSYNC signal and VSYNC signal are negative-polarity input

HSYNC		Field	Field determination flag(Note)	Display dot line selection bit	Display dot line
VSYNC and VSYNC control signal in microcomputer	(n-1) field (Odd-numbered) 	Odd			
Upper : VSYNC signal	(n) field (Even-numbered) 	Even	0 (T2 > T1)	0	Dot line 1
Lower : VSYNC control signal in microcomputer	(n+1) field (Odd-numbered) 	Odd	1 (T3 < T2)	1	Dot line 0
				0	Dot line 0
				1	Dot line 1

When using the field determination flag, be sure to set bit 0 of the PWM mode register 1 (address 020A16) to "0."



When the display dot line selection bit is "0," the "□" font is displayed at even field, the "▨" font is displayed at odd field. Bit 7 of the I/O polarity control register can be read as the field determination flag : "1" is read at odd field, "0" is read at even field.

OSD ROM font configuration diagram

Note : The field determination flag changes at a rising edge of the VSYNC control signal (negative-polarity input) in the microcomputer.

Fig. 12.11.19 Relation Between Field Determination Flag and Display Font

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12.11.6 Memory for OSD

There are 2 types of memory for OSD : OSD ROM (addresses 1080016 to 157FF16 and 1800016 to 1ACFF16) used to specify character dot data and OSD RAM (addresses 070016 to 07A716 and 080016 to 0FDF16) used to specify the kinds of display characters, display colors, and SPRITE display. The following describes each type of memory.

(1) OSD ROM (addresses 1080016 to 157FF16, 1800016 to 1ACFF16)

The dot pattern data for OSD characters is stored in the character font area in the OSD ROM and the CD font data for OSD characters is stored in the color dot font area in the OSD ROM. To specify the kinds of the character font and the CD font, it is necessary to write the character code into the OSD RAM.

The modes are selected by bit 3 of the OSD control register 3 for each screen.

The character font data storing address is shown in Figure 12.11.20. The CD font data storing address is shown in Figure 2.11.21. The 510 kinds of character font and 62 kinds of CD font can be stored.

OSD ROM address of character font data

OSD ROM address bit	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Line number / Character code / Area bit	1	0	Line number				Character code								Area bit		

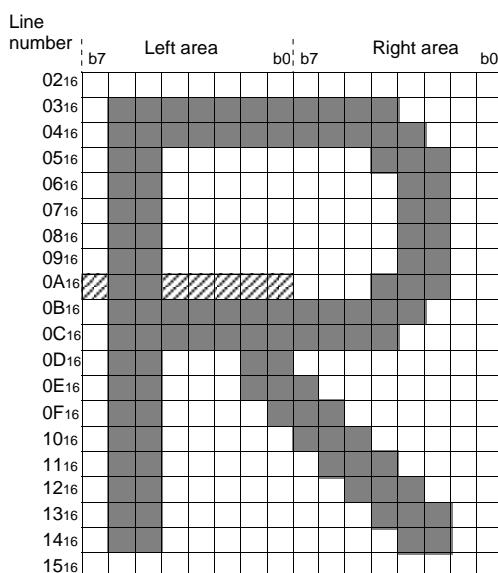
Line number = "02₁₆" to "15₁₆"

Character code = "00₁₆" to "1FF₁₆" ("0FF₁₆" and "100₁₆" can not be used. Write "FF₁₆" to corresponding addresses.)

Area bit = 0: Left area

1: Right area

For example : The font data of the hatching area of the character code AA₁₆ is 1|0010|1001|0101|0100₂ = 12954₁₆



Character code AA₁₆

Fig. 12.11.20 Character Font Data Storing Address

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OSD ROM address of CD font data

OSD ROM address bit	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Line number/CD code/Area bit	1	1	0	Plain selection bit	Line number				CD code				Area bit				

Line number = "0016" to "1916"

CD code = "0016" to "3F16" ("1F16" and "2016" cannot be used. Write "FF16" to the corresponding address.)

Area bit = 0 : Left area 1 : Right area

Example) "0316" is stored to address 1A77516 (Plain 2), "C016" is stored to address 1977516 (Plain 1), and "F816" is stored to address 1877516 (Plain 0) as the font data of the hatching area of the CD code 3A16.

Plain 2
(Color pallet selection bit 2)

Plain 1
(Color pallet selection bit 1)

Plain 0
(Color pallet selection bit 0)

Line number	b7	Left area	b0	b7	Right area	b0
0016	4	4 4 4 4 4 4 4	4	4 4 4 4 4 4 4	4 4 4 4 4 4 4	4
0116	4	4 4 4 4 4 4 4	4	4 4 4 4 4 4 4	4 4 4 4 4 4 4	4
0216	4	4 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 4 4
0316	4	4 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 4 4
0416	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
0516	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
0616	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
0716	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
0816	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
0916	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
0A16	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
0B16	4	4 0 2 2 2 3	3	3 3 3 2 2 2	0 4 4	4
0C16	4	4 0 2 2 2 3	3	3 3 3 2 2 2	0 4 4	4
0D16	4	4 0 2 2 2 3	3	3 3 3 2 2 2	0 4 4	4
0E16	4	4 0 2 2 2 3	3	3 3 3 2 2 2	0 4 4	4
0F16	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
1016	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
1116	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
1216	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
1316	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
1416	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
1516	4	4 0 0 0 0 1 1	1	1 1 1 0 0 0 0	0 0 4 4	4
1616	4	4 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0 0 4 4	4
1716	4	4 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0 0 4 4	4
1816	4	4 4 4 4 4 4 4	4	4 4 4 4 4 4 4	4 4 4 4 4 4	4
1916	4	4 4 4 4 4 4 4	4	4 4 4 4 4 4 4	4 4 4 4 4	4

CD code 3A16

When bit 3 of OSD control register 3 is “0 (1)”

- Color pallet set by RC13 to RC16 of OSD RAM is selected
- Color pallet 1 (9) is selected
- Color pallet 2 (10) is selected
- Color pallet 3 (11) is selected
- Color pallet 4 (12) is selected

Line number	b7	Left area	b0	b7	Right area	b0
00 ₁₆						
01 ₁₆						
02 ₁₆						
03 ₁₆						
04 ₁₆						
05 ₁₆						
06 ₁₆						
07 ₁₆						
08 ₁₆						
09 ₁₆						
0A ₁₆						
0B ₁₆						
0C ₁₆						
0D ₁₆						
0E ₁₆						
0F ₁₆						
10 ₁₆						
11 ₁₆						
12 ₁₆						
13 ₁₆						
14 ₁₆						
15 ₁₆						
16 ₁₆						
17 ₁₆						
18 ₁₆						
19 ₁₆						

Display example

Fig. 12.11.21 Color Dot Font Data Storing Address

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(2) OSD RAM (addresses 070016 to 07A716, 080016 to 0FFF16)

The OSD RAM for SPRITE consisting of 3 planes, is assigned to addresses 070016 to 07A716. Each plane corresponds to each color pallet selection bit and the color pallet of each dot is determined from among 8 kinds.

The OSD RAM for character is allocated at addresses 080016 to 0FFF16, and is divided into a display character code specification part, color code 1 specification part, and color code 2 specification part for each block. Tables 2.11.4 and 2.11.5 show the contents of the OSD RAM.

For example, to display 1 character position (the left edge) in block 1, write the character code in address 080016, write color code 1 at 082016, and write color code 2 at 084016. The structure of the OSD RAM is shown in Figure 12.11.23.

Note : For the layer 2's OSD mode block with dot size of 1.5Tc X 1/2H and 1.5Tc X 1H, the 3nth (n = 1 to 10) character is skipped as compared with ordinary block (blocks with dot size of 1Tc X 1/2H, or blocks on the layer 1). Accordingly, maximum 22 characters are only displayed in 1 block. Blocks with dot size of 1Tc X 1/2H and 1Tc X 1H, or blocks on the layer 1

However, note the following:

- In OSD mode

The character is not displayed, and only the left 1/3 part of the 22nd character back ground is displayed in the 22nd's character area.

When not displaying this background, set transparent for background.

- In CDOSD mode

The character is not displayed, and color pallet color specified by bit 3 to 6 of color code 1 can be output in the 22nd's character area (left 1/3 part).

The RAM data for the 3nth character does not effect the display.

Any character data can be stored here (refer to Figure 12.11.22).

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Table 12.11.3 Contents of OSD RAM (SPRITE)

Line (from top)	Dot (from left)	Plain 0 (Color pallet selection bit 0)	Plain 1 (Color pallet selection bit 1)	Plain 2 (Color pallet selection bit 2)
Line 1	Dots 1 to 8 Dots 9 to 16	070016 070116	074016 074116	078016 078116
Line 2	Dots 1 to 8 Dots 9 to 16	070216 070316	074216 074316	078216 078316
:	:	:	:	:
Line 19	Dots 1 to 8 Dots 9 to 16	072416 072516	076416 076516	07A416 07A516
Line 20	Dots 1 to 8 Dots 9 to 16	072616 072716	076616 076716	07A616 07A716

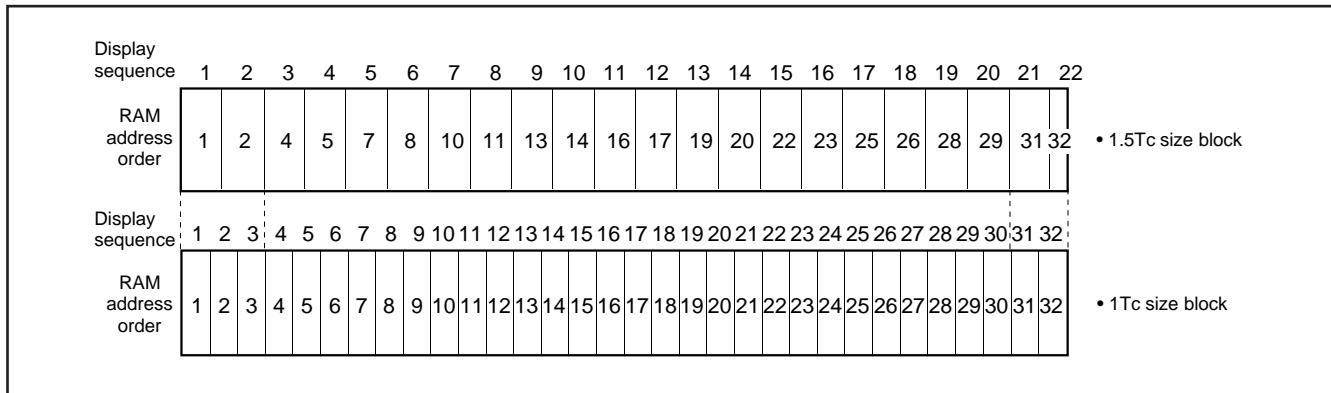
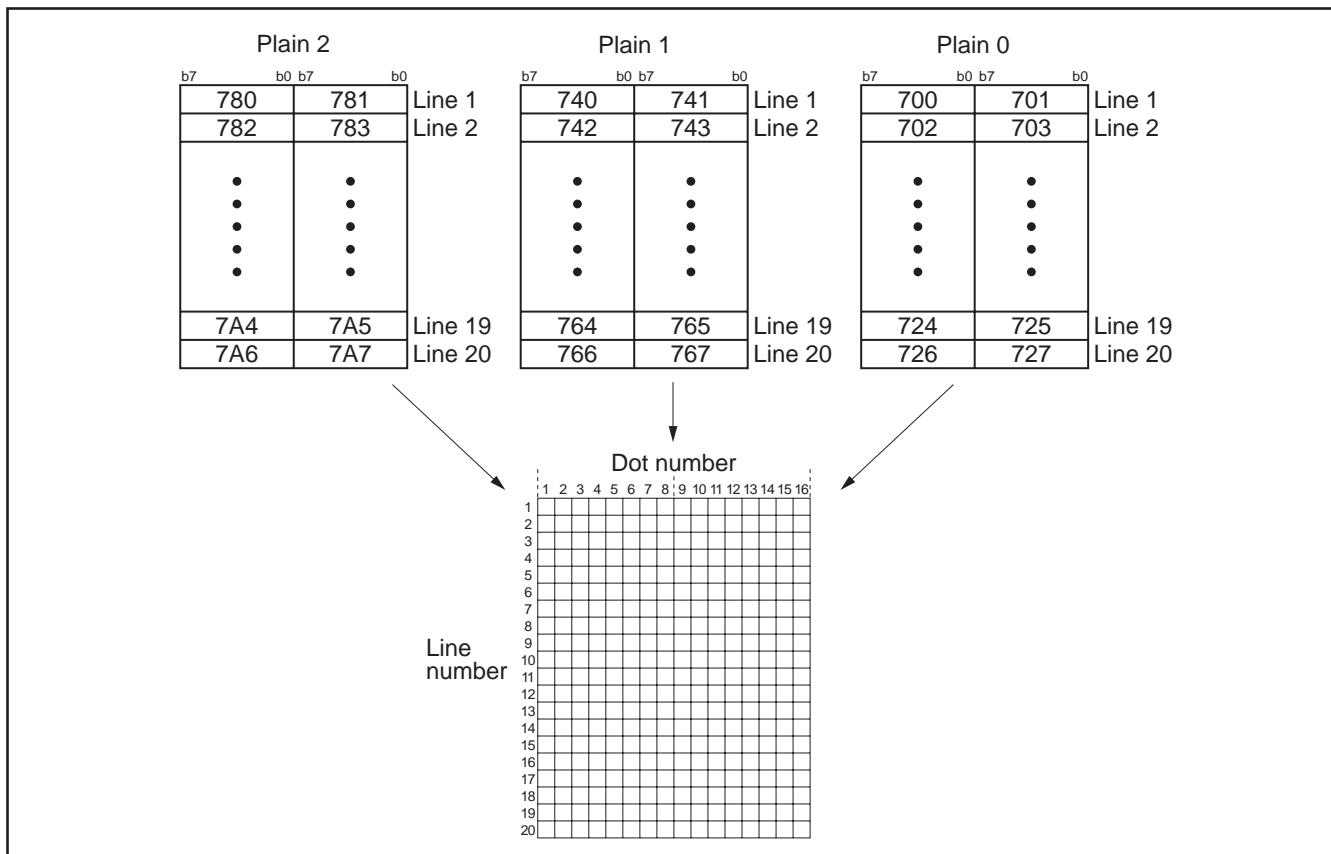


Fig. 12.11.22 RAM Data for 3nth Character

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PRELIMINARY
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Table 12.11.14 Contents of OSD RAM (Character)

Block	Display Position (from left)	Character Code Specification	Color Code 1 Specification	Color Code 2 Specification
Block 1	1st character	080016	082016	084016
	2nd character	080116	082116	084116
	:	:	:	:
	31st character	081E16	083E16	085E16
Block 2	32nd character	081F16	083F16	085F16
	1st character	088016	08A016	08C016
	2nd character	088116	08A116	08C116
	:	:	:	:
Block 3	31st character	089E16	08BE16	08DE16
	32nd character	089F16	08BF16	08DF16
	1st character	090016	092016	094016
	2nd character	090116	092116	094116
Block 4	:	:	:	:
	31st character	091E16	093E16	095E16
	32nd character	091F16	093F16	095F16
	1st character	098016	09A016	09C016
Block 5	2nd character	098116	09A116	09C116
	:	:	:	:
	31st character	099E16	09BE16	09DE16
	32nd character	099F16	09BF16	09DF16
Block 6	1st character	0A0016	0A2016	0A4016
	2nd character	0A0116	0A2116	0A4116
	:	:	:	:
	31st character	0A1E16	0A3E16	0A5E16
Block 7	32nd character	0A1F16	0A3F16	0A5F16
	1st character	0A8016	0AA016	0AC016
	2nd character	0A8116	0AA116	0AC116
	:	:	:	:
Block 8	31st character	0A9E16	0ABE16	0ADE16
	32nd character	0A9F16	0ABF16	0ADF16
	1st character	0B0016	0B2016	0B4016
	2nd character	0B0116	0B2116	0B4116
Block 9	:	:	:	:
	31st character	0B1E16	0B3E16	0B5E16
	32nd character	0B1F16	0B3F16	0B5F16
	1st character	0B8016	0BA016	0BC016
Block 10	2nd character	0B8116	0BA116	0BC116
	:	:	:	:
	31st character	0B9E16	0BBE16	0BDE16
	32nd character	0B9F16	0BBF16	0BDF16
	1st character	0C0016	0C2016	0C4016
	2nd character	0C0116	0C2116	0C4116
	:	:	:	:
	31st character	0C1E16	0C3E16	0C5E16
	32nd character	0C1F16	0C3F16	0C5F16
	1st character	0C8016	0CA016	0CC016
	2nd character	0C8116	0CA116	0CC116
	:	:	:	:
	31st character	0C9E16	0CBE16	0CDE16
	32nd character	0C9F16	0CBF16	0CDF16

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Table 12.11.15 Contents of OSD RAM (continued)

Block	Display Position (from left)	Character Code Specification	Color Code 1 Specification	Color Code 2 Specification
Block 11	1st character	0D0016	0D2016	0D4016
	2nd character	0D0116	0D2116	0D4116
	:	:	:	:
	31st character	0D1E16	0D3E16	0D5E16
Block 12	32nd character	0D1F16	0D3F16	0D5F16
	1st character	0D8016	0DA016	0DC016
	2nd character	0D8116	0DA116	0DC116
	:	:	:	:
Block 13	31st character	0D9E16	0DBE16	0DDE16
	32nd character	0D9F16	0DBF16	0DDF16
	1st character	0E0016	0E2016	0E4016
	2nd character	0E0116	0E2116	0E4116
Block 14	:	:	:	:
	31st character	0E1E16	0E3E16	0E5E16
	32nd character	0E1F16	0E3F16	0E5F16
	1st character	0E8016	0EA016	0EC016
Block 15	2nd character	0E8116	0EA116	0EC116
	:	:	:	:
	31st character	0E9E16	0EBE16	0EDE16
	32nd character	0E9F16	0EBF16	0EDF16
Block 16	1st character	0F0016	0F2016	0F4016
	2nd character	0F0116	0F2116	0F4116
	:	:	:	:
	31st character	0F1E16	0F3E16	0F5E16
	32nd character	0F1F16	0F3F16	0F5F16
	1st character	0F8016	0FA016	0FC016
	2nd character	0F8116	0FA116	0FC116
	:	:	:	:
	31st character	0F9E16	0FBE16	0FDE16
	32nd character	0F9F16	0FBF16	0FDF16

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Note: Do not read from/write to the addresses in Table 12.11.6.

Table 12.11.6 List of Access Disable Addresses

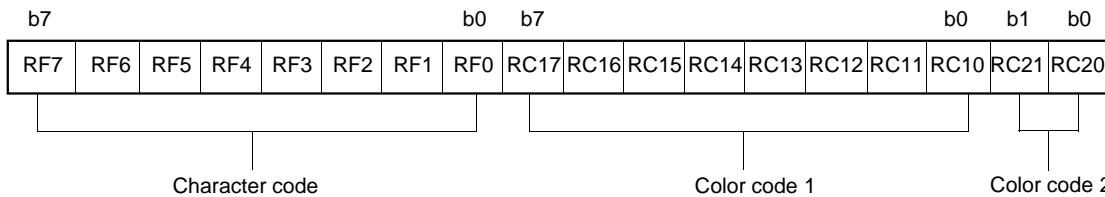
0860 ₁₆ to 087F ₁₆	0C60 ₁₆ to 0C7F ₁₆
08E0 ₁₆ to 08FF ₁₆	0CE0 ₁₆ to 0CFF ₁₆
0960 ₁₆ to 097F ₁₆	0D60 ₁₆ to 0D7F ₁₆
09E0 ₁₆ to 09FF ₁₆	0DE0 ₁₆ to 0DFF ₁₆
0A60 ₁₆ to 0A7F ₁₆	0E60 ₁₆ to 0E7F ₁₆
0AE0 ₁₆ to 0AFF ₁₆	0EE0 ₁₆ to 0EFF ₁₆
0B60 ₁₆ to 0B7F ₁₆	0F60 ₁₆ to 0F7F ₁₆
0BE0 ₁₆ to 0BFF ₁₆	0FE0 ₁₆ to 0FFF ₁₆

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Blocks 1 to 16



Bit	CC mode		OSD mode		CDOSD mode	
	Bit name	Function	Bit name	Function	Bit name	Function
RF0	Character code (Low-order 8 bits)	Specify character code in OSD ROM (See note 3)	Character code (Low-order 8 bits)	Specify character code in OSD ROM (See note 3)	CD code (6 bits)	Specify character code in OSD ROM (color dot) (See note 4)
RF1						
RF2						
RF3						
RF4						
RF5						
RF6						
RF7						
RC10	Character code (High-order 1 bits)		Character code (High-order 1 bits)		Not used	
RC11	Character	Color pallet selection bit 0	Character	Color pallet selection bit	Dot color	Specify a dot which selects color pallet 0 or 8 by OSD ROM (See note 6)
RC12		Color pallet selection bit 1		Color pallet selection bit		
RC13		Color pallet selection bit 2		Color pallet selection bit		
RC14	Italic control	0: Italic OFF 1: Italic ON	Character background	Color pallet selection bit 3		
RC15	Flash control	0: Flash OFF 1: Flash ON		Color pallet selection bit 0		
RC16	Underline control	0: Underline OFF 1: Underline ON		Color pallet selection bit 1		
RC17	OUT2 output control	0: OUT2 output OFF 1: OUT2 output ON	OUT2 output control	0: OUT2 output OFF 1: OUT2 output ON	OUT2 output control	0: OUT2 output OFF 1: OUT2 output ON
RC20	Character background	Color pallet selection bit 0	Character background	Color pallet selection bit 2	Not used	
RC21		Color pallet selection bit 1		Color pallet selection bit 3		

Notes 1: Read value of bits 2 to 7 of the color code 2 is undefined.

2: For "not used" bits, the write value is read.

3: Do not use character code "0FF16," "10016."

4: Do not use character code "1F16," "2016."

5: Refer to Figure 12.11.24.

6: Only CDOSD mode, a dot which selects color pallet 0 or 8 is colored to the color pallet set by RC13 to RC16 of OSD RAM in character units.

Fig. 12.11.23 Structure of OSD RAM

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12.11.7 Character Color

As shown in Figure 2.11.24, there are 16 built-in color pallets. Color pallet 0 is fixed at transparent, and color pallet 8 is fixed at black.

The remaining 14 colors can be set to any of the 64 colors available.

The setting procedure for character colors is as follows:

- CC mode 8 kinds

Color pallet selection range (color pallets 0 to 7 or 8 to 15) can be selected by bit 0 of the OSD control register 3 (address 021916). Color pallets are set by bits RC11 to RC13 of the OSD RAM from among the selection range.

- OSD mode 15 kinds

Color pallets are set by bits RC11 to RC14 of the OSD RAM.

- CDOSD mode 8 kinds

Color pallet selection range (color pallets 0 to 7 or 8 to 15) can be selected by bit 3 of the OSD control register 3 (address 021916). Color pallets are set in dot units according to the CD font data (the OSD RAM<color dot font> contents) from among the selection range.

Only in CDOSD mode, a dot which selects color pallet 0 or 8 is colored to the color pallet set by RC13 to RC16 of OSD RAM in character units.

- SPRITE display 8 kinds

Color pallet selection range (color pallets 0 to 7 or 8 to 15) can be selected by bit 4 of the OSD control register 3 (address 021916).

Color pallets are set in dot units according to the CD font data (the OSD RAM<color dot font> contents) from among the selection range.

Notes 1: Color pallet 8 is always selected for bordering and solid space output (OUT 1 output) regardless of the set value in the register.

2: Color pallet 0 (transparent) and the transparent setting of other color pallets will differ. When there are multiple layers overlapping (on top of each other, piled up), and the priority layer is color pallet 0 (transparent), the bottom layer is displayed, but if the priority layer is the transparent setting of any other color pallet, the background is displayed without displaying the bottom layer (refer to Figure 12.11.26).

12.11.8 Character Background Color

The display area around the characters can be colored in with a character background color. Character background colors are set in character units.

- CC mode 4 kinds

Color pallet selection range (color pallets 0 to 3, 4 to 7, 8 to 11, or 12 to 15) can be selected by bits 1 and 2 of the OSD control register 3 (address 021916). Color pallets are set by bits RC20 and RC21 of the OSD RAM from among the selection range.

- OSD mode 15 kinds

Color pallets are set by bits RC15, RC16, RC20, and RC21 of the OSD RAM.

Note : The character background is displayed in the following part:
(character display area) – (character font) – (border).

Accordingly, the character background color and the color signal for these two sections cannot be mixed.

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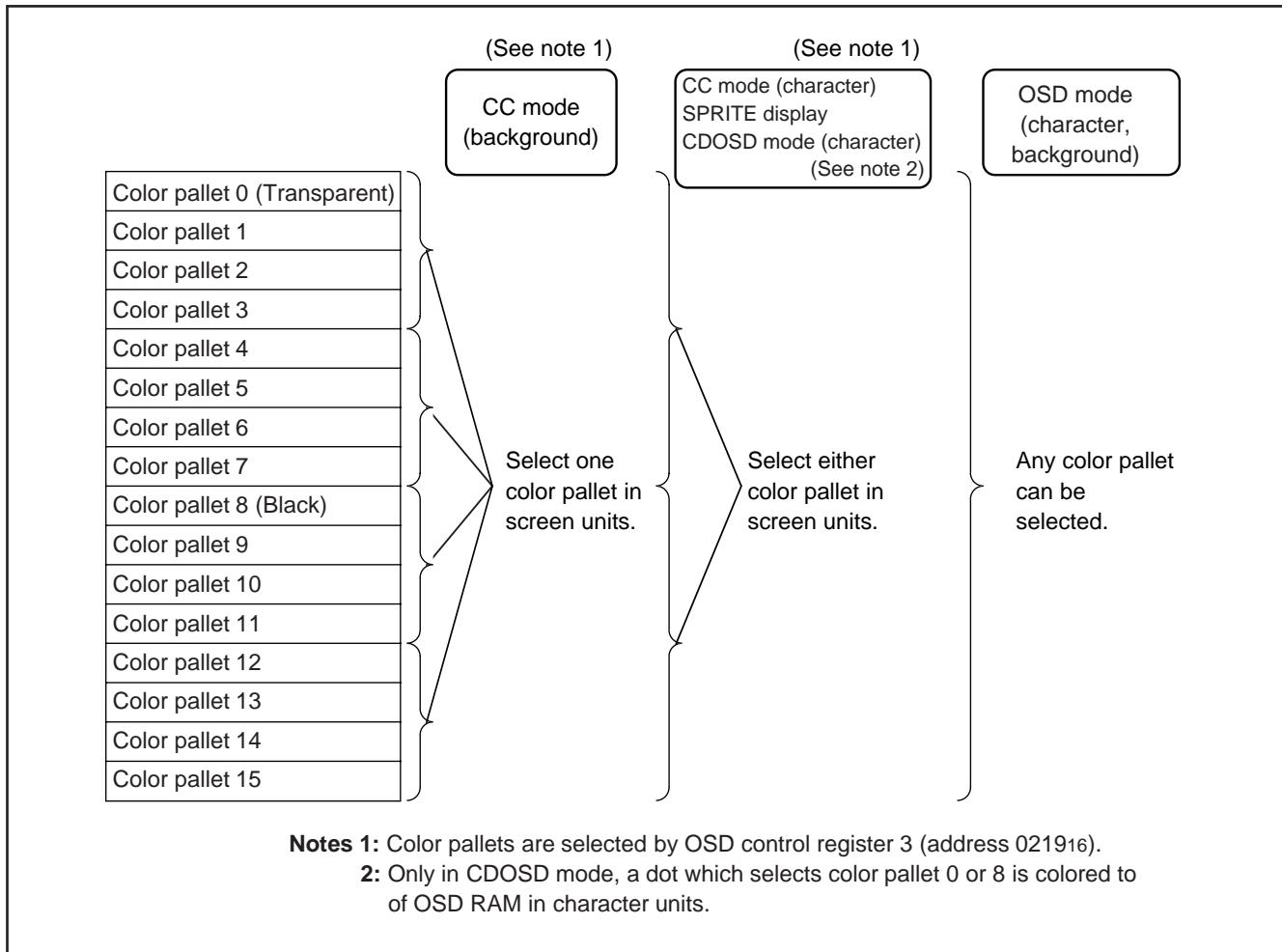


Fig. 12.11.24 Color Code Selection

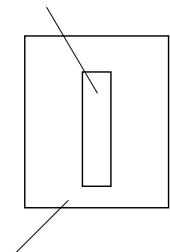
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Dot area specified to color pallet 1



Set values of OSD RAM (RC16 to RC13)

0000 0001 0010



Dot area specified to color pallet 0

When setting black and blue to color pallets 1 and 2, respectively
(only in CDOSD mode).

Fig. 12.11.25 Set of Color Pallet 0 or 8 in CDROM Mode

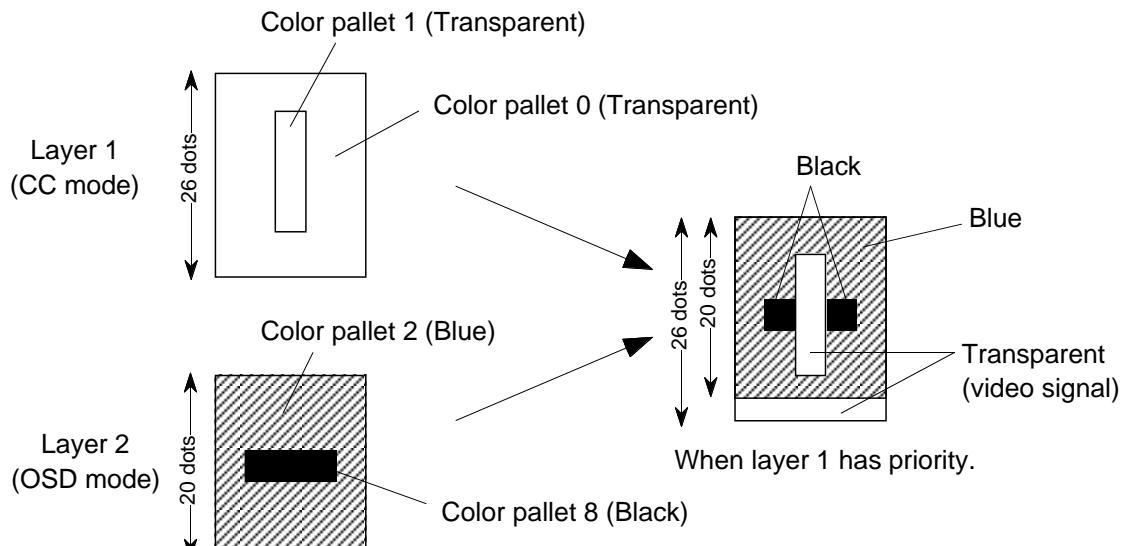


Fig. 12.11.26 Difference Between Color Code 0 (Transparent) and Transparent Setting of Other Color Codes

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OSD Control Register 3

b7 b6 b5 b4 b3 b2 b1 b0



OSD control register 3 (OC3) [Address 0219₁₆]

B	Name	Functions	After reset	R	W
0	CC mode character color selection bit (OC30)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
1, 2	CC mode character background color selection bits (OC31, OC32) (See note)	b1 b0 0 0: Color code 0 to 3 0 1: Color code 4 to 7 1 0: Color code 8 to 11 1 1: Color code 12 to 15	0	R	W
3	CDOSD mode character color selection bit (OC33)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
4	SPRITE color selection bit (OC34)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
5	OSD mode window control bit (OC35)	0: Window OFF 1: Window ON	0	R	W
6	CC mode window control bit (OC36)	0: Window OFF 1: Window ON	0	R	W
7	CDOSD mode window control bit (OC37)	0: Window OFF 1: Window ON	0	R	W

Note: Color pallet 8 is always selected for solid space (when OUT1 output is selected), regardless of value of this register.

Fig. 12.11.27 OSD Control Register 3

Color Pallet Register i

b7 b6 b5 b4 b3 b2 b1 b0



Color pallet register i (CRI) (i = 1 to 7, 9 to 15) [Addresses 0241₁₆ to 0247₁₆, 0249₁₆ to 024F₁₆]

B	Name	Functions	After reset	R	W
0, 1	R signal output control bits (CRI0, CRI1)	b0 b1 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R	W
2, 3	G signal output control bits (CRI2, CRI3)	b3 b2 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R	W
4, 5	B signal output control bits (CRI4, CRI5)	b5 b4 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R	W
6	OUT1 signal output control bit (CRI6)	0: No output 1: Output	Indeterminate	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—

Note: When selecting digital output, the output is Vcc at all values other than "00."

Fig. 12.11.28 Color Pallet Register i (i = 1 to 7, 9 to 15)

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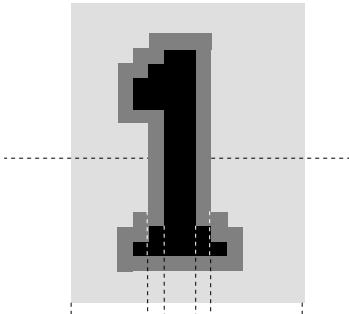
PRELIMINARY

Notice: This is not a final specification.
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12.11.9 OUT1, OUT2 Signals

The OUT1, OUT2 signals are used to control the luminance of the video signal. The output waveform of the OUT1, OUT2 signals is controlled by bit 6 of the color code register i (refer to Figure 86), bits

2 and 7 of the block control register i (refer to Figure 63) and RC17 of OSD RAM. The setting values for controlling OUT1, OUT2 and the corresponding output waveform is shown in Figure 12.11.29



OUT1 signal	Conditions		OUT1 control bit (See note) (b6 of color pallet register i)	Output waveform		
	OUT2 output control (RC 17 of OSD RAM)	Border output control bit (See note) (Bit 2 of block control register i)		Background	Character	
OUT1 signal	0	0	0	H	L	
			1	H	L	
		1	0	H	L	
			1	H	L	
	1	0	0	H	L	
			1	H	L	
		1	0	H	L	
			1	H	L	
OUT2 signal	0	X	X	X	H	
	1	X	X	X	L	

Notes 1: This control is only valid in the OSD mode. It is invalid in CC/CDOSD mode.

2: In the CDOSD mode, coloring is performed for each dot. Accordingly, OUT1 outputs to dots which bit 6 of the color pallet register i is set to "0."

3: OUT2 cannot be output in sprite OSD.

4: X is an arbitrary value.

Fig. 12.11.29 Setting Value for Controlling OUT1, OUT2 and Corresponding Output Waveform

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

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PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

12.11.10 Attribute

The attributes (flash, underline, italic) are controlled to the character font. The attributes to be controlled are different depending on each mode.

CC mode Flash, underline, italic for each character
OSD mode Border (all bordered, shadow bordered can be selected) for each block

(1) Under line

The underline is output at the 23rd and 24th lines in vertical direction only in the CC mode. The underline is controlled by RC16 of OSD RAM. The color of underline is the same color as that of the character font.

(2) Flash

The parts of the character font, the underline, and the character background are flashed only in the CC mode. The flash for each character is controlled by RC15 of OSD RAM. The ON/OFF for flash is controlled by bit 3 of the OSD control register 1 (refer to Figure 12.11.3). When this bit is "0", only character font and underline flash. When "1", for a character without solid space output, R, G, B and OUT1 (all display area) flash, for a character with solid space output, only R, G and B (all display area) flash. The flash cycle bases on the VSYNC count.

<NTSC method>

- VSYNC cycle \times 48 \approx 800 ms (at flash ON)
- VSYNC cycle \times 16 \approx 267 ms (at flash OFF)

(3) Italic

The italic is made by slanting the font stored in OSD ROM to the right only in the CC mode. The italic is controlled by RC14 of OSD RAM.

The display example of attribute is shown in Figure 12.11.31. In this case, "R" is displayed.

Notes 1: When setting both the italic and the flash, the italic character flashes.

2: When a flash character (with flash character background) ajoin on the right side of a non-flash italic character, parts out of the non-flash italic character is also flashed.

3: OUT2 is not flashed.

4: When the pre-divide ratio = 1, the italic character with slant of 1 dot \times 5 steps is displayed (refer to Figure 12.11.30 (c)). When the pre-divide ratio = 2, the italic character with slant of 1/2 dot \times 10 steps is displayed (refer to Figure 12.11.30 (d)).

5: The boundary of character color is displayed in italic. However, the boundary of character background color is not affected by the italic (refer to Figure 12.11.31).

6: The adjacent character (one side or both side) to an italic character is displayed in italic even when the character is not specified to display in italic (refer to Figure 12.11.31).

7: When displaying the 32nd character in the italic and when solid space is off (OC14 = "0"), parts out of character area is not displayed.

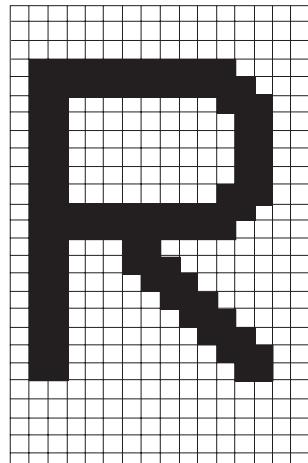
8: When displaying the italic character in the block with the pre-divide ratio = 1, set the OSD clock frequency to 11 MHz to 14 MHz.

M37280MF-XXXSP, M37280MK-XXXSP

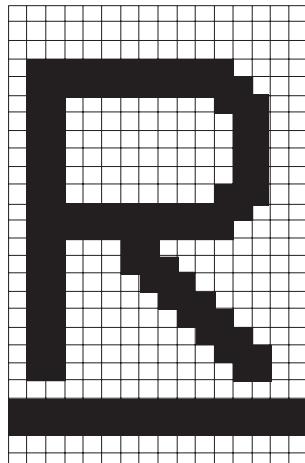
M37280EKSP

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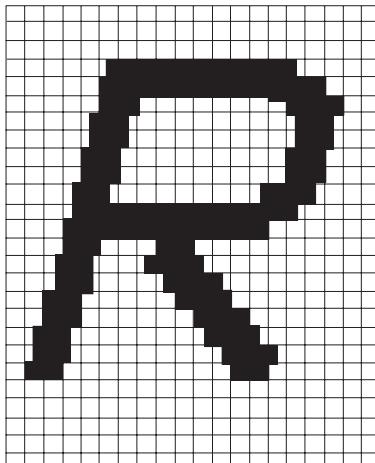
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.



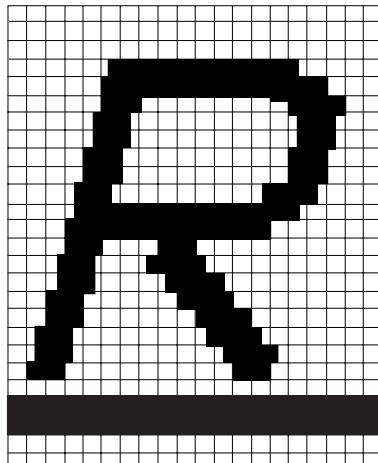
(a) Ordinary



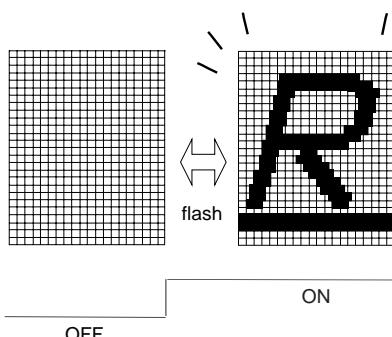
(b) Underline



(c) Italic



(d) Under line and Italic



(e) Under line and Italic and flash

Color code 1	
Bit 6	Bit 4
0	0

Color code 1	
Bit 6	Bit 4
1	0

Color code		
Bit 4 (RC 16)	Bit 5 (RC 15)	Bit 6 (RC 16)
1	1	1

Fig. 12.11.30 Example of Attribute Display (in CC Mode)

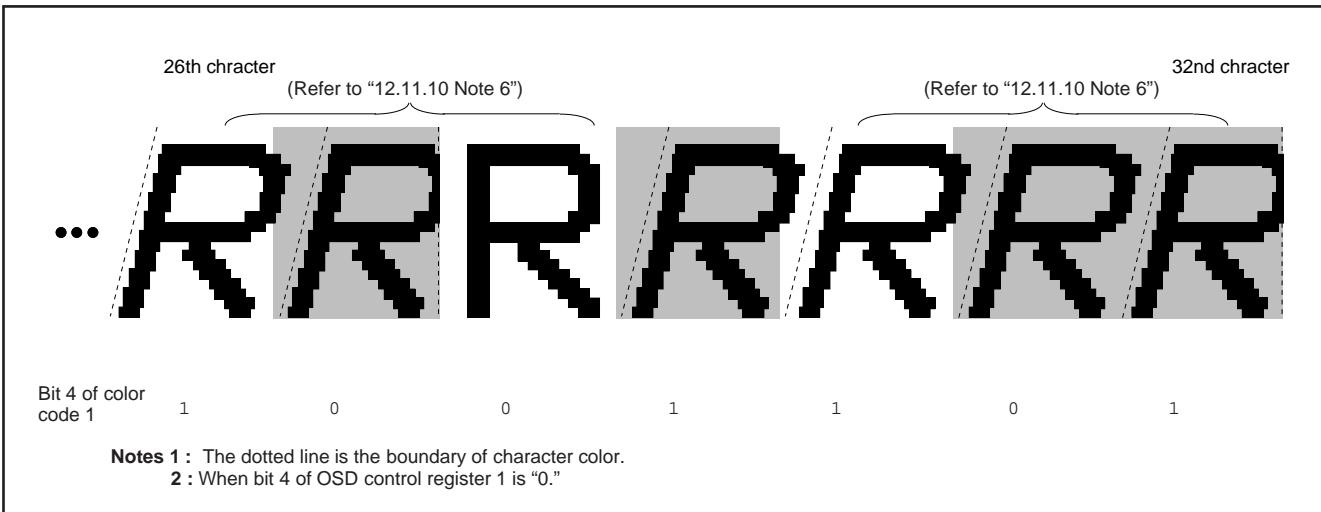
**M37280MF-XXXSP, M37280MK-XXXSP
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Fig. 12.11.31 Example of Italic Display

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(4) Border

The border is output only in the OSD mode. The all bordered (bordering around of character font) and the shadow bordered (bordering right and bottom sides of character font) are selected (refer to Figure 12.11.31) by bit 2 of the OSD control register 1 (refer to Figure 12.11.3). The ON/OFF switch for borders can be controlled in block units by bit 2 of the block control register i (refer to Figure 12.11.4).

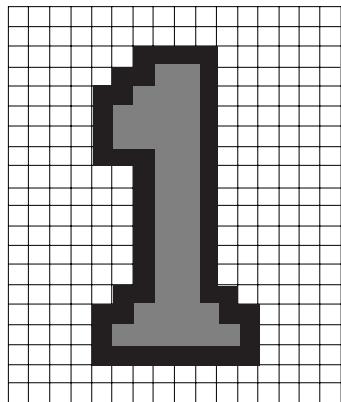
The OUT1 signal is used for border output. The border color is fixed at color code 8 (block). The border color for each screen is specified by the border color register i.

The horizontal size (x) of border is 1Tc (OSD clock cycle divided in the pre-divide circuit) regardless of the character font dot size. However, only when the pre-divide ratio = 2 and character size = 1.5Tc, the horizontal size is 1.5Tc. The vertical size (y) different depending on the screen scan mode and the vertical dot size of character font.

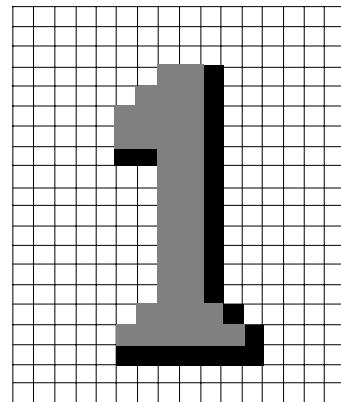
Notes 1: The border dot area is the shaded area as shown in Figure 12.11.34.

2: When the border dot overlaps on the next character font, the character font has priority (refer to Figure 12.11.35 A). When the border dot overlaps on the next character back ground, the border has priority (refer to Figure 12.11.35 B).

3: The border in vertical out of character area is not displayed (refer to Figure 12.11.35).

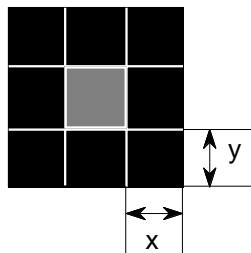


All bordered



Shadow bordered

Fig. 12.11.32 Example of Border Display



Border dot size	Scan mode	Normal scan mode		Bi-scan mode	
	Vertical dot size of character font	1/2H	1H, 2H, 3H	1/2H, 1H, 2H, 3H	
Horizontal size (x)		1Tc (OSD clock cycle divided in pre-divide circuit) 1.5Tc when selecting 1.5Tc for character size.			
Vertical size (y)		1/2H	1H	1H	

Fig. 12.11.33 Horizontal and Vertical Size of Border

M37280MF-XXXSP, M37280MK-XXXSP

M37280EKSP

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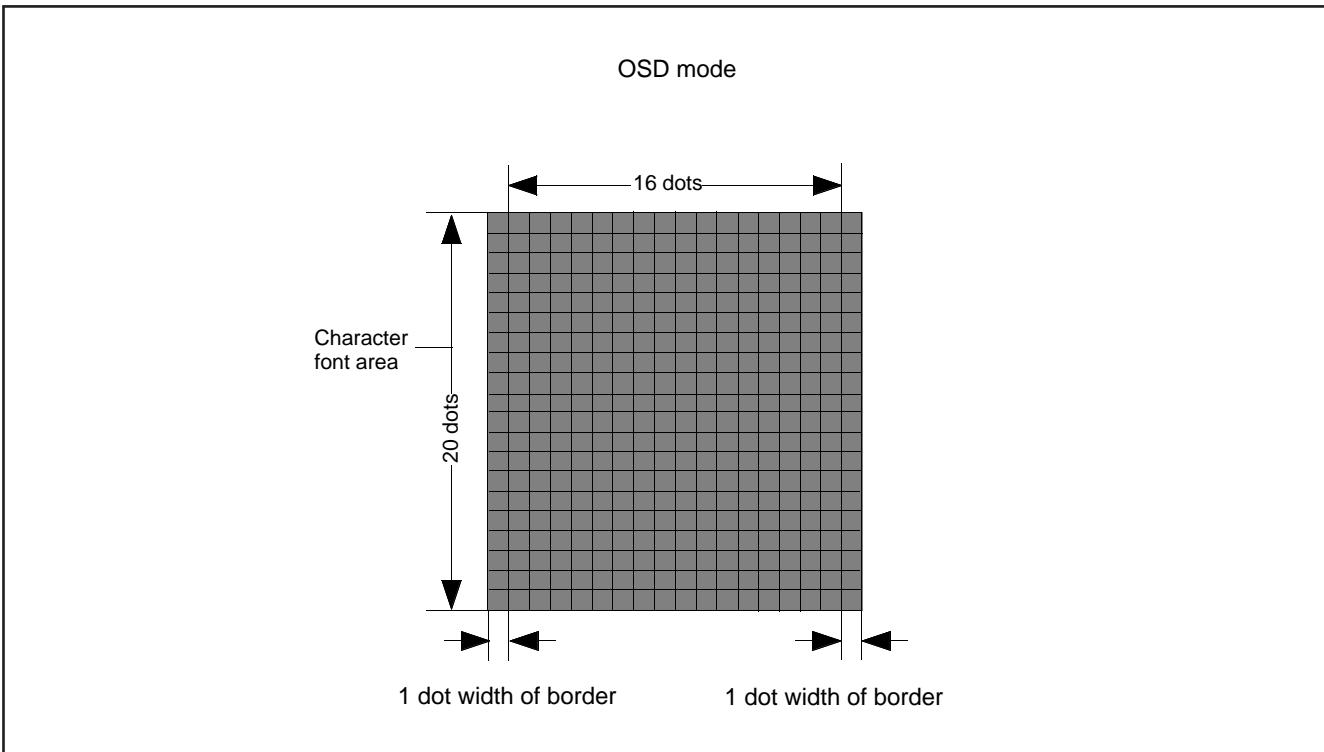


Fig. 12.11.34 Border Area

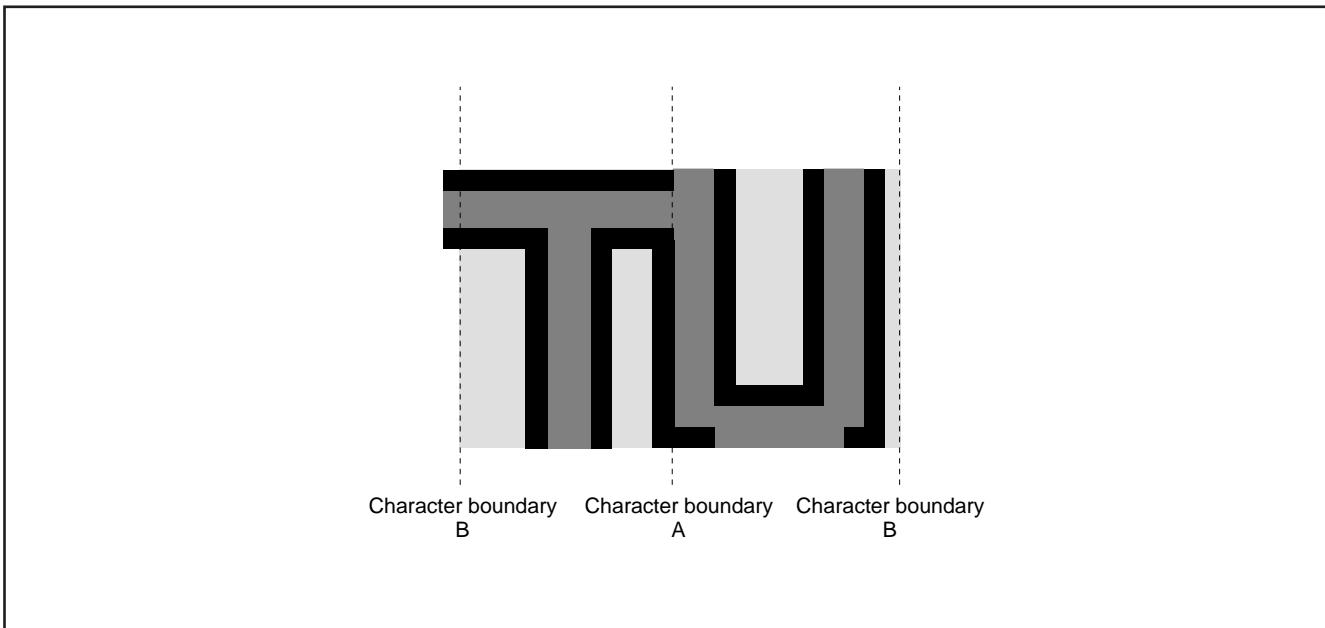


Fig. 12.11.35 Border Priority

M37280MF-XXXSP, M37280MK-XXXSP

M37280EKSP

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and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

12.11.11 Multiline Display

This microcomputer can ordinarily display 16 lines on the CRT screen by displaying 16 blocks at different vertical positions. In addition, it can display up to 16 lines by using OSD interrupts.

An OSD interrupt request occurs at the point at which display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical position registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block. The mode in which an OSD interrupt occurs is different depending on the setting of the OSD control register 2 (refer to Figure 12.11.7).

- When bit 7 of the OSD control register 2 is “0”

An OSD interrupt request occurs at the completion of layer 1 block display.

- When bit 7 of the OSD control register 2 is “1”

An OSD interrupt request occurs at the completion of layer 2 block display.

Notes 1: An OSD interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to off display by the display control bit of the block control register i (addresses 00D016 to 00DF16), an OSD interrupt request does not occur (refer to Figure 12.11.36 (A)).

2: When another block display appears while one block is displayed, an OSD interrupt request occurs only once at the end of the another block display (refer to Figure 12.11.36 (B)).

3: On the screen setting window, an OSD interrupt occurs even at the end of the CC mode block (off display) out of window (refer to Figure 12.11.36 (C)).

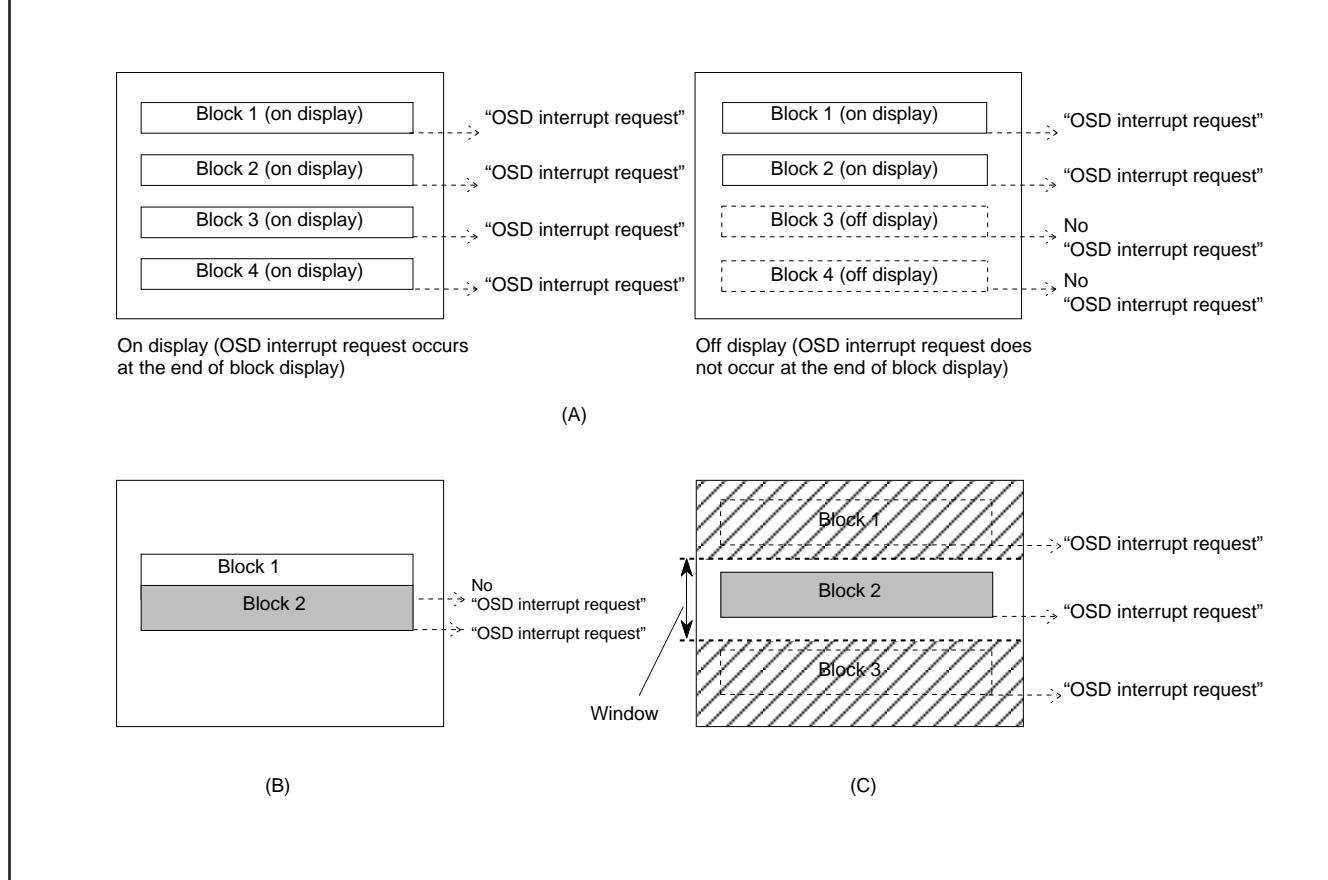


Fig. 12.11.36 Note on Occurrence of OSD Interrupt

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PRELIMINARY

Notice: This is not a final specification.
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12.11.12 Automatic Solid Space Function

This function generates automatically the solid space (OUT1 or OUT2 blank output) of the character area in the CC mode.

The solid space is output in the following area :

- Any character area except character code "00916"
- Character area on the left and right sides of the above character

This function is turned on and off by bit 4 of the OSD control register 1 (refer to Figure 12.11.3).

And the OUT1 output or OUT2 output can be selected by bit 3 of OSD control register 2.

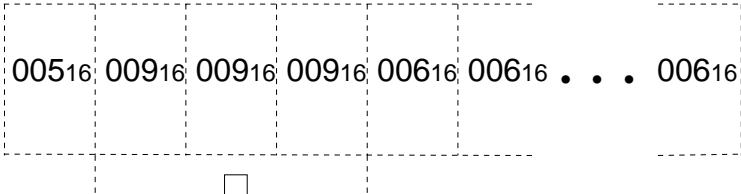
Note: When selecting OUT1 as solid space output, character background color with solid space output is fixed to color pallet 8 (black) regardless of setting.

Table 12.11.7 Setting for Automatic Solid Space

Bit 4 of OSD Control Register 1	0				1			
Bit 3 of OSD Control Register 2	0		1		0		1	
RC17 of OSD RAM	0	1	0	1	0	1	0	1
OUT1 Output Signal	•Character font area •Character background area		•Character font area •Character background area		•Solid space area		•Character font area •Character background area	
OUT2 Output Signal	OFF	•Character display area	OFF	•Character display area	OFF	•Character display area	OFF	•Solid space •Character display area

When setting the character code "00516" as the character A, "00616" as the character B.

(OSD RAM)



(Display screen)

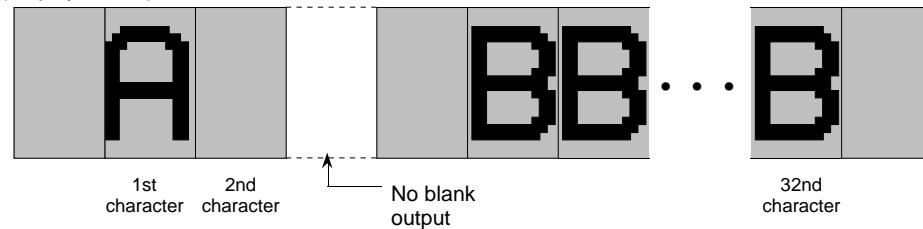


Fig. 12.11.37 Display Screen Example of Automatic Solid Space

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PRELIMINARY

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12.11.13 Scan Mode

This microcomputer has the bi-scan mode for corresponding to HSYNC of double speed frequency. In the bi-scan mode, the vertical start display position and the vertical size is two times as compared with the normal scan mode. The scan mode is selected by bit 1 of the OSD control register 1 (refer to Figure 12.11.3).

Table 12.11.8 Setting for Scan Mode

Parameter	Scan Mode	Normal Scan	Bi-Scan
Bit 1 of OSD Control Register 1		0	1
Vertical Display Start Position		Value of vertical position register $\times 1H$	Value of vertical position register $\times 2H$
Vertical Dot Size		1TC \times 1/2H 1TC \times 1H 2TC \times 2H 3TC \times 3H	1TC \times 1H 1TC \times 2H 2TC \times 4H 3TC \times 6H

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PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

12.11.14 Window Function

The window function can be set windows on-screen, and output OSD within only the area where the window is set.

The ON/OFF for vertical window function is performed by bit 5 of OSD control register 1 and is used to select vertical window function or vertical blank function by bit 6 of OSD control register 2. Accordingly, the vertical window function cannot be used simultaneously with the vertical blank function. The display mode to validate the window function is selected by bits 5 to 7 of OSD control register 3. The top boundary is set by top border control registers 1 and 2 (TB1, TB2) and the bottom boundary is set by bottom border control registers 1 and 2 (BB1, BB2).

The ON/OFF for horizontal window function is performed by bit 4 of OSD control register 2 and is used interchangeably for the horizontal blank function with bit 5 of OSD control register 2. Accordingly, the horizontal blank function cannot be used simultaneously with the horizontal window function. The display mode to validate the window function is selected by bits 5 to 7 of OSD control register 3. The left boundary is set by left border control registers 1 and 2 (LB1 and LB2), and the right boundary is set by right border control registers 1 and 2 (RB1 and RB2).

Notes 1: When using vertical window, do not set "0016" or "0116" to TB1 at TB2 = "0016."

2: When using horizontal window, do not set LB1 = LB2 = "0016."

3: Horizontal blank and horizontal window, as well as vertical blank and vertical window can not be used simultaneously.

4: When using horizontal window, set as follows:

$(LB1 + LB2 \times 16^2) < (RB1 + RB2 \times 16^2)$.

5: When using vertical window, set as follows:

$(TB1 + TB2 \times 16^2) < (BB1 + BB2 \times 16^2)$.

6: When the window function is ON by OSD control registers 1 and 2, the window function of OUT2 is valid in all display mode regardless of setting value of OSD control register 3 (bits 5 to 7). For example, even when make the window function valid in only CC mode, the function of OUT2 is valid in OSD and CDOSD modes.

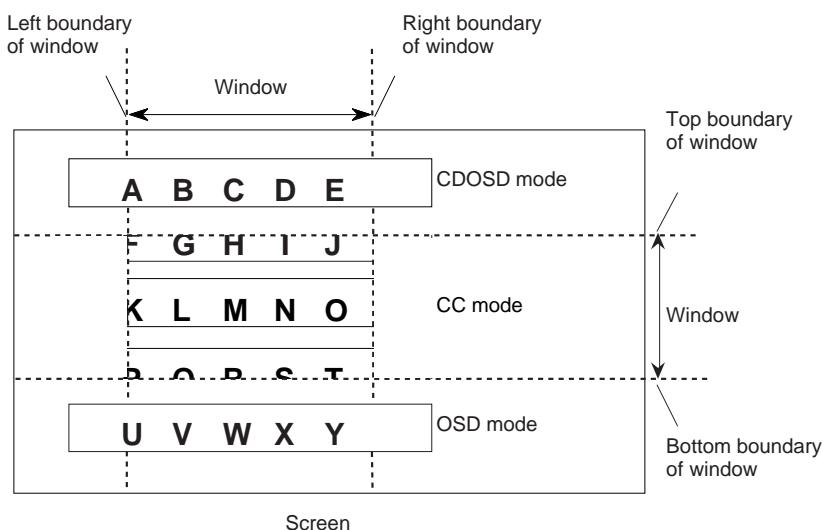


Fig. 12.11.38 Example of window function (When CC Mode Is Valid)

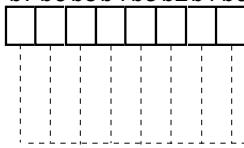
M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

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PRELIMINARY
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Top Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0



Top border control register 1 (TB1) [Address 021C16]

B	Name	Functions	After reset	R/W
0 to 7	Control bits of top border (TB10 to TB17)	Top border position (low-order 8 bits) TH X (setting value of low-order 2 bits of TB2 $\times 16^2$ + setting value of high-order 4 bits of TB1 $\times 16^1$ + setting value of low-order 4 bits of TB1 $\times 16^0$)	Indeterminate	R/W

Notes 1: Do not set "0016" or "0116" to the TB1 at TB2 = "0016."

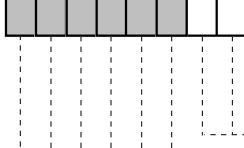
2: TH is cycle of HSYNC.

3: TB2 is top border control register 2.

Fig. 12.11.39 Top Border Control Register 1

Top Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0



Top border control register 2 (TB2) [Address 021E16]

B	Name	Functions	After reset	R/W
0, 1	Control bits of top border (TB20, TB21)	Top border position (high-order 2 bits) TH X (setting value of low-order 2 bits of TB2 $\times 16^2$ + setting value of high-order 4 bits of TB1 $\times 16^1$ + setting value of low-order 4 bits of TB1 $\times 16^0$)	Indeterminate	R/W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R

Notes 1: Do not set "0016" or "0116" to the TB1 at TB2 = "0016."

2: TH is cycle of HSYNC.

3: TB1 is top border control register 1.

Fig. 12.11.40 Top Border Control Register 2

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PRELIMINARY

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Bottom Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Bottom border control register 1 (BB1) [Address 021D16]

B	Name	Functions	After reset	R W
0 to 7	Control bits of bottom border (BB10 to BB17)	Bottom border position (low-order 8 bits) TH \times (setting value of low-order 2 bits of BB2 \times 16 ² + setting value of high-order 4 bits of BB1 \times 16 ¹ + setting value of low-order 4 bits of BB1 \times 16 ⁰)	Indeterminate	R W

Notes 1: Set values fit for the following condition:

$$(TB1 + TB2 \times 16^2) < (BB1 + BB2 \times 16^2).$$

2: TH is cycle of HSYNC.

3: BB2 is bottom border control register 2.

Fig. 12.11.41 Bottom Border Control Register 1

Bottom Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Bottom border control register 2 (BB2) [Address 021F16]

B	Name	Functions	After reset	R W
0, 1	Control bits of bottom border (BB20, BB21)	Bottom border position (high-order 2 bits) TH \times (setting value of low-order 2 bits of BB2 \times 16 ² + setting value of high-order 4 bits of BB1 \times 16 ¹ + setting value of low-order 4 bits of BB1 \times 16 ⁰)	Indeterminate	R W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R —

Notes 1: Set values fit for the following condition:

$$(TB1 + TB2 \times 16^2) < (BB1 + BB2 \times 16^2).$$

2: TH is cycle of HSYNC.

3: BB1 is bottom border control register 1.

Fig. 12.11.42 Bottom Border Control Register 2

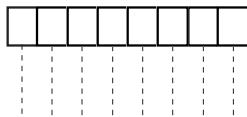
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PRELIMINARY
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Some parametric limits are subject to change.

Left Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0



Left border control register 1 (LB1) [Address 025016]

B	Name	Functions	After reset	R	W
0	Control bits of left border (LB10 to LB17)	Left border position (low-order 8 bits) Tosc X (setting value of low-order 3 bits of LB2 $\times 16^2$ + setting value of high-order 4 bits of LB1 $\times 16^1$ + setting value of low-order 4 bits of LB1 $\times 16^0$)	1	R	W
1 to 7			0		

Notes 1: Do not set LB1 = LB2 = "0016."

2: Set values fit for the following condition:
(LB1 + LB2 $\times 16^2$) < (RB1 + RB2 $\times 16^2$).

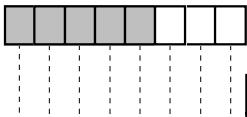
3: Tosc is OSD oscillation period.

4: LB2 is left border control register 2.

Fig. 12.11.43 Left BorderControl Register 1

Left Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0



Left border control register 2 (LB2) [Address 025116]

B	Name	Functions	After reset	R	W
0 to 2	Control bits of left border (LB20 to LB22)	Left border position (high-order 3 bits) Tosc X (setting value of low-order 3 bits of LB2 $\times 16^2$ + setting value of high-order 4 bits of LB1 $\times 16^1$ + setting value of low-order 4 bits of LB1 $\times 16^0$)	0	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		0	R	W

Notes 1: Do not set LB1 = LB2 = "0016."

2: Set values fit for the following condition:
(LB1 + LB2 $\times 16^2$) < (RB1 + RB2 $\times 16^2$).

3: Tosc is OSD oscillation period.

4: LB1 is left border control register 1.

Fig. 12.11.44 Left Border Control Register 2

M37280MF-XXXSP, M37280MK-XXXSP

M37280EKSP

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and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Right Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0



Right border control register 1 (RB1) [Address 0252₁₆]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of right border (RB10 to RB17)	Right border position (low-order 8 bits) Tosc X (setting value of low-order 3 bits of RB2 $\times 16^2$ + setting value of high-order 4 bits of RB1 $\times 16^1$ + setting value of low-order 4 bits of RB1 $\times 16^0$)	1	R	W

Notes 1: Set values fit for the following condition:

$(LB1 + LB2 \times 16^2) < (RB1 + RB2 \times 16^2)$.

2: Tosc is OSD oscillation period.

3: RB2 is right border control register 2.

Fig. 12.11.45 Right Border Control Register 1

Right Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0



Right border control register 2 (RB2) [Address 0253₁₆]

B	Name	Functions	After reset	R	W
0 to 2	Control bits of right border (RB20 to RB22)	Right border position (high-order 3 bits) Tosc X (setting value of low-order 3 bits of RB2 $\times 16^2$ + setting value of high-order 4 bits of RB1 $\times 16^1$ + setting value of low-order 4 bits of RB1 $\times 16^0$)	1	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0".		0	R	W

Notes 1: Set values fit for the following condition:

$(LB1 + LB2 \times 16^2) < (RB1 + RB2 \times 16^2)$.

2: Tosc is OSD oscillation period.

3: RB1 is right border control register 1.

Fig. 12.11.46 Right Border Control Register 2

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

12.11.15 Blank Function

The blank function can output blank (OUT1) area on all sides (vertical and horizontal) of the screen.

The ON/OFF for vertical blank function is performed by bit 5 of the OSD control register 1 and is used to select vertical window function or vertical blank function by bit 6 of the OSD control register 2. Accordingly, the vertical blank function cannot be used simultaneously with the vertical window function. The top border is set by the top border control registers 1 and 2 (TB1, TB2), and the bottom border is set by the bottom border control registers 1 and 2 (BB1, BB2), in 1H units.

The ON/OFF for horizontal blank function is performed by bit 4 of the OSD control register 2 and is used interchangeably for the horizontal window function with bit 5 of the OSD control register 2. Accordingly, the horizontal blank function cannot be used simultaneously with the horizontal window function. The left border is set by the left border control registers 1 and 2 (LB1, LB2) and the right border is set by the right border control registers 1 and 2 (RB1, RB2), in 1Tosc units.

The OSD output (except raster) in area with blank output is not deleted.

These blank signals are not output in the horizontal/vertical blanking interval.

Notes 1: When using vertical blank, do not set "0016" and "0116" to TB1 at TB2 = "0016."

2: When using horizontal blank, do not set LB1 = LB2 = "0016."

3: Horizontal blank and horizontal window, as well as vertical blank and vertical window can not be used simultaneously.

4: When using horizontal blank, set as follows:

$(LB1 + LB2 \times 16^2) < (RB1 + RB2 \times 16^2)$.

5: When using vertical blank, set as follows:

$(TB1 + TB2 \times 16^2) < (BB1 + BB2 \times 16^2)$.

6: When all-blocks display is OFF (bit 0 of OSD control register 1 = "0"), do not use vertical blank.

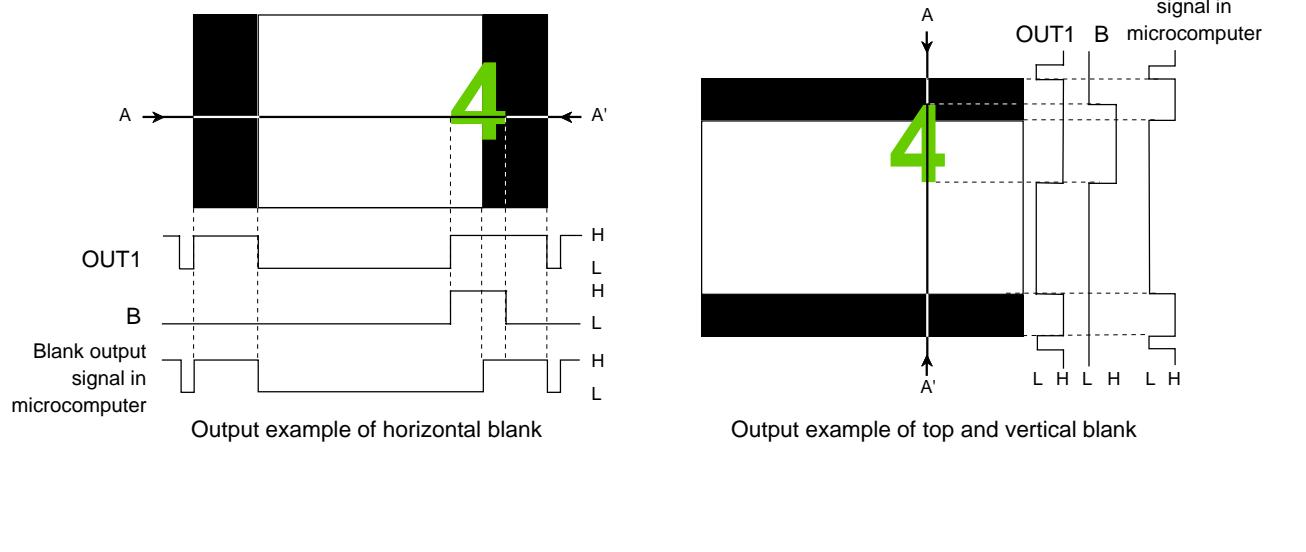


Fig. 12.11.47 Blank Output Example (When OSD Output is B + OUT1)

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

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PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

12.11.16 SPRITE OSD Function

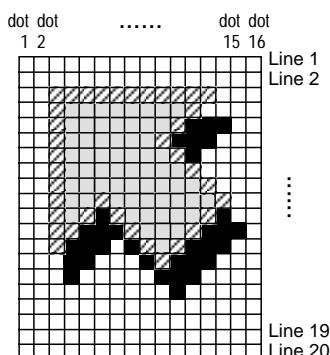
This is especially suitable for cursor and other displays as its function allows for display in any position, regardless of the validity of other OSDs or display positions. The sprite font is a RAM font consisting of 16 horizontal dots 5 20 vertical dots, three planes, and three bits of data per dot. Each plane has corresponding color pallet selection bits, and 8 kinds of color pallets can be selected by the plane bit combination (three bits) for each dot. In addition, the selection range (color pallets 0 to 7 and 8 to 15) can be set, per screen, by bit 4 of the OSD control register 3. The color pallet is set in dot units according to the selection range and the OSD RAM (SPRITE) contents from among the selection range. It is possible to arbitrarily add font data by software for the RAM font in the SPRITE font.

The SPRITE OSD control register can control SPRITE display, dot size, interrupt position, and interrupt generation factors for the SPRITE OSD. The display position can also be set independently of the block display by the SPRITE horizontal position registers and the sprite horizontal vertical position registers. At this time, the horizontal position is set in 2048 steps in 1Tosc units, and the vertical position is set in 1024 steps in 1TH units. When SPRITE display overlaps with other OSDs, SPRITE display is always given priority. However, the SPRITE display overlaps with the OSD which includes OUT2 output, OUT2 in the OSD is output without masking.

Notes 1: The SPRITE OSD function cannot output OUT2.

2: When using SPRITE OSD, do not set HS1 < "3016." at HS2 = "0016."

3: When using SPRITE OSD, do not set VS1 = VS2 = "0016."



Example of SPRITE font

Video adjustment

Tint	-	•	•		•	•	+
Contrast	-	•	•		•	•	+
Color tone	-	•	•		•	•	+
Picture	-	•	•		•	•	+
Brightness	-	•	•		•	•	+

Example of cursor display

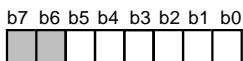
Fig. 12.11.48 SPRITE OSD Display Example

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
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SPRITE OSD Control Register



SPRITE OSD control register (SC) [Address 0258:6]

B	Name	Functions	After reset	R	W
0	SPRITE OSD control bit (SC0)	0: Stopped 1: Operating	0	R	W
1	Pre-divide ratio selection bit (SC1)	0: Pre-divide ratio 1 1: Pre-divide ratio 2	0	R	W
2, 3	Dot size selection bits (SC2, SC3)	b3 b2 0 0: 1Tc × 1/2H 0 1: 1Tc × 1H 1 0: 2Tc × 1H 1 1: 2Tc × 2H	0	R	W
4	Interrupt occurrence position selection bit (SC4)	0: After display of horizontal 20 dots 1: After display of horizontal 10 dots or 20 dots	0	R	W
5	XIN/4096 • SPRITE interrupt source switch bit (SC5)	0: XIN/4096 interrupt 1: SPRITE OSD interrupt	0	R	W
6, 7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0".		0	R	—

Notes
1: Tc : Pre-devided clock period for OSD
2: H : HSYNC

Fig. 12.11.49 SPRITE OSD Control Register

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

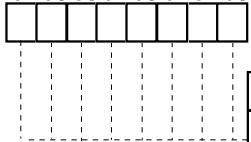
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

SPRITE Horizontal Position Register 1

b7 b6 b5 b4 b3 b2 b1 b0



SPRITE horizontal position register 1 (HS1) [Address 025616]

B	Name	Functions	After reset	R:W
0 to 7	Horizontal display start position control bits of SPRITE OSD (HS10 to HS17)	Horizontal display start position (low-order 8 bits) Tosc \times (setting value of low-order 2 bits of HS2 $\times 16^2$ + setting value of high-order 4 bits of HS1 $\times 16^1$ + setting value of low-order 4 bits of HS1 $\times 16^0$)	Indeterminate	R:W

Notes 1: Do not set HS1 < "3016" at HS2 = "0016."

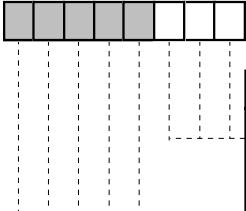
2: Tosc is OSD oscillation period.

3: HS2 is SPRITE horizontal position register 2.

Fig. 12.11.50 SPRITE Horizontal Position Register 1

SPRITE Horizontal Position Register 2

b7 b6 b5 b4 b3 b2 b1 b0



SPRITE horizontal position register 2 (HS2) [Address 025716]

B	Name	Functions	After reset	R:W
0 to 2	Horizontal display start position control bits of SPRITE OSD (HS20 to HS22)	Horizontal display start position (high-order 3 bits) Tosc \times (setting value of low-order 2 bits of HS2 $\times 16^2$ + setting value of high-order 4 bits of HS1 $\times 16^1$ + setting value of low-order 4 bits of HS1 $\times 16^0$)	Indeterminate	R:W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R—

Notes 1: Do not set HS1 < "3016" at HS2 = "0016."

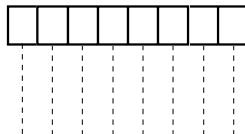
2: Tosc is oscillation period.

3: HS1 is SPRITE horizontal position register 1.

Fig. 12.11.51 SPRITE Horizontal Position Register 2

M37280MF-XXXSP, M37280MK-XXXSP
M37280EKSPSINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLERSPRITE Vertical Position Register 1

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE vertical position register 1 (VS1) [Address 0254₁₆]

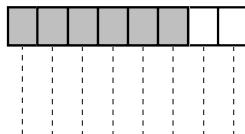
B	Name	Functions	After reset	R	W
0	Vertical display start position (low-order 8 bits) TH X		1	R	W
1 to 7	control bits of SPRITE OSD (VS10 to VS17)	(setting value of low-order 2 bits of VS2 $\times 16^2$ + setting value of high-order 4 bits of VS1 $\times 16^1$ + setting value of low-order 4 bits of VS1 $\times 16^0$)	0		

Notes 1: Do not set "0016" to the VS1 at VS2 = "0016."**2:** TH is cycle of HSYNC.**3:** VS2 is SPRITE vertical position register 2.

Fig. 12.11.52 SPRITE Vertical Position Register 1

SPRITE Vertical Position Register 2

b7 b6 b5 b4 b3 b2 b1 b0

SPRITE vertical position register 2 (VS2) [Address 0255₁₆]

B	Name	Functions	After reset	R	W
0, 1	Vertical start position control bits of SPRITE OSD (VS20, VS21)	Vertical display start position (high-order 2 bits) TH X (setting value of low-order 2 bits of VS2 $\times 16^2$ + setting value of high-order 4 bits of VS1 $\times 16^1$ + setting value of low-order 4 bits of VS1 $\times 16^0$)	0	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0".		0	R	—

Notes 1: Do not set "0016" to the VS1 at VS2 = "0016."**2:** TH is cycle of HSYNC.**3:** VS1 is SPRITE vertical position register 1.

Fig. 12.11.53 SPRITE Vertical Position Register 2

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PRELIMINARY

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12.11.7 OSD Output Pin Control

The OSD output pins R(R1), G(G1), B(B1) and OUT1 can also function as ports P52 to P55. Set the corresponding bit of the OSD port control register (address 00CB16) to "0" to specify these pins as OSD output pins, or set it to "1" to specify it as a general-purpose port P5 pin.

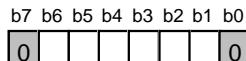
Pins R0, G0 and B0 can also function as ports P17, P15 and P16, respectively. Set bit 1 of the OSD port control register to "0" to specify these pins as a general-purpose output port P1 pin, or set it to "1" to specify it as OSD output pins. When "0," 4-adjustment-level analog output is output from pins R, G and B. When "1," the value which is converted from the analog to the 2-bit digital is output as follows: the high-order bit is output pins R1, G1 and B1 and the low-order bit is output from pins R0, G0 and B0.

The OUT2 can also function as Port P10. Set bit 0 of the port P1 direction register (address 00C316) to "1" (output mode). After that, set bit 6 of the OSD port control register to "1" to specify the pin as OSD output pin, or set it to "0" to specify as port P10 pin.

The input polarity of the HSYNC, VSYNC and output polarity of signals R, G, B, OUT1 and OUT2 can be specified with the I/O polarity control register (address 021716). Set a bit to "0" to specify positive polarity; set it to "1" to specify negative polarity (refer to Figure 12.11.18). The OSD port control register is shown in Figure 12.11.54.

Note: When using ports P52 to P54 as general-purpose pins, set bit 2 of OSD control register 2 (address 021516) to "0."

OSD Port Control Register



OSD port control register (PF) [Address 00CB16]

b	Name	Functions	After reset	R	W
0	Fix this bit to "0"		0	R	W
1	R, G, B output method selection bit (RGB2BIT)	0 : 4-adjustment-level analog is output from pins R, G, B. 1 : Value which is converted from 4-adjustment-level analog to 2-bit digital is output as below: High-order: from R1, G1, B1 Low-order: from R0, G0, B0	0	R	W
2	Port P52 output signal selection bit (R)	0 : R signal output 1 : Port P52 output	0	R	W
3	Port P53 output signal selection bit (G)	0 : G signal output 1 : Port P53 output	0	R	W
4	Port P54 output signal selection bit (B)	0 : B signal output 1 : Port P54 output	0	R	W
5	Port P55 output signal selection bit (OUT1)	0 : OUT1 signal output 1 : Port P55 output	0	R	W
6	Port P10 output signal selection bit (OUT2)	0 : Port P10 signal output 1 : OUT2 output	0	R	W
7	Fix this bit to "0"		0	R	W

Fig. 12.11.54 OSD Port Control Register

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

12.11.18 Raster Coloring Function

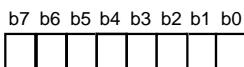
An entire screen (raster) can be colored by setting the bits 6 to 0 of the raster color register. Since each of the R, G, B, OUT1, and OUT2 pins can be switched to raster coloring output, 64 raster colors can be obtained.

When the character color/the character background color overlaps with the raster color, the color (R, G, B, OUT1, OUT2), specified for the character color/the character background color, takes priority of the raster color. This ensures that the character color/the character background color is not mixed with the raster color.

The structure of the raster color register is shown in Figure 12.11.55, the example of raster coloring is shown in Figure 12.11.56.

Note : Raster is not output to the area which includes blank output.

Raster Color Register



Raster color register (RC) [Address 021816]

B	Name	Functions	At reset	R	W
0, 1	Raster color R control bits (RC0, RC1)	b0 b1 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
2, 3	Raster color G control bits (RC2, RC3)	b3 b2 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
4, 5	Raster color B control bits (RC4, RC5)	b5 b4 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
6	Raster color OUT1 control bits (RC6)	0: No output 1: Output	0	R	W
7	Raster color OUT2 control bits (RC7)	0: No output 1: Output	0	R	W

Note: When selecting digital output, Vcc is output at any other values except "00."

Fig. 12.11.54 Raster Color Register

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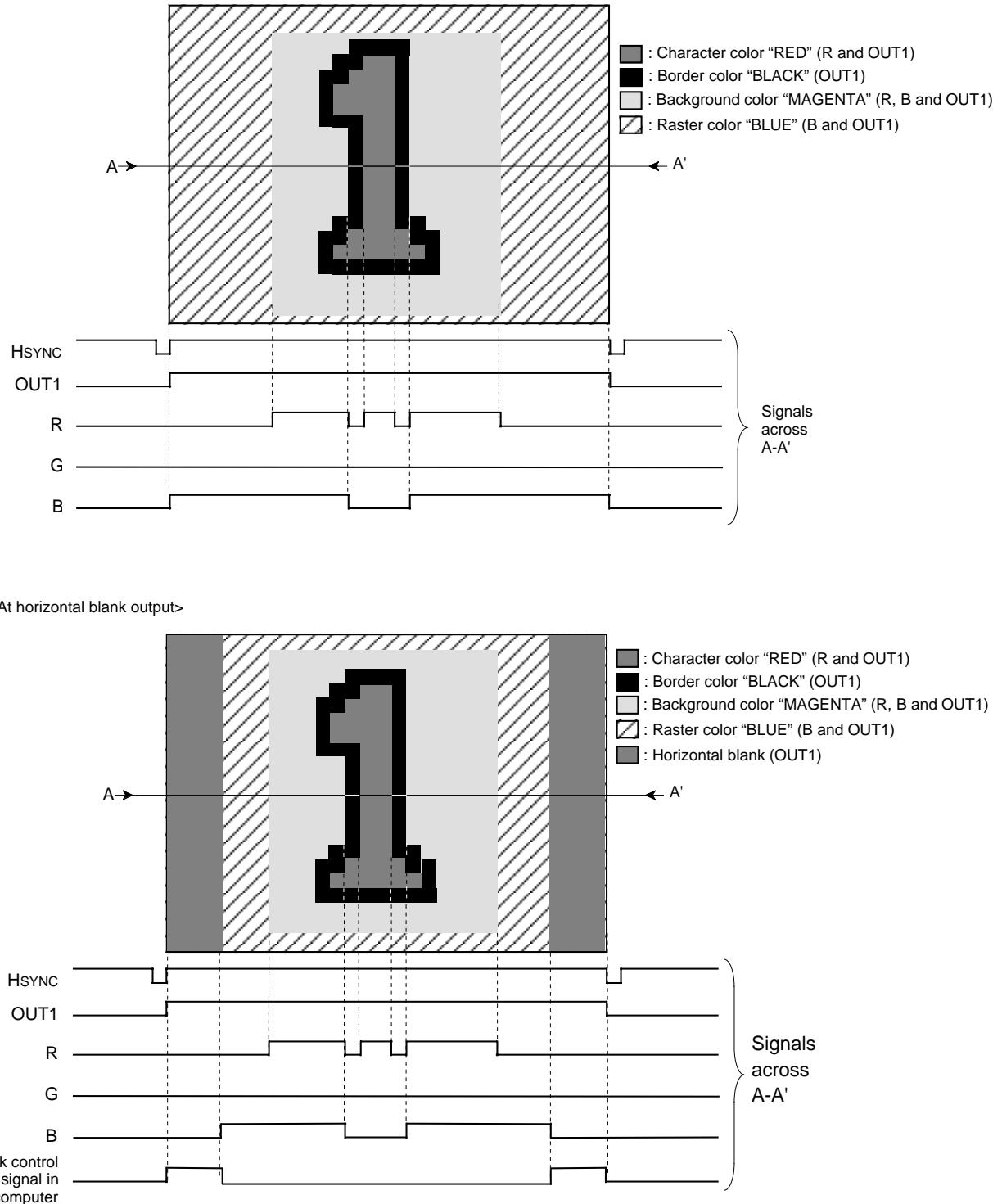


Fig. 12.11.56 Example of Raster Coloring

13. SOFTWARE RUNAWAY DETECT FUNCTION

This microcomputer has a function to decode undefined instructions to detect a software runaway.

When an undefined op-code is input to the CPU as an instruction code during operation, the following processing is done.

- ① The CPU generates an undefined instruction decoding signal.
- ② The device is internally reset because of occurrence of the undefined instruction decoding signal.
- ③ As a result of internal reset, the same reset processing as in the case of ordinary reset operation is done, and the program restarts from the reset vector.

Note, however, that the software runaway detecting function cannot be invalid.

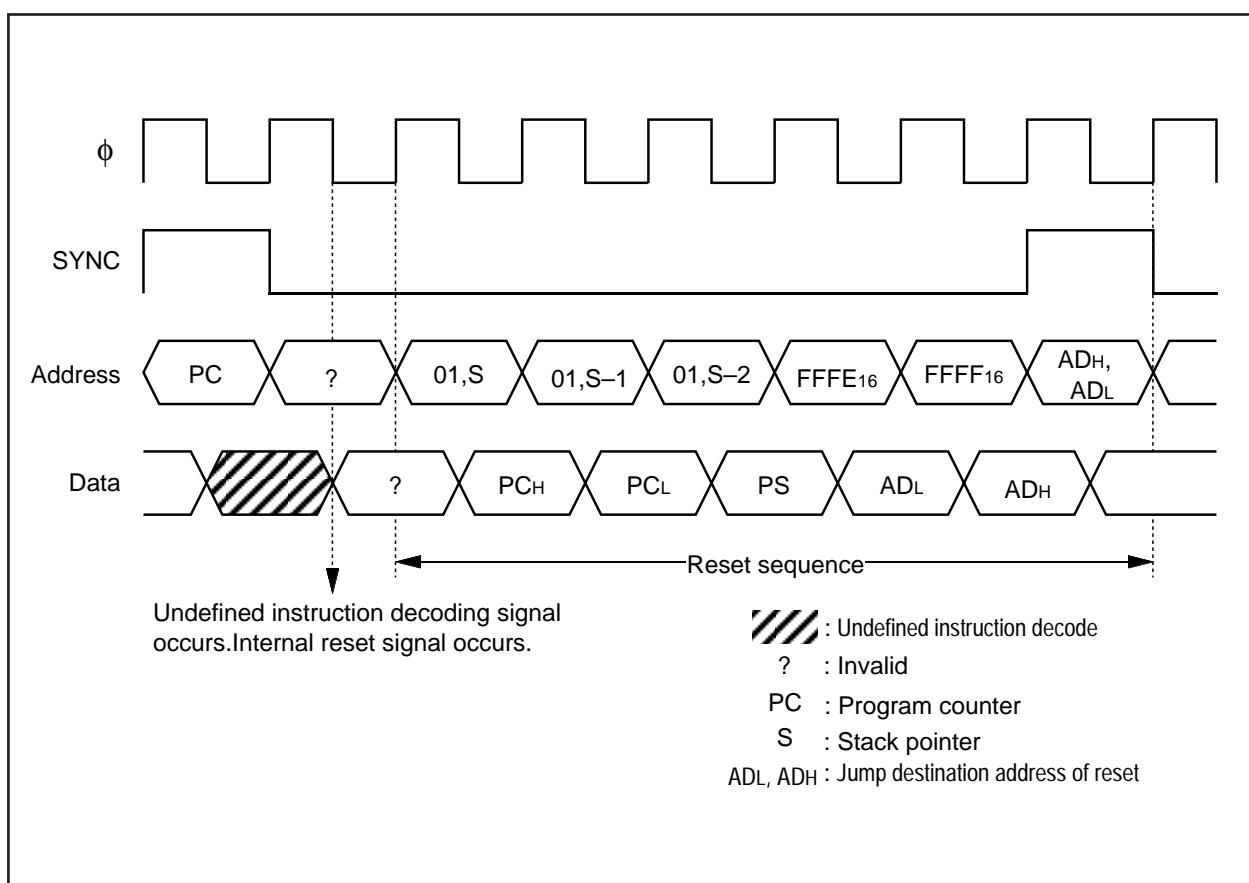


Fig.13.1 Sequence at Detecting Software Runaway Detection

PRELIMINARY

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14. RESET CIRCUIT

When the oscillation of a quartz-crystal oscillator or a ceramic resonator is stable and the power source voltage is $5\text{ V} \pm 10\%$, hold the **RESET** pin at LOW for $2\text{ }\mu\text{s}$ or more, then return to HIGH. Then, as shown in Figure 14.2, reset is released and the program starts from the address formed by using the content of address **FFFF16** as the high-order address and the content of the address **FFFE16** as the low-order address. The internal state of microcomputer at reset are shown in Figures 12.2.2 to 12.2.7.

An example of the reset circuit is shown in Figure 14.1.

The reset input voltage must be kept 0.9 V or less until the power source voltage surpasses 4.5 V .

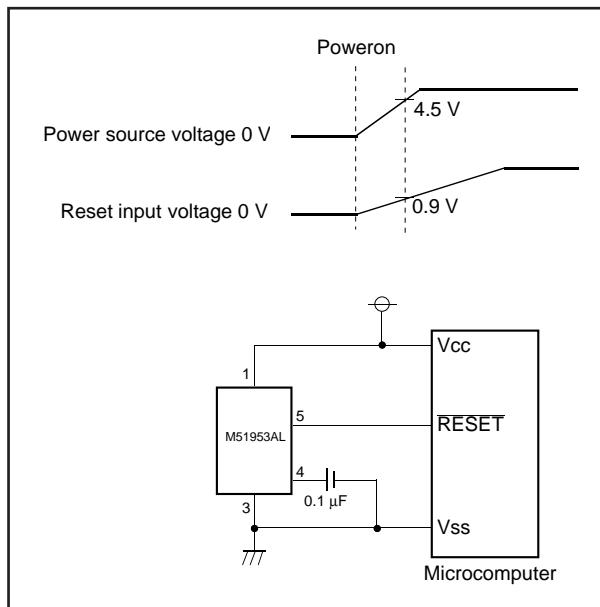


Fig.14.1 Example of Reset Circuit

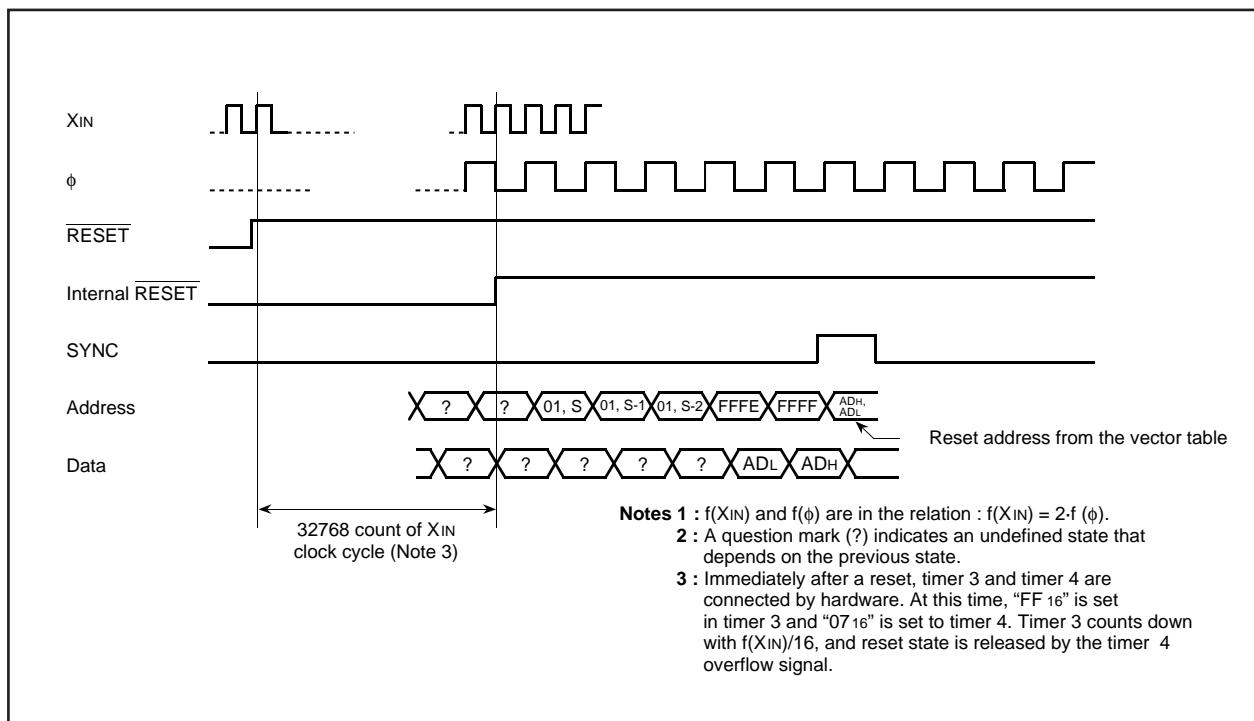


Fig.14.2 Reset Sequence

PRELIMINARY

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M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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15. CLOCK GENERATING CIRCUIT

This microcomputer has 2 built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XcIN and XcOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XcIN and XcOUT. When using XcIN-XcOUT as sub-clock, clear bits 5 and 4 of the clock source control register to "0." To supply a clock signal externally, input it to the XIN (XcIN) pin and make the XOUT (XcOUT) pin open. When not using XcIN clock, connect the XcIN to Vss and make the XcOUT pin open.

After reset has completed, the internal clock ϕ is half the frequency of XIN. Immediately after poweron, both the XIN and XcIN clock start oscillating. To set the internal clock ϕ to low-speed operation mode, set bit 7 of the CPU mode register (address 00FB16) to "1."

15.1 OSCILLATION CONTROL

15.1.1 Stop Mode

The built-in clock generating circuit is shown in Figure 120. When the STP instruction is executed, the internal clock ϕ stops at HIGH. At the same time, timers 3 and 4 are connected by hardware and "FF16" is set in timer 3 and "0716" is set in timer 4. Select f(XIN)/16 or f(XcIN)/16 as the timer 3 count source (set both bit 0 of the timer mode register 2 and bit 6 at address 00C716 to "0" before the execution of the STP instruction). Moreover, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction. The oscillator restarts when external interrupt is accepted. However, the internal clock ϕ keeps its HIGH level until timer 4 overflows, allowing time for oscillation stabilization when a ceramic resonator or a quartz-crystal oscillator is used.

15.1.2 Wait Mode

When the WIT instruction is executed, the internal clock ϕ stops in the HIGH level but the oscillator continues running. This wait state is released at reset or when an interrupt is accepted (Note). Since the oscillator does not stop, the next instruction can be executed at once.

Note: In the wait mode, the following interrupts are invalid.

- VSYNC interrupt
- OSD interrupt
- All timers interrupts using TIM2 pin input as count source
- All timers interrupt using TIM3 pin input as count source
- Data slicer interrupt
- Multi-master I²C-BUS interface interrupt
- f(XIN)/4096 interrupt
- All timer interrupts using f(XIN)/2 or f(XcIN)/2 as count source
- All timer interrupts using f(XIN)/4096 or f(XcIN)/4096 as count source
- A-D conversion interrupt
- SPRITE OSD interrupt

15.1.3 Low-speed Mode

If the internal clock is generated from the sub-clock (XcIN), a low power consumption operation can be realized by stopping only the main clock XIN. To stop the main clock, set bit 6 (CM6) of the CPU mode register (00FB16) to "1." When the main clock XIN is restarted, the program must allow enough time to for oscillation to stabilize. Note that in low-power-consumption mode the XcIN-XcOUT drivability can be reduced, allowing even lower power consumption. To reduce the XcIN-XcOUT drivability, clear bit 5 (CM5) of the CPU mode register (00FB16) to "0." At reset, this bit is set to "1" and strong drivability is selected to help the oscillation to start. When an STP instruction is executed, set this bit to "1" by software before executing.

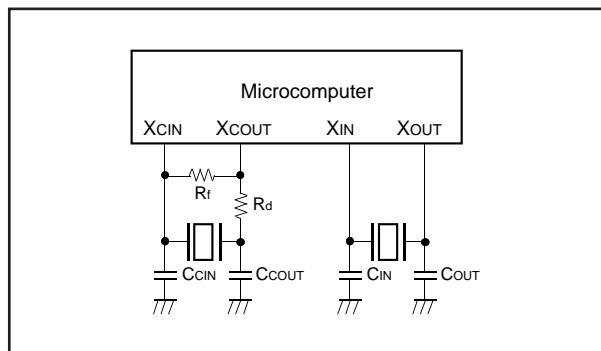


Fig.15.1 Ceramic Resonator Circuit Example

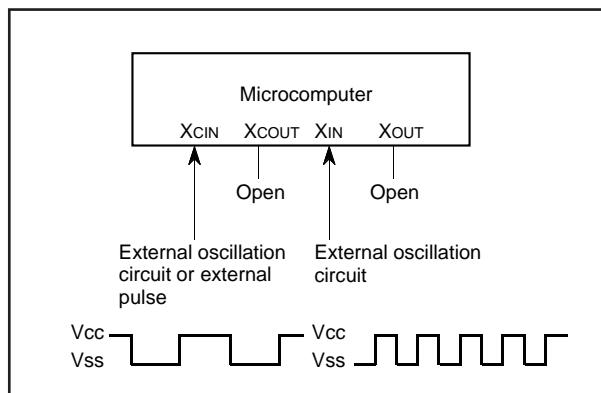


Fig.15.2 External Clock Input Circuit Example

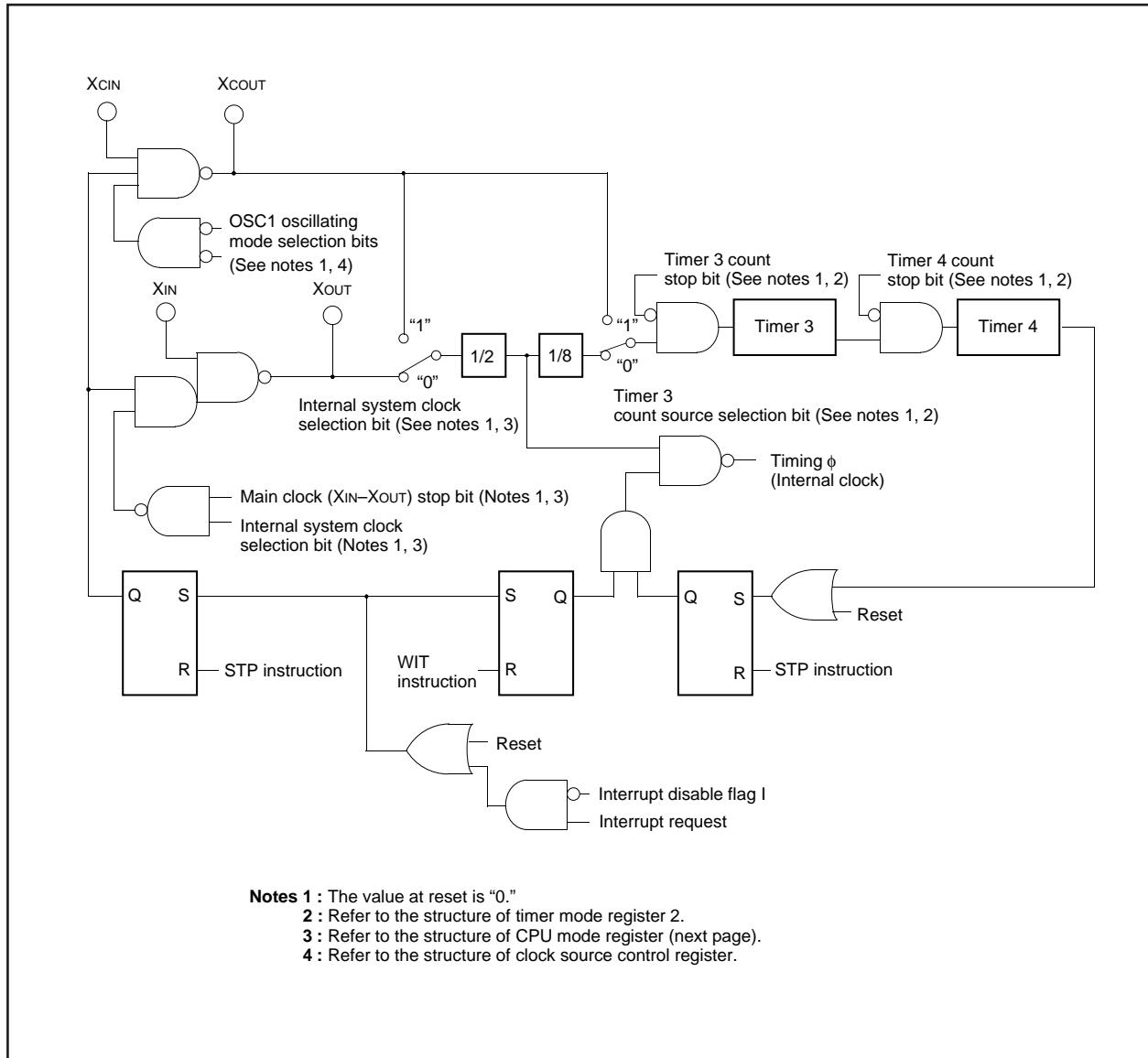
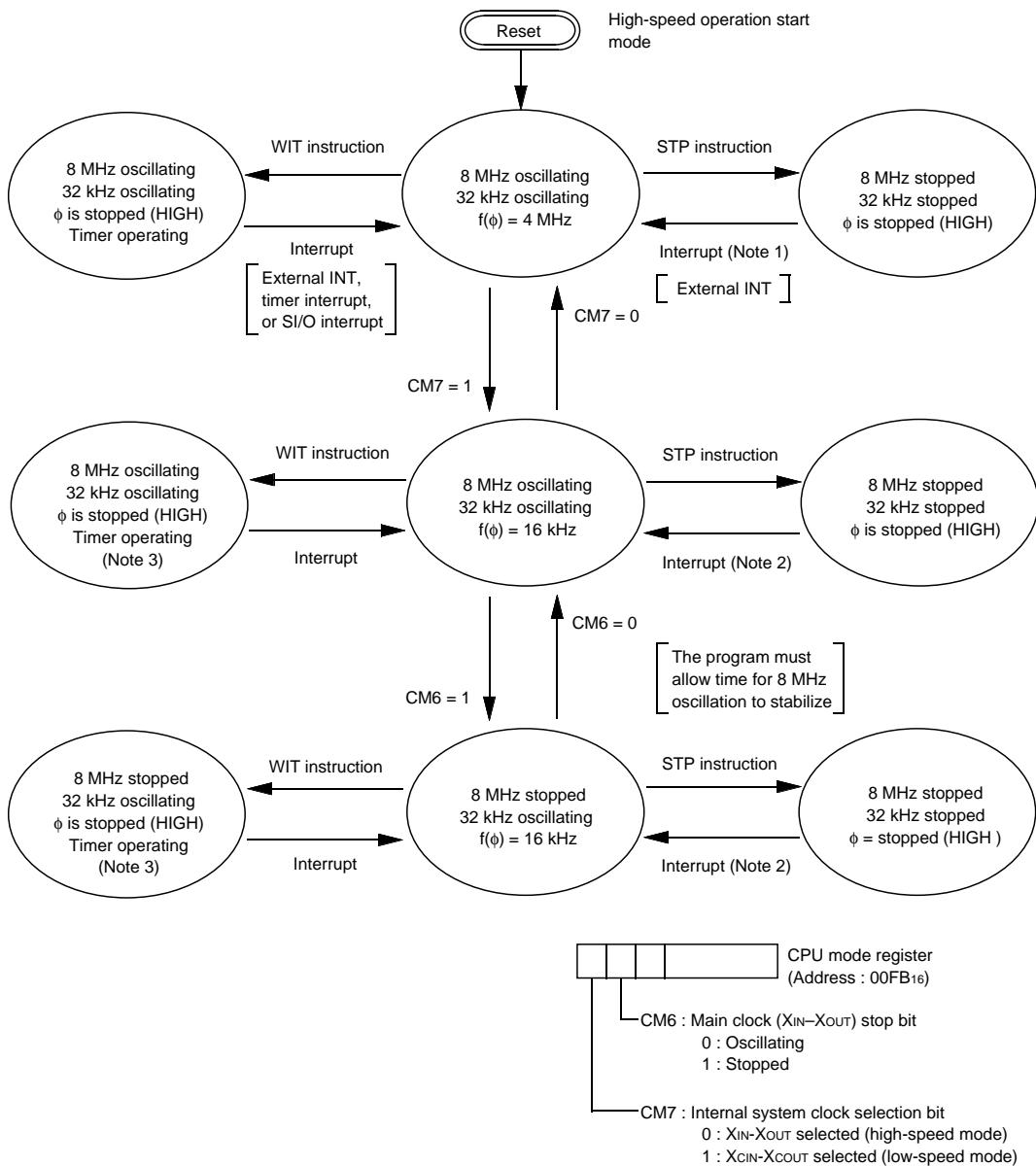


Fig.15.3 Clock Generating Circuit Block Diagram



The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. The ϕ indicates the internal clock.

Notes 1: When the STP state is ended, a delay of approximately 4 ms is automatically generated by timer 3 and timer 4.

2: The delay after the STP state ends is approximately 1 s.

3: When the internal clock ϕ divided by 8 is used as the timer count source, the frequency of the count source is 2 kHz.

Fig.15.4 State Transitions of System Clock

16. DISPLAY OSCILLATION CIRCUIT

The OSD oscillation circuit has a built-in clock oscillation circuits, so that a clock for OSD can be obtained simply by connecting an LC, a ceramic resonator, or a quartz-crystal oscillator across the pins OSC1 and OSC2. Which of the sub-clock or the OSD oscillation circuit is selected by setting bits 5 and 4 of the clock control register (address 021616).

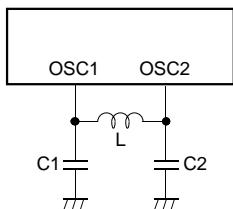


Fig.16.1 Display Oscillation Circuit

17. AUTO-CLEAR CIRCUIT

When a power source is supplied, the auto-clear function will operate by connecting the following circuit to the RESET pin.

18. ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to SERIES 740 <Software> User's Manual for details.

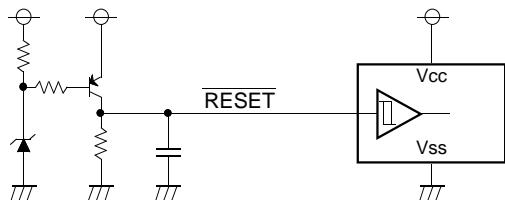
19. MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to SERIES 740 <Software> User's Manual for details.

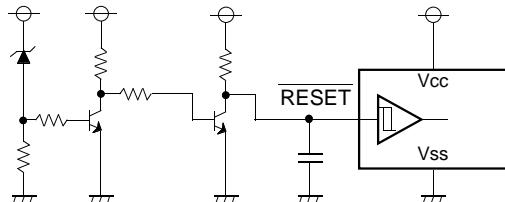
20. PROGRAMMING NOTES

- The divide ratio of the timer is $1/(n+1)$.
- Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- After the ADC and SBC instructions are executed (in the decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.
- An NOP instruction is needed immediately after the execution of a PLP instruction.
- In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu\text{F}$) directly between the Vcc pin–Vss pin, AVcc pin–Vss pin, and the Vcc pin–CNVss pin, using a thick wire.

Circuit example 1



Circuit example 2



Note : Make the level change from "L" to "H" at the point at which the power source voltage exceeds the specified voltage.

Fig.17.1 Auto-clear Circuit Example

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PRELIMINARY
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21. ABSOLUTE MAXIMUM RATINGS

Symbol	Parametear	Conditions	Ratings	Unit
Vcc, AVCC	Power source voltage Vcc, AVCC		-0.3 to 6	V
VI	Input voltage CNVss		-0.3 to 6	V
VI	Input voltage P00-P07, P10-P17, P20-P27, P30, P31, P40-P46, P64, P63, P70-P72, XIN, HSYNC, VSYNC, RESET	All voltages are based on Vss. Output transistors are cut off.	-0.3 to Vcc + 0.3	V
VO	Output voltage P03, P10-P17, P20-P27, P30-P32, P47, P51-P57, P60-P62, P65-P67, SOUT, SCLK, XOUT, OSC2		-0.3 to Vcc + 0.3	V
VO	Output voltage P00-P02, P04-P07, P50		-0.3 to 13	V
IOH	Circuit current P52-P55, P10, P03, P15-P17, P20-P27, P30, P31		0 to 1 (See note 1)	mA
IOL1	Circuit current P52-P57, P10, P03, P15-P17, P20-P27, P65-P67, SOUT, SCLK		0 to 2 (See note 2)	mA
IOL2	Circuit current P11-P14		0 to 6 (See note 2)	mA
IOL3	Circuit current P00-P02, P04-P07, P32, P47, P50 P51, P60-P62		0 to 1 (See note 2)	mA
IOL4	Circuit current P30, P31		0 to 10 (See note 3)	mA
Pd	Power dissipation	Ta = 25 °C	550	mW
Topr	Operating temperature		-10 to 70	°C
Tstg	Storage temperature		-40 to 125	°C

22. RECOMMENDED OPERATING CONDITIONS (Ta = -10 °C to 70 °C, Vcc = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vcc, AVCC	Power source voltage (See note 4), During CPU, OSD, data slicer operation	4.5	5.0	5.5	V
Vcc, AVCC	RAM hold voltage (when clock is stopped)	2.0		5.5	V
Vss	Power source voltage	0	0	0	V
VIH1	HIGH input voltage P00-P07, P10-P17, P20-P27, P30, P31, P40-P46, P63, P64, P70-P72, HSYNC, VSYNC, RESET, XIN	0.8VCC		Vcc	V
VIH2	HIGH input voltage SCL1, SCL2, SDA1, SDA2	0.7VCC		Vcc	V
VIL1	LOW input voltage P00-P07, P10-P17, P20-P27, P30, P31, P40-P46, P63, P64, P70-P72	0		0.4 Vcc	V
VIL2	LOW input voltage SCL1, SCL2, SDA1, SDA2	0		0.3 Vcc	V
VIL3	LOW input voltage (See note 6) RESET, XIN, OSC1, HSYNC, VSYNC, INT1, INT2, INT3, TIM2, TIM3, SCLK, SIN	0		0.2 Vcc	V
IOH	HIGH average output current (See note 1) P52-P55, P10, P03, P15-P17, P20-P27, P30, P31			1	mA
IOL1	LOW average output current (See note 2) P51-P57, P10, P03, P15-P17, P20-P27, SOUT, SCLK, P47, P65-P67			2	mA
IOL2	LOW average output current (See note 2) P11-P14			6	mA
IOL3	LOW average output current (See note 2) P00-P02, P04-P07, P32, P47, P50, P51, P60-P62			1	mA
IOL4	LOW average output current (See note 3) P30, P31			10	mA
f(XIN)	Oscillation frequency (for CPU operation) (See note 5) XIN	7.9	8.0	8.1	MHz
f(XCIN)	Oscillation frequency (for sub-clock operation) XCIN	29	32	35	kHz
fosc	Oscillation frequency (for OSD) OSC1	LC oscillating mode	11.0		27.0
		Ceramic oscillating mode	25.5	26.5	27.5
RL	Load resistance During R,G,B analog output	20.0			
fhs1	Input frequency TIM2, TIM3, INT1, INT2, INT3			100	kHz
fhs2	Input frequency SCLK			1	MHz
fhs3	Input frequency SCL1, SCL2			400	kHz
fhs4	Input frequency Horizontal sync. signal of video signal	15.262	15.734	16.206	kHz
VI	Input amplitude video signal CVIN	1.5	2.0	2.5	V

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
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23. ELECTRIC CHARACTERISTICS (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(XIN) = 8 MHz, T_a = -10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	Test circuit	
			Min.	Typ.	Max.			
ICC	Power source current	System operation	V _{CC} = 5.5 V, f(XIN) = 8 MHz	CRT OFF Data slicer OFF		15	30	1
				CRT ON (digital output) Data slicer ON		30	50	
				CRT ON (analog output) Data slicer ON		50	70	
			V _{CC} = 5.5 V, f(XIN) = 0, f(XCIN) = 32 kHz, OSD OFF, Data slicer OFF, Low-power dissipation mode set (CM5 = "0", CM6 = "1")			60	200	
		Wait mode	V _{CC} = 5.5 V, f(XIN) = 8 MHz			2	4	
			V _{CC} = 5.5 V, f(XIN) = 0, f(XCIN) = 32 kHz, Low-power dissipation mode set (CM5 = "0", CM6 = "1")			25	100	
		Stop mode	V _{CC} = 5.5 V, f(XIN) = 0 f(XCIN) = 0			1	10	
VOH	HIGH output voltage	P52-P55, P10, P03, P15-P17, P20-P27, P30, P31	V _{CC} = 4.5 V I _{OH} = -0.5 mA		2.4		V	2
VOL	LOW output voltage	SOUT, SCLK, P00-P07, P10, P15-P17, P20-P27, P32, P47, P50-P57, P60-P62, P65-P67	V _{CC} = 4.5 V I _{OL} = 0.5 mA			0.4	V	3
	LOW output voltage	P30, P31	V _{CC} = 4.5 V I _{OL} = 10.0 mA			3.0		
	LOW output voltage	P11-P14	V _{CC} = 4.5 V	I _{OL} = 3 mA		0.4		
VT+ - VT-	Hysteresis (See note 6)		V _{CC} = 5.0 V		0.5	1.3	V	4
	RESET, HSYNC, VSYNC, INT1, INT2, INT3, TIM2, TIM3, S _{IN} , SCLK, SCL1, SCL2, SDA1, SDA2							
I _{IZH}	HIGH input leak current	RESET, P03, P10-P17, P20-P27, P30, P31, P40-P46, P63, P64, P70-P72, HSYNC, VSYNC	V _{CC} = 5.5 V V _I = 5.5 V			5	μA	5
I _{IZL}	LOW input leak current	RESET, P00-P07, P10-P17, P20-P27, P30, P31, P40-P46, P63, P64, P70-P72, HSYNC, VSYNC	V _{CC} = 5.5 V V _I = 0 V			5	mA	
O _{ZH}	HIGH input leak current	P00-P02, P04-P07, P50	V _{CC} = 5.5 V V _I = 12 V			10	μA	6
R _{BS}	I ² C-BUS-BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		V _{CC} = 4.5 V			130	Ω	

Notes 1: The total current that flows out of the IC must be 20 or less.

2: The total input current to IC (I_{OL1} + I_{OL2} + I_{OL3}) must be 20 mA or less.

3: The total average input current for ports P30, P31 to IC must be 10 mA or less.

4: Connect 0.1 μF or more capacitor externally between the power source pins V_{CC}-V_{SS} and AV_{CC}-V_{SS} so as to reduce power source noise.

Also connect 0.1 μF or more capacitor externally between the pins V_{CC}-CNV_{SS}.

5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8 MHz.

6: P16, P41-P44 have the hysteresis when these pins are used as interrupt input pins or timer input pins. P11-P14 have the hysteresis when these pins are used as multi-master I²C-BUS interface ports. P17, P46 and P72 have the hysteresis when these pins are used as serial I/O pins.

7: When using the sub-clock, set f_{CLK} < f_{CPU}/3.

8: Pin names in each parameter is described as below.

(1) Dedicated pins: dedicated pin names.

(2) Double-/triple-function ports

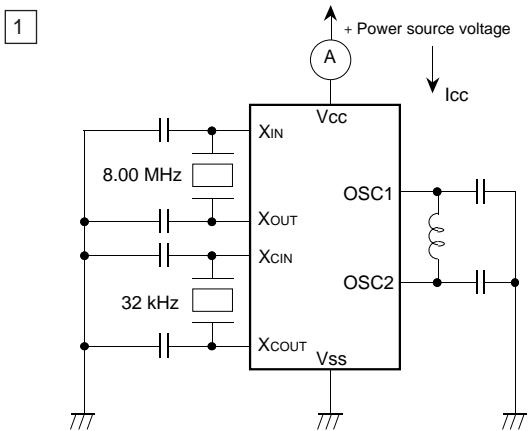
- When the same limits: I/O port name.

- When the limits of functions except ports are different from I/O port limits: function pin name.

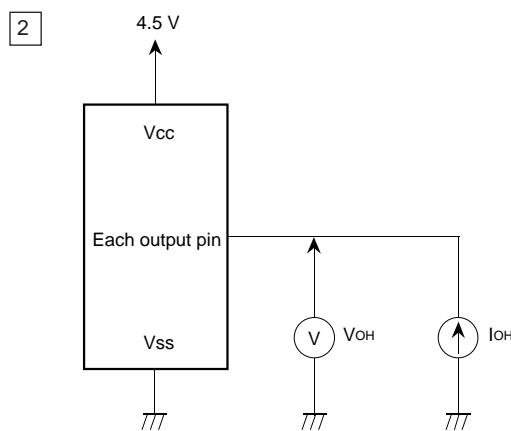
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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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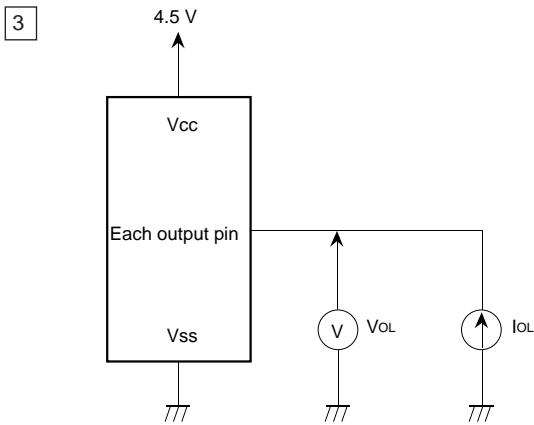
PRELIMINARY
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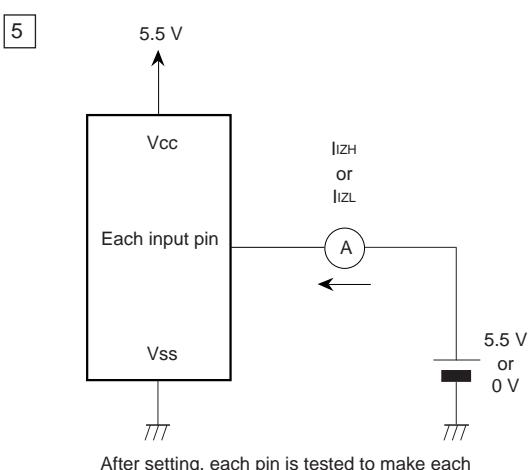
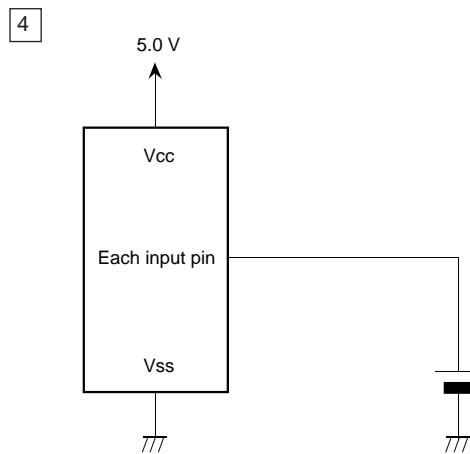
Pin V_{cc} is confirmed the operation and tested the current with a ceramic resonator.



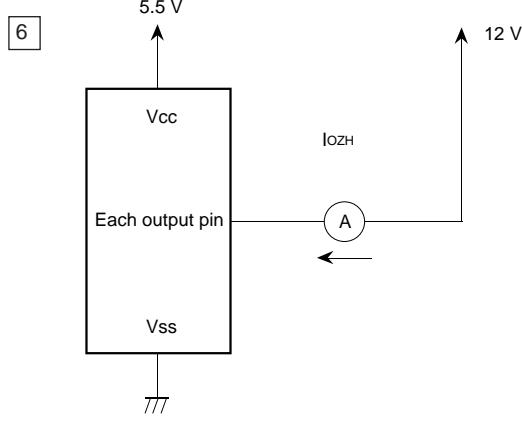
After setting, each pin is tested to make each output pin OFF.



After setting, each pin is tested to make each output pin OFF.



After setting, each pin is tested to make each output pin OFF.



After setting, each pin is tested to make each output pin OFF.

Fig.23.1 Test circuit

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

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PRELIMINARY
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24. ANALOG R, G, B OUTPUT CHARACTERISTICS

($V_{CC} = 5 V \pm 10\%$, $V_{SS} = 0 V$, $f(XIN) = 8 \text{ MHz}$, $T_a = -10^\circ\text{C}$ to 70°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
R_O	Output resistance	$V_{CC} = 4.5 V$			2	$k\Omega$
V_{OE}	Output deviation	$V_{CC} = 5.5 V$			± 0.5	V
T_{ST}	Settling time	$V_{CC} = 4.5 V$, load capacity of 10 pF, load resistor of 20 $k\Omega$, 70 % DC level			50	ns

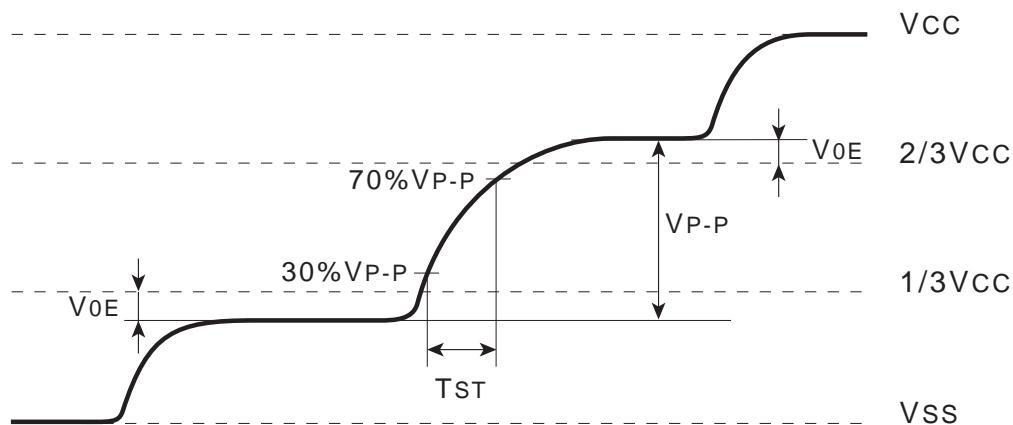


Fig.24.1 Analog R, G, B, Output Characteristics

25. A-D CONVERTER CHARACTERISTICS

($V_{CC} = 5 V \pm 10\%$, $V_{SS} = 0 V$, $f(XIN) = 8 \text{ MHz}$, $T_a = -10^\circ\text{C}$ to 70°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Absolute accuracy (excluding quantization error)	$V_{CC} = 5 V$			± 2.5	LSB
T_{CONV}	Conversion time		12.25		12.5	μs
R_{LADDER}	Ladder resistor			25		$k\Omega$
V_{IA}	Analog input voltage		0		V_{REF}	V

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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26. MULTI-MASTER I²C-BUS BUS LINE CHARACTERISTICS

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
tBUF	Bus free time	4.7		1.3		μs
tHD; STA	Hold time for START condition	4.0		0.6		μs
tLOW	LOW period of SCL clock	4.7		1.3		μs
tR	Rising time of both SCL and SDA signals		1000	20+0.1Cb	300	ns
tHD; DAT	Data hold time	0		0	0.9	μs
tHIGH	HIGH period of SCL clock	4.0		0.6		μs
tF	Falling time of both SCL and SDA signals		300	20+0.1Cb	300	ns
tsU; DAT	Data set-up time	250		100		ns
tsU; STA	Set-up time for repeated START condition	4.7		0.6		μs
tsU; STO	Set-up time for STOP condition	4.0		0.6		μs

Note: C_b = total capacitance of 1 bus line

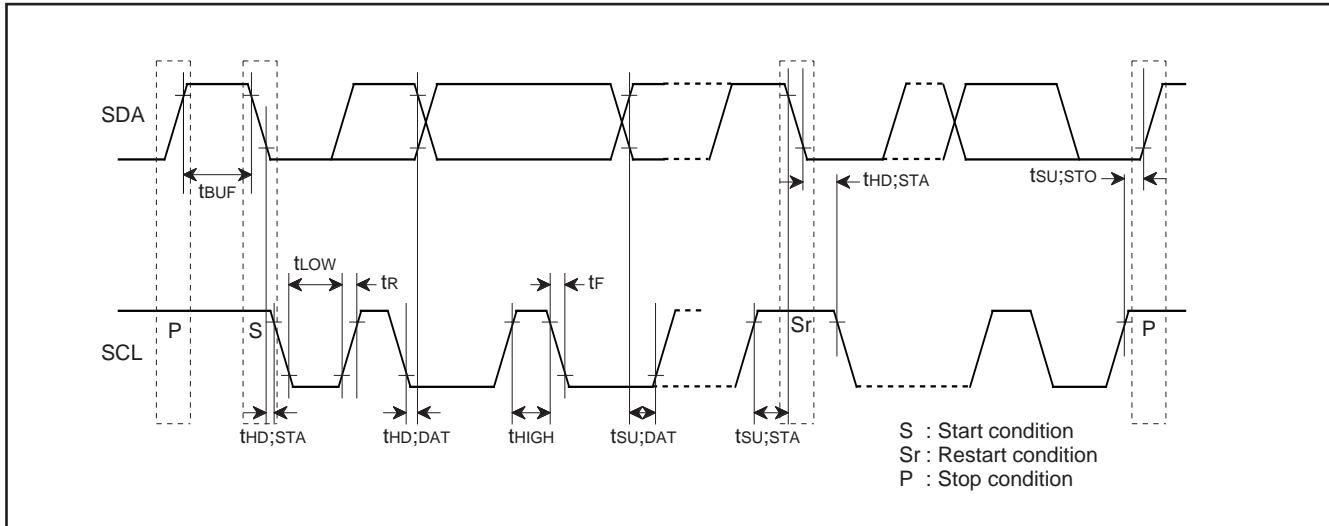


Fig.26.1 Definition Diagram of Timing on Multi-master I²C-BUS

27. DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- Mask ROM Order Confirmation Form
- Mark Specification Form
- Data to be written to ROM, in EPROM form (32-pin DIP Type 27C101, three identical copies) or FDK

28. PROM PROGRAMMING METHOD

The built-in PROM of the One Time PROM version (blank) and the built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37280EKSP	PCA7401

The PROM of the One Time PROM version (blank) is not tested or screened in the assembly process nor any following processes. To ensure proper operation after programming, the procedure shown in Figure 29.1 is recommended to verify programming.

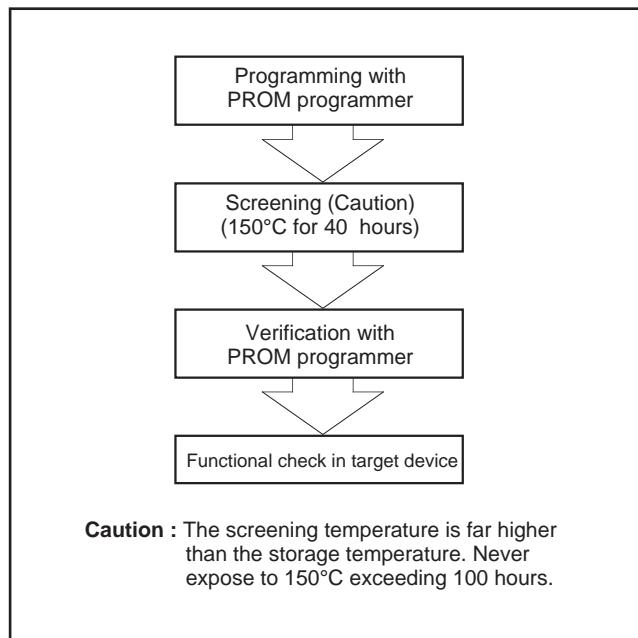


Fig. 29.1 Programming and Testing of One Time PROM Version

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
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29. MASK CONFIRMATION FORM

GZZ-SH52-83B < 84A0 >

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37280MK-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
Receipt	Date :
	Section head signature

Note : Please fill in all items marked *.

* Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

*1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

--	--	--

(hexadecimal notation)

EPROM type (indicate the type used)

<input type="checkbox"/> 27C101	
EPROM address	
00000 ₁₆	Product name ASCII code : 'M37280MK'
0000F ₁₆	
01000 ₁₆	Program ROM 60 K bytes
0FFFF ₁₆	
10800 ₁₆	OSD ROM
157FF ₁₆	
18000 ₁₆	OSD ROM
1ACFF ₁₆	
1B000 ₁₆	Expansion ROM (20K bytes)
1FFFF ₁₆	

(1) Set "FF₁₆" in the shaded area.

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M37280MF-XXXSP, M37280MK-XXXSP

M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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GZZ-SH52-83B < 84A0 >

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37280MK-XXXSP MITSUBISHI ELECTRIC

(2) Write the ASCII codes that indicate the product name of "M37280MK—" to addresses 00000₁₆ to 0000F₁₆.

Addresses 00000₁₆ to 0000F₁₆ store the product name.

ASCII codes 'M37280MK-' are listed on the right.

The addresses and data are in hexadecimal notation.

address and data are described in hexadecimal notation.

Note: If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Please make sure the data is written correctly.

Address	Address
00000 ₁₆	'M' = 4 D ₁₆
00001 ₁₆	'3' = 3 3 ₁₆
00002 ₁₆	'7' = 3 7 ₁₆
00003 ₁₆	'2' = 3 2 ₁₆
00004 ₁₆	'8' = 3 8 ₁₆
00005 ₁₆	'0' = 3 0 ₁₆
00006 ₁₆	'M' = 4 D ₁₆
00007 ₁₆	'K' = 4 B ₁₆
	'-' = 2 D ₁₆
	FF ₁₆
	FF ₁₆
	FF ₁₆
	FF ₁₆
	FF ₁₆
	FF ₁₆
	FF ₁₆
	FF ₁₆

*2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered. Fill the appropriate mark specification form (64P4B for M37280MK-XXXSP) and attach to the mask ROM confirmation form.

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Rev. 1.0

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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GZZ-SH52-83B < 84A0 >

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37280MK-XXXSP MITSUBISHI ELECTRIC

Note: Input "FF₁₆" to the following addresses in OSD ROM

109FE ₁₆ to 10A0116	1803E ₁₆ to 1804116	1903E ₁₆ to 1904116	1A03E ₁₆ to 1A04116
10DFE ₁₆ to 10E0116	180BE ₁₆ to 180C116	190BE ₁₆ to 190C116	1A0BE ₁₆ to 1A0C116
111FE ₁₆ to 1120116	1813E ₁₆ to 1814116	1913E ₁₆ to 1914116	1A13E ₁₆ to 1A14116
115FE ₁₆ to 1160116	181BE ₁₆ to 181C116	191BE ₁₆ to 191C116	1A1BE ₁₆ to 1A1C116
119FE ₁₆ to 11A0116	1823E ₁₆ to 1824116	1923E ₁₆ to 1924116	1A23E ₁₆ to 1A24116
11DFE ₁₆ to 11E0116	182BE ₁₆ to 182C116	192BE ₁₆ to 192C116	1A2BE ₁₆ to 1A2C116
121FE ₁₆ to 1220116	1833E ₁₆ to 1834116	1933E ₁₆ to 1934116	1A33E ₁₆ to 1A34116
125FE ₁₆ to 1260116	183BE ₁₆ to 183C116	193BE ₁₆ to 193C116	1A3BE ₁₆ to 1A3C116
129FE ₁₆ to 12A0116	1843E ₁₆ to 1844116	1943E ₁₆ to 1944116	1A43E ₁₆ to 1A44116
12DFE ₁₆ to 12E0116	184BE ₁₆ to 184C116	194BE ₁₆ to 194C116	1A4BE ₁₆ to 1A4C116
131FE ₁₆ to 1320116	1853E ₁₆ to 1854116	1953E ₁₆ to 1954116	1A53E ₁₆ to 1A54116
135FE ₁₆ to 1360116	185BE ₁₆ to 185C116	195BE ₁₆ to 195C116	1A5BE ₁₆ to 1A5C116
139FE ₁₆ to 13A0116	1863E ₁₆ to 1864116	1963E ₁₆ to 1964116	1A63E ₁₆ to 1A64116
13DFE ₁₆ to 13E0116	186BE ₁₆ to 186C116	196BE ₁₆ to 196C116	1A6BE ₁₆ to 1A6C116
141FE ₁₆ to 1420116	1873E ₁₆ to 1874116	1973E ₁₆ to 1974116	1A73E ₁₆ to 1A74116
145FE ₁₆ to 1460116	187BE ₁₆ to 187C116	197BE ₁₆ to 197C116	1A7BE ₁₆ to 1A7C116
149FE ₁₆ to 14A0116	1883E ₁₆ to 1884116	1983E ₁₆ to 1984116	1A83E ₁₆ to 1A84116
14DFE ₁₆ to 14E0116	188BE ₁₆ to 188C116	198BE ₁₆ to 198C116	1A8BE ₁₆ to 1A8C116
151FE ₁₆ to 1520116	1893E ₁₆ to 1894116	1993E ₁₆ to 1994116	1A93E ₁₆ to 1A94116
155FE ₁₆ to 1560116	189BE ₁₆ to 189C116	199BE ₁₆ to 199C116	1A9BE ₁₆ to 1A9C116
1580016 to 17FFF ₁₆	18A3E ₁₆ to 18A4116	19A3E ₁₆ to 19A4116	1AA3E ₁₆ to 1AA4116
	18ABE ₁₆ to 18AC116	19ABE ₁₆ to 19AC116	1AABE ₁₆ to 1AAC116
	18B3E ₁₆ to 18B4116	19B3E ₁₆ to 19B4116	1AB3E ₁₆ to 1AB4116
	18BBE ₁₆ to 18BC116	19BBE ₁₆ to 19BC116	1ABBE ₁₆ to 1ABC116
	18C3E ₁₆ to 18C4116	19C3E ₁₆ to 19C4116	1AC3E ₁₆ to 1AC4116
	18CBE ₁₆ to 18CC116	19CBE ₁₆ to 19CC116	1ACBE ₁₆ to 1ACC116
	18D0016 to 18FFF ₁₆	19D0016 to 19FFF ₁₆	

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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GZZ-SH52-84B < 84A0 >

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37280MF-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
Receipt	Date :
	Section head signature

Note : Please fill in all items marked *.

* Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

*1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

--	--	--

(hexadecimal notation)

EPROM type (indicate the type used)

<input type="checkbox"/> 27C101	
EPROM address	
00000 ₁₆	Product name ASCII code : 'M37280MF'
0000F ₁₆	
01000 ₁₆	Program ROM 60 K bytes
0FFF ₁₆	
10800 ₁₆	OSD ROM
157FF ₁₆	
18000 ₁₆	OSD ROM
1ACFF ₁₆	
1FFFF ₁₆	

(1) Set "FF₁₆" in the shaded area.

(1/3)

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH52-84B < 84A0 >

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37280MF-XXXSP MITSUBISHI ELECTRIC

(2) Write the ASCII codes that indicate the product name of "M37280MF—" to addresses 00000₁₆ to 0000F₁₆.

Addresses 00000₁₆ to 0000F₁₆ store the product name.

ASCII codes 'M37280MF-' are listed on the right.

The addresses and data are in hexadecimal notation.

address and data are described in hexadecimal notation.

Note: If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Please make sure the data is written correctly.

Address	Address
00000 ₁₆	'M' = 4 D ₁₆
00001 ₁₆	'3' = 3 3 ₁₆
00002 ₁₆	'7' = 3 7 ₁₆
00003 ₁₆	'2' = 3 2 ₁₆
00004 ₁₆	'8' = 3 8 ₁₆
00005 ₁₆	'0' = 3 0 ₁₆
00006 ₁₆	'M' = 4 D ₁₆
00007 ₁₆	'F' = 4 6 ₁₆
00008 ₁₆	'-' = 2 D ₁₆
00009 ₁₆	FF ₁₆
0000A ₁₆	FF ₁₆
0000B ₁₆	FF ₁₆
0000C ₁₆	FF ₁₆
0000D ₁₆	FF ₁₆
0000E ₁₆	FF ₁₆
0000F ₁₆	FF ₁₆

*2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered. Fill the appropriate mark specification form (64P4B for M37280MF-XXXSP) and attach to the mask ROM confirmation form.

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M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ-SH52-84B < 84A0 >

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37280MF-XXXSP MITSUBISHI ELECTRIC

Note: Input "FF₁₆" to the following addresses in OSD ROM

109FE ₁₆ to 10A0116	1803E ₁₆ to 1804116	1903E ₁₆ to 1904116	1A03E ₁₆ to 1A04116
10DFE ₁₆ to 10E0116	180BE ₁₆ to 180C116	190BE ₁₆ to 190C116	1A0BE ₁₆ to 1A0C116
111FE ₁₆ to 1120116	1813E ₁₆ to 1814116	1913E ₁₆ to 1914116	1A13E ₁₆ to 1A14116
115FE ₁₆ to 1160116	181BE ₁₆ to 181C116	191BE ₁₆ to 191C116	1A1BE ₁₆ to 1A1C116
119FE ₁₆ to 11A0116	1823E ₁₆ to 1824116	1923E ₁₆ to 1924116	1A23E ₁₆ to 1A24116
11DFE ₁₆ to 11E0116	182BE ₁₆ to 182C116	192BE ₁₆ to 192C116	1A2BE ₁₆ to 1A2C116
121FE ₁₆ to 1220116	1833E ₁₆ to 1834116	1933E ₁₆ to 1934116	1A33E ₁₆ to 1A34116
125FE ₁₆ to 1260116	183BE ₁₆ to 183C116	193BE ₁₆ to 193C116	1A3BE ₁₆ to 1A3C116
129FE ₁₆ to 12A0116	1843E ₁₆ to 1844116	1943E ₁₆ to 1944116	1A43E ₁₆ to 1A44116
12DFE ₁₆ to 12E0116	184BE ₁₆ to 184C116	194BE ₁₆ to 194C116	1A4BE ₁₆ to 1A4C116
131FE ₁₆ to 1320116	1853E ₁₆ to 1854116	1953E ₁₆ to 1954116	1A53E ₁₆ to 1A54116
135FE ₁₆ to 1360116	185BE ₁₆ to 185C116	195BE ₁₆ to 195C116	1A5BE ₁₆ to 1A5C116
139FE ₁₆ to 13A0116	1863E ₁₆ to 1864116	1963E ₁₆ to 1964116	1A63E ₁₆ to 1A64116
13DFE ₁₆ to 13E0116	186BE ₁₆ to 186C116	196BE ₁₆ to 196C116	1A6BE ₁₆ to 1A6C116
141FE ₁₆ to 1420116	1873E ₁₆ to 1874116	1973E ₁₆ to 1974116	1A73E ₁₆ to 1A74116
145FE ₁₆ to 1460116	187BE ₁₆ to 187C116	197BE ₁₆ to 197C116	1A7BE ₁₆ to 1A7C116
149FE ₁₆ to 14A0116	1883E ₁₆ to 1884116	1983E ₁₆ to 1984116	1A83E ₁₆ to 1A84116
14DFE ₁₆ to 14E0116	188BE ₁₆ to 188C116	198BE ₁₆ to 198C116	1A8BE ₁₆ to 1A8C116
151FE ₁₆ to 1520116	1893E ₁₆ to 1894116	1993E ₁₆ to 1994116	1A93E ₁₆ to 1A94116
155FE ₁₆ to 1560116	189BE ₁₆ to 189C116	199BE ₁₆ to 199C116	1A9BE ₁₆ to 1A9C116
1580016 to 17FFF16	18A3E ₁₆ to 18A4116	19A3E ₁₆ to 19A4116	1AA3E ₁₆ to 1AA4116
	18ABE ₁₆ to 18AC116	19ABE ₁₆ to 19AC116	1AABE ₁₆ to 1AAC116
	18B3E ₁₆ to 18B4116	19B3E ₁₆ to 19B4116	1AB3E ₁₆ to 1AB4116
	18BBE ₁₆ to 18BC116	19BBE ₁₆ to 19BC116	1ABBE ₁₆ to 1ABC116
	18C3E ₁₆ to 18C4116	19C3E ₁₆ to 19C4116	1AC3E ₁₆ to 1AC4116
	18CBE ₁₆ to 18CC116	19CBE ₁₆ to 19CC116	1ACBE ₁₆ to 1ACC116
	18D0016 to 18FFF16	19D0016 to 19FFF16	

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M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

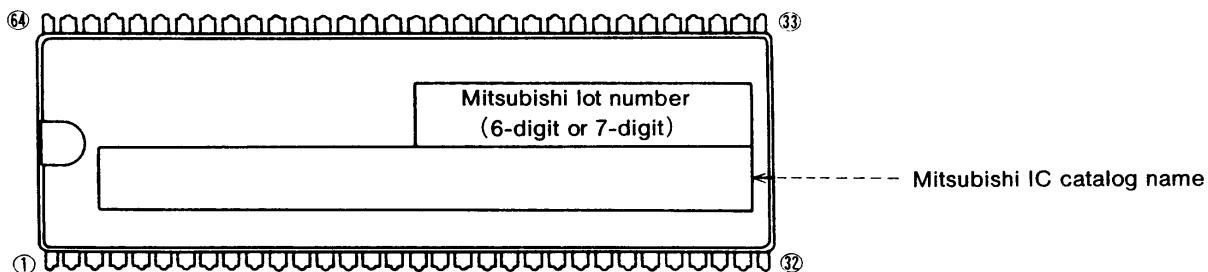
30. MARK SPECIFICATION FORM

64P4B (64-PIN SHRINK DIP) MARK SPECIFICATION FORM

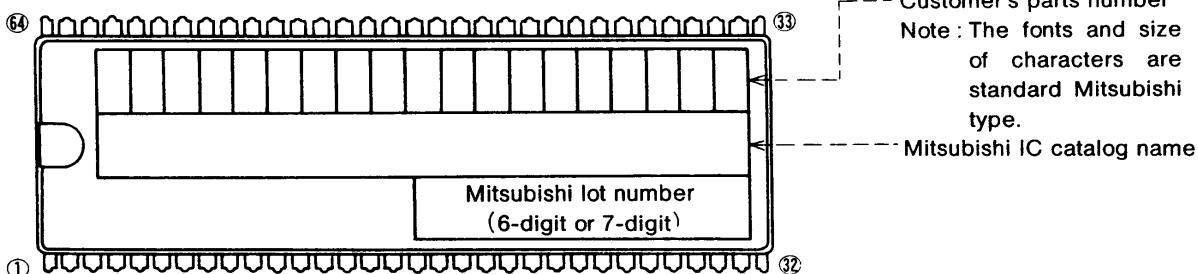
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



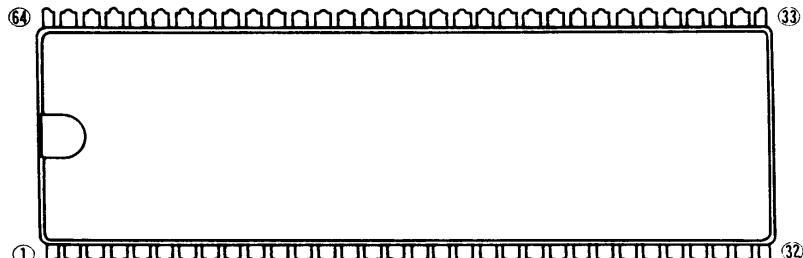
Note1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type.

3 : Customer's parts number can be up to 19 characters :

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

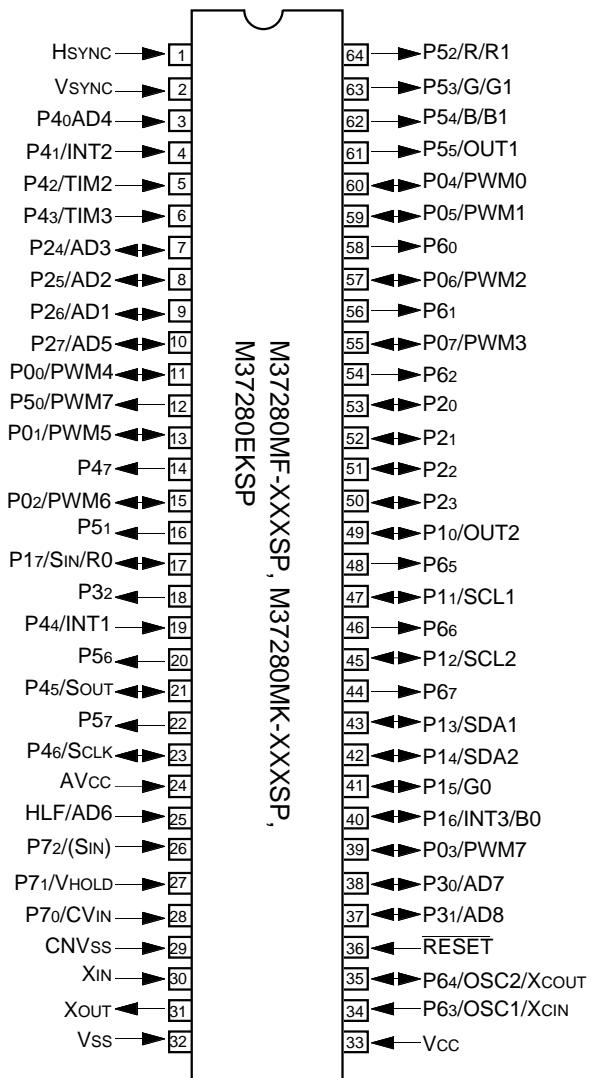
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

31. APPENDIX

Pin Configuration (TOP VIEW)



Outline 64P4B

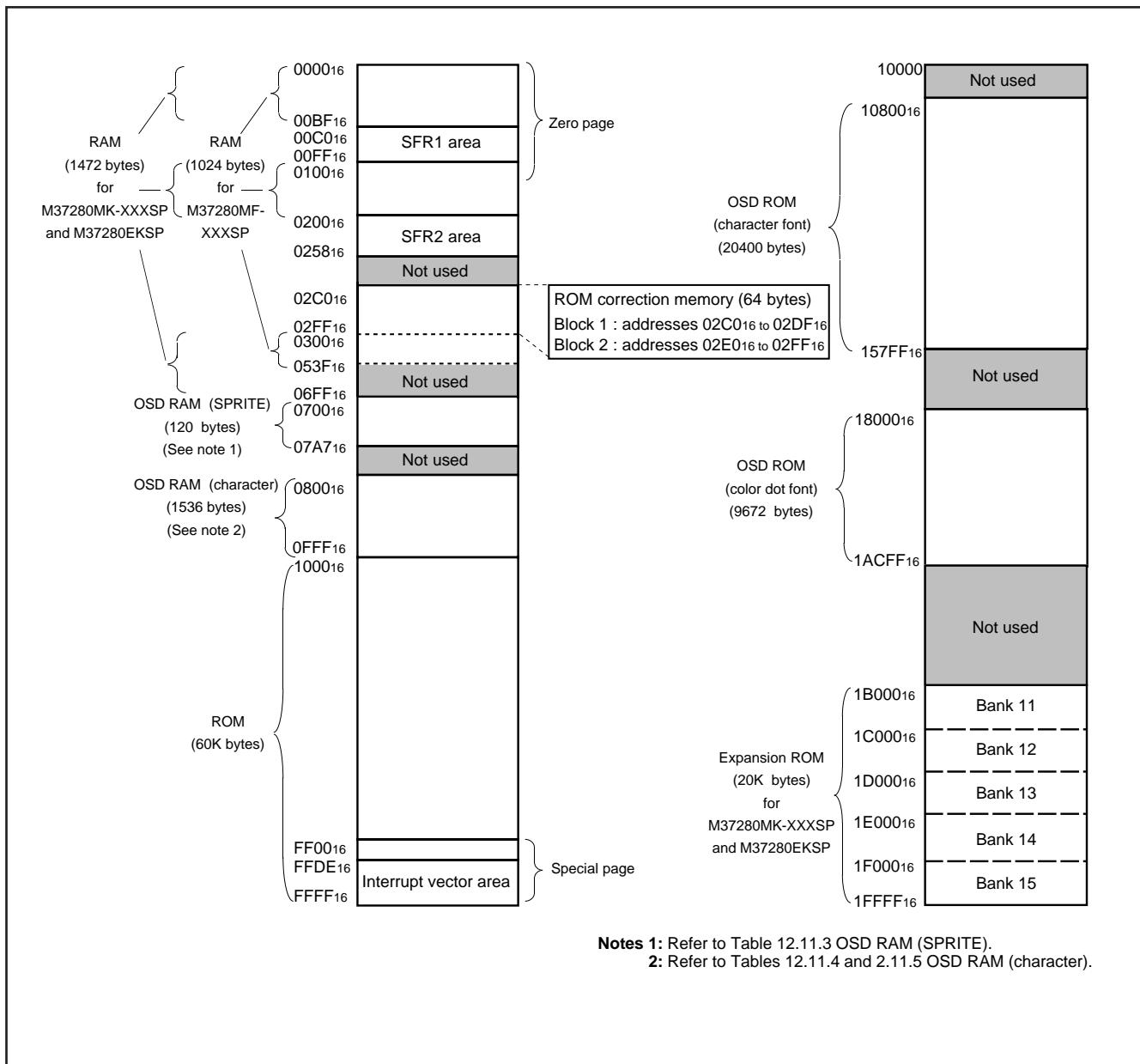
M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY

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Memory Map



Notes 1: Refer to Table 12.11.3 OSD RAM (SPRITE).

2: Refer to Tables 12.11.4 and 2.11.5 OSD RAM (character).

Memory Map of Special Function Register (SFR)

■ SFR1 area (addresses C0₁₆ to DF₁₆)

Bit allocation

: } Function bit
Name : }

-  : No function bit
-  : Fix to this bit to "0"
(do not write to "1")

State immediately after reset

0 : "0" immediately after reset

? : Indeterminate immediately after reset

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY

Notice: This is not a final specification.
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■ SFR1 area (addresses E016 to FF16)

Bit allocation

<input type="checkbox"/>	: Function bit
<input name="" type="checkbox"/>	: No function bit
<input type="checkbox" value="0"/>	: Fix to this bit to "0" (do not write to "1")
<input type="checkbox" value="1"/>	: Fix to this bit to "1" (do not write to "0")

State immediately after reset

<input type="checkbox" value="0"/>	: "0" immediately after reset
<input type="checkbox" value="1"/>	: "1" immediately after reset
<input type="checkbox" value="?"/>	: Indeterminate immediately after reset

Address Register

Address	Register	Bit allocation								State immediately after reset								
		b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0	
E016	Data slicer control register 1 (DSC1)	0	0	0	0	0	DSC12	DSC11	DSC10	?	0	?	0	?	?	0	?	
E116	Data slicer control register 2 (DSC2)	0	DSC25	DSC24	DSC23	0	DSC20			0016								
E216	Caption data register 1 (CD1)	CDL17	CDL16	CDL15	CDL14	CDL13	CDL12	CDL11	CDL10	0016								
E316	Caption data register 2 (CD2)	CDH17	CDH16	CDH15	CDH14	CDH13	CDH12	CDH11	CDH10	0016								
E416	Caption data register 3 (CD3)	CDL27	CDL26	CDL25	CDL24	CDL23	CDL22	CDL21	CDL20	0016								
E516	Caption data register 4 (CD4)	CDH27	CDH26	CDH25	CDH24	CDH23	CDH22	CDH21	CDH20	0016								
E616	Caption Position register (CPS)	CPS7	CPS6	CPS5	CPS4	CPS3	CPS2	CPS1	CPS0	0016								
E716	Data slicer test register 2									0016								
E816	Data slicer test register 1									0016								
E916	Sync signal counter register (HC)			HC5	HC4	HC3	HC2	HC1	HC0	0016								
EA16	Clock run-in detect register (CRD)	CRD7	CRD6	CRD5	CRD4	CRD3				0016								
EB16	Data clock position register (DPS)	DPS7	DPS6	DPS5	DPS4	DPS3	0	0	1	0916								
EC16										?								
ED16	Bank control register (BK)	BK7	BK6	0	0	BK3	BK2	BK1	BK0	0016								
EE16	A-D conversion register (AD)	0	0	ADVREF	ADSTR	ADIN2	ADIN1	ADIN0		0016								
EF16	A-D control register (ADCON)									?								
F016	Timer 1 (T1)									0016								
F116	Timer 2 (T2)									0716								
F216	Timer 3 (T3)									FF16								
F316	Timer 4 (T4)									0716								
F416	Timer mode register 1 (TM1)	TM17	TM16	TM15	TM14	TM13	TM12	TM11	TM10	0016								
F516	Timer mode register 2 (TM2)	TM27	TM26	TM25	TM24	TM23	TM22	TM21	TM20	0016								
F616	I ² C data shift register (S0)	D7	D6	D5	D4	D3	D2	D1	D0	?								
F716	I ² C address register (S0D)	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW	0016								
F816	I ² C status register (S1)	MST	TRX	BB	PIN	AL	AAS	AD0	LRB	0	0	0	1	0	0	0	?	
F916	I ² C control register (S1D)	BSEL1	BSEL0	10BIT	SAD	ALS	ES0	BC2	BC1	BC0	0016							
FA16	I ² C clock control register (S2)	ACK	ACK	FAST	MODE	CCR4	CCR3	CCR2	CCR1	CCR0	0016							
FB16	CPU mode register (CM)	CM7	CM6	CM5	1	1	CM2	0	0	3C16								
FC16	Interrupt request register 1 (IREQ1)	ADR	VSCR	OSDR	TM4R	TM3R	TM2R	TM1R		0016								
FD16	Interrupt request register 2 (IREQ2)	0	TM56R	IICR	IN2R	CKR	SIOR	DSR	IN1R	0016								
FE16	Interrupt control register 1 (ICON1)	ADE	VSCE	OSDE	TM4E	TM3E	TM2E	TM1E		0016								
FF16	Interrupt control register 2 (ICON2)	TM56S	TM56E	IICE	IN2E	CKE	SIOE	DSE	IN1E	0016								

■ SFR2 area (addresses 200₁₆ to 21F₁₆)

Bit allocation

: } Function bit
Name : }

 : No function bit

- 0** : Fix to this bit to "0"
(do not write to "1")
- 1** : Fix to this bit to "1"
(do not write to "0")

State immediately after reset

0 : “0” immediately after reset

1 : “1” immediately after reset

: Indeterminate immediately after reset

Address	Register	Bit allocation								State immediately after reset	
		b7							b0	b7	b0
20016	PWM0 register (PWM0)									?	
20116	PWM1 register (PWM1)									?	
20216	PWM2 register (PWM2)									?	
20316	PWM3 register (PWM3)									?	
20416	PWM4 register (PWM4)									?	
20516	PWM5 register (PWM5)									?	
20616	PWM6 register (PWM6)									?	
20716	PWM7 register (PWM7)									?	
20816										?	
20916										?	
20A16	PWM mode register 1 (PN)			PN4	PN3				PN0		0016
20B16	PWM mode register 2 (PW)	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0		0016
20C16	ROM correction address 1 (high-order)										0016
20D16	ROM correction address 1 (low-order)										0016
20E16	ROM correction address 2 (high-order)										0016
20F16	ROM correction address 2 (low-order)										0016
21016	ROM correction enable register (RCR)			0	0		RCR1	RCR0			0016
21116	Test register	0016									0016
21216	Interrupt input polarity register (IP)	AD/INT3	POL3		POL2	POL1					0016
21316	Serial I/O mode register (SM)	SM6	SM5	SM4	SM3	SM2	SM1	SM0			0016
21416	Serial I/O register (SIO)										?
21516	OSD control register 2(OC2)	OC27	OC26	OC25	OC24	OC23	OC12	OC21	OC20		0016
21616	Clock control register (CS)	0	0	0	0	CS2	CS1	CS0			0016
21716	I/O polarity control register (PC)	PC7	PC6	PC5	PC4	PC2	PC1	PC0			8016
21816	Raster color register (RC)				RC4	RC3	RC2	RC1	RC0		0016
21916	OSD control register 3(OC3)	OC37	OC36	OC35	OC34	OC33	OC32	OC31	OC30		0016
21A16	Timer 5 (TM5)										0716
21B16	Timer 6 (TM6)										FF16
21C16	Top border control register 1 (TB1)	TB17	TB16	TB15	TB14	TB13	TB12	TB11	TB10		?
21D16	Bottom border control register 1 (BB1)	BB17	BB16	BB15	BB14	BB13	BB12	BB11	BB10		?
21E16	Top border control register 1 (TB2)							TB21	TB20		?
21F16	Bottom border control register 1 (BB2)							BB21	BB20		?

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

■ SFR2 area (addresses 220_{16} to $23F_{16}$)

Bit allocation

| | : } Function bit
 | | : }
Name : }

 : No function bit

- 0** : Fix to this bit to "0" (do not write to "1")
- 1** : Fix to this bit to "1" (do not write to "0")

State immediately after reset

0 : “0” immediately after reset

1 : "1" immediately after reset

? : Indeterminate immediately after reset

Address	Register
22016	Vertical position register 1 ₁ (VP1 ₁)
22116	Vertical position register 1 ₂ (VP1 ₂)
22216	Vertical position register 1 ₃ (VP1 ₃)
22316	Vertical position register 1 ₄ (VP1 ₄)
22416	Vertical position register 1 ₅ (VP1 ₅)
22516	Vertical position register 1 ₆ (VP1 ₆)
22616	Vertical position register 1 ₇ (VP1 ₇)
22716	Vertical position register 1 ₈ (VP1 ₈)
22816	Vertical position register 1 ₉ (VP1 ₉)
22916	Vertical position register 1 ₁₀ (VP1 ₁₀)
22A16	Vertical position register 1 ₁₁ (VP1 ₁₁)
22B16	Vertical position register 1 ₁₂ (VP1 ₁₂)
22C16	Vertical position register 1 ₁₃ (VP1 ₁₃)
22D16	Vertical position register 1 ₁₄ (VP1 ₁₄)
22E16	Vertical position register 1 ₁₅ (VP1 ₁₅)
22F16	Vertical position register 1 ₁₆ (VP1 ₁₆)
23016	Vertical position register 2 ₁ (VP2 ₁)
23116	Vertical position register 2 ₂ (VP2 ₂)
23216	Vertical position register 2 ₃ (VP2 ₃)
23316	Vertical position register 2 ₄ (VP2 ₄)
23416	Vertical position register 2 ₅ (VP2 ₅)
23516	Vertical position register 2 ₆ (VP2 ₆)
23616	Vertical position register 2 ₇ (VP2 ₇)
23716	Vertical position register 2 ₈ (VP2 ₈)
23816	Vertical position register 2 ₉ (VP2 ₉)
23916	Vertical position register 2 ₁₀ (VP2 ₁₀)
23A16	Vertical position register 2 ₁₁ (VP2 ₁₁)
23B16	Vertical position register 2 ₁₂ (VP2 ₁₂)
23C16	Vertical position register 2 ₁₃ (VP2 ₁₃)
23D16	Vertical position register 2 ₁₄ (VP2 ₁₄)
23E16	Vertical position register 2 ₁₅ (VP2 ₁₅)
23F16	Vertical position register 2 ₁₆ (VP2 ₁₆)

Bit allocation

State immediately after reset

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

■ SFR2 area (addresses 240₁₆ to 258₁₆)

Bit allocation

 : } Function bit

 : No function bit

 : Fix to this bit to "0"
(do not write to "1")

 : Fix to this bit to "1"
(do not write to "0")

State immediately after reset

 : "0" immediately after reset

 : "1" immediately after reset

 : Indeterminate immediately
after reset

Address Register

240₁₆

241₁₆ Color pallet register 1 (CR1)

242₁₆ Color pallet register 2 (CR2)

243₁₆ Color pallet register 3 (CR3)

244₁₆ Color pallet register 4 (CR4)

245₁₆ Color pallet register 5 (CR5)

246₁₆ Color pallet register 6 (CR6)

247₁₆ Color pallet register 7 (CR7)

248₁₆

249₁₆ Color pallet register 9 (CR9)

24A₁₆ Color pallet register10 (CR10)

24B₁₆ Color pallet register 11 (CR11)

24C₁₆ Color pallet register 12 (CR12)

24D₁₆ Color pallet register 13 (CR13)

24E₁₆ Color pallet register 14 (CR14)

24F₁₆ Color pallet register 15 (CR15)

250₁₆ Left border control register 1 (LB1)

251₁₆ Left border control register 2 (LB2)

252₁₆ Right border control register 1 (RB1)

253₁₆ Right border control register 2 (RB2)

254₁₆ SPRITE vertical position register 1 (VS1)

255₁₆ SPRITE vertical position register 2 (VS2)

256₁₆ SPRITE horizontal position register 1 (HS1)

257₁₆ SPRITE horizontal position register 2 (HS2)

258₁₆ SPRITE OSD control register (SC)

Bit allocation

b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
	CR ₁ 6	CR ₁ 5	CR ₁ 4	CR ₁ 3	CR ₁ 2	CR ₁ 1	CR ₁ 0		?						
	CR ₂ 6	CR ₂ 5	CR ₂ 4	CR ₂ 3	CR ₂ 2	CR ₂ 1	CR ₂ 0		?						
	CR ₃ 6	CR ₃ 5	CR ₃ 4	CR ₃ 3	CR ₃ 2	CR ₃ 1	CR ₃ 0		?						
	CR ₄ 6	CR ₄ 5	CR ₄ 4	CR ₄ 3	CR ₄ 2	CR ₄ 1	CR ₄ 0		?						
	CR ₅ 6	CR ₅ 5	CR ₅ 4	CR ₅ 3	CR ₅ 2	CR ₅ 1	CR ₅ 0		?						
	CR ₆ 6	CR ₆ 5	CR ₆ 4	CR ₆ 3	CR ₆ 2	CR ₆ 1	CR ₆ 0		?						
	CR ₇ 6	CR ₇ 5	CR ₇ 4	CR ₇ 3	CR ₇ 2	CR ₇ 1	CR ₇ 0		?						
	CR ₉ 6	CR ₉ 5	CR ₉ 4	CR ₉ 3	CR ₉ 2	CR ₉ 1	CR ₉ 0		?						
	CR ₁₀ 6	CR ₁₀ 5	CR ₁₀ 4	CR ₁₀ 3	CR ₁₀ 2	CR ₁₀ 1	CR ₁₀ 0		?						
	CR ₁₁ 6	CR ₁₁ 5	CR ₁₁ 4	CR ₁₁ 3	CR ₁₁ 2	CR ₁₁ 1	CR ₁₁ 0		?						
	CR ₁₂ 6	CR ₁₂ 5	CR ₁₂ 4	CR ₁₂ 3	CR ₁₂ 2	CR ₁₂ 1	CR ₁₂ 0		?						
	CR ₁₃ 6	CR ₁₃ 5	CR ₁₃ 4	CR ₁₃ 3	CR ₁₃ 2	CR ₁₃ 1	CR ₁₃ 0		?						
	CR ₁₄ 6	CR ₁₄ 5	CR ₁₄ 4	CR ₁₄ 3	CR ₁₄ 2	CR ₁₄ 1	CR ₁₄ 0		?						
	CR ₁₅ 6	CR ₁₅ 5	CR ₁₅ 4	CR ₁₅ 3	CR ₁₅ 2	CR ₁₅ 1	CR ₁₅ 0		?						
	LB17	LB16	LB15	LB14	LB13	LB12	LB11	LB10	0116						
								LB22	LB21	LB20					
	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	FF16						
								RB22	RB21	RB20					
	VS17	VS16	VS15	VS14	VS13	VS12	VS11	VS10	0716						
								VS21	VS20						
	HS17	HS16	HS15	HS14	HS13	HS12	HS11	HS10	0016						
								HS22	HS21	HS20					
								SC5	SC4	SC3	SC2	SC1	SC0	0016	

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

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PRELIMINARY

Notice: This is not a final specification.
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Internal State of Processor Status Register and Program Counter at Reset

Register	Bit allocation								State immediately after reset												
	b7	N	V	T	B	D	I	Z	C	b0	b7	b0	?	?	?	?	?	?	?	?	
Processor status register (PS)													?	?	?	?	?	?	1	?	?
Program counter (PCH)													Contents of address FFFF ₁₆								
Program counter (PCL)													Contents of address FFFE ₁₆								

Structure of Register

The figure of each register structure describes its functions, contents at reset, and attributes as follows:

<Example>

CPU Mode Register

Values immediately after reset release (Note 1)

Bit attributes (Note 2)

	Name	Functions	After reset	R:W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: 1 0: } Not available 1 1: }	0	R:W
2	Stack page selection bit (See note) (CM2)	0: 0 page 1: 1 page	0	R:W
3, 4	Fix these bits to "1."		1	R:W
5	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is "0."		1	R:W
6, 7	Clock switch bits (CM6, CM7)	b7 b6 0 0: f(XIN) = 8 MHz 0 1: f(XIN) = 12 MHz 1 0: f(XIN) = 16 MHz 1 1: Do not set	0	R:W

■ : Bit in which nothing is assigned

Notes 1: Values immediately after reset release

0 "0" after reset release

1 "1" after reset release

Indeterminate***Indeterminate after reset release

2: Bit attributes*****The attributes of control register bits are classified into 3 types : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

R*****Read

R Read enabled
- Read disabled

W*****Write

W Write enabled
- Write disabled
* "0" can be set by software, but "1" cannot be set.

PRELIMINARY

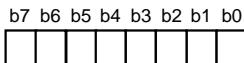
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M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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Address 00C1₁₆, 00C3₁₆, 00C5₁₆

Port Pi Direction Register



Port Pi direction register (Di) (i=0,1,2) [Addresses 00C1₁₆, 00C3₁₆, 00C5₁₆]

B	Name	Functions	After reset	R	W
0	Port Pi direction register	0 : Port Pi ₀ input mode 1 : Port Pi ₀ output mode	0	R	W
1		0 : Port Pi ₁ input mode 1 : Port Pi ₁ output mode	0	R	W
2		0 : Port Pi ₂ input mode 1 : Port Pi ₂ output mode	0	R	W
3		0 : Port Pi ₃ input mode 1 : Port Pi ₃ output mode	0	R	W
4		0 : Port Pi ₄ input mode 1 : Port Pi ₄ output mode	0	R	W
5		0 : Port Pi ₅ input mode 1 : Port Pi ₅ output mode	0	R	W
6		0 : Port Pi ₆ input mode 1 : Port Pi ₆ output mode	0	R	W
7		0 : Port Pi ₇ input mode 1 : Port Pi ₇ output mode	0	R	W

Address 00C7₁₆

Port P3 Direction Register

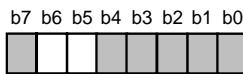


Port P3 direction register (D3) [Address 00C7₁₆]

B	Name	Functions	After reset	R	W
0	Port P3 direction register	0 : Port P3 ₀ input mode 1 : Port P3 ₀ output mode	0	R	W
1		0 : Port P3 ₁ input mode 1 : Port P3 ₁ output mode	0	R	W
2 to 5	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
6	Timer 3 count source selection bit (T3SC)	Refer to Timer section.		0	R
7	Ports P6 ₃ , P6 ₄ selection bits (P6IM)	Refer to clock control register (address 0216 ₁₆).		0	R

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M37280EKSPSINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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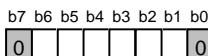
Port P4 Direction Register

Port P3 direction register (D4) [Address 00C7₁₆]

B	Name	Functions	After reset	R	W
0	Fix this bit to "0"		0	R	W
1 to 4	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	W
5	Port P4 direction register	0 : Port P4 ₅ input mode 1 : Port P4 ₅ output mode	0	R	—
		0 : Port P4 ₆ input mode 1 : Port P4 ₇ output mode	0	R	W
7	Nothing is assigned. This bit is write disable bit. When this bit is read out, the values is "0."		0	R	W

Address 00CB₁₆

OSD Port Control Register

OSD port control register (PF) [Address 00CB₁₆]

b	Name	Functions	After reset	R	W
0	Fix this bit to "0"		0	R	W
1	R, G, B output method selection bit (RGB2BIT)	0 : 4-adjustment-level analog is output from pins R, G, B. 1 : Value which is converted from 4-adjustment-level analog to 2-bit digital is output as below: High-order: from R1, G1, B1 Low-order: from R0, G0, B0	0	R	W
2	Port P5 ₂ output signal selection bit (R)	0 : R signal output 1 : Port P5 ₂ output	0	R	W
3	Port P5 ₃ output signal selection bit (G)	0 : G signal output 1 : Port P5 ₃ output	0	R	W
4	Port P5 ₄ output signal selection bit (B)	0 : B signal output 1 : Port P5 ₄ output	0	R	W
5	Port P5 ₅ output signal selection bit (OUT1)	0 : OUT1 signal output 1 : Port P5 ₅ output	0	R	W
6	Port P1 ₀ output signal selection bit (OUT2)	0 : Port P1 ₀ signal output 1 : OUT2 output	0	R	W
7	Fix this bit to "0"		0	R	W

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
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Address 00CE₁₆

OSD Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

OSD control register 1 (OC1) [Address 00CE16]

B	Name	Functions	After reset	R:W
0	OSD control bit (OC10) (See note 1)	0 : All-blocks display off 1 : All-blocks display on	0	R:W
1	Scan mode selection bit (OC11)	0 : Normal scan mode 1 : Bi-scan mode	0	R:W
2	Border type selection bit (OC12)	0 : All bordered 1 : Shadow bordered (See note 2)	0	R:W
3	Flash mode selection bit (OC13)	0 : Color signal of character background part does not flash 1 : Color signal of character background part flashes	0	R:W
4	Automatic solid space control bit (OC14)	0 : OFF 1 : ON	0	R:W
5	Vertical window/blank control bit (OC15)	0 : OFF 1 : ON	0	R:W
6, 7	Layer mixing control bits (OC16, OC17) (See note 3)	b7 b6 0 0: Logic sum (OR) of layer 1's color and layer 2's color 0 1: Layer 1's color has priority 1 0: Layer 2's color has priority 1 1: Do not set.	0	R:W

Notes 1 : Even this bit is switched during display, the display screen remains unchanged until a rising (falling) of the next VSYNC.

2 : Shadow border is output at right and bottom side of the font.

3 : OUT2 is always ORed, regardless of values of these bits.

Address 00CF₁₆

Horizontal Position Register

b7 b6 b5 b4 b3 b2 b1 b0

Horizontal position register (HP) [Address 00CF16]

B	Name	Functions	After reset	R:W
0 to 7	Control bits of horizontal display start positions (HP0 to HP7)	Horizontal display start positions 4Tosc X (setting value of high-order 4 bits $\times 16^1$ + setting value of low-order 4 bits $\times 16^0$)	0	R:W

Notes 1. The setting value synchronizes with the VSYNC.

2. Tosc = OSD oscillation period.

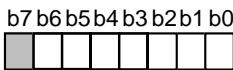
M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
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Address 00D0₁₆ to 00DF₁₆

Block Control Register i



Block control register i (BCi) (i=1 to 16) [Addresses 00D0₁₆ to 00DF₁₆]

B	Name	Functions				After reset	R : W		
0, 1	Display mode selection bits (BCi0, BCi1)	b1	b0	Functions		Indeterminate	R : W		
		0	0	Display OFF					
		0	1	OSD mode					
		1	0	CC mode					
2	Border control bit (BCi2)	0 : Border OFF 1 : Border ON				Indeterminate	R : W		
3, 4	Dot size selection bits (BCi3, BCi4)	b6	b5	b4	b3	Pre-divide ratio	Dot size		
		0	0	0	0	X 1	1Tc X 1/2H		
				0	1		1Tc X 1H		
				1	0		2Tc X 2H		
5, 6	Pre-divide ratio selection bit (BCi5, BCi6)	0	1	1	1	X 2	3Tc X 3H		
				0	0		1Tc X 1/2H		
				0	1		1Tc X 1H		
				1	0		2Tc X 2H		
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.	1	1	1	1	X 3	3Tc X 3H		
				0	0		1.5Tc X 1/2H (See note 3)		
				0	1		1.5Tc X 1H (See note 3)		
				1	0		1Tc X 1/2H		

Notes 1: Tc : OSD clock cycle divided in pre-divide circuit

2: H : HSYNC

3: This character size is available only in Layer 2. At this time, set layer 1's pre-divide ratio = X 2, layer 1's horizontal dot size = 1Tc.

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M37280EKSPSINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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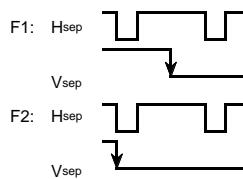
b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 0 0

Data slicer control register 1(DSC1) [Address 00E0₁₆]

B	Name	Functions	After reset	R : W
0	Data slicer and timing signal generating circuit control bit (DSC10)	0: Stopped 1: Operating	0	R : W
1	Selection bit of data slice reference voltage generating field (DSC11)	0: F2 1: F1	0	R : W
2	Reference clock source selection bit (DSC12)	0: Video signal 1: HSYNC signal	0	R : W
3 to 7	Fix these bits to "0."		0	R : W

Definition of fields 1 (F1) and 2 (F2)

Address 00E1₁₆Data Slicer Control Register 2

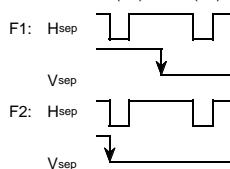
b7 b6 b5 b4 b3 b2 b1 b0

0

Data slicer control register 2 (DSC2) [Address 00E1₁₆]

B	Name	Functions	After reset	R : W
0	Caption data latch completion flag 1 (DSC20)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R : —
1	Fix this bit to "0."		0	R : W
2	Test bit	Read-only	Indeterminate	R : —
3	Field determination flag(DSC23)	0: F2 1: F1	Indeterminate	R : —
4	Vertical synchronous signal (V _{sep}) generating method selection bit (DSC24)	0: Method (1) 1: Method (2)	0	R : W
5	V-pulse shape determination flag (DSC25)	0: Match 1: Mismatch	Indeterminate	R : —
6	Fix this bit to "0."		0	R : W
7	Test bit	Read-only	Indeterminate	R : —

Definition of fields 1 (F1) and 2 (F2)



PRELIMINARY

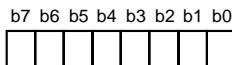
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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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Address 00E6₁₆

Caption Position Register

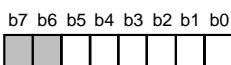


Caption Position Register (CPS) [Address 00E6₁₆]

B	Name	Functions	After reset	R	W
0 to 4	Caption position bits(CPS0 to CPS4)		0	R	W
5	Caption data latch completion flag 2 (CPS5)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	—
6, 7	Slice line mode specification bits (in 1 field) (CPS6, CPS7)	Refer to the corresponding Table (Table 12.10.1).	0	R	W

Address 00E9₁₆

Sync Pulse Counter Register

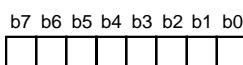


Sync pulse counter register (HC) [Address 00E9₁₆]

B	Name	Functions	After reset	R	W
0 to 4	Count value (HC0 to HC4)		Indeterminate	R	—
5	Count source (HC5)	0: HSYNC signal 1: Composite sync signal	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Address 00E4₁₆

Clock Run-in Detect Register



Clock run-in detect register (CRD) [Address 00EA₁₆]

B	Name	Functions	After reset	R	W
0 to 2	Test bits	Read-only	0	R	—
3 to 7	Clock run-in detection bit(CRD3 to CRD7)	Number of reference clocks to be counted in one clock run-in pulse period.	0	R	—

PRELIMINARY

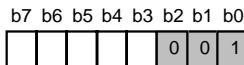
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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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Address 00EB₁₆

Data Clock Position Register

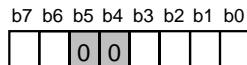


Data clock position register (DPS) [Address 00EB₁₆]

B	Name	Functions	After reset	R	W
0	Fix these bits to "1."		1	R	W
1,2	Fix this bit to "0."		0	R	W
3	Data clock position set bits (DPS3 to DPS7)		1	R	W
4 to 7			0		

Address 00ED₁₆

Bank Control Register



Bank control register (BK) [Address 00ED₁₆]

B	Name	Functions				After reset	R	W
0 to 3	Bank selection bits (BK0 to BK3)	Bank number is selected (bank 11 to 15)				0	R	W
4, 5	Fix these bits to "0".					0	R	W
6, 7	Bank control bits (BK6, BK7)	b7	b6	Bank ROM	Address 1000 ₁₆ level access	0	R	W
		0	X	Not used	Read out from extra area (programmable)			
		1	0	Used	Read out the data from area specified by the bank selection bits			
		1	1	Used	Read out from extra area (data-dedicated)			

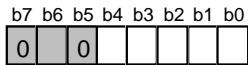
M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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Address 00EF₁₆

A-D Control Register



A-D control register (ADCON) [Address 00EF₁₆]

B	Name	Functions	After reset	R : W
0 to 2	Analog input pin selection bits (ADIN0 to ADIN2)	b2 b1 b0 0 0 0 : AD1 0 0 1 : AD2 0 1 0 : AD3 0 1 1 : AD4 1 0 0 : AD5 1 0 1 : AD6 1 1 0 : AD7 1 1 1 : AD8	0	R : W
3	A-D conversion completion bit (ADSTR)	0: Conversion in progress 1: Conversion completed	1	R : W
4	Vcc connection selection bit (ADVREF)	0: OFF 1: ON	0	R : W
5	Fix this bit to "0."		0	R : W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R : —
7	Fix this bit to "0."		0	R : W

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
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Address 00F4₁₆

Timer Mode Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 1 (TM1) [Address 00F4₁₆]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (TM10)	0: f(XIN)/16 or f(XCIN)/16 (Note) 1: Count source selected by bit 5 of TM1	0	R	W
1	Timer 2 count source selection bit 1 (TM11)	0: Count source selected by bit 4 of TM1 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (TM12)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (TM13)	0: Count start 1: Count stop	0	R	W
4	Timer 2 count source selection bit 2 (TM14)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Timer 1 overflow	0	R	W
5	Timer 1 count source selection bit 2 (TM15)	0: f(XIN)/4096 or f(XCIN)/4096 (See note) 1: External clock from TIM2 pin	0	R	W
6	Timer 5 count source selection bit 2 (TM16)	0: Timer 2 overflow 1: Timer 4 overflow	0	R	W
7	Timer 6 internal count source selection bit (TM17)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Timer 5 overflow	0	R	W

Note: Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

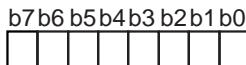
M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
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Address 00F5₁₆

Timer Mode Register 2



Timer mode register 2 (TM2) [Address 00F5₁₆]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (TM20)	(b6 at address 00C716) ↓ b0 0 0 : f(XIN)/16 or f(XCIN)/16 (See note) 1 0 : f(XCIN) 0 1 : } External clock from TIM3 pin 1 1 : }	0	R	W
1, 4	Timer 4 count source selection bits (TM21, TM24)	b4 b1 0 0 : Timer 3 overflow signal 0 1 : f(XIN)/16 or f(XCIN)/16 (See note) 1 0 : f(XIN)/2 or f(XCIN)/2 (See note) 1 1 : f(XCIN)	0	R	W
2	Timer 3 count stop bit (TM22)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (TM23)	0: Count start 1: Count stop	0	R	W
5	Timer 5 count stop bit (TM25)	0: Count start 1: Count stop	0	R	W
6	Timer 6 count stop bit (TM26)	0: Count start 1: Count stop	0	R	W
7	Timer 5 count source selection bit 1 (TM27)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Count source selected by bit 6 of TM1	0	R	W

Note: Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

PRELIMINARY

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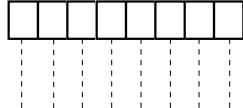
M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

Address 00F6₁₆

I²C Data Shift Register

b₇ b₆ b₅ b₄ b₃ b₂ b₁ b₀



I²C data shift register 1 (S0) [Address 00F6₁₆]

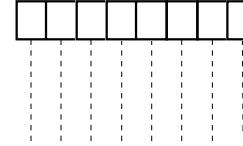
B	Name	Functions	After reset	R	W
0 to 7	D0 to D7	This is an 8-bit shift register to store receive data and write transmit data.	Indeterminate	R	W

Note: To write data into the I²C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

Address 00F7₁₆

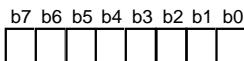
I²C Address Register

b₇ b₆ b₅ b₄ b₃ b₂ b₁ b₀



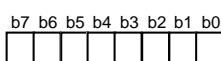
I²C address register (S0D) [Address 00F7₁₆]

B	Name	Functions	After reset	R	W
0	Read/write bit (RBW)	0: Read 1: Write	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	The address data transmitted from the master is compared with the contents of these bits.	0	R	W

M37280MF-XXXSP, M37280MK-XXXSP
M37280EKSPSINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLERAddress 00F8₁₆I²C Status RegisterI²C status register (S1) [Address 00F8₁₆]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0" 1 : Last bit = "1" (See note)	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected (See note)	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address match 1 : Address mismatch (See note)	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected (See note)	0	R	—
4	I ² C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	0	R	W
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave receive mode 0 1 : Slave transmit mode 1 0 : Master receive mode 1 1 : Master transmit mode	0	R	W

Note : These bits and flags can be read out, but cannot be written.

Address 00F9₁₆I²C Control RegisterI²C control register (S1D) [Address 00F9₁₆]

B	Name	Functions	After reset	R	W
0 to 2	Bit counter (Number of transmit/receive bits) (BC0 to BC2)	b2 b1 b0 0 0 0:8 0 0 1:7 0 1 0:6 0 1 1:5 1 0 0:4 1 0 1:3 1 1 0:2 1 1 1:1	0	R	W
3	I ² C-BUS interface use enable bit (ES0)	0: Disabled 1: Enabled	0	R	W
4	Data format selection bit(ALS)	0: Addressing format 1: Free data format	0	R	W
5	Addressing format selection bit (10BIT SAD)	0: 7-bit addressing format 1: 10-bit addressing format	0	R	W
6, 7	Connection control bits between I ² C-BUS interface and ports (BSEL0, BSEL1)	b7 b6 Connection port (See note) 0 0: None 0 1: SCL1, SDA1 1 0: SCL2, SDA2 1 1: SCL1, SDA1, SCL2, SDA2	0	R	W

PRELIMINARY

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M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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Address 00FA₁₆

I²C Clock Control Register

b7 b6 b5 b4 b3 b2 b1 b0



I²C clock control register (S2) [Address 00FA₁₆]

B	Name	Functions			After reset	R W
0 to 4	SCL frequency control bits (CCR0 to CCR4)	Setup value of CCR4-CCR0	Standard clock mode	High speed clock mode	0	R W
		00 to 02	Setup disabled	Setup disabled		
		03	Setup disabled	333		
		04	Setup disabled	250		
		05	100	400 (See note)		
		06	83.3	166		
		:	500/CCR value	1000/CCR value		
		1D	17.2	34.5		
		1E	16.6	33.3		
		1F	16.1	32.3		
		(at $\phi = 4$ MHz, unit : kHz)				
		5	SCL mode specification bit (FAST MODE)	0: Standard clock mode 1: High-speed clock mode	0	R W
		6	ACK bit (ACK BIT)	0: ACK is returned. 1: ACK is not returned.	0	R W
		7	ACK clock bit (ACK)	0: No ACK clock 1: ACK clock	0	R W

Note: At 400 kHz in the high-speed clock mode, the duty is as below.

"0" period : "1" period = 3 : 2

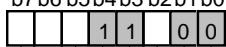
In the other cases, the duty is as below.

"0" period : "1" period = 1 : 1

Address 00FB₁₆

CPU Mode Register

b7 b6 b5 b4 b3 b2 b1 b0



CPU mode register (CM) [Address 00FB₁₆]

B	Name	Functions	After reset	R W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: } 1 0: } Not available 1 1: }	0	R W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R W
3, 4	Fix these bits to "1."		1	R W
5	XCOUT drivability selection bit (CM5)	0: LOW drive 1: HIGH drive	1	R W
6	Main Clock (XIN-XOUT) stop bit (CM6)	0: Oscillating 1: Stopped	0	R W
7	Internal system clock selection bit (CM7)	0: XIN-XOUT selected (high-speed mode) 1: XcIN-XcOUT selected (low-speed mode)	0	R W

Note: This bit is set to "1" after the reset release.

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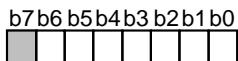
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY

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Address 00FC₁₆

Interrupt Request Register 1



Interrupt request register 1 (IREQ1) [Address 00FC₁₆]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	A-D conversion • INT3 interrupt request bit (ADR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

*: "0" can be set by software, but "1" cannot be set.

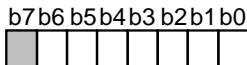
M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
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Address 00FC₁₆

Interrupt Request Register 1



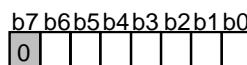
Interrupt request register 1 (IREQ1) [Address 00FC₁₆]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	A-D conversion • INT3 interrupt request bit (ADR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

*: "0" can be set by software, but "1" cannot be set.

Address 00FD₁₆

Interrupt Request Register 2



Interrupt request register 2 (IREQ2) [Address 00FD₁₆]

B	Name	Functions	After reset	R	W
0	INT1 interrupt request bit (IN1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Data slicer interrupt request bit (DSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Serial I/O interrupt request bit (SIOR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	f(XIN)/4096 • SPRITE OSD interrupt request bit (CKR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	INT2 interrupt request bit (IN2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	Multi-master I ² C-BUS interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	Timer 5 • 6 interrupt request bit (TM56R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Fix this bit to "0."		0	R	W

*: "0" can be set by software, but "1" cannot be set.

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Address 00FE₁₆

Interrupt Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address 00FE₁₆]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	OSD interrupt enable bit (OSDE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	A-D conversion • INT3 interrupt enable bit (ADE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Address 00FF₁₆

Interrupt Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 2 (ICON2) [Address 00FF₁₆]

B	Name	Functions	After reset	R	W
0	INT1 interrupt enable bit (IN1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Data slicer interrupt enable bit (DSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (SIOE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	f(Xin)/4096 • SPRITE OSD interrupt enable bit (CKE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	INT2 interrupt enable bit (IN2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	Multi-master I ² C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Timer 5 • 6 interrupt enable bit (TM56E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Timer 5 • 6 interrupt switch bit (TM56S)	0 : Timer 5 1 : Timer 6	0	R	W

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PRELIMINARY
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Address 020A₁₆

PWM Mode Register 1

b7 b6 b5 b4 b3 b2 b1 b0

PWM mode register 1 (PN) [Address 020A₁₆]

B	Name	Functions	After reset	R	W
0	PWM counts source selection bit (PN0)	0 : Count source supply 1 : Count source stop	0	R	W
1, 2	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
3	PWM output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	P0 ₃ /PWM7 output selection bit (PN4)	0 : P0 ₃ output 1 : PWM7 output	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Address 020B₁₆

PWM Mode Register 2

b7 b6 b5 b4 b3 b2 b1 b0

PWM mode register 2 (PW) [Address 020B₁₆]

B	Name	Functions	After reset	R	W
0	P0 ₄ /PWM0 output selection bit (PW0)	0 : P0 ₄ output 1 : PWM0 output	0	R	W
1	P0 ₅ /PWM1 output selection bit (PW1)	0 : P0 ₅ output 1 : PWM1 output	0	R	W
2	P0 ₆ /PWM2 output selection bit (PW2)	0 : P0 ₆ output 1 : PWM2 output	0	R	W
3	P0 ₇ /PWM3 output selection bit (PW3)	0 : P0 ₇ output 1 : PWM3 output	0	R	W
4	P0 ₀ /PWM4 output selection bit (PW4)	0 : P0 ₀ output 1 : PWM4 output	0	R	W
5	P0 ₁ /PWM5 output selection bit (PW5)	0 : P0 ₁ output 1 : PWM5 output	0	R	W
6	P0 ₂ /PWM6 output selection bit (PW6)	0 : P0 ₂ output 1 : PWM6 output	0	R	W
7	P0 ₅ /PWM7 output selection bit (PW7)	0 : P0 ₅ output 1 : PWM7 output	0	R	W

PRELIMINARY

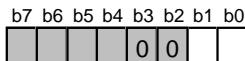
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M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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Address 0210₁₆

ROM Correction Enable Register

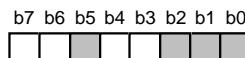


ROM correction enable register (RCR) [Address 0210₁₆]

B	Name	Functions	After reset	R	W
0	Block 1 enable bit (RCR0)	0: Disabled 1: Enabled	0	R	W
1	Block 2 enable bit (RCR1)	0: Disabled 1: Enabled	0	R	W
2, 3	Fix these bits to "0."		0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Address 0212₁₆

Interrupt Input Polarity Register



Interrupt input polarity register (IP) [Address 0212₁₆]

B	Name	Functions	After reset	R	W
0 to 2	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
3	INT1 polarity switch bit (POL1)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	INT2 polarity switch bit (POL2)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is "0."		0	R	—
6	INT3 polarity switch bit (POL3)	0 : Positive polarity 1 : Negative polarity	0	R	W
7	A-D conversion • INT3 interrupt source selection bit (AD/INT3SEL)	0 : INT3 interrupt 1 : A-D conversion interrupt	0	R	W

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY

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Address 021316

Serial I/O Mode Register

b7 b6 b5 b4 b3 b2 b1 b0



Serial I/O mode register (SM) [Address 021316]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: $f(XIN)/8$ or $f(XCIN)/8$ 0 1: $f(XIN)/16$ or $f(XCIN)/16$ 1 0: $f(XIN)/32$ or $f(XCIN)/32$ 1 1: $f(XIN)/64$ or $f(XCIN)/64$	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Port function selection bit (SM3)	0: P11, P13 1: SCL1, SDA1	0	R	W
4	Port function selection bit (SM4)	0: P12, P14 1: SCL2, SDA2	0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W
6	SIN pin switch bit (SM6)	0: P17 is SIN pin. 1: P72 is SIN pin.	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

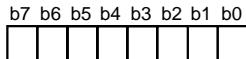
M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY
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Address 0215₁₆

OSD Control Register 2



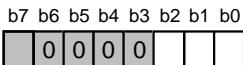
OSD control register 2 (OC2) [Address 0215₁₆]

B	Name	Functions				At reset	R	W
0, 1	Display layer selection bits (OC20, OC21)	b1	b0	Layer 1	Layer 2	0	R	W
		0	0	CC, OSD, CDOSD	—			
		0	1	CC, OSD	CDOSD			
		1	0	CC, CDOSD	OSD			
		1	1	CC	CDOSD OSD			
2	R, G, B signal output selection bit(OC22)	0: Digital output (See note) 1: Analog output (4 gradations)				0	R	W
3	Solid space output bit (OC23)	0: OUT1 output 1: OUT2 output				0	R	W
4	Horizontal window/blank control bit (OC24)	0: OFF 1: ON				0	R	W
5	Window/blank selection bit 1 (horizontal) (OC25)	0: Horizontal blank function 1: Horizontal window function				0	R	W
6	Window/blank selection bit 2 (vertical) (OC26)	0: Vertical blank function 1: Vertical window function				0	R	W
7	OSD interrupt request selection bit (OC27)	0: At completion of layer 1 block display 1: At completion of layer 2 block display				0	R	W

Note: When setting bit 1 of the OSD port control register to "1," the value which is converted from the 4-adjustment-level analog to the 2-bit digital is output regardless of this bit value as follows : the high-order bit (R1, G1 and B1) is output from pins P52, P53 and P54, and the low-order bit is (R0, G0 and B0) output from pins P17, P15 and P16. And besides, when not using OSD function, the low-power dissipation can realize by setting this bit to "0."

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M37280EKSPSINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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Clock Control Register

Clock control register (CS) [Address 0216₁₆]

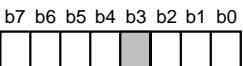
B	Name	Functions	After reset	R	W
0	Clock selection bit (CS0)	0: Data slicer clock 1: OSC1 clock	0	R	W
1, 2	OSC1 oscillating mode selection bits (CS1, CS2)	b ₂ b ₁ 0 0: 32kHz oscillating mode. 0 1: Used as input port of P6 ₃ and P6 ₄ (See note 1). 1 0: LC oscillating mode 1 1: Ceramic • quartz-crystal oscillating mode	0	R	W
3 to 6	Fix these bits to "0."		0	R	W
7	Test bit (See note 2)		0	R	W

Note 1: Set bit 7 of address 00C7₁₆ to "1", when OSC1 and OSC2 are used as P6₃ and P6₄.

2: Be sure to set bit 7 to "0" for program of the mask and the EPROM versions. For the emulator MCU version (M37280ERSS), be sure to set bit 7 to "1" when using the data slicer clock for software debugging.

Address 0217₁₆

I/O Polarity Control Register

I/O polarity control register (PC) [Address 0217₁₆]

B	Name	Functions	After reset	R	W
0	Hsync input polarity switch bit (PC0)	0: Positive polarity input 1: Negative polarity input	0	R	W
1	Vsync input polarity switch bit (PC1)	0: Positive polarity input 1: Negative polarity input	0	R	W
2	R, G, B output polarity switch bit (PC2)	0: Positive polarity output 1: Negative polarity output	0	R	W
3	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0".		0	R	—
4	OUT1 output polarity switch bit (PC4)	0: Positive polarity output 1: Negative polarity output	0	R	W
5	OUT2 output polarity switch bit (PC5)	0: Positive polarity output 1: Negative polarity output	0	R	W
6	Display dot line selection bit (PC6) (See note)	0: " " at even field " " at odd field 1: " " at even field " " at odd field	0	R	W
7	Field determination flag(PC7)	0: Even field 1: Odd field	1	R	—

Note: Refer to Fig. 12.11.19.

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Address 021816

Raster Color Register

b7 b6 b5 b4 b3 b2 b1 b0



Raster color register (RC) [Address 021816]

B	Name	Functions	At reset	R	W
0, 1	Raster color R control bits (RC0, RC1)	b0 b1 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
2, 3	Raster color G control bits (RC2, RC3)	b3 b2 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
4, 5	Raster color B control bits (RC4, RC5)	b5 b4 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	0	R	W
6	Raster color OUT1 control bits (RC6)	0: No output 1: Output	0	R	W
7	Raster color OUT2 control bits (RC7)	0: No output 1: Output	0	R	W

Note: When selecting digital output, Vcc is output at any other values except "00."

Address 021916

OSD Control Register 3

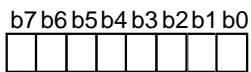
b7 b6 b5 b4 b3 b2 b1 b0



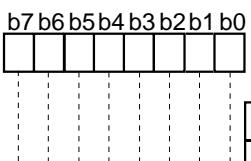
OSD control register 3 (OC3) [Address 021916]

B	Name	Functions	After reset	R	W
0	CC mode character color selection bit (OC30)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
1, 2	CC mode character background color selection bits (OC31, OC32) (See note)	b1 b1 0 0: Color code 0 to 3 0 1: Color code 4 to 7 1 0: Color code 8 to 11 1 1: Color code 12 to 15	0	R	W
3	CDOSD mode character color selection bit (OC33)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
4	SPRITE color selection bit (OC34)	0: Color code 0 to 7 1: Color code 8 to 15	0	R	W
5	OSD mode window control bit (OC35)	0: Window OFF 1: Window ON	0	R	W
6	CC mode window control bit (OC36)	0: Window OFF 1: Window ON	0	R	W
7	CDOSD mode window control bit (OC37)	0: Window OFF 1: Window ON	0	R	W

Note: Color pallet 8 is always selected for solid space (when OUT1 output is selected), regardless of value of this register.

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M37280EKSPSINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLERAddress 021C₁₆Top Border Control Register 1Top border control register 1 (TB1) [Address 021C₁₆]

B	Name	Functions	After reset	R:W
0 to 7	Control bits of top border (TB10 to TB17)	Top border position (low-order 8 bits) TH X (setting value of low-order 2 bits of TB2 $\times 16^2$ + setting value of high-order 4 bits of TB1 $\times 16^1$ + setting value of low-order 4 bits of TB1 $\times 16^0$)	Indeterminate	R:W

Notes 1: Do not set "0016" or "0116" to the TB1 at TB2 = "0016."**2:** TH is cycle of HSYNC.**3:** TB2 is top border control register 2.Address 021D₁₆Bottom Border Control Register 1Bottom border control register 1 (BB1) [Address 021D₁₆]

B	Name	Functions	After reset	R:W
0 to 7	Control bits of bottom border (BB10 to BB17)	Bottom border position (low-order 8 bits) TH X (setting value of low-order 2 bits of BB2 $\times 16^2$ + setting value of high-order 4 bits of BB1 $\times 16^1$ + setting value of low-order 4 bits of BB1 $\times 16^0$)	Indeterminate	R:W

Notes 1: Set values fit for the following condition: $(TB1 + TB2 \times 16^2) < (BB1 + BB2 \times 16^2)$.**2:** TH is cycle of HSYNC.**3:** BB2 is bottom border control register 2.

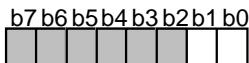
M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
Notice: This is not a final specification.
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Address 021E₁₆

Top Border Control Register 2



Top border control register 2 (TB2) [Address 021E₁₆]

B	Name	Functions	After reset	R:W
0, 1	Control bits of top border (TB20, TB21)	Top border position (high-order 2 bits) TH X (setting value of low-order 2 bits of TB2 $\times 16^2$ + setting value of high-order 4 bits of TB1 $\times 16^1$ + setting value of low-order 4 bits of TB1 $\times 16^0$)	Indeterminate	R:W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R:-

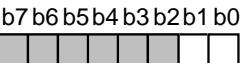
Notes 1: Do not set "0016" or "0116" to the TB1 at TB2 = "0016."

2: TH is cycle of HSYNC.

3: TB1 is top border control register 1.

Address 021F₁₆

Bottom Border Control Register 2



Bottom border control register 2 (BB2) [Address 021F₁₆]

B	Name	Functions	After reset	R:W
0, 1	Control bits of bottom border (BB20, BB21)	Bottom border position (high-order 2 bits) TH X (setting value of low-order 2 bits of BB2 $\times 16^2$ + setting value of high-order 4 bits of BB1 $\times 16^1$ + setting value of low-order 4 bits of BB1 $\times 16^0$)	Indeterminate	R:W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R:-

Notes 1: Set values fit for the following condition:

$(TB1 + TB2 \times 16^2) < (BB1 + BB2 \times 16^2)$.

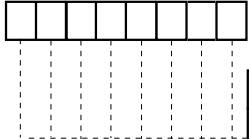
2: TH is cycle of HSYNC.

3: BB1 is bottom border control register 1.

M37280MF-XXXSP, M37280MK-XXXSP
M37280EKSPSINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLERAddresses 0220₁₆ to 022F₁₆

Vertical Position Register 1i

b7 b6 b5 b4 b3 b2 b1 b0

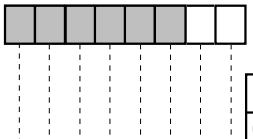
Vertical position register 1i (VP1i) (i = 1 to 16) [Addresses 0220₁₆ to 022F₁₆]

B	Name	Functions	After reset	R:W
0 to 7	Control bits of vertical display start positions (VP1i0 to VP1i7) (See note 1)	Vertical display start positions (low-order 8 bits) TH X (setting value of low-order 2 bits of VP2i $\times 16^2$ + setting value of low-order 4 bits of VP1i $\times 16^1$ + setting value of low-order 4 bits of VP1i $\times 16^0$)	Indeterminate	R:W

Notes 1: Do not "0016" and "0116" to VP1i at VP2i = "0016."**2:** TH is cycle of HSYNC.**3:** VP2i is vertical position register 2i.Addresses 0230₁₆ to 023F₁₆

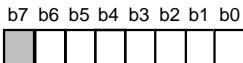
Vertical Position Register 2i

b7 b6 b5 b4 b3 b2 b1 b0

Vertical position register 2i (VP2i) (i = 1 to 16) [Addresses 0230₁₆ to 023F₁₆]

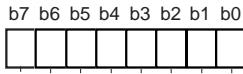
B	Name	Functions	After reset	R:W
0, 1	Control bits of vertical display start positions (VP2i0, VP2i1) (See note 1)	Vertical display start positions (high-order 2 bits) TH X (setting value of low-order 2 bits of VP2i $\times 16^2$ + setting value of low-order 4 bits of VP1i $\times 16^1$ + setting value of low-order 4 bits of VP1i $\times 16^0$)	Indeterminate	R:W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R:-

Notes 1: Do not set "0016" and "0116" to VP1i at VP2i = "0016."**2:** TH is cycle of HSYNC.**3:** VP1i is vertical position register 1i.

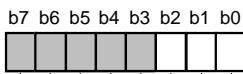
Addresses 0241₁₆ to 0247₁₆, 0249₁₆ to 024F₁₆**Color Pallet Register i**Color pallet register i (CRI) (i = 1 to 7, 9 to 15) [Addresses 0241₁₆ to 0247₁₆, 0249₁₆ to 024F₁₆]

B	Name	Functions	After reset	R : W
0, 1	R signal output control bits (CRI0, CRI1)	b0 b1 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R : W
2, 3	G signal output control bits (CRI2, CRI3)	b3 b2 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R : W
4, 5	B signal output control bits (CRI4, CRI5)	b5 b4 0 0: No output (See note) 0 1: 1/3 Vcc 1 0: 2/3 Vcc 1 1: Vcc	Indeterminate	R : W
6	OUT1 signal output control bit (CRI6)	0: No output 1: Output	Indeterminate	R : W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R : —

Note: When selecting digital output, the output is Vcc at all values other than "00."

M37280MF-XXXSP, M37280MK-XXXSP
M37280EKSPSINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLERAddress 0250₁₆Left Border Control Register 1Left border control register 1 (LB1) [Address 0250₁₆]

B	Name	Functions	After reset	R	W
0	Control bits of left border (LB10 to LB17)	Left border position (low-order 8 bits) Tosc X (setting value of low-order 3 bits of LB2 × 16 ² + setting value of high-order 4 bits of LB1 × 16 ¹ + setting value of low-order 4 bits of LB1 × 16 ⁰)	1	R	W
1 to 7			0		

Notes 1: Do not set LB1 = LB2 = "00₁₆."**2:** Set values fit for the following condition:(LB1 + LB2 × 16²) < (RB1 + RB2 × 16²).**3:** Tosc is OSD oscillation period.**4:** LB2 is left border control register 2.Address 0251₁₆Left Border Control Register 2Left border control register 2 (LB2) [Address 0251₁₆]

B	Name	Functions	After reset	R	W
0 to 2	Control bits of left border (LB20 to LB22)	Left border position (high-order 3 bits) Tosc X (setting value of low-order 3 bits of LB2 × 16 ² + setting value of high-order 4 bits of LB1 × 16 ¹ + setting value of low-order 4 bits of LB1 × 16 ⁰)	0	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		0	R	W

Notes 1: Do not set LB1 = LB2 = "00₁₆."**2:** Set values fit for the following condition:(LB1 + LB2 × 16²) < (RB1 + RB2 × 16²).**3:** Tosc is OSD oscillation period.**4:** LB1 is left border control register 1.

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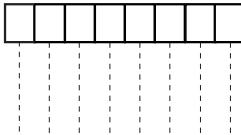
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
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Address 0252₁₆

Right Border Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0



Right border control register 1 (RB1) [Address 0252₁₆]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of right border (RB10 to RB17)	Right border position (low-order 8 bits) Tosc \times (setting value of low-order 3 bits of RB2 $\times 16^2$ + setting value of high-order 4 bits of RB1 $\times 16^1$ + setting value of low-order 4 bits of RB1 $\times 16^0$)	1	R	W

Notes 1: Set values fit for the following condition:

(LB1 + LB2 $\times 16^2$) < (RB1 + RB2 $\times 16^2$).

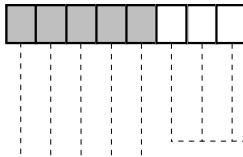
2: Tosc is OSD oscillation period.

3: RB2 is right border control register 2.

Address 0253₁₆

Right Border Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0



Right border control register 2 (RB2) [Address 0253₁₆]

B	Name	Functions	After reset	R	W
0 to 2	Control bits of right border (RB20 to RB22)	Right border position (high-order 3 bits) Tosc \times (setting value of low-order 3 bits of RB2 $\times 16^2$ + setting value of high-order 4 bits of RB1 $\times 16^1$ + setting value of low-order 4 bits of RB1 $\times 16^0$)	1	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0".		0	R	W

Notes 1: Set values fit for the following condition:

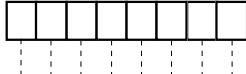
(LB1 + LB2 $\times 16^2$) < (RB1 + RB2 $\times 16^2$).

2: Tosc is OSD oscillation period.

3: RB1 is right border control register 1.

M37280MF-XXXSP, M37280MK-XXXSP
M37280EKSPSINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLERAddress 0254₁₆SPRITE Vertical Position Register 1

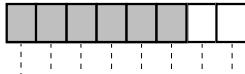
b7 b6 b5 b4 b3 b2 b1 b0

SPRITE vertical position register 1 (VS1) [Address 0254₁₆]

B	Name	Functions	After reset	R	W
0	Vertical display start position (low-order 8 bits) $T_H X$	Vertical display start position (low-order 8 bits) $T_H X$ (setting value of low-order 2 bits of VS2 $\times 16^2$ + setting value of high-order 4 bits of VS1 $\times 16^1$ + setting value of low-order 4 bits of VS1 $\times 16^0$)	1	R	W
1 to 7	control bits of SPRITE OSD (VS10 to VS17)		0		

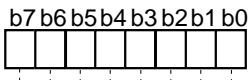
Notes 1: Do not set "0016" to the VS1 at VS2 = "0016."**2:** T_H is cycle of HSYNC.**3:** VS2 is SPRITE vertical position register 2.Address 0255₁₆SPRITE Vertical Position Register 2

b7 b6 b5 b4 b3 b2 b1 b0

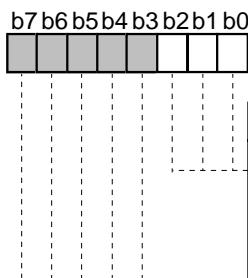
SPRITE vertical position register 2 (VS2) [Address 0255₁₆]

B	Name	Functions	After reset	R	W
0, 1	Vertical start position control bits of SPRITE OSD (VS20, VS21)	Vertical display start position (high-order 2 bits) $T_H X$ (setting value of low-order 2 bits of VS2 $\times 16^2$ + setting value of high-order 4 bits of VS1 $\times 16^1$ + setting value of low-order 4 bits of VS1 $\times 16^0$)	0	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0".		0	R	—

Notes 1: Do not set "0016" to the VS1 at VS2 = "0016."**2:** T_H is cycle of HSYNC.**3:** VS1 is SPRITE vertical position register 1.

Address 0256₁₆SPRITE Horizontal Position Register 1SPRITE horizontal position register 1 (HS1) [Address 0256₁₆]

B	Name	Functions	After reset	R:W
0 to 7	Horizontal display start position control bits of SPRITE OSD (HS10 to HS17)	Horizontal display start position (low-order 8 bits) Tosc X (setting value of low-order 2 bits of HS2 $\times 16^2$ + setting value of high-order 4 bits of HS1 $\times 16^1$ + setting value of low-order 4 bits of HS1 $\times 16^0$)	Indeterminate	R:W

Notes 1: Do not set HS1 < "3016" at HS2 = "0016."**2:** Tosc is OSD oscillation period.**3:** HS2 is SPRITE horizontal position register 2.Address 0257₁₆SPRITE Horizontal Position Register 2SPRITE horizontal position register 2 (HS2) [Address 0257₁₆]

B	Name	Functions	After reset	R:W
0 to 2	Horizontal display start position control bits of SPRITE OSD (HS20 to HS22)	Horizontal display start position (high-order 3 bits) Tosc X (setting value of low-order 2 bits of HS2 $\times 16^2$ + setting value of high-order 4 bits of HS1 $\times 16^1$ + setting value of low-order 4 bits of HS1 $\times 16^0$)	Indeterminate	R:W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R:-

Notes 1: Do not set HS1 < "3016" at HS2 = "0016."**2:** Tosc is oscillation period.**3:** HS1 is SPRITE horizontal position register 1.

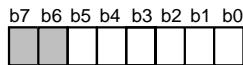
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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

PRELIMINARY
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Address 0258₁₆

SPRITE OSD Control Register



SPRITE OSD control register (SC) [Address 0258₁₆]

B	Name	Functions	After reset	R	W
0	SPRITE OSD control bit (SC0)	0: Stopped 1: Operating	0	R	W
1	Pre-divide ratio selection bit (SC1)	0: Pre-divide ratio 1 1: Pre-divide ratio 2	0	R	W
2, 3	Dot size selection bits (SC2, SC3)	b3 b2 0 0: 1Tc × 1/2H 0 1: 1Tc × 1H 1 0: 2Tc × 1H 1 1: 2Tc × 2H	0	R	W
4	Interrupt occurrence position selection bit (SC4)	0: After display of horizontal 20 dots 1: After display of horizontal 10 dots or 20 dots	0	R	W
5	XIN/4096 • SPRITE interrupt source switch bit (SC5)	0: XIN/4096 interrupt 1: SPRITE OSD interrupt	0	R	W
6, 7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0".		0	R	—

Notes 1: Tc : Pre-devided clock period for OSD
2: H : HSYNC

M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

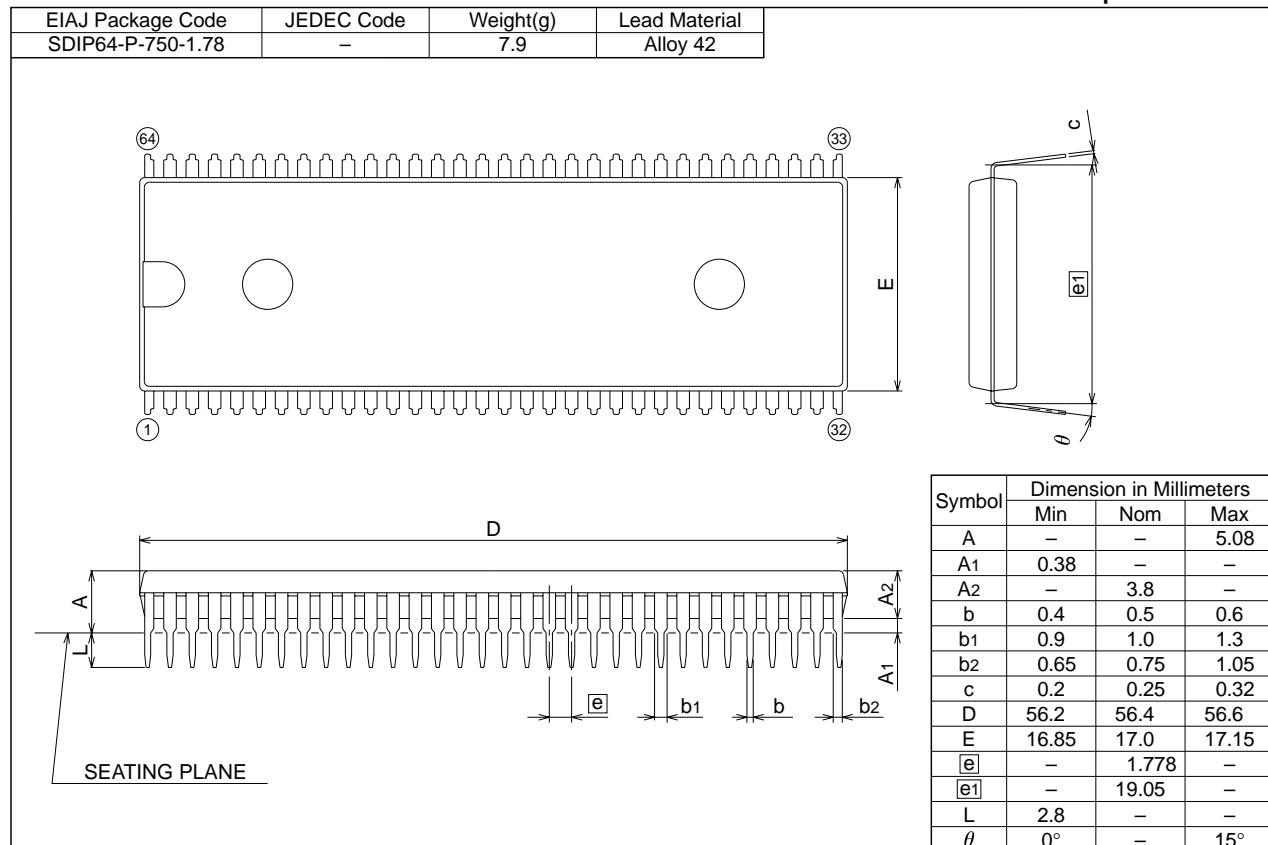
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
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PRELIMINARY
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32. PACKAGE OUTLINE

64P4B

Plastic 64pin 750mil SDIP



PRELIMINARY

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M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER
and ON-SCREEN DISPLAY CONTROLLER

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REVISION DESCRIPTION LIST		M37280MF-XXXSP, M37280MK-XXXSP M37280EKSP
Rev. No.	Revision Description	Rev. date
1.0	First Edition	980731