

### FEATURES

- Operate with 3.3 V supply
- Interoperable with 5 V logic
- EIA RS-422 and RS-485 compliant over full common-mode range
- Data rate options
  - ADM3483/ADM3488: 250 kbps
  - ADM3485/ADM3490/ADM3491: 10 Mbps
- Half- and full-duplex options
- Reduced slew rates for low EMI (ADM3483 and ADM3488)
- 2 nA supply current in shutdown mode (ADM3483/ADM3485/ADM3491)
- Up to 32 transceivers on the bus
- −7 V to +12 V bus common-mode range
- Specified over the −40°C to +85°C temperature range
- 8 ns skew (ADM3485/ADM3490/ADM3491)
- 8-lead SOIC and 14-lead SOIC (ADM3491 only) packages

### APPLICATIONS

- Low power RS-485/RS-422 applications
- Telecom
- Industrial process control
- HVAC

### GENERAL DESCRIPTION

The ADM3483/ADM3485/ADM3488/ADM3490/ADM3491 are low power, differential line transceivers designed to operate using a single 3.3 V power supply. Low power consumption, coupled with a shutdown mode, makes the ADM3483/ADM3485/ADM3488/ADM3490/ADM3491 ideal for power-sensitive applications.

The ADM3488/ADM3490/ADM3491 feature full-duplex communication, while the ADM3483/ADM3485 are designed for half-duplex communication.

The ADM3483/ADM3488 feature slew rate limited drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250 kbps.

The ADM3485/ADM3490/ADM3491 transmit at up to 10 Mbps. The receiver input impedance is 12 kΩ, allowing up to 32 transceivers to be connected on the bus. A thermal shutdown circuit prevents excessive power dissipation caused by bus contention or by output shorting. If a significant temperature increase is detected

### FUNCTIONAL BLOCK DIAGRAMS

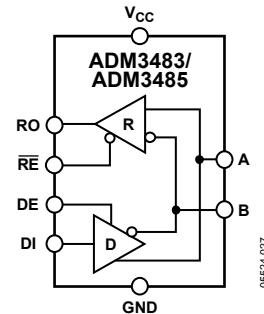


Figure 1.

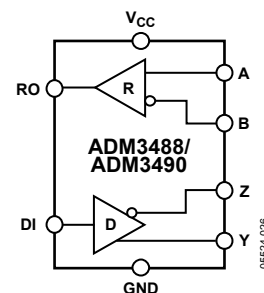


Figure 2.

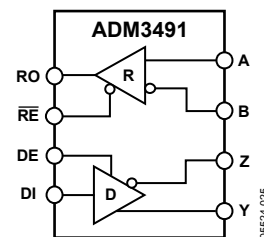


Figure 3.

in the internal driver circuitry during fault conditions, then the thermal shutdown circuit forces the driver output into a high impedance state. If the inputs are unconnected (floating), the receiver contains a fail-safe feature that results in a logic high output state. The parts are fully specified over the commercial and industrial temperature ranges. The ADM3483/ADM3485/ADM3488/ADM3490 are available in 8-lead SOIC\_N; the ADM3491 is available in a 14-lead SOIC\_N.

#### Rev. E

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## REVISION HISTORY

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### 10/05—Revision 0: Initial Version

Table 1. ADM34xx Part Comparison

| Part No. | Guaranteed Data Rate (Mbps) | Supply Voltage (V) | Half-/Full-Duplex | Slew Rate Limited | Driver/Receiver Enable | Shutdown Current (nA) | Pin Count |
|----------|-----------------------------|--------------------|-------------------|-------------------|------------------------|-----------------------|-----------|
| ADM3483  | 0.25                        | 3.0 to 3.6         | Half              | Yes               | Yes                    | 2                     | 8         |
| ADM3485  | 10                          | 3.0 to 3.6         | Half              | No                | Yes                    | 2                     | 8         |
| ADM3488  | 0.25                        | 3.0 to 3.6         | Full              | Yes               | No                     | N/A                   | 8         |
| ADM3490  | 10                          | 3.0 to 3.6         | Full              | No                | No                     | N/A                   | 8         |
| ADM3491  | 10                          | 3.0 to 3.6         | Full              | No                | Yes                    | 2                     | 14        |

## SPECIFICATIONS

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

| Parameter                                                      | Min            | Typ   | Max      | Unit          | Test Conditions/Comments                                                                                          |
|----------------------------------------------------------------|----------------|-------|----------|---------------|-------------------------------------------------------------------------------------------------------------------|
| <b>DRIVER</b>                                                  |                |       |          |               |                                                                                                                   |
| Differential Output Voltage ( $V_{OD}$ )                       | 2.0            |       |          | V             | $R_L = 100 \Omega$ (RS-422), $V_{CC} = 3.3 \text{ V} \pm 5\%$ (see Figure 17)                                     |
|                                                                | 1.5            |       |          | V             | $R_L = 54 \Omega$ (RS-485) (see Figure 17)                                                                        |
|                                                                | 1.5            |       |          | V             | $R_L = 60 \Omega$ (RS-485), $V_{CC} = 3.3 \text{ V}$ (see Figure 18)                                              |
| $\Delta  V_{OD} $ for Complementary Output States <sup>1</sup> |                |       | 0.2      | V             | $R_L = 54 \Omega$ or $100 \Omega$ (see Figure 17)                                                                 |
| Common-Mode Output Voltage ( $V_{OC}$ )                        |                |       | 3        | V             | $R_L = 54 \Omega$ or $100 \Omega$ (see Figure 17)                                                                 |
| $\Delta  V_{OC} $ for Common-Mode Output Voltage <sup>1</sup>  |                |       | 0.2      | V             | $R_L = 54 \Omega$ or $100 \Omega$ (see Figure 17)                                                                 |
| <b>DRIVER INPUT LOGIC</b>                                      |                |       |          |               |                                                                                                                   |
| CMOS Input Logic Threshold Low ( $V_{IL}$ )                    |                |       | 0.8      | V             | DE, DI, $\overline{RE}$                                                                                           |
| CMOS Input Logic Threshold High ( $V_{IH}$ )                   | 2.0            |       |          | V             | DE, DI, $\overline{RE}$                                                                                           |
| CMOS Logic Input Current ( $I_{IN1}$ )                         |                |       | $\pm 2$  | $\mu\text{A}$ | DE, DI, $\overline{RE}$                                                                                           |
| Input Current—A, B ( $I_{IN2}$ )                               |                |       | 1.0      | mA            | $V_{IN} = 12 \text{ V}$ , DE = 0 V, $V_{CC} = 0 \text{ V}$ or 3.6 V                                               |
|                                                                |                |       | −0.8     | mA            | $V_{IN} = -7 \text{ V}$ , DE = 0 V, $V_{CC} = 0 \text{ V}$ or 3.6 V                                               |
| Output Leakage—Y, Z ( $I_O$ )                                  |                | 0.1   |          | $\mu\text{A}$ | $V_{IN} = 12 \text{ V}$ , DE = 0 V, $\overline{RE} = 0 \text{ V}$ , $V_{CC} = 0 \text{ V}$ or 3.6 V, ADM3491 only |
|                                                                |                | −0.1  |          | $\mu\text{A}$ | $V_{IN} = -7 \text{ V}$ , DE = 0 V, $\overline{RE} = 0 \text{ V}$ , $V_{CC} = 0 \text{ V}$ or 3.6 V, ADM3491 only |
| Output Leakage (Y, Z) in Shutdown Mode ( $I_O$ )               |                | 0.01  |          | $\mu\text{A}$ | $V_{IN} = 12 \text{ V}$ , DE = 0 V, $\overline{RE} = V_{CC}$ , $V_{CC} = 0 \text{ V}$ or 3.6 V, ADM3491 only      |
|                                                                |                | −0.01 |          | $\mu\text{A}$ | $V_{IN} = -7 \text{ V}$ , DE = 0 V, $\overline{RE} = V_{CC}$ , $V_{CC} = 0 \text{ V}$ or 3.6 V, ADM3491 only      |
| <b>RECEIVER</b>                                                |                |       |          |               |                                                                                                                   |
| Differential Input Threshold Voltage ( $V_{TH}$ )              | −0.2           |       | +0.2     | V             | $-7 \text{ V} < V_{CM} < +12 \text{ V}$                                                                           |
| Input Hysteresis ( $\Delta V_{TH}$ )                           |                | 50    |          | mV            | $V_{CM} = 0 \text{ V}$                                                                                            |
| CMOS Output Voltage High ( $V_{OH}$ )                          | $V_{CC} - 0.4$ |       |          | V             | $I_{OUT} = -1.5 \text{ mA}$ , $V_{ID} = 200 \text{ mV}$ (see Figure 19)                                           |
| CMOS Output Voltage Low ( $V_{OL}$ )                           |                |       | 0.4      | V             | $I_{OUT} = 2.5 \text{ mA}$ , $V_{ID} = 200 \text{ mV}$ (see Figure 19)                                            |
| Three-State Output Leakage Current ( $I_{OZR}$ )               |                |       | $\pm 1$  | $\mu\text{A}$ | $V_{CC} = 3.6 \text{ V}$ , $0 \text{ V} \leq V_{OUT} \leq V_{CC}$                                                 |
| Input Resistance ( $R_{IN}$ )                                  | 12             |       |          | k $\Omega$    | $-7 \text{ V} < V_{CM} < +12 \text{ V}$                                                                           |
| <b>POWER SUPPLY CURRENT</b>                                    |                |       |          |               |                                                                                                                   |
| Supply Current ( $I_{CC}$ )                                    |                | 1.1   | 2.2      | mA            | DE = $V_{CC}$ , $\overline{RE} = 0 \text{ V}$ or $V_{CC}$ , no load, DI = 0 V or $V_{CC}$                         |
|                                                                |                | 0.95  | 1.9      | mA            | DE = 0 V, $\overline{RE} = 0 \text{ V}$ , no load, DI = 0 V or $V_{CC}$                                           |
| Supply Current in Shutdown Mode ( $I_{SHDN}$ )                 |                | 0.002 | 1        | $\mu\text{A}$ | DE = 0 V, $\overline{RE} = V_{CC}$ , DI = $V_{CC}$ or 0 V                                                         |
| Driver Short-Circuit Output Current ( $I_{OSD}$ )              |                |       | −250     | mA            | $V_{OUT} = -7 \text{ V}$                                                                                          |
|                                                                |                |       | 250      | mA            | $V_{OUT} = 12 \text{ V}$                                                                                          |
| Receiver Short-Circuit Output Current ( $I_{OSR}$ )            | $\pm 8$        |       | $\pm 60$ | mA            | $0 \text{ V} < V_{RO} < V_{CC}$                                                                                   |

<sup>1</sup> $\Delta V_{OD}$  and  $\Delta V_{OC}$  are the changes in  $V_{OD}$  and  $V_{OC}$ , respectively, when DI input changes state.

**TIMING SPECIFICATIONS—ADM3485/ADM3490/ADM3491**

$V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

| Parameter                                                               | Min | Typ | Max | Unit | Test Conditions/Comments                          |
|-------------------------------------------------------------------------|-----|-----|-----|------|---------------------------------------------------|
| <b>DRIVER</b>                                                           |     |     |     |      |                                                   |
| Differential Output Delay ( $t_{DD}$ )                                  | 1   | 22  | 35  | ns   | $R_L = 60\ \Omega$ (see Figure 20 and Figure 26)  |
| Differential Output Transition Time ( $t_{TD}$ )                        | 3   | 8   | 25  | ns   | $R_L = 60\ \Omega$ (see Figure 20 and Figure 26)  |
| Propagation Delay, Low-to-High Level ( $t_{PLH}$ )                      | 7   | 22  | 35  | ns   | $R_L = 27\ \Omega$ (see Figure 21 and Figure 27)  |
| Propagation Delay, High-to-Low Level ( $t_{PHL}$ )                      | 7   | 22  | 35  | ns   | $R_L = 27\ \Omega$ (see Figure 21 and Figure 27)  |
| $ t_{PLH} - t_{PHL} $ Propagation Delay Skew <sup>1</sup> ( $t_{PDS}$ ) |     |     | 8   | ns   | $R_L = 27\ \Omega$ (see Figure 21 and Figure 27)  |
| <b>DRIVER OUTPUT ENABLE/DISABLE TIMES (ADM3485/ADM3491 ONLY)</b>        |     |     |     |      |                                                   |
| Output Enable Time to Low Level ( $t_{PZL}$ )                           |     | 45  | 90  | ns   | $R_L = 110\ \Omega$ (see Figure 23 and Figure 29) |
| Output Enable Time to High Level ( $t_{PZH}$ )                          |     | 45  | 90  | ns   | $R_L = 110\ \Omega$ (see Figure 22 and Figure 28) |
| Output Disable Time from High Level ( $t_{PHZ}$ )                       |     | 40  | 80  | ns   | $R_L = 110\ \Omega$ (see Figure 22 and Figure 28) |
| Output Disable Time from Low Level ( $t_{PLZ}$ )                        |     | 40  | 80  | ns   | $R_L = 110\ \Omega$ (see Figure 23 and Figure 29) |
| Output Enable Time from Shutdown to Low Level ( $t_{PSL}$ )             |     | 650 | 900 | ns   | $R_L = 110\ \Omega$ (see Figure 23 and Figure 29) |
| Output Enable Time from Shutdown to High Level ( $t_{PSH}$ )            |     | 650 | 900 | ns   | $R_L = 110\ \Omega$ (see Figure 22 and Figure 28) |

<sup>1</sup> Measured on  $|t_{PLH}(Y) - t_{PHL}(Y)|$  and  $|t_{PLH}(Z) - t_{PHL}(Z)|$ .

**TIMING SPECIFICATIONS—ADM3483/ADM3488**

$V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

| Parameter                                                               | Min | Typ  | Max  | Unit          | Test Conditions/Comments                          |
|-------------------------------------------------------------------------|-----|------|------|---------------|---------------------------------------------------|
| <b>DRIVER</b>                                                           |     |      |      |               |                                                   |
| Differential Output Delay ( $t_{DD}$ )                                  | 600 | 900  | 1400 | ns            | $R_L = 60\ \Omega$ (see Figure 20 and Figure 26)  |
| Differential Output Transition Time ( $t_{TD}$ )                        | 400 | 700  | 1200 | ns            | $R_L = 60\ \Omega$ (see Figure 20 and Figure 26)  |
| Propagation Delay, Low-to-High Level ( $t_{PLH}$ )                      | 700 | 1000 | 1500 | ns            | $R_L = 27\ \Omega$ (see Figure 21 and Figure 27)  |
| Propagation Delay, High-to-Low Level ( $t_{PHL}$ )                      | 700 | 1000 | 1500 | ns            | $R_L = 27\ \Omega$ (see Figure 21 and Figure 27)  |
| $ t_{PLH} - t_{PHL} $ Propagation Delay Skew <sup>1</sup> ( $t_{PDS}$ ) |     | 100  |      | ns            | $R_L = 27\ \Omega$ (see Figure 21 and Figure 27)  |
| <b>DRIVER OUTPUT ENABLE/DISABLE TIMES (ADM3483 ONLY)</b>                |     |      |      |               |                                                   |
| Output Enable Time to Low Level ( $t_{PZL}$ )                           |     | 900  | 1300 | ns            | $R_L = 110\ \Omega$ (see Figure 23 and Figure 29) |
| Output Enable Time to High Level ( $t_{PZH}$ )                          |     | 600  | 800  | ns            | $R_L = 110\ \Omega$ (see Figure 22 and Figure 28) |
| Output Disable Time from High Level ( $t_{PHZ}$ )                       |     | 50   | 80   | ns            | $R_L = 110\ \Omega$ (see Figure 22 and Figure 28) |
| Output Disable Time from Low Level ( $t_{PLZ}$ )                        |     | 50   | 80   | ns            | $R_L = 110\ \Omega$ (see Figure 23 and Figure 29) |
| Output Enable Time from Shutdown to Low Level ( $t_{PSL}$ )             |     | 1.9  | 2.7  | $\mu\text{s}$ | $R_L = 110\ \Omega$ (see Figure 23 and Figure 29) |
| Output Enable Time from Shutdown to High Level ( $t_{PSH}$ )            |     | 2.2  | 3.0  | $\mu\text{s}$ | $R_L = 110\ \Omega$ (see Figure 22 and Figure 28) |

<sup>1</sup> Measured on  $|t_{PLH}(Y) - t_{PHL}(Y)|$  and  $|t_{PLH}(Z) - t_{PHL}(Z)|$ .

**TIMING SPECIFICATIONS—ADM3483/ADM3485/ADM3488/ADM3490/ADM3491**

$V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 5.

| Parameter                                                                  | Min | Typ | Max  | Unit | Test Conditions/Comments                                                                   |
|----------------------------------------------------------------------------|-----|-----|------|------|--------------------------------------------------------------------------------------------|
| <b>RECEIVER</b>                                                            |     |     |      |      |                                                                                            |
| Time to Shutdown ( $t_{SHDN}$ )                                            |     |     |      |      |                                                                                            |
| ADM3483/ADM3485/ADM3491 <sup>1</sup>                                       | 80  | 190 | 300  | ns   |                                                                                            |
| Propagation Delay, Low-to-High Level ( $t_{RPLH}$ )                        |     |     |      |      |                                                                                            |
| ADM3485/ADM3490/ADM3491                                                    | 25  | 65  | 90   | ns   | $V_{ID} = 0\text{ V to }3.0\text{ V}$ , $C_L = 15\text{ pF}$ (see Figure 24 and Figure 30) |
| ADM3483/ADM3488                                                            | 25  | 75  | 120  | ns   |                                                                                            |
| Propagation Delay, High-to-Low Level ( $t_{RPHL}$ )                        |     |     |      |      |                                                                                            |
| ADM3485/ADM3490/ADM3491                                                    | 25  | 65  | 90   | ns   | $V_{ID} = 0\text{ V to }3.0\text{ V}$ , $C_L = 15\text{ pF}$ (see Figure 24 and Figure 30) |
| ADM3483/ADM3488                                                            | 25  | 75  | 120  | ns   |                                                                                            |
| $ t_{PLH} - t_{PHL} $ Propagation Delay Skew ( $t_{RPDS}$ )                |     |     |      |      |                                                                                            |
| ADM3485/ADM3490/ADM3491                                                    |     |     | 10   | ns   | $V_{ID} = 0\text{ V to }3.0\text{ V}$ , $C_L = 15\text{ pF}$ (see Figure 24 and Figure 30) |
| ADM3483/ADM3488                                                            |     |     | 20   | ns   |                                                                                            |
| <b>RECEIVER OUTPUT ENABLE/DISABLE TIMES (ADM3483/ADM3485/ADM3491 ONLY)</b> |     |     |      |      |                                                                                            |
| Output Enable Time to Low Level ( $t_{PRZL}$ )                             |     | 25  | 50   | ns   | $C_L = 15\text{ pF}$ (see Figure 25 and Figure 31)                                         |
| Output Enable Time to High Level ( $t_{PRZH}$ )                            |     | 25  | 50   | ns   | $C_L = 15\text{ pF}$ (see Figure 25 and Figure 31)                                         |
| Output Disable Time from High Level ( $t_{PRHZ}$ )                         |     | 25  | 45   | ns   | $C_L = 15\text{ pF}$ (see Figure 25 and Figure 31)                                         |
| Output Disable Time from Low Level ( $t_{PRLZ}$ )                          |     | 25  | 45   | ns   | $C_L = 15\text{ pF}$ (see Figure 25 and Figure 31)                                         |
| Output Enable Time from Shutdown to Low Level ( $t_{PRSL}$ )               |     | 720 | 1400 | ns   | $C_L = 15\text{ pF}$ (see Figure 25 and Figure 31)                                         |
| Output Enable Time from Shutdown to High Level ( $t_{PRSH}$ )              |     | 720 | 1400 | ns   | $C_L = 15\text{ pF}$ (see Figure 25 and Figure 31)                                         |

<sup>1</sup> The transceivers are put into shutdown by bringing the  $\overline{RE}$  high and DE low. If the inputs are in this state for less than 80 ns, the parts are guaranteed not to enter shutdown. If the parts are in this state for 300 ns or more, the parts are guaranteed to enter shutdown.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 6.**

| Parameter                                      | Rating                                             |
|------------------------------------------------|----------------------------------------------------|
| $V_{CC}$ to GND                                | 7 V                                                |
| Digital I/O Voltage (DE, $\overline{RE}$ , DI) | -0.3 V to +6 V                                     |
| Digital I/O Voltage (RO)                       | $V_{CC} - 0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$ |
| Driver Output/Receiver Input Voltage           | -7.5 V to +12.5 V                                  |
| Operating Temperature Range                    | $-40^\circ\text{C}$ to $+85^\circ\text{C}$         |
| Storage Temperature Range                      | $-65^\circ\text{C}$ to $+125^\circ\text{C}$        |
| $\theta_{JA}$ Thermal Impedance                |                                                    |
| 8-Lead SOIC                                    | 121°C/W                                            |
| 14-Lead SOIC                                   | 86°C/W                                             |
| Lead Temperature                               |                                                    |
| Soldering (10 sec)                             | 300°C                                              |
| Vapor Phase (60 sec)                           | 215°C                                              |
| Infrared (15 sec)                              | 220°C                                              |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.**

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

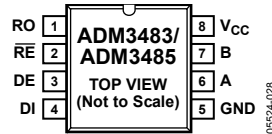


Figure 4. ADM3483/ADM3485 Pin Configuration

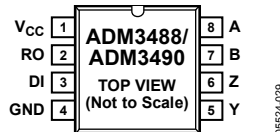


Figure 5. ADM3488/ADM3490 Pin Configuration

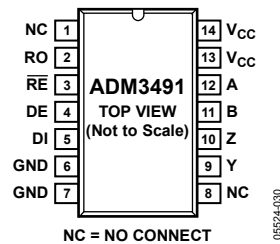


Figure 6. ADM3491 Pin Configuration

Table 7. Pin Function Descriptions

| ADM3483/<br>ADM3485 Pin No. | ADM3488/<br>ADM3490 Pin No. | ADM3491<br>Pin No. | Mnemonic        | Description                                                                                                                                                                                                                                                                                                   |
|-----------------------------|-----------------------------|--------------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                           | 2                           | 2                  | RO              | Receiver Output. When enabled, if $A > B$ by 200 mV, then RO = high. If $A < B$ by 200 mV, then RO = low.                                                                                                                                                                                                     |
| 2                           | Not applicable              | 3                  | $\overline{RE}$ | Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state. If $\overline{RE}$ is high and DE is low, the device enters a low power shutdown mode.                                                                                                 |
| 3                           | Not applicable              | 4                  | DE              | Driver Output Enable. A high level enables the driver differential Output A and Output B. A low level places it in a high impedance state. If $\overline{RE}$ is high and DE is low, the device enters a low power shutdown mode.                                                                             |
| 4                           | 3                           | 5                  | DI              | Driver Input. With a half-duplex part when the driver is enabled, a logic low on DI forces A low and B high while a logic high on DI forces A high and B low. With a full-duplex part when the driver is enabled, a logic low on DI forces Y low and Z high while a logic high on DI forces Y high and Z low. |
| 5                           | 4                           | 6, 7               | GND             | Ground.                                                                                                                                                                                                                                                                                                       |
| Not applicable              | 5                           | 9                  | Y               | Noninverting Driver Output.                                                                                                                                                                                                                                                                                   |
| Not applicable              | 6                           | 10                 | Z               | Inverting Driver Output.                                                                                                                                                                                                                                                                                      |
| 6                           | Not applicable              | Not applicable     | A               | Noninverting Receiver Input A and Noninverting Driver Output A.                                                                                                                                                                                                                                               |
| Not applicable              | 8                           | 12                 | A               | Noninverting Receiver Input A.                                                                                                                                                                                                                                                                                |
| 7                           | Not applicable              | Not applicable     | B               | Inverting Receiver Input B and Inverted Driver Output B.                                                                                                                                                                                                                                                      |
| Not applicable              | 7                           | 11                 | B               | Inverting Receiver Input B.                                                                                                                                                                                                                                                                                   |
| 8                           | 1                           | 13, 14             | V <sub>CC</sub> | Power Supply (3.3 V $\pm$ 0.3 V).                                                                                                                                                                                                                                                                             |
| Not applicable              | Not applicable              | 1, 8               | NC              | No Connect.                                                                                                                                                                                                                                                                                                   |

## TYPICAL PERFORMANCE CHARACTERISTICS

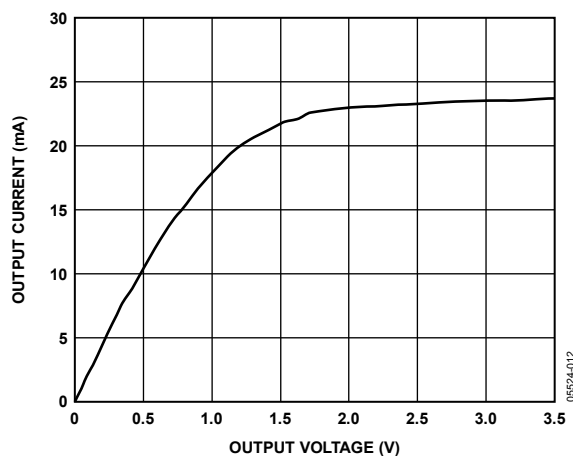


Figure 7. Output Current vs. Receiver Output Low Voltage

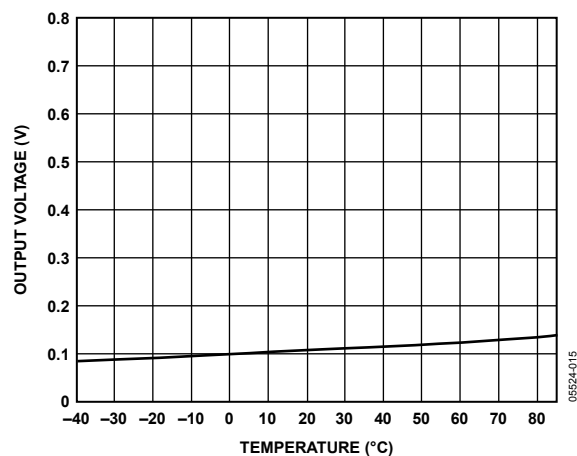
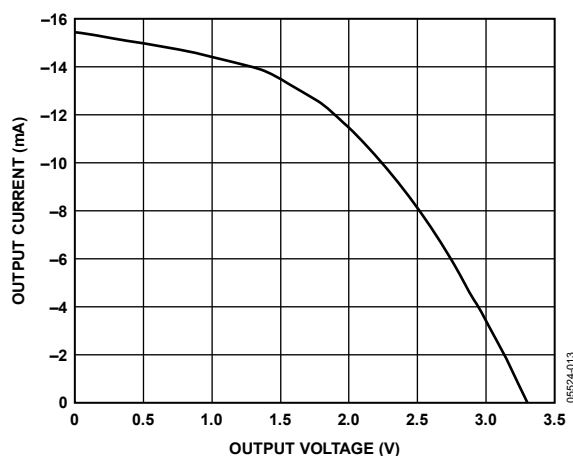
Figure 10. Receiver Output Low Voltage vs. Temperature,  $I_{RO} = 2.5$  mA

Figure 8. Output Current vs. Receiver Output High Voltage

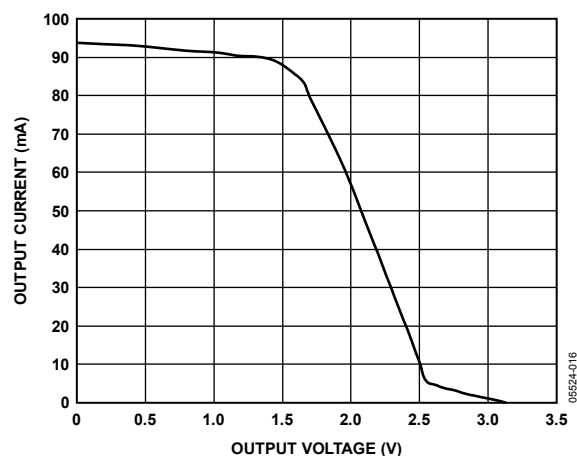
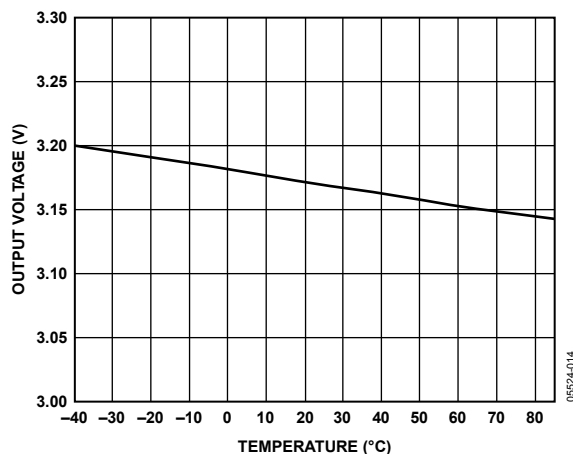
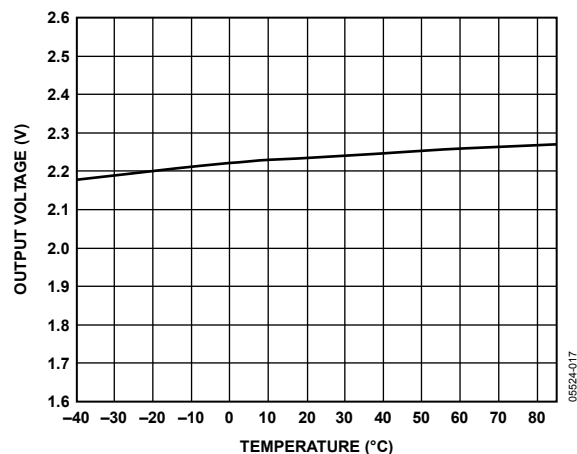


Figure 11. Driver Output Current vs. Differential Output Voltage

Figure 9. Receiver Output High Voltage vs. Temperature,  $I_{RO} = 1.5$  mAFigure 12. Driver Differential Output Voltage vs. Temperature,  $R_L = 54 \Omega$

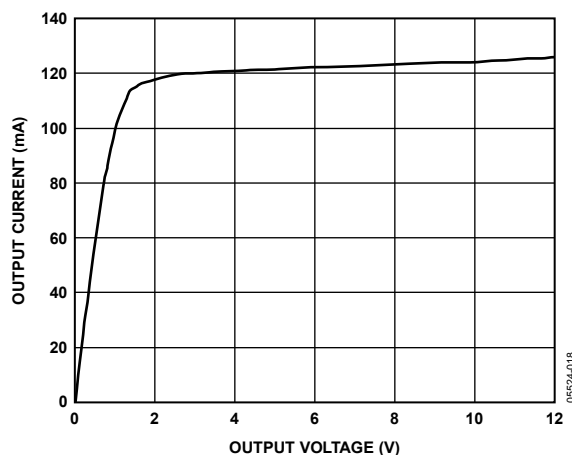


Figure 13. Output Current vs. Driver Output Low Voltage

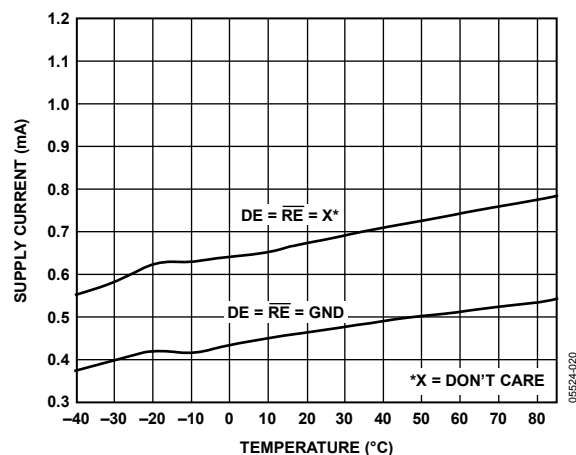


Figure 15. Supply Current vs. Temperature

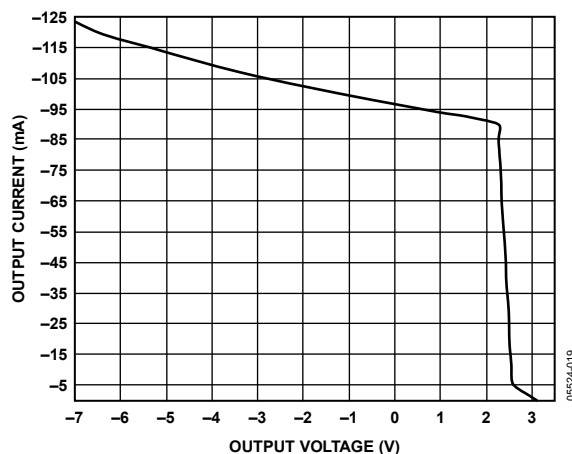


Figure 14. Output Current vs. Driver Output High Voltage

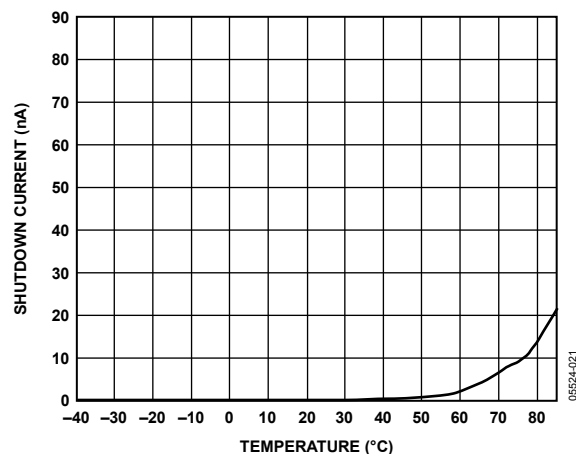


Figure 16. Shutdown Current vs. Temperature

## TEST CIRCUITS

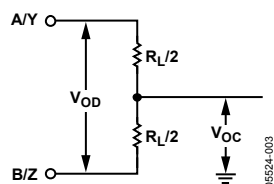


Figure 17. Differential Output Voltage and Common-Mode Voltage Drivers

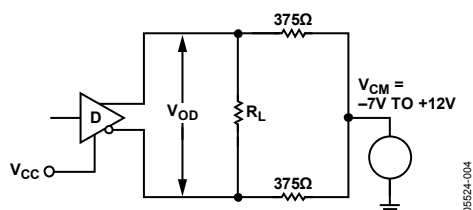


Figure 18. Differential Output Voltage Drivers with Varying Common-Mode Voltage

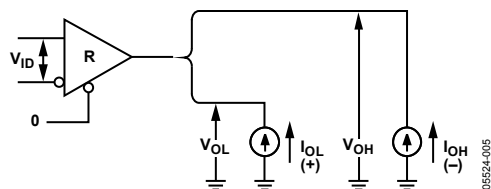
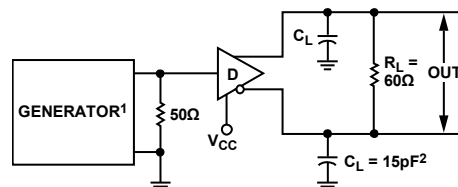
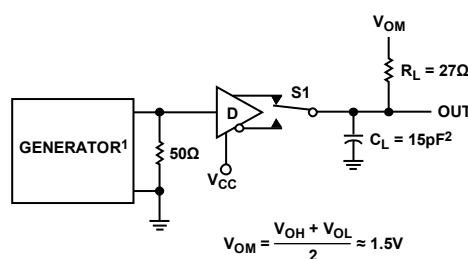


Figure 19. CMOS Output Voltage High and CMOS Output Voltage Low Receivers



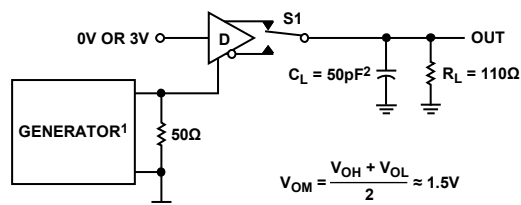
<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 20. Driver Differential Output Delay and Transition Times



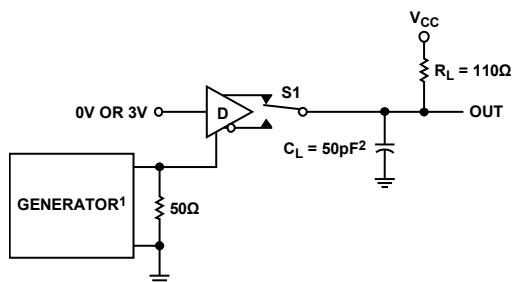
<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 21. Driver Propagation Delays



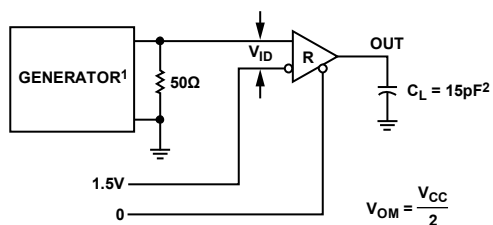
<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 22. Driver Enable and Disable Times ( $t_{PZH}$ ,  $t_{PSH}$ ,  $t_{PHZ}$ )



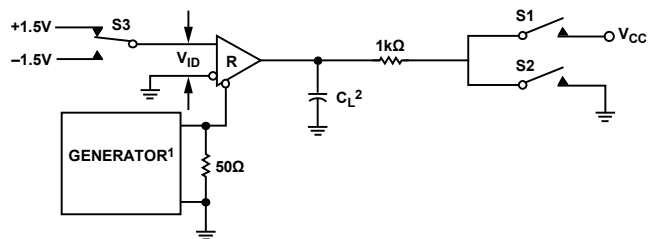
<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 23. Driver Enable and Disable Times ( $t_{PZL}$ ,  $t_{PSL}$ ,  $t_{PLZ}$ )



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 24. Receiver Propagation Delays



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 25. Receiver Enable and Disable Times

## SWITCHING CHARACTERISTICS

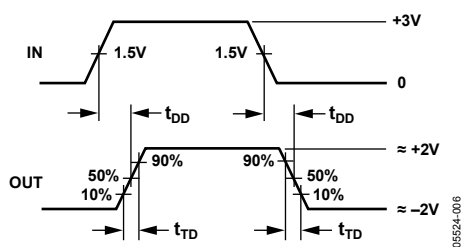


Figure 26. Driver Differential Output Delay and Transition Times

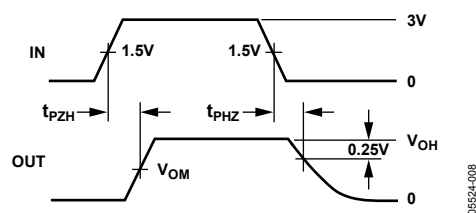
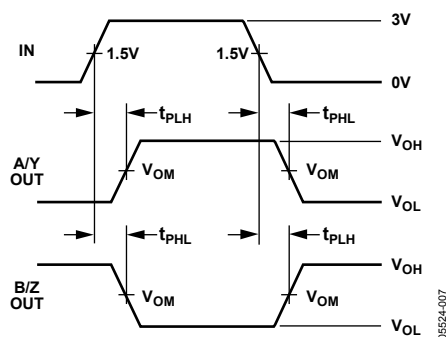
Figure 28. Driver Enable and Disable Times ( $t_{PZH}$ ,  $t_{PSH}$ ,  $t_{PHZ}$ )

Figure 27. Driver Propagation Delays

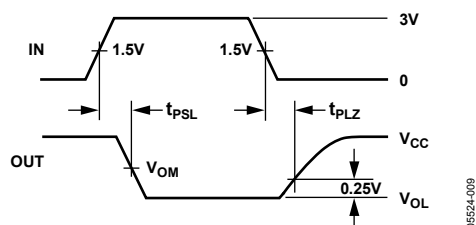
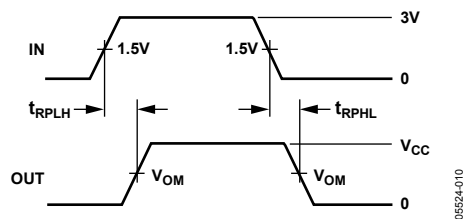
Figure 29. Driver Enable and Disable Times ( $t_{PZL}$ ,  $t_{PSL}$ ,  $t_{PLZ}$ )

Figure 30. Receiver Propagation Delays

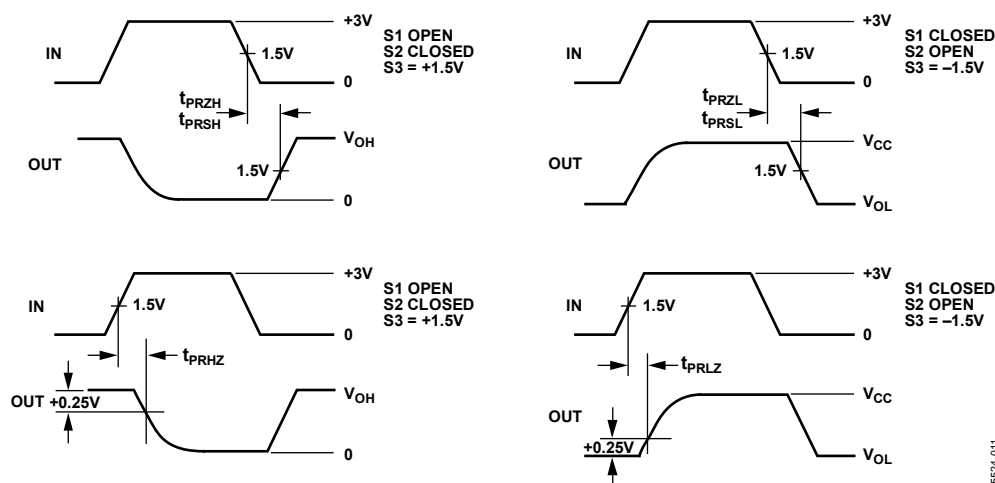


Figure 31. Receiver Enable and Disable Times

## CIRCUIT DESCRIPTION

The ADM3483/ADM3485/ADM3488/ADM3490/ADM3491 are low power transceivers for RS-485 and RS-422 communications. The ADM3483/ADM3488 transmit and receive at data rates up to 250 kbps; the ADM3485/ADM3490/ADM3491 transmit at up to 10 Mbps. The ADM3488/ADM3490/ADM3491 are full-duplex transceivers, while the ADM3483/ADM3485 are half-duplex transceivers. Driver enable (DE) and receiver enable ( $\overline{\text{RE}}$ ) pins are included on the ADM3483/ADM3485/ADM3491. When disabled, the driver and receiver outputs are high impedance.

### DEVICES WITH RECEIVER/DRIVER ENABLES (ADM3483/ADM3485/ADM3491)

Table 8. Transmitting Truth Table

| Transmitting Input     |    |                | Transmitting Output |                     | Mode     |
|------------------------|----|----------------|---------------------|---------------------|----------|
| $\overline{\text{RE}}$ | DE | DI             | B <sup>1</sup>      | A <sup>1</sup>      |          |
| X <sup>2</sup>         | 1  | 1              | 0                   | 1                   | Normal   |
| X <sup>2</sup>         | 1  | 0              | 1                   | 0                   | Normal   |
| 0                      | 0  | X <sup>2</sup> | High-Z <sup>3</sup> | High-Z <sup>3</sup> | Normal   |
| 1                      | 0  | X <sup>2</sup> | High-Z <sup>3</sup> | High-Z <sup>3</sup> | Shutdown |

<sup>1</sup> A and B outputs are Y and Z, respectively, for full-duplex part (ADM3491).

<sup>2</sup> X = don't care.

<sup>3</sup> High-Z = high impedance.

Table 9. Receiving Truth Table

| Receiving Input        |                 |                      | Receiving Output    | Mode     |
|------------------------|-----------------|----------------------|---------------------|----------|
| $\overline{\text{RE}}$ | DE <sup>1</sup> | A – B                | RO                  |          |
| 0                      | 0               | $\geq +0.2\text{ V}$ | 1                   | Normal   |
| 0                      | 0               | $\leq -0.2\text{ V}$ | 0                   | Normal   |
| 0                      | 0               | Inputs Open          | 1                   | Normal   |
| 1                      | 0               | X <sup>2</sup>       | High-Z <sup>3</sup> | Shutdown |

<sup>1</sup> DE is a don't care; X for the full-duplex part (ADM3491).

<sup>2</sup> X = don't care.

<sup>3</sup> High-Z = high impedance.

### DEVICES WITHOUT RECEIVER/DRIVER ENABLES— ADM3488/ADM3490

Table 10. Transmitting Truth Table

| Transmitting Input | Transmitting Output |   |
|--------------------|---------------------|---|
| DI                 | Z                   | Y |
| 1                  | 0                   | 1 |
| 0                  | 1                   | 0 |

Table 11. Receiving Truth Table

| Receiving Input      | Receiving Output |
|----------------------|------------------|
| A – B                | RO               |
| $\geq +0.2\text{ V}$ | 1                |
| $\leq -0.2\text{ V}$ | 0                |
| Inputs open          | 1                |

### REDUCED EMI AND REFLECTIONS (ADM3483/ADM3488)

The ADM3483/ADM3488 are slew rate limited transceivers, minimizing EMI and reducing reflections caused by improperly terminated cables.

### LOW POWER SHUTDOWN MODE (ADM3483/ADM3485/ADM3491)

A low power shutdown mode is initiated by bringing  $\overline{\text{RE}}$  high and DE low. The devices do not shut down unless both the driver and receiver are disabled (high impedance). In shutdown mode, the devices typically draw only 2 nA of supply current. For these devices, the  $t_{\text{PSH}}$  and  $t_{\text{PSL}}$  enable times assume the part is in the low power shutdown mode; the  $t_{\text{PZH}}$  and  $t_{\text{PZL}}$  enable times assume the receiver or driver was disabled, but the part is not shut down.

### DRIVER OUTPUT PROTECTION

Two methods are implemented to prevent excessive output current and power dissipation caused by faults or by bus contention. Current limit protection on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see the Typical Performance Characteristics section). In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively.

### PROPAGATION DELAY

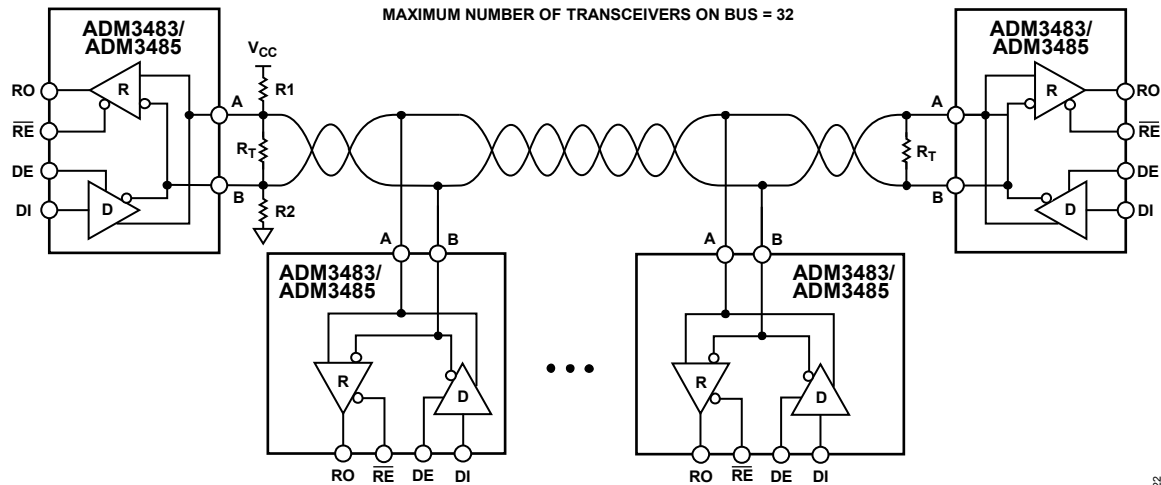
Skew time is the difference between the low-to-high and high-to-low propagation delays. Small driver/receiver skew times help maintain a symmetrical mark-space ratio (50% duty cycle). The receiver skew time ( $|t_{\text{PRLH}} - t_{\text{PRHL}}|$ ) is under 10 ns (20 ns for ADM3483/ADM3488). The driver skew times are 8 ns for ADM3485/ADM3490/ADM3491 and typically under 100 ns for ADM3483/ADM3488.

### TYPICAL APPLICATIONS

The ADM3483/ADM3485/ADM3491 transceivers are designed for half-duplex bidirectional data communications on multipoint bus transmission lines, Figure 32 and Figure 33 show typical network applications circuits. The ADM3488 and the ADM3490 full-duplex transceivers are designed to be used in a daisy-chain network topology or in a point-to-point application, see Figure 34 and Figure 35. The ADM3491 can be used as line repeat Figure 36. To minimize reflections, the line must be terminated at both ends in its characteristic impedance, and stub lengths off the main line must be kept as short as possible. The slew rate limited ADM3483/ADM3488 are more tolerant of imperfect termination.

**LINE LENGTH vs. DATA RATE**

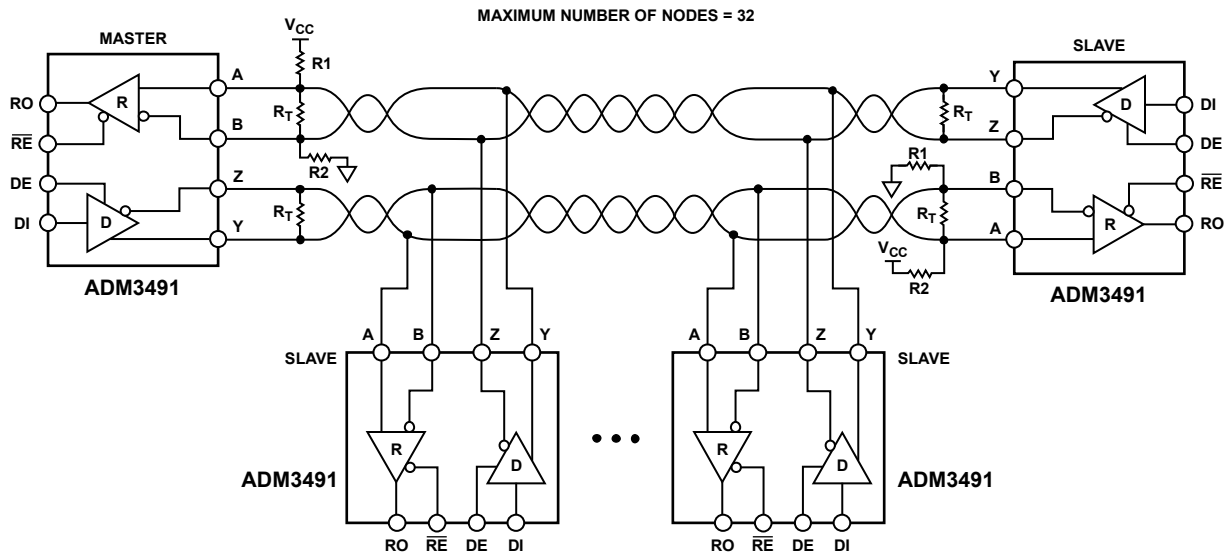
The RS-485 and RS-422 standards cover line lengths up to 4000 feet. For line lengths greater than 4000 feet, see Figure 36.

**NOTES**

1.  $R_T$  IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.

Figure 32. ADM3483/ADM3485 Typical Half-Duplex RS-485 Network

05524-022

**NOTES**

1.  $R_T$  IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.

Figure 33. ADM3491 Typical Full-Duplex RS-485 Network

05524-090

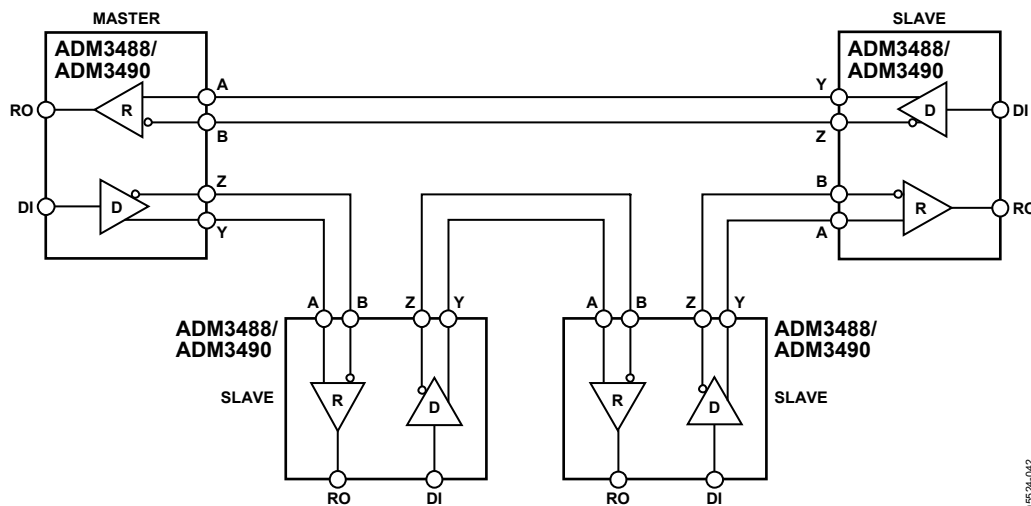


Figure 34. ADM3488/ADM3490 Full-Duplex Daisy-Chain Network

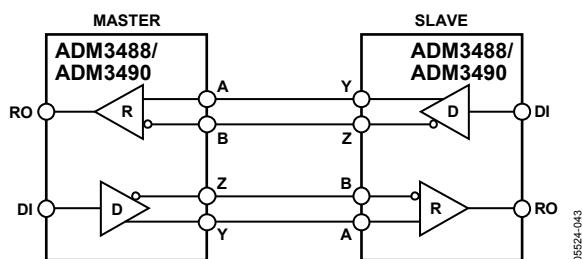
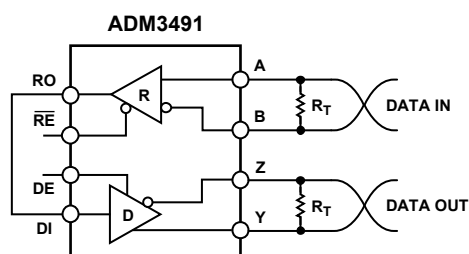


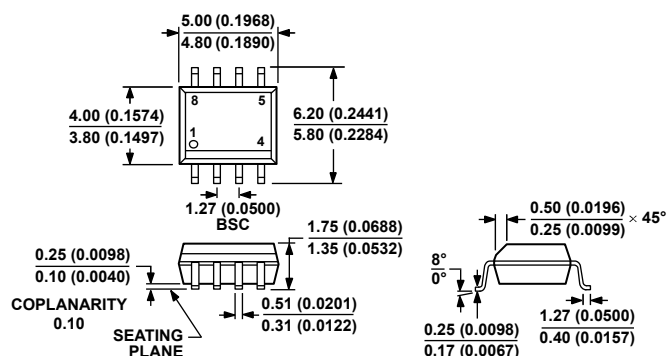
Figure 35. ADM3488/ADM3490 Full-Duplex Point-to-Point Applications



NOTES  
1.  $R_T$  IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.

Figure 36. Line Repeater for ADM3491

## OUTLINE DIMENSIONS

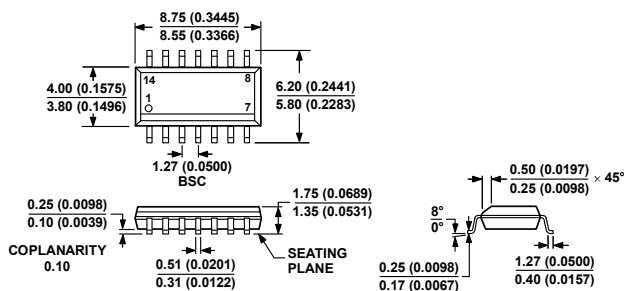


COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 37. 8-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
(R-8)

Dimensions shown in millimeters and (inches)

012407-A



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 38. 14-Lead Narrow Body Small Outline [SOIC\_N]  
Narrow Body  
(R-14)

Dimensions shown in millimeters and (inches)

000006-A

**ORDERING GUIDE**

| Model <sup>1</sup> | Temperature Range | Package Description                        | Package Option | Ordering Quantity |
|--------------------|-------------------|--------------------------------------------|----------------|-------------------|
| ADM3483ARZ         | –40°C to +85°C    | 8-Lead Narrow Body Small Outline (SOIC_N)  | R-8            |                   |
| ADM3483ARZ–REEL7   | –40°C to +85°C    | 8-Lead Narrow Body Small Outline (SOIC_N)  | R-8            | 1,000             |
| ADM3485ARZ         | –40°C to +85°C    | 8-Lead Narrow Body Small Outline (SOIC_N)  | R-8            |                   |
| ADM3485ARZ–REEL7   | –40°C to +85°C    | 8-Lead Narrow Body Small Outline (SOIC_N)  | R-8            | 1,000             |
| ADM3488ARZ         | –40°C to +85°C    | 8-Lead Narrow Body Small Outline (SOIC_N)  | R-8            |                   |
| ADM3488ARZ–REEL7   | –40°C to +85°C    | 8-Lead Narrow Body Small Outline (SOIC_N)  | R-8            | 1,000             |
| ADM3490ARZ         | –40°C to +85°C    | 8-Lead Narrow Body Small Outline (SOIC_N)  | R-8            |                   |
| ADM3490ARZ–REEL7   | –40°C to +85°C    | 8-Lead Narrow Body Small Outline (SOIC_N)  | R-8            | 1,000             |
| ADM3491AR          | –40°C to +85°C    | 14-Lead Narrow Body Small Outline (SOIC_N) | R-14           |                   |
| ADM3491AR–REEL     | –40°C to +85°C    | 14-Lead Narrow Body Small Outline (SOIC_N) | R-14           | 2,500             |
| ADM3491AR–REEL7    | –40°C to +85°C    | 14-Lead Narrow Body Small Outline (SOIC_N) | R-14           | 1,000             |
| ADM3491ARZ         | –40°C to +85°C    | 14-Lead Narrow Body Small Outline (SOIC_N) | R-14           |                   |
| ADM3491ARZ–REEL    | –40°C to +85°C    | 14-Lead Narrow Body Small Outline (SOIC_N) | R-14           | 2,500             |
| ADM3491ARZ–REEL7   | –40°C to +85°C    | 14-Lead Narrow Body Small Outline (SOIC_N) | R-14           | 1,000             |

<sup>1</sup> Z = RoHS Compliant Part.

## NOTES

## NOTES