VND920P

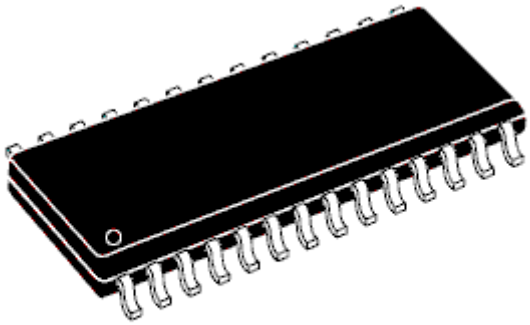
Double channel high side solid state relay

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VND920P	16 mΩ	35 A	36 V(1)

1. Per channel with all the output pins connected to the PCB.

- CMOS compatible input
- Proportional load current sense
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current limitation
- Protection against loss of ground and loss of V_{CC}
- Very low standby power dissipation
- Reverse battery protection (a)



SO-28 (DOUBLE ISLAND)

Description

The VND920P is a double chip device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. Built-in analog current sense output delivers a current proportional to the load current. Device automatically turns off in case of ground pin disconnection

a. See *Figure 8: Application schematic on page 16*

Table 1. Device summary

Package	Tube	Tube (lead free)	Tape and reel	Tape and reel (lead free)
SO-28	VND920P	VND920P-E	VND920P13TR	VND920PTR-E

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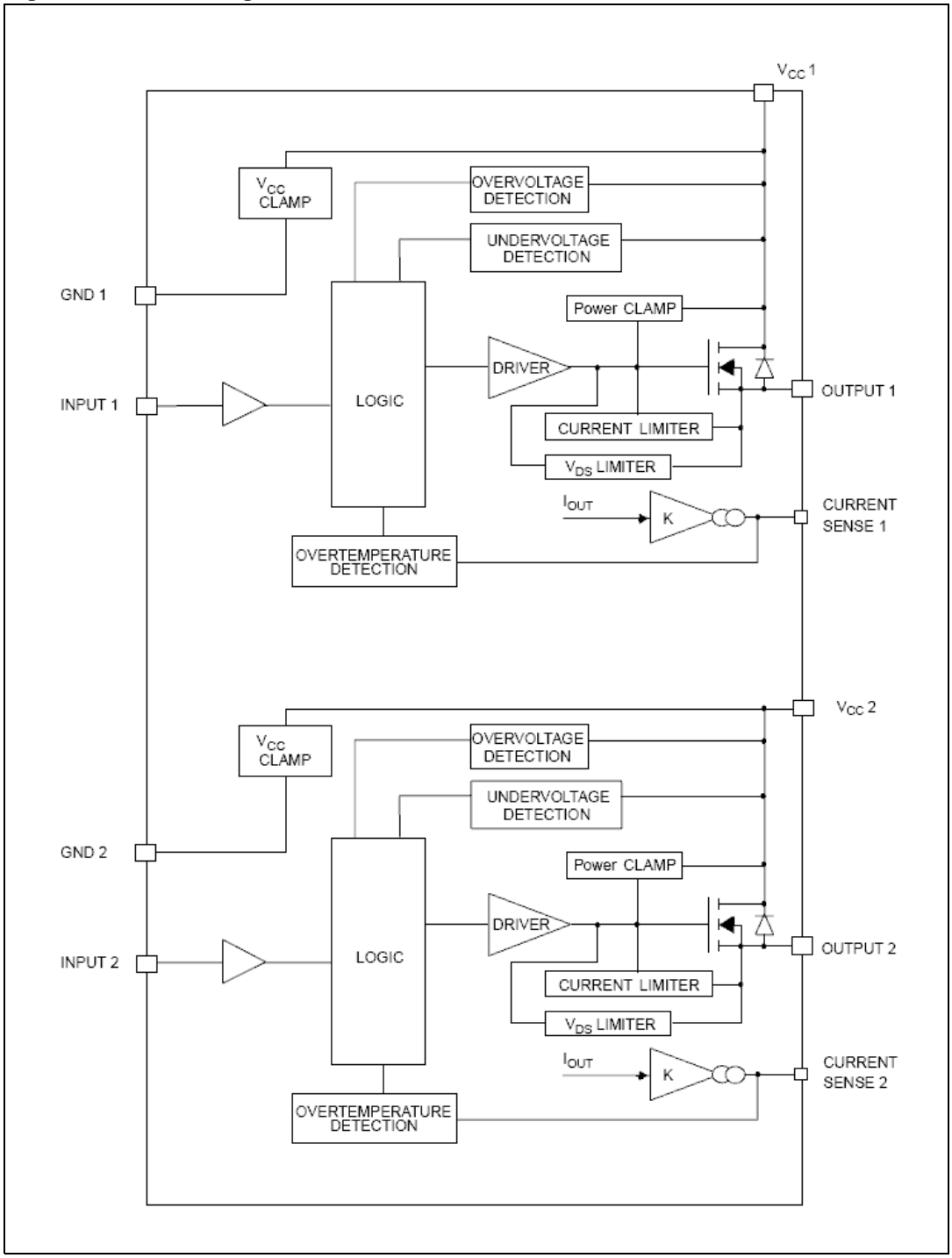
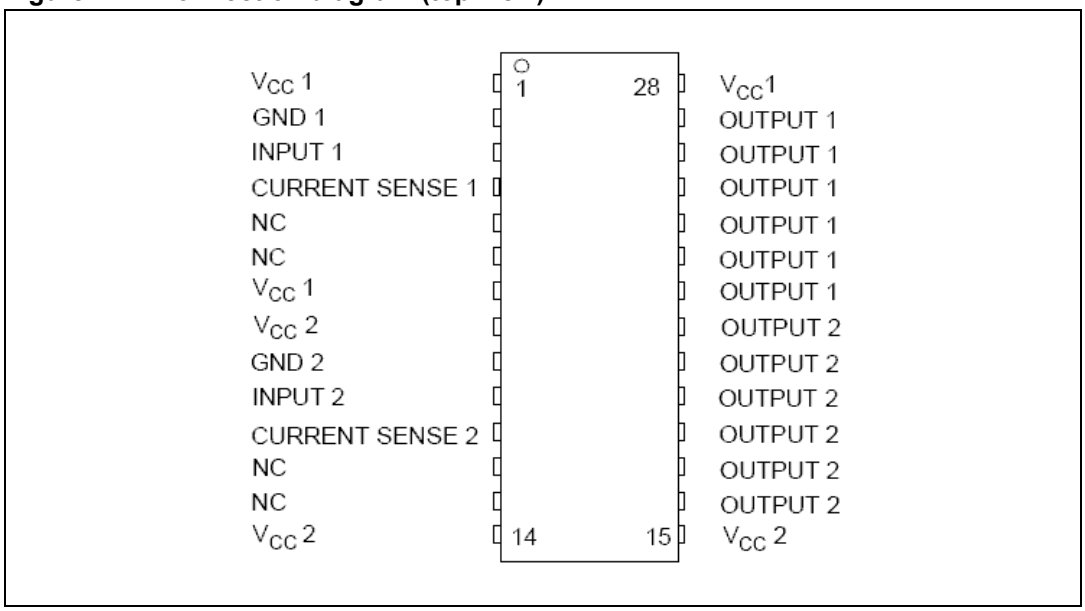
1 Block diagram

Figure 1. Block diagram



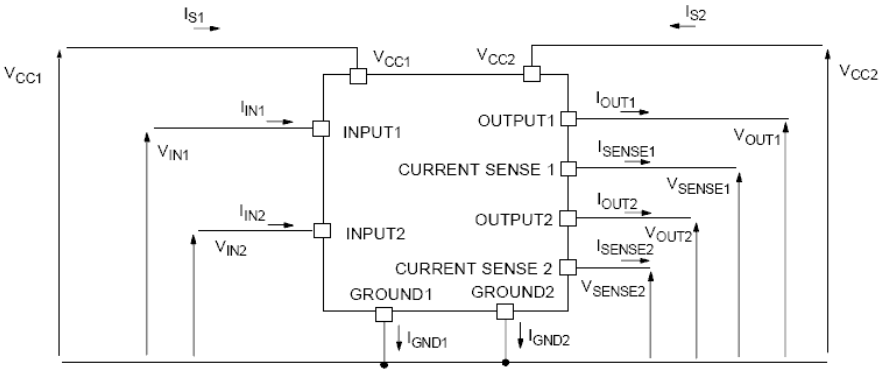
2 Pin description

Figure 2. Connection diagram (top view)



3 Electrical specification

Figure 3. Current and voltage conventions



3.1 Absolute maximum rating

Table 2. Absolute maximum rating (per each channel)

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-21	A
I_{IN}	DC input current	+/-10	mA
V_{CSENSE}	Current sense maximum voltage	-3 +15	V V
V_{ESD}	Electrostatic discharge (human body model: R=1.5 KΩ; C=100 pF) - Input - Current sense - Output - V_{CC}	 4000 2000 5000 5000	 V V V V
E_{MAX}	Maximum switching energy (L=0.25 mH; R_L=0 Ω; V_{bat}=13.5 V; T_{jstart}=150 °C; I_L=45 A)	355	mJ
P_{tot}	Power dissipation $T_l \leq 25$ °C	6.25 (1)	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	- 40 to 150	°C
T_{STG}	Storage temperature	- 55 to 150	°C

1. Per Island

3.2 Thermal data

Table 3. Thermal data (per island)

Symbol	Parameter	Value	Unit
$R_{thj\text{-}lead}$	Thermal resistance junction-lead	20	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (one chip on)	55(1)	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (two chip on)	42(1)	°C/W

1. When mounted on a standard single-sided FR-4 board with 1 cm^2 of Cu (at least 35 µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

3.3 Electrical characteristics

8 V < V_{CC} < 36 V; -40 °C < T_j < 150 °C unless otherwise specified.

Per island.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Power						
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36			V
R_{ON}	On-state resistance	I_{OUT}=10 A; T_j =25 °C I_{OUT}=10 A I_{OUT}=3 A; V_{CC}=6 V			16 32 55	mΩ mΩ mΩ
V_{CLAMP}	Clamp voltage	I_{CC}=20 mA (1)	41	48	55	V
I_S	Supply current	Off-state; V_{CC}=13 V; V_{IN}=V_{OUT}=0 V Off-state; V_{CC}=13 V; V_{IN}=V_{OUT}=0 V; T_j=25 °C On-state; V_{CC}=13 V; V_{IN}=5 V; I_{OUT}=0 A; R_{SENSE}=3.9 KΩ		10 10	25 20 5	µA µA mA
$I_{L(off1)}$	Off-state output current	V_{IN}=V_{OUT}=0 V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN}=0 V; V_{OUT}=3.5 V	-75		0	µA
$I_{L(off3)}$	Off-state output current	V_{IN}=V_{OUT}=0 V; V_{CC}=13 V; T_j=125 °C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN}=V_{OUT}=0 V; V_{CC}=13 V; T_j=25 °C			3	µA
Switching (V_{CC}=13 V)						
$t_{d(on)}$	Turn-on delay time	R_L = 1.3 Ω (see *Figure 5*)		50		µs
$t_{d(off)}$	Turn-off delay time	R_L = 1.3 Ω (see *Figure 5*)		50		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 1.3 Ω (see *Figure 5*)		See relative diagram		V/µs

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 1.3 Ω (see *Figure 5*)		See relative diagram		V/µs
Logic input						
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	V_{IN} = 3.25 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN}=1 mA I_{IN}=-1 mA	6	6.8 -0.7	8	V V
Current sense (9 V ≤ V_{CC} ≤ 16 V) (see *Figure 4*)						
K_1	I_{OUT}/I_{SENSE}	I_{OUT}=1 A; V_{SENSE}=0.5 V; T_j= -40 °C...150 °C	3300	4400	6000	
dK_1/K_1	Current sense ratio drift	I_{OUT}=1 A; V_{SENSE}=0.5 V; T_j= -40 °C...+150 °C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=10 A; V_{SENSE}=4 V; T_j= -40 °C T_j= 25 °C...150 °C	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current sense ratio drift	I_{OUT}=10 A; V_{SENSE}=4 V; T_j= -40 °C...+150 °C	-8		-8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}=30 A; V_{SENSE}=4 V; T_j= -40 °C T_j= 25 °C...150 °C	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current sense ratio drift	I_{OUT}=30 A; V_{SENSE}=4 V; T_j= -40 °C...+150 °C	-6		+6	%
I_{SENSEO}	Analog sense leakage current	V_{CC}=6...16 V; I_{OUT}=0 A; V_{SENSE}=0 V; T_j= -40 °C...+150 °C	0		10	µA
V_{SENSE}	Max analog sense output voltage	V_{CC}=5.5 V; I_{OUT}=5 A; R_{SENSE}=10KΩ V_{CC}>8 V; I_{OUT}=10 A; R_{SENSE}=10KΩ	2 4			V V
V_{SENSEH}	Sense voltage in over temperature conditions	V_{CC}=13 V; R_{SENSE}=3.9 KΩ		5.5		V
$R_{VSENSEH}$	Analog sense output impedance in over temperature condition	V_{CC}=13 V; T_j>T_{TSD}; All channel open		400		Ω
t_{DSENSE}	Current sense delay response	to 90 % I_{SENSE} (2)			500	µs
Protection						
T_{TSD}	Shutdown temperature		150	175	200	°C

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
I_{lim}	DC short circuit current	V_{CC}=13 V 5 V < V_{CC} < 36 V	30	45	75 75	A A
V_{demag}	Turn-off output clamp voltage	I_{OUT}=2 A; V_{IN}=0 V; L=6 mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output voltage drop limitation	I_{OUT}=1 A; T_j=-40 °C....+150 °C		50		mV

1. V_{clamp} and V_{OV} are correlated. Typical difference is 5 V.
2. Current sense signal delay after positive input slope

Note: Sense pin doesn't have to be left floating.

Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT}

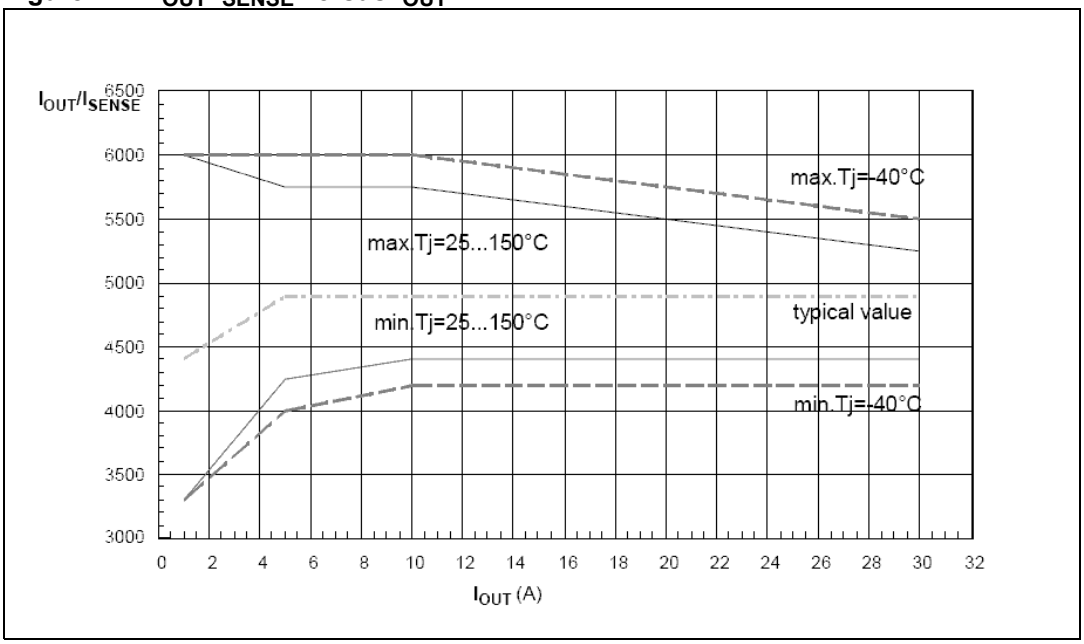


Figure 5. Switching characteristics (resistive load R_L=1.3 Ω)

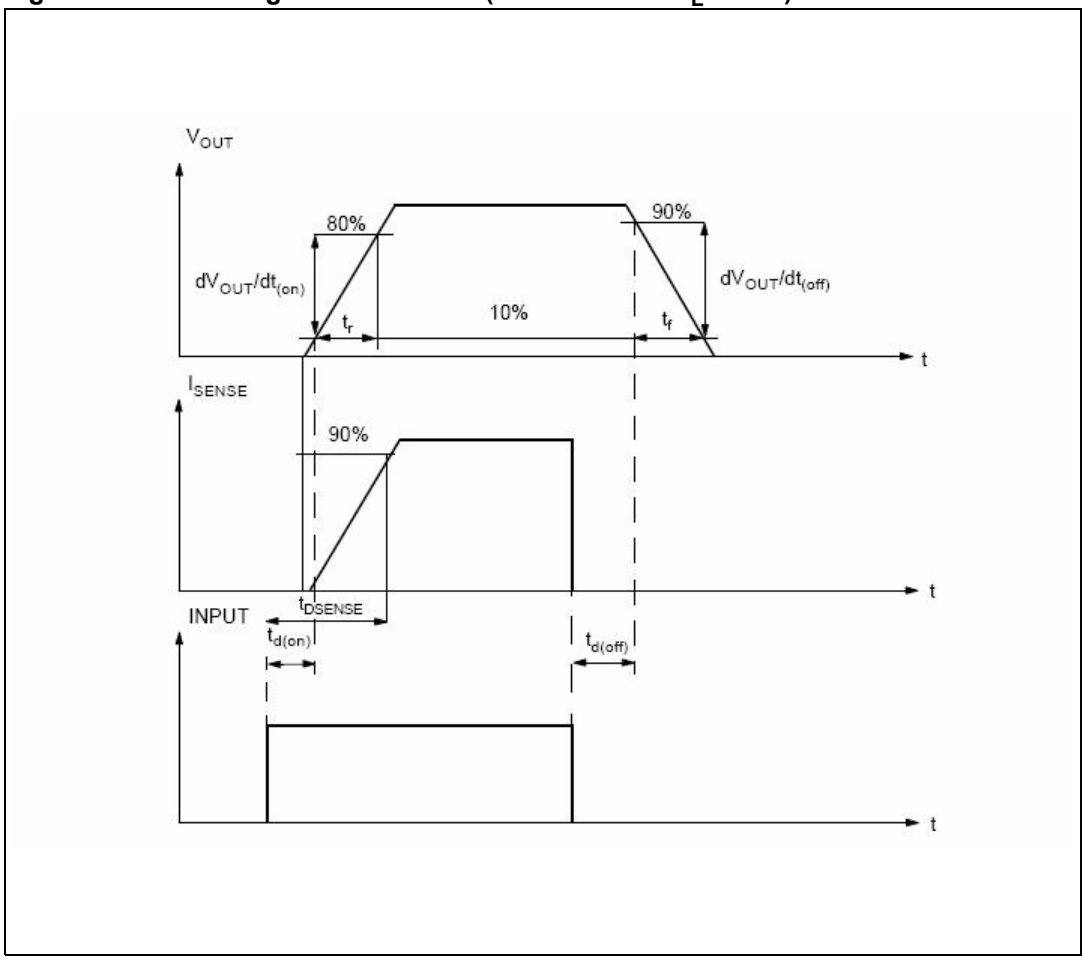
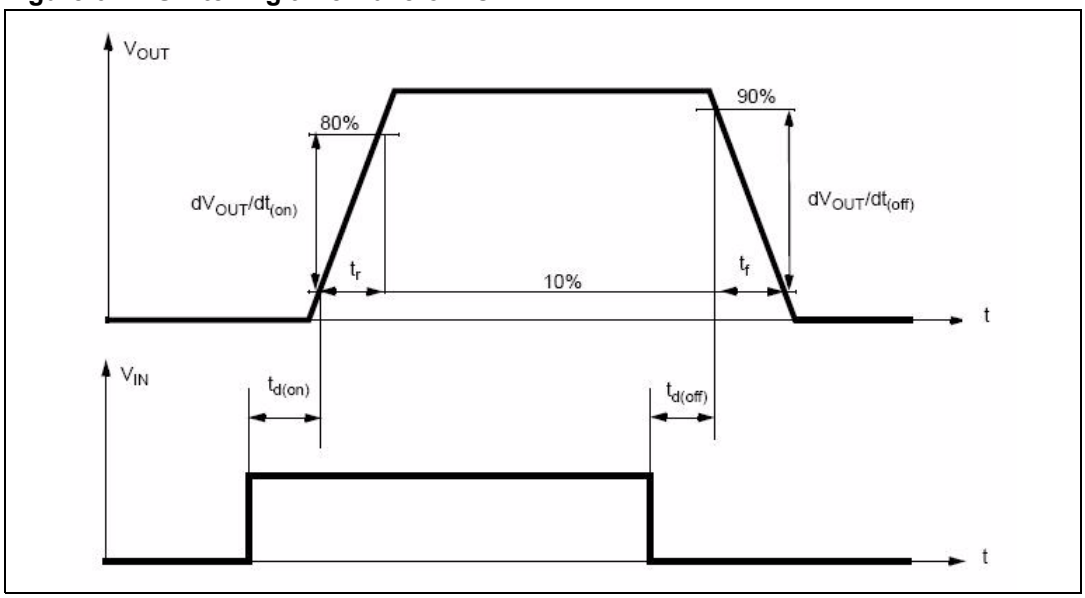


Figure 6. Switching time waveforms



3.4 Truth table

Table 5. Truth table (per each channel)

Condition	Input	Output	Current sense
Normal operation	L H	L H	0 Nominal
Over temperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 ($T_j < T_{TSD}$) 0 ($T_j > T_{TSD}$) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

3.5 Electrical transient requirements

Table 6. Electrical transient requirements (part 1/3)

ISO T/R 7637/1 test pulse	Test levels				
	I	II	III	IV	Delays and impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

Table 7. Electrical transient requirements (part 2/3)

ISO T/R 7637/1 test pulse	Test levels results			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C

Table 7. Electrical transient requirements (part 2/3) (continued)

ISO T/R 7637/1 test pulse	Test levels results			
	I	II	III	IV
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 8. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms

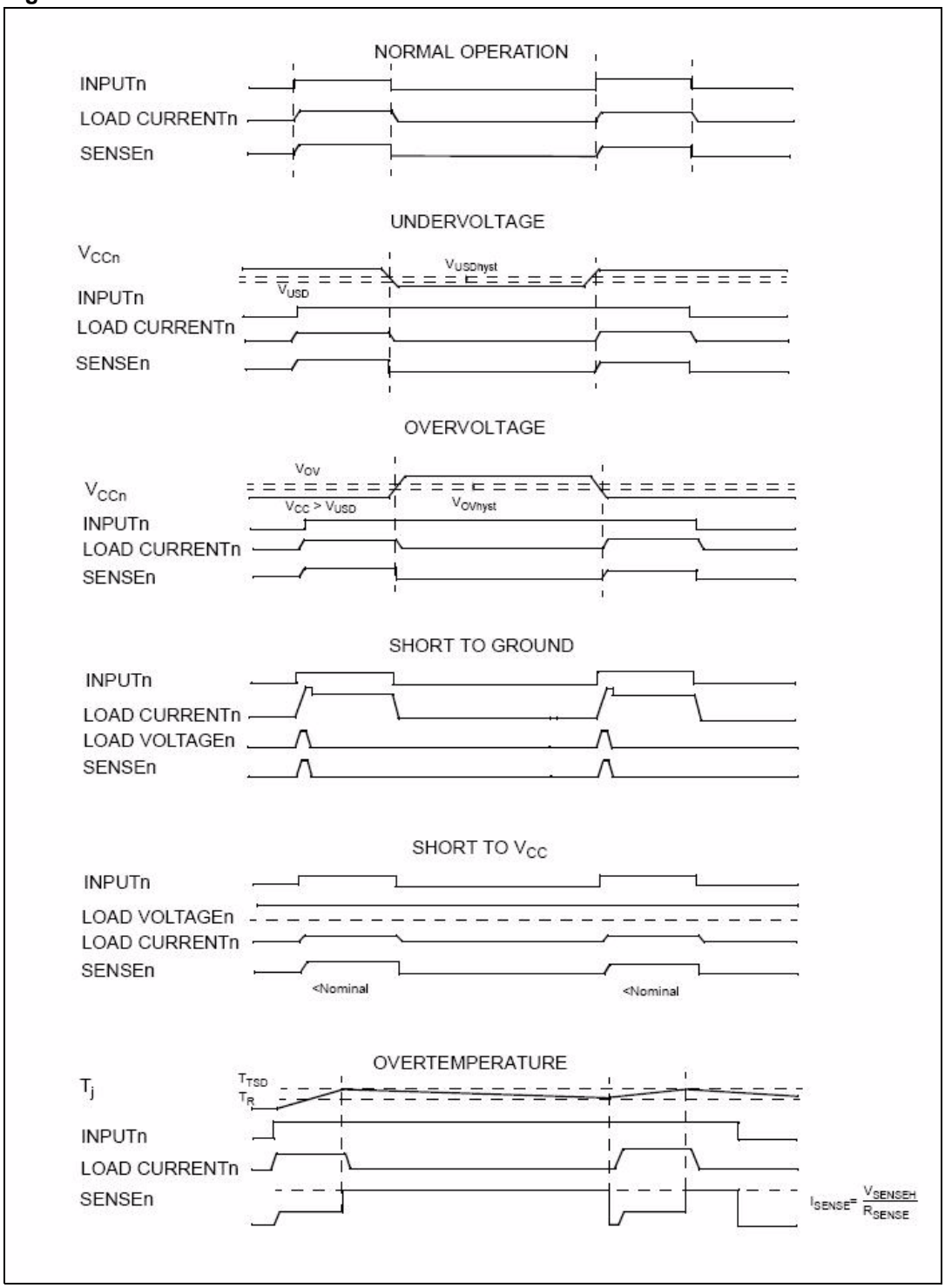
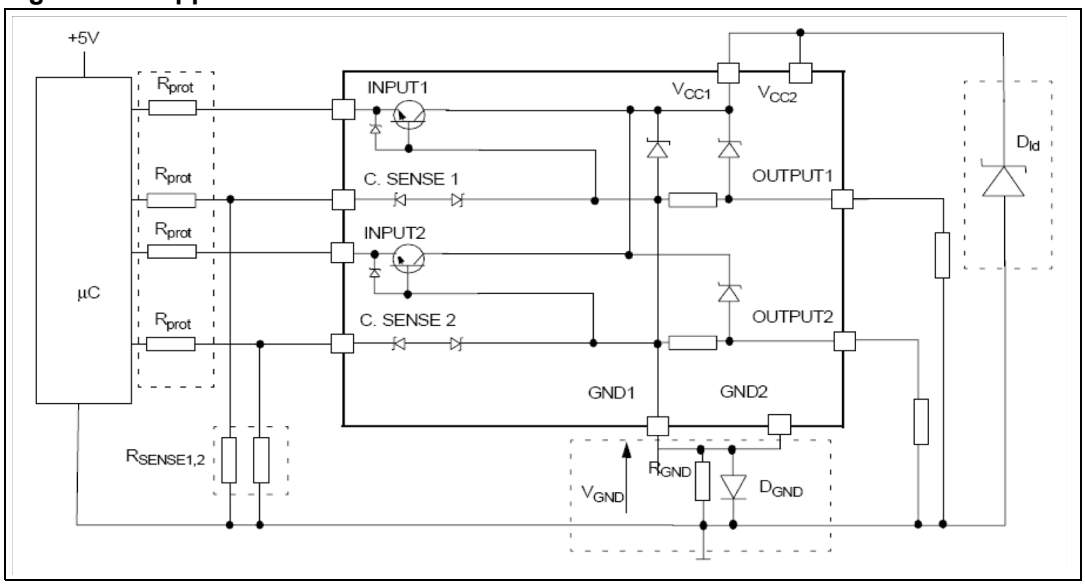


Figure 8. Application schematic



3.5.1 GND protection network against reverse battery

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600\ mV / (I_{S(on)max})$

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet. Power dissipation in R_{GND} (when $V_{CC}<0$: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are on in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line. A resistor (R_{GND}=1 kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≅600 mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in input and status lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused input and status pin is to leave them unconnected.

3.5.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.5.3 µC I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V 5 kΩ $\leq R_{prot} \leq$ 65 kΩ.

Recommended R_{prot} value is 10 kΩ.

Figure 9. Off-state output current

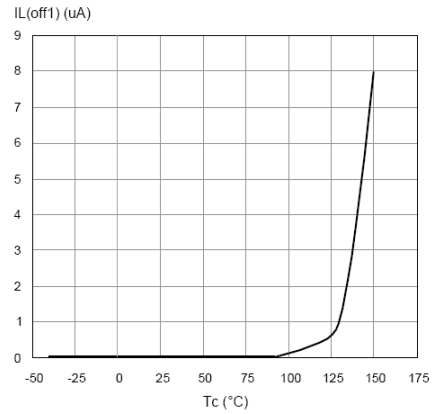


Figure 10. High level input current

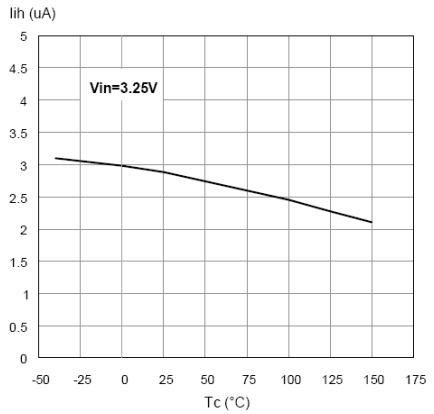


Figure 11. Input clamp voltage

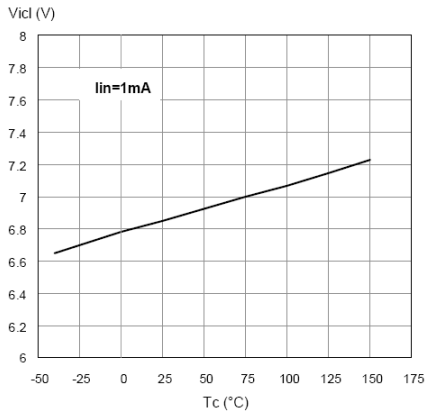


Figure 12. Input high level

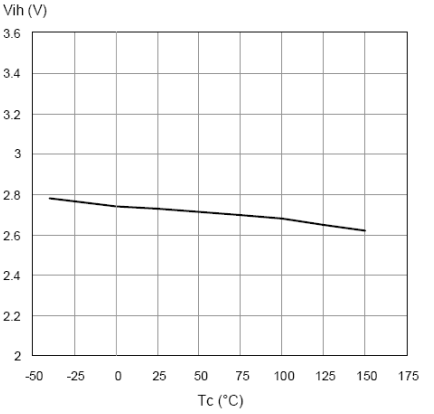


Figure 13. Input low level

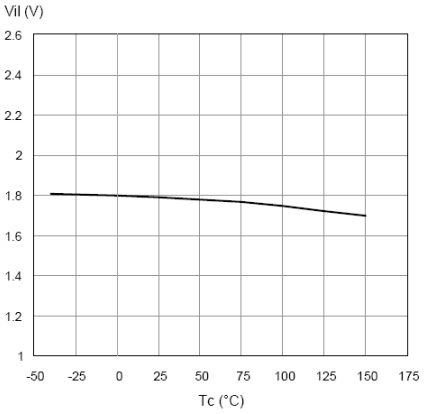


Figure 14. Input hysteresis voltage

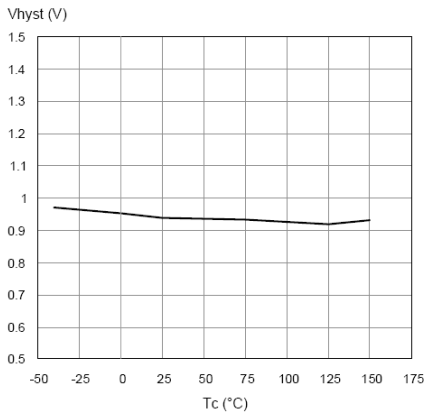


Figure 15. Overvoltage shutdown

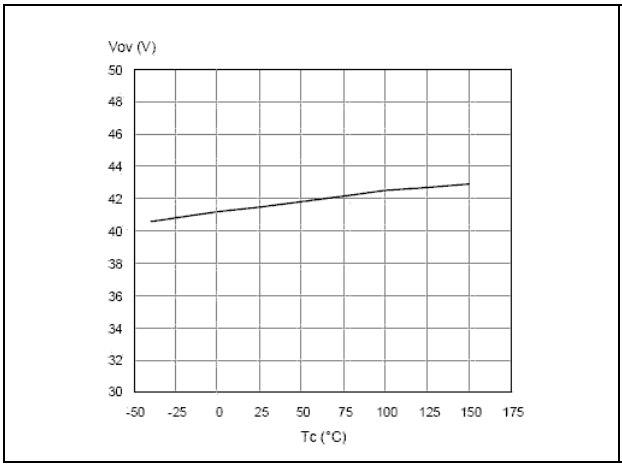


Figure 16. I_{LIM} vs T_{case}

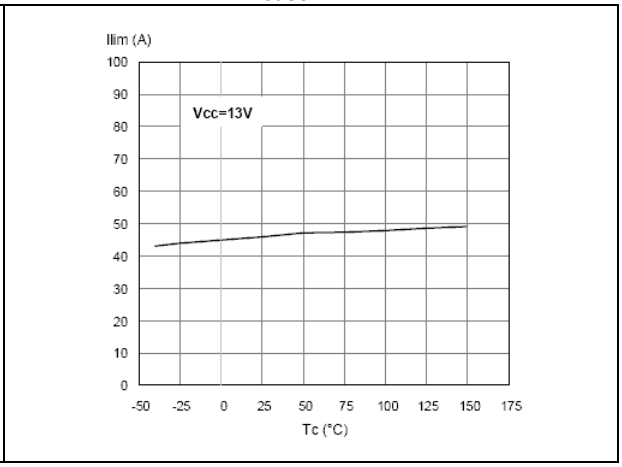


Figure 17. Turn-on voltage slope (part 1/2)

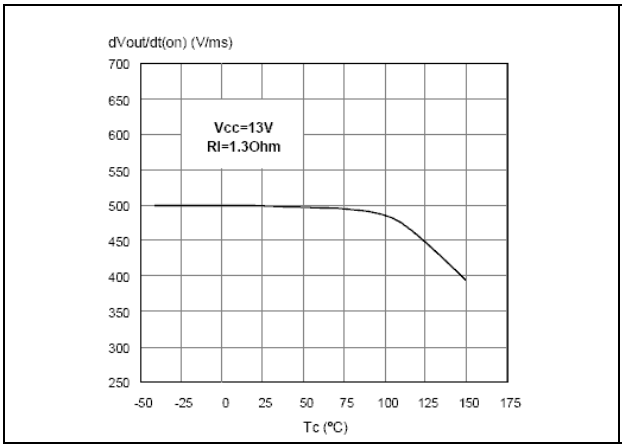


Figure 18. Turn-off voltage slope (part2/2)

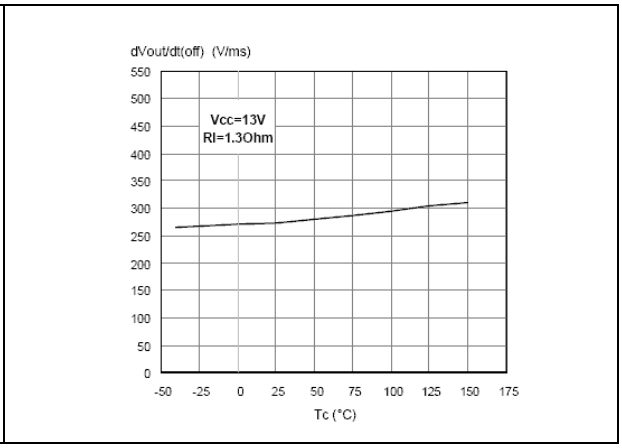


Figure 19. On-state resistance vs T_{case}

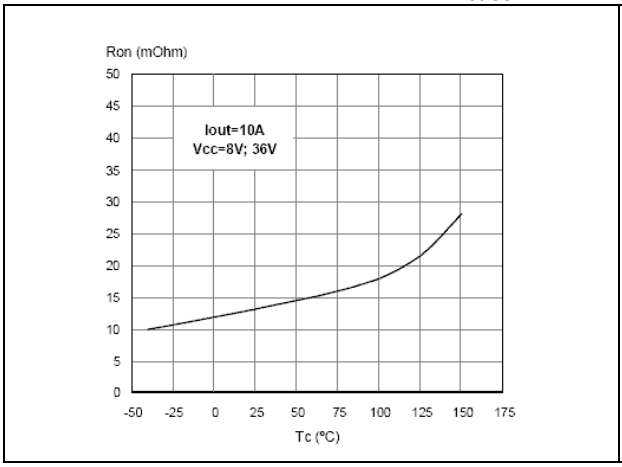


Figure 20. On-state resistance vs V_{CC}

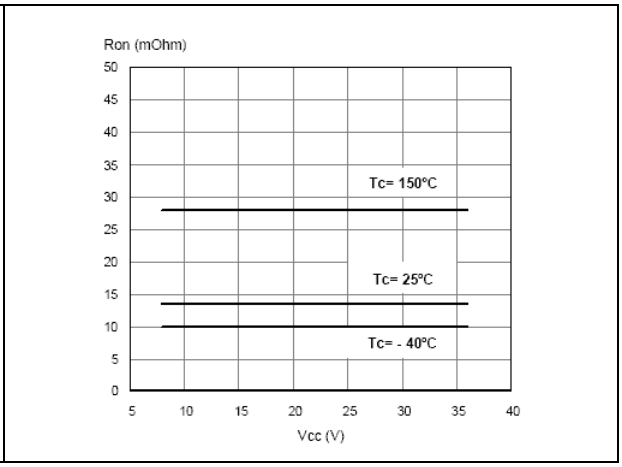
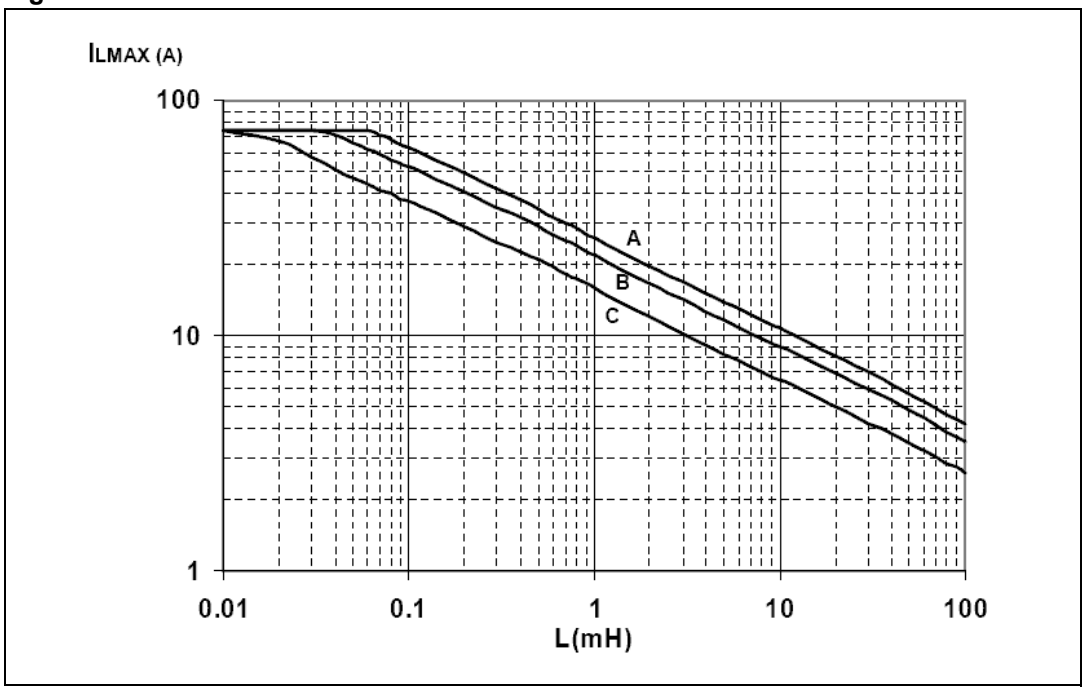


Figure 21. Maximum turn-off current versus load inductance



Legend:

A= Single pulse at T_{Jstart}=150 ºC

B= Repetitive pulse at T_{Jstart}=100 ºC

C= Repetitive pulse at T_{Jstart}=125 ºC

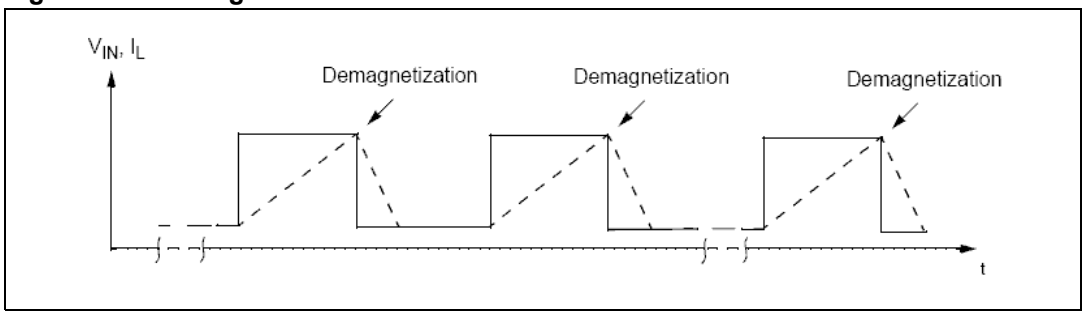
Conditions:

V_{CC}=13.5 V

Values are generated with R_L=0Ω

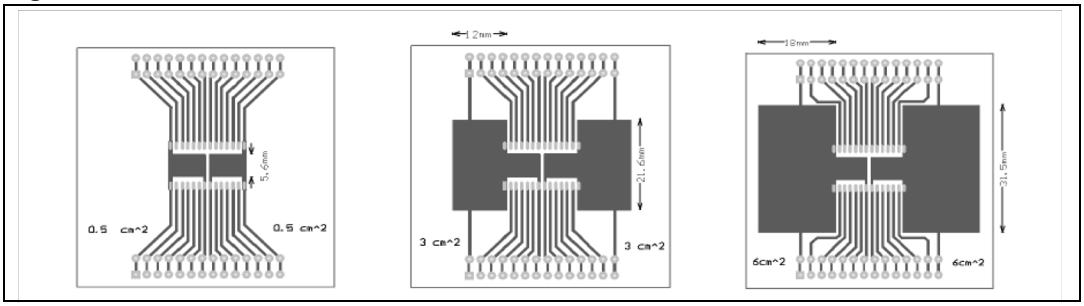
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Figure 22. Demagnetization



4 SO-28 double island thermal data

Figure 23. SO-28 double island PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area=58 mm x 58 mm, PCB thickness=2 mm, Cu thickness=35 µm, Copper areas: 0.5 cm^2, 3 cm^2, 6 cm^2

Table 9. Thermal calculation according to the PCB heatsink area

Chip1	Chip2	T_{jchip1}	T_{jchip2}	Note
On	Off	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
Off	On	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
On	On	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1} = P_{dchip2}$
On	On	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

R_{thA} = Thermal resistance junction to ambient with one chip On

R_{thB} = Thermal resistance junction to ambient with both chips On and $P_{dchip1}=P_{dchip2}$

R_{thC} = Mutual thermal resistance

Figure 24. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

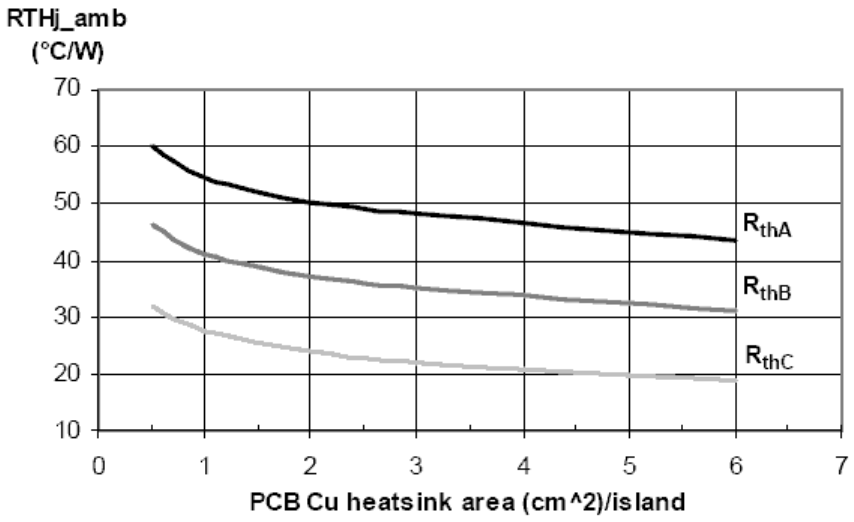


Figure 25. SO-28 thermal impedance junction ambient single pulse

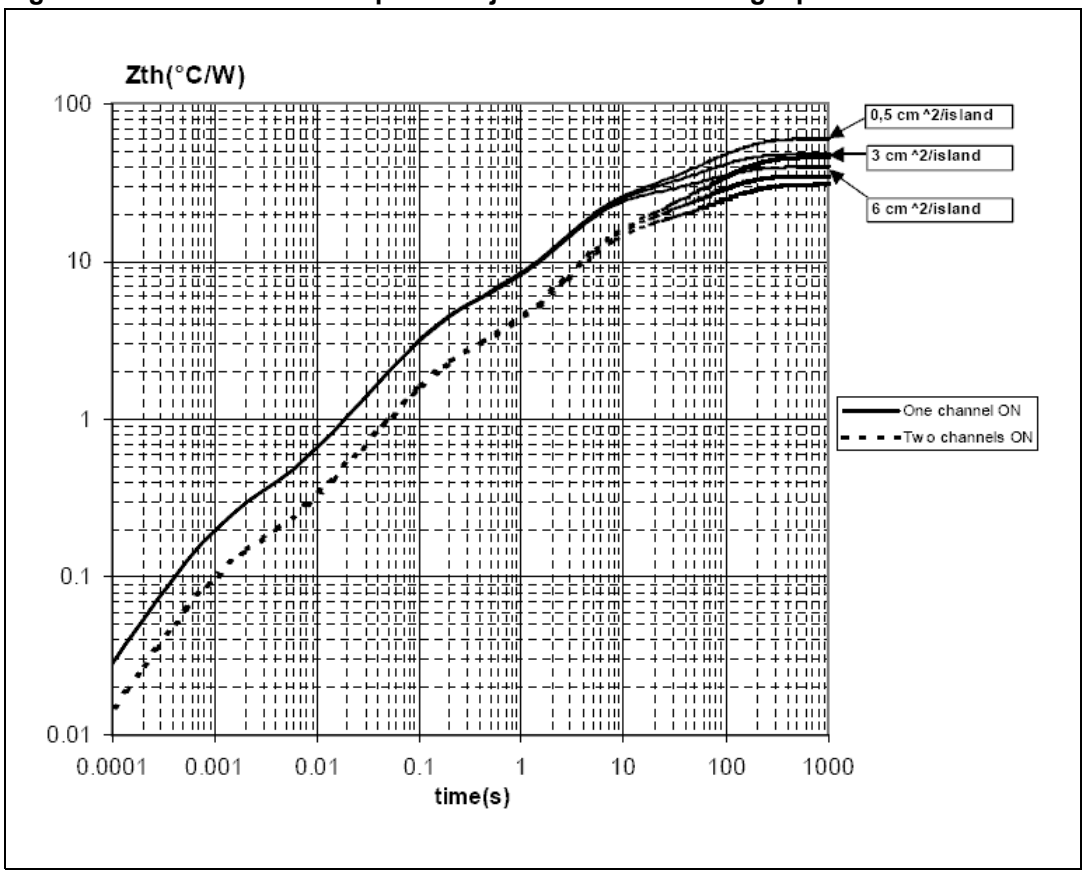
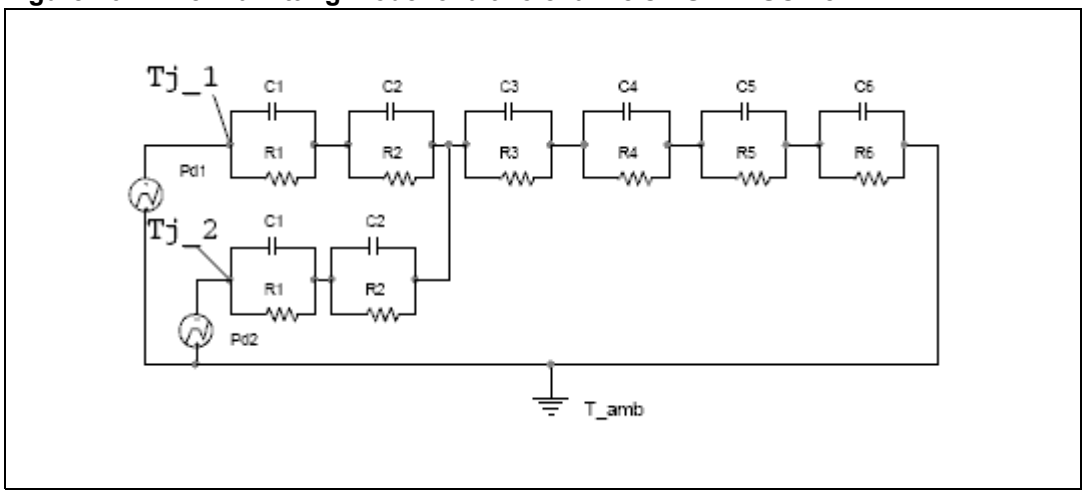


Figure 26. Thermal fitting model of a two channels HSD in SO-28



Pulse calculation formula

$$\delta = R_{TH} \cdot \delta + Z_{THtp}(1$$

where $= t_p /$

Table 10. Thermal parameter

Area/island(cm^2)	0.5	6
R1=(°C/W)	0.02	
R2=(°C/W)	0.1	
R3=(°C/W)	2.2	
R4=(°C/W)	11	
R5=(°C/W)	15	
R6=(°C/W)	30	13
C1=(W.s/°C	0.0015	
C2=(W.s/°C)	7.00E-03	
C3=(W.s/°C)	1.50E-02	
C4=(W.s/°C)	0.2	
C5=(W.s/°C)	1.5	
C6=(W.s/°C)	5	8

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

Figure 27. SO-28 mechanical data

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.30	0.004		0.012
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	17.7		18.1	0.697		0.713
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		16.51			0.650	
F	7.40		7.60	0.291		0.299
L	0.40		1.27	0.016		0.050
S	8 (max.)					

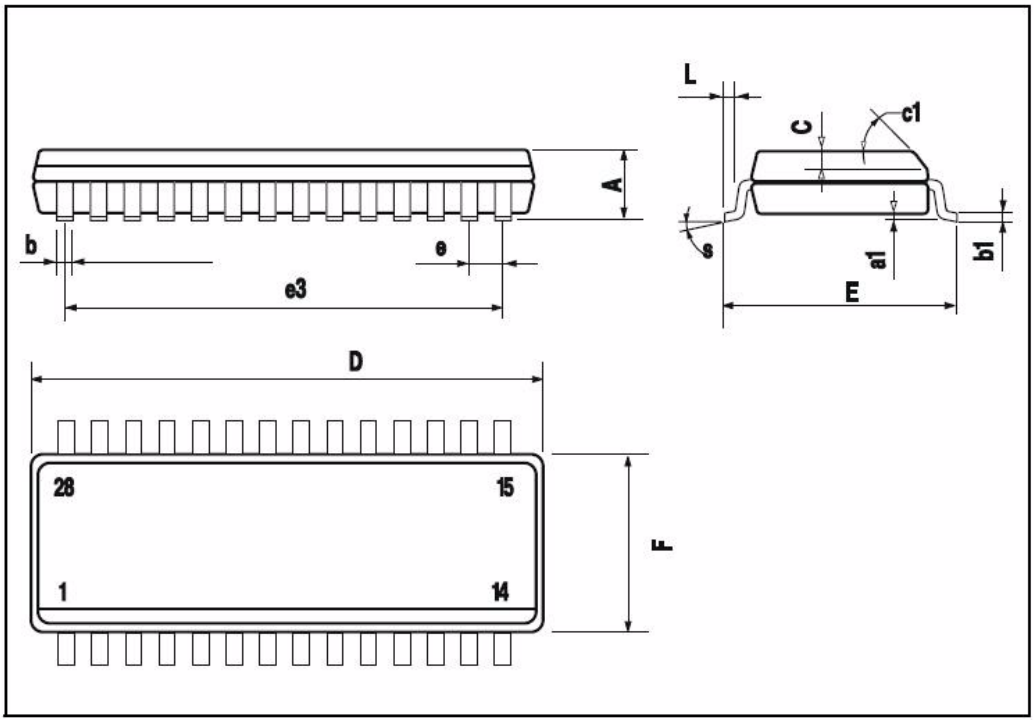
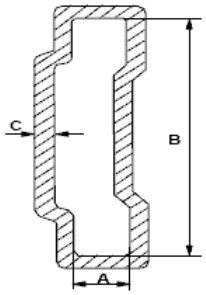


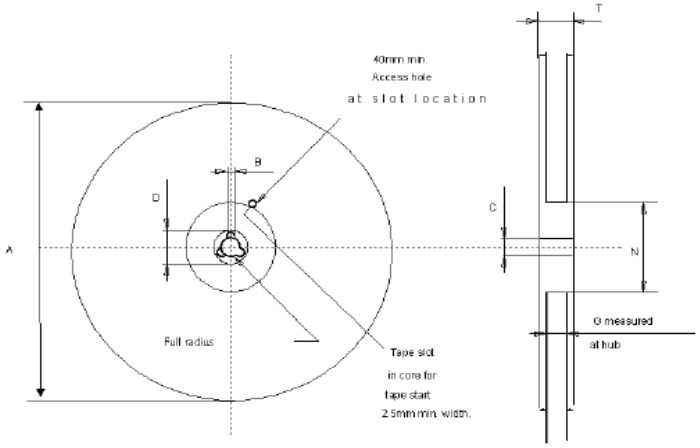
Figure 28. SO-28 tube shipment (no suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 29. Tape and reel shipment (suffix "13TR")



REEL DIMENSIONS

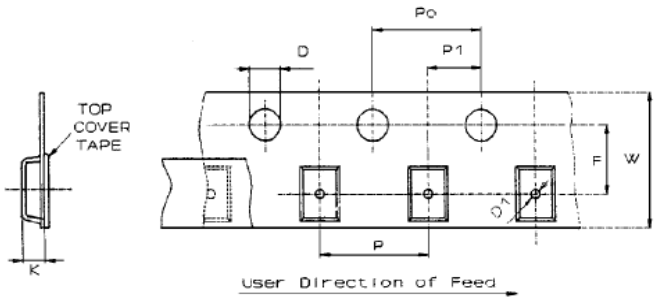
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

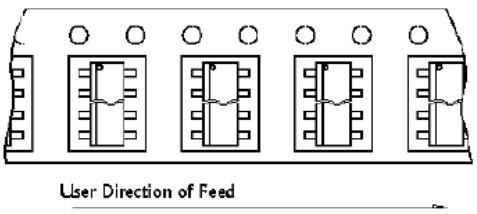
TAPE DIMENSIONS

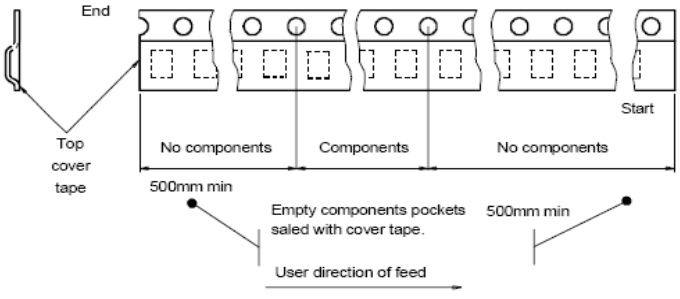
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 11. Document revision history

Date	Revision	Changes
05-Mar-2006	1	Initial release.
16-Apr-2009	2	Document reformatted. Added *Table 1: Device summary on page 1*. Updated *Section 5: Package information on page 24*

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