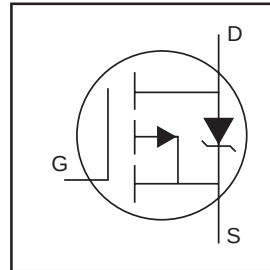


IRF9530NS/L

HEXFET® Power MOSFET

- Advanced Process Technology
- Surface Mount (IRF9530NS)
- Low-profile through-hole (IRF9530NL)
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated



$$V_{DS} = -100V$$

$$R_{DS(on)} = 0.20\Omega$$

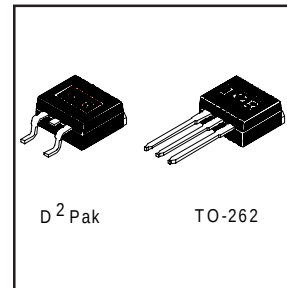
$$I_D = -14A$$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF9530NL) is available for low-profile applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ -10V⑤	-14	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ -10V⑤	-10	
I_{DM}	Pulsed Drain Current ①⑤	-56	
P_D @ $T_A = 25^\circ C$	Power Dissipation	3.8	W
P_D @ $T_C = 25^\circ C$	Power Dissipation	79	W
	Linear Derating Factor	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	250	mJ
I_{AR}	Avalanche Current①	-8.4	A
E_{AR}	Repetitive Avalanche Energy①	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	-5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

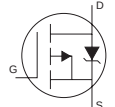
IRF9530NS/L

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V$, $I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.20	Ω	$V_{GS} = -10V$, $I_D = -8.4A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
g_{fs}	Forward Transconductance	3.2	—	—	S	$V_{DS} = -50V$, $I_D = -8.4A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	$V_{DS} = -100V$, $V_{GS} = 0V$
		—	—	-250		$V_{DS} = -80V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	58	nC	$I_D = -8.4A$
Q_{gs}	Gate-to-Source Charge	—	—	8.3		$V_{DS} = -80V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	32		$V_{GS} = -10V$, See Fig. 6 and 13 ④ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = -50V$
t_r	Rise Time	—	58	—		$I_D = -8.4A$
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		$R_G = 9.1\Omega$
t_f	Fall Time	—	46	—		$R_D = 6.2\Omega$, See Fig. 10 ④
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	760	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	260	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	170	—		$f = 1.0MHz$, See Fig. 5 ⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-14	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ① ⑤	—	—	-56		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	$T_J = 25^\circ\text{C}$, $I_S = -8.4A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	130	190	ns	$T_J = 25^\circ\text{C}$, $I_F = -8.4A$
Q_{rr}	Reverse Recovery Charge	—	650	970	nC	$di/dt = -100A/\mu s$ ④ ⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

② Starting $T_J = 25^\circ\text{C}$, $L = 7.0mH$
 $R_G = 25\Omega$, $I_{AS} = -8.4A$. (See Figure 12)

⑤ Uses IRF9530N data and test conditions

③ $I_{SD} \leq -8.4A$, $di/dt \leq -490A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

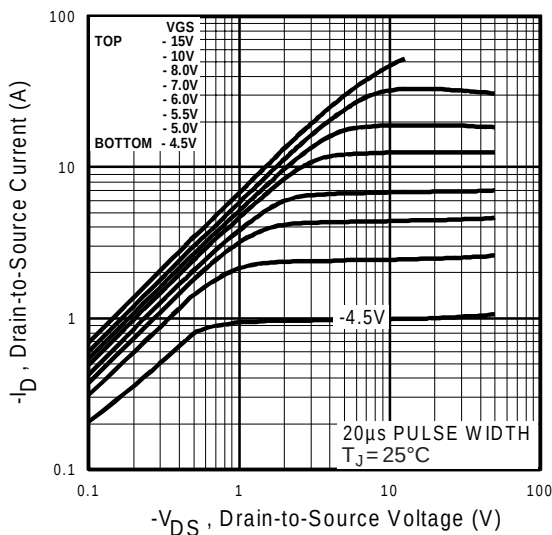


Fig 1. Typical Output Characteristics

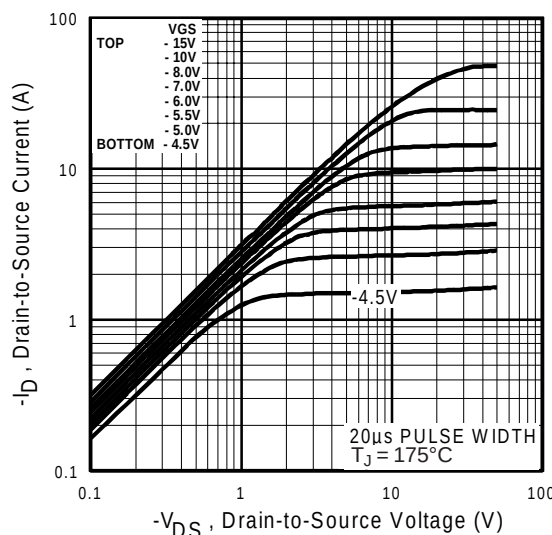


Fig 2. Typical Output Characteristics

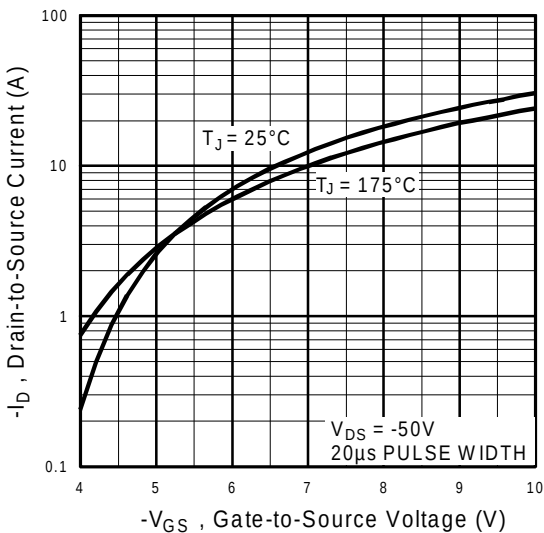


Fig 3. Typical Transfer Characteristics

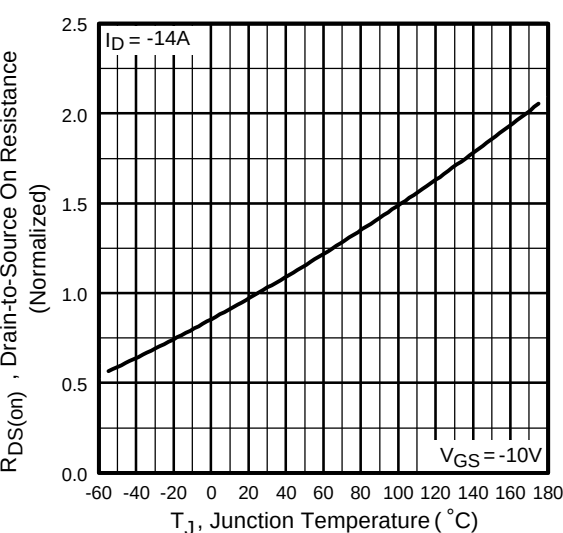


Fig 4. Normalized On-Resistance Vs. Temperature

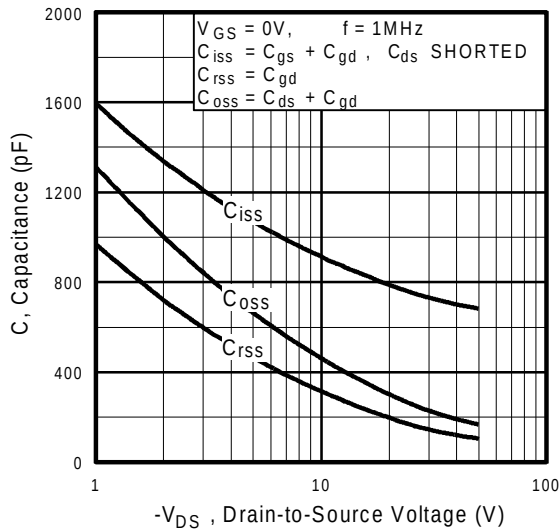


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

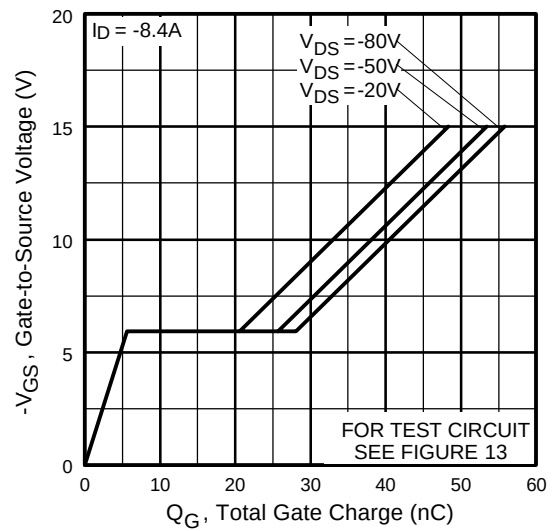


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

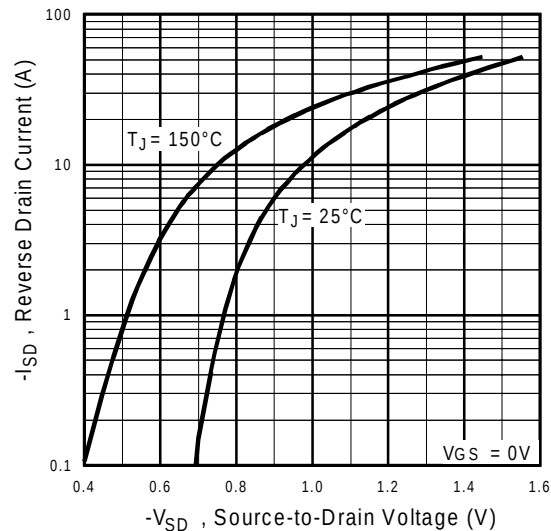


Fig 7. Typical Source-Drain Diode Forward Voltage

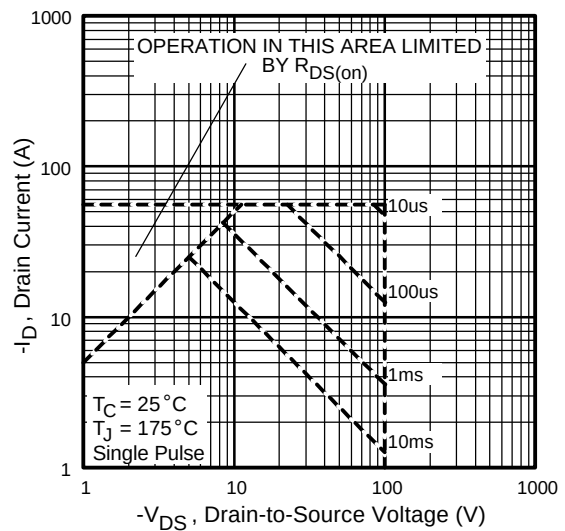


Fig 8. Maximum Safe Operating Area

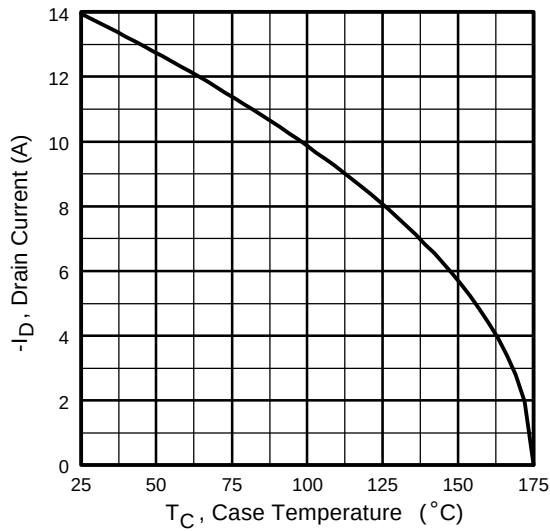


Fig 9. Maximum Drain Current Vs. Case Temperature

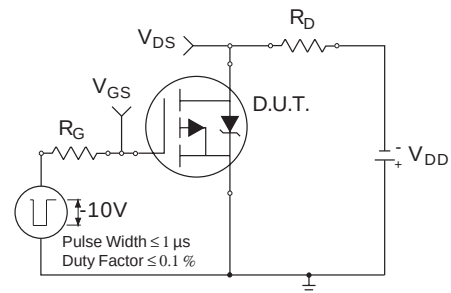


Fig 10a. Switching Time Test Circuit

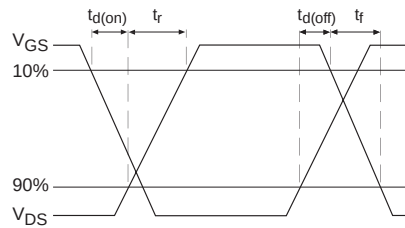


Fig 10b. Switching Time Waveforms

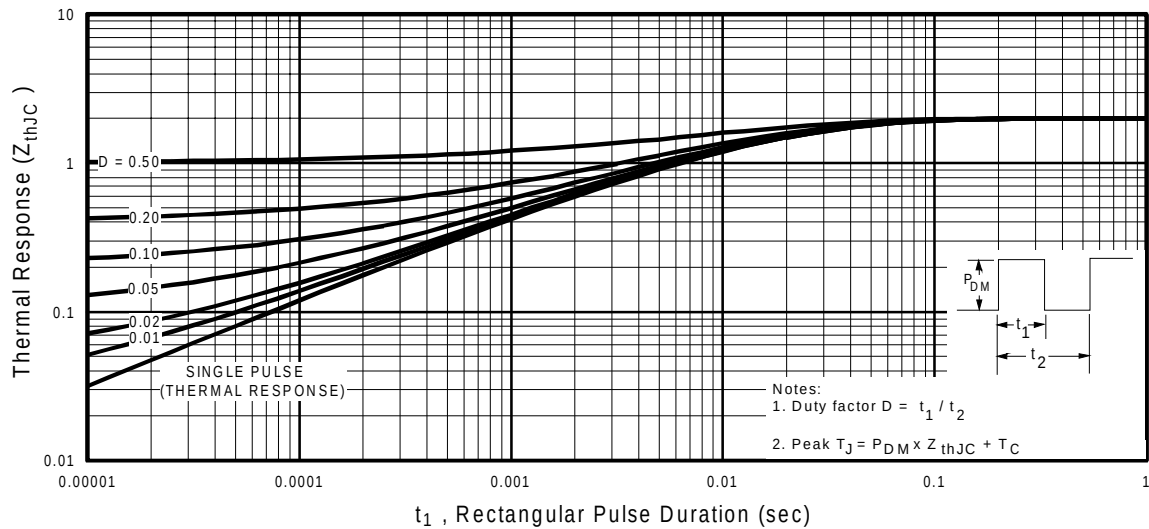


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

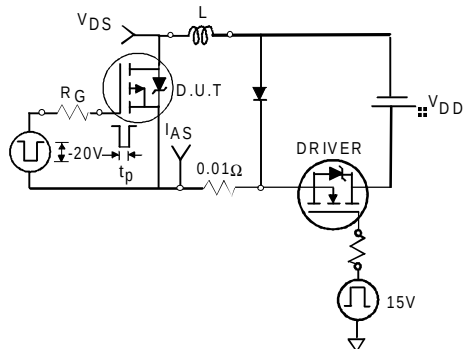


Fig 12a. Unclamped Inductive Test Circuit

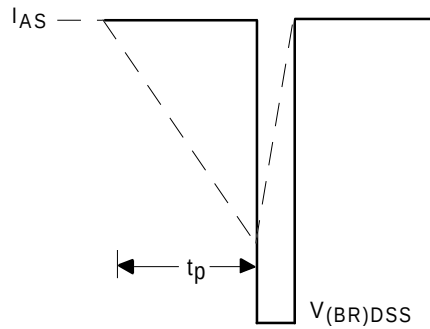


Fig 12b. Unclamped Inductive Waveforms

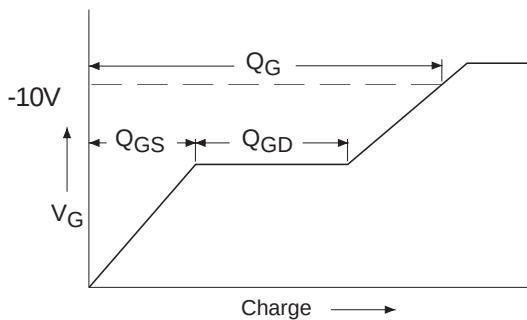


Fig 13a. Basic Gate Charge Waveform

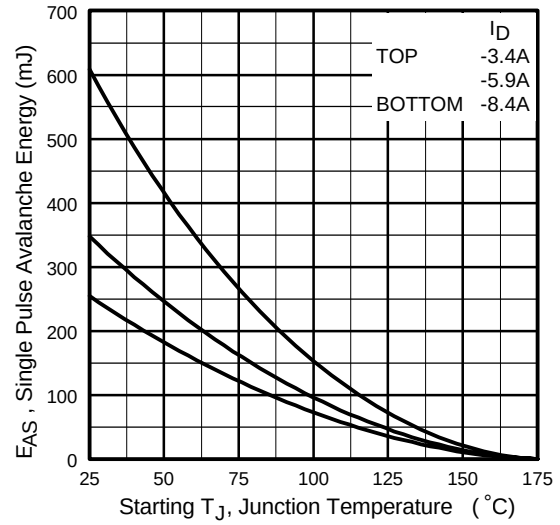


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

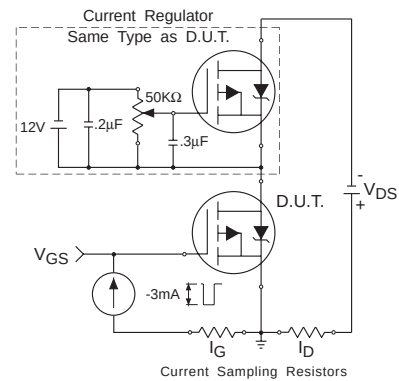
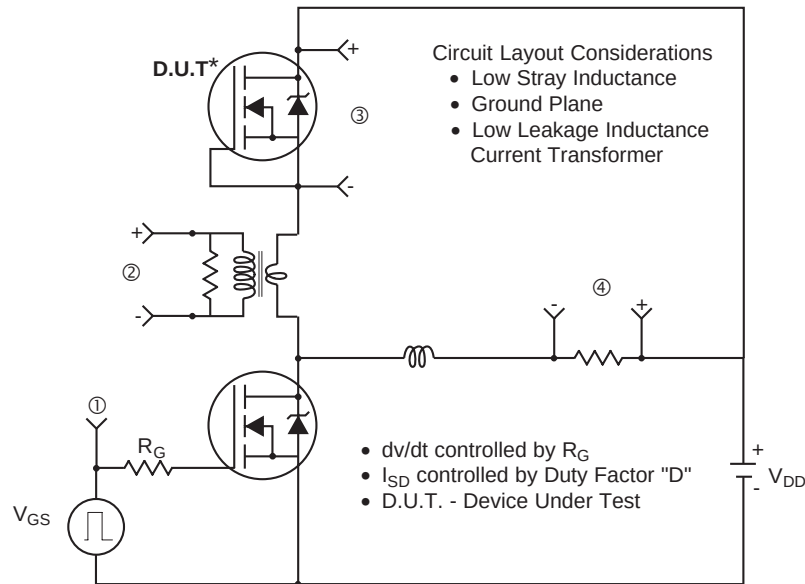
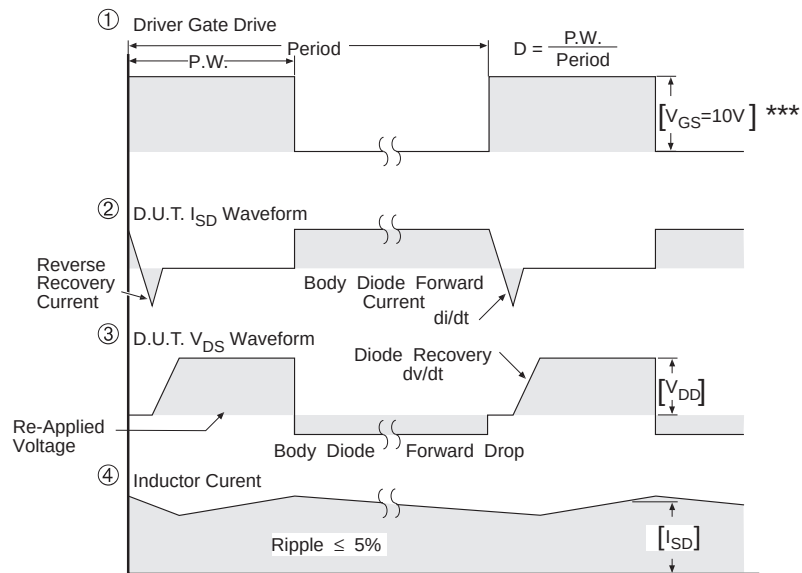


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

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The technical drawing illustrates the dimensions for a 3-lead gate array package. It includes three views: a top view, a side view, and a minimum recommended footprint.

Top View Dimensions:

- Overall width: 10.54 (.415) and 10.29 (.405)
- Lead pitch: 1.40 (.055) MAX.
- Lead width: 1.78 (.070) and 1.27 (.050)
- Lead spacing: 1.40 (.055) and 1.14 (.045)
- Lead length: 5.08 (.200)
- Lead thickness: 0.93 (.037) and 0.69 (.027)
- Lead diameter: 0.25 (.010)
- Lead material: (M)
- Lead finish: (B)
- Lead plating: (A)
- Lead coating: (M)

Side View Dimensions:

- Overall height: 4.69 (.185) and 4.20 (.165)
- Lead height: 1.32 (.052) and 1.22 (.048)
- Lead width: 2.79 (.110) and 2.29 (.090)
- Lead length: 5.28 (.208) and 4.78 (.188)
- Lead thickness: 0.55 (.022) and 0.46 (.018)
- Lead diameter: 1.39 (.055) and 1.14 (.045)

Minimum Recommended Footprint Dimensions:

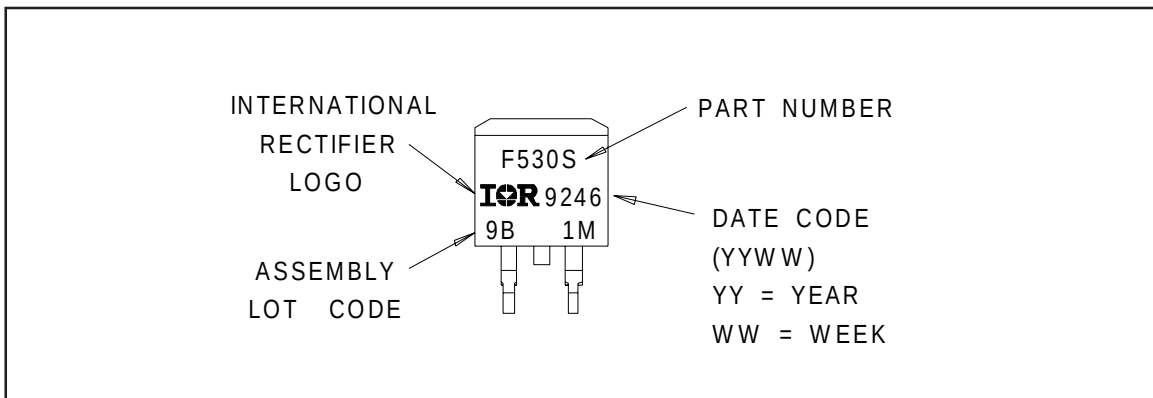
- Overall width: 10.16 (.400) REF.
- Lead width: 6.47 (.255) and 6.18 (.243)
- Lead length: 2.61 (.103) and 2.32 (.091)
- Lead diameter: 8.89 (.350) REF.

Lead Assignments:

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

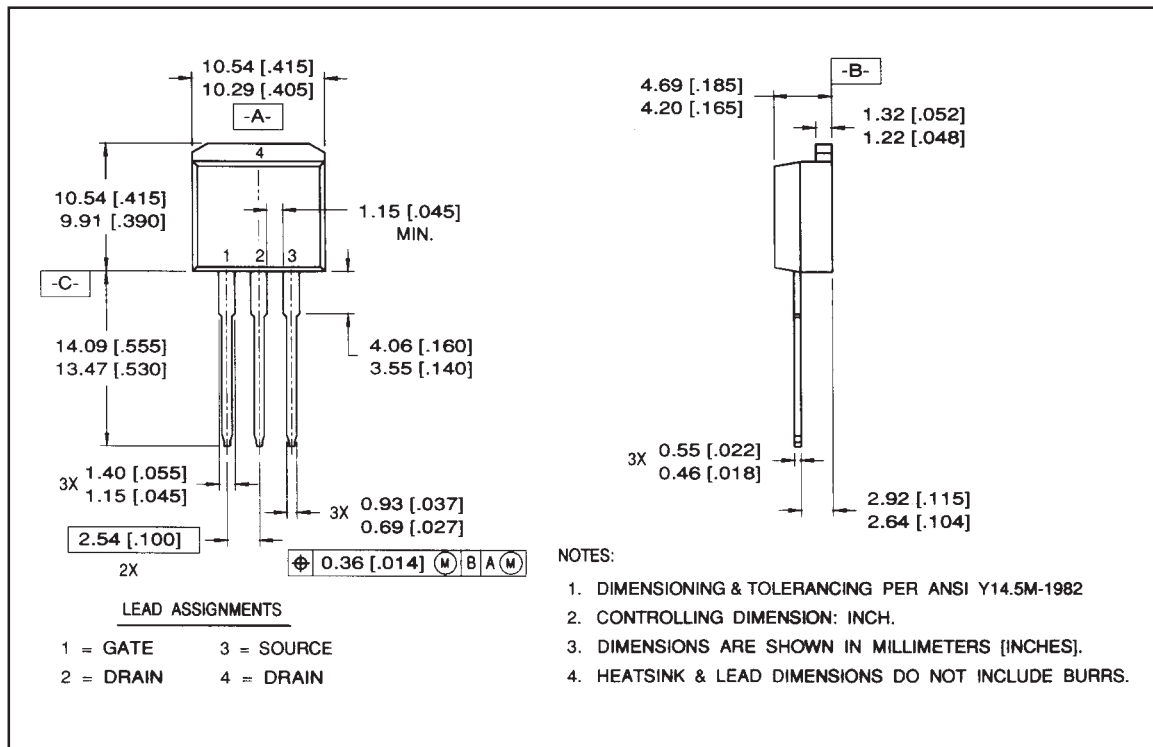
Notes:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

D²Pak

Package Outline

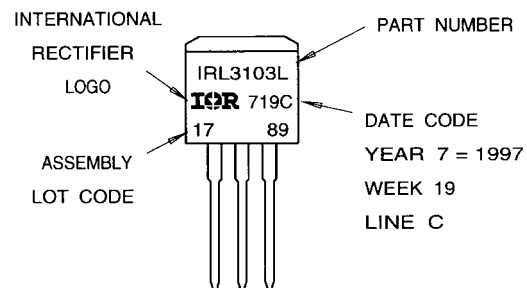
TO-262 Outline



Part Marking Information

TO-262

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

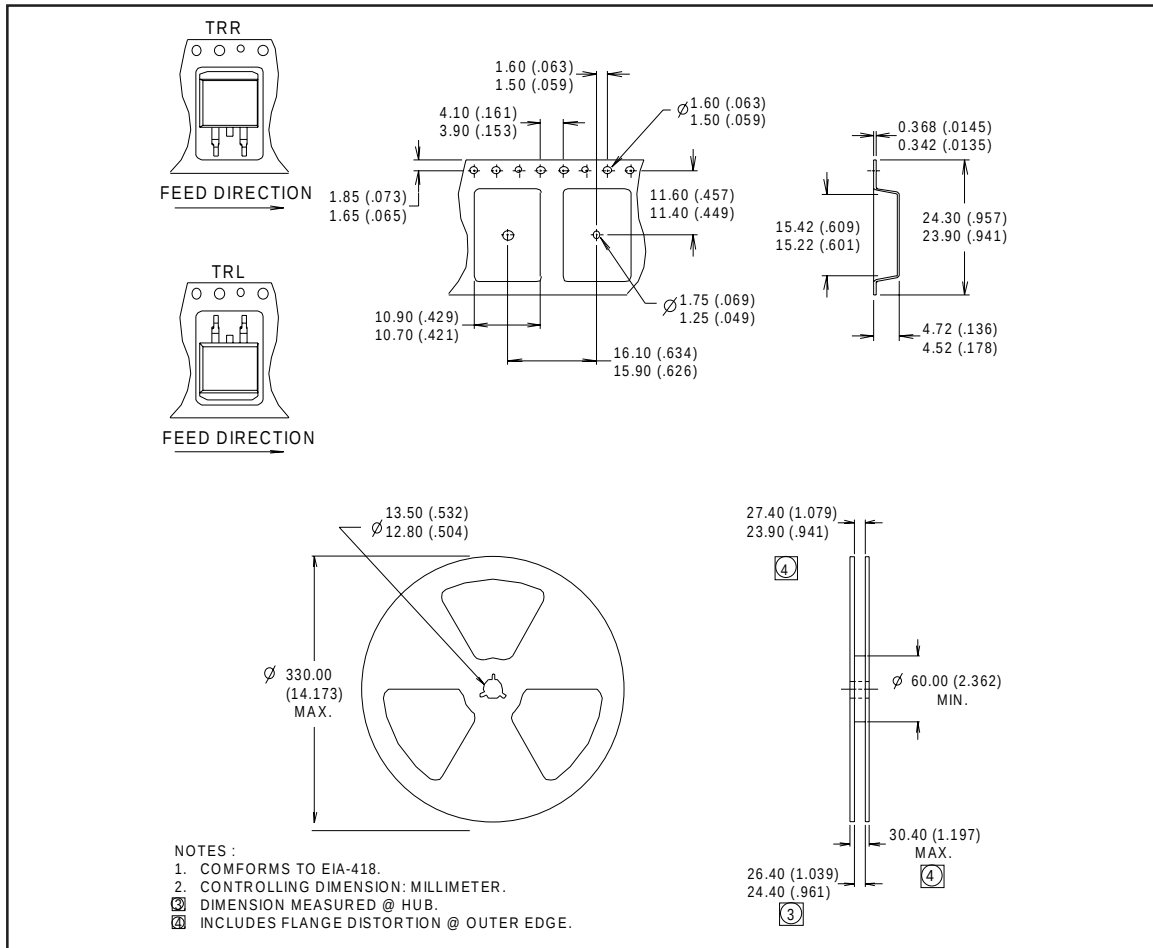


IRF9530NS/L

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Tape & Reel Information

D²Pak



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EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

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