



# CY6116A CY6117A

## 2K x 8 Static RAM

### Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**  
— 20 ns
- **Low active power**  
— 550 mW
- **Low standby power**  
— 110 mW
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

### Functional Description

The CY6116A and CY6117A are high-performance CMOS static RAMs organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and active LOW output enable ( $\overline{OE}$ ), and three-state drivers. The CY6116A and CY6117A have an automatic power-down feature, reducing the power consumption by 83% when deselected.

Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into

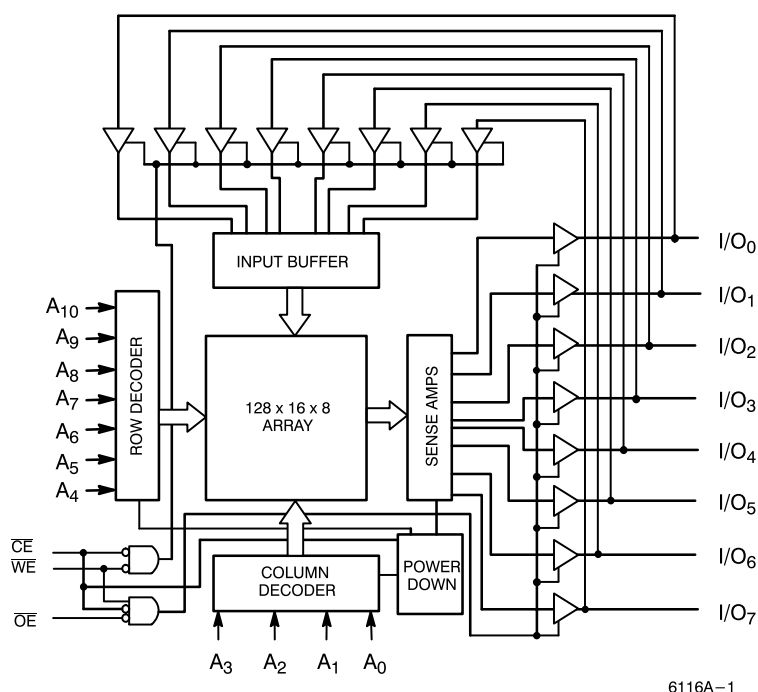
the memory location specified on the address pins (A<sub>0</sub> through A<sub>10</sub>).

Reading the device is accomplished by taking chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) LOW while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in high-impedance state when chip enable ( $\overline{CE}$ ) is HIGH or write enable ( $\overline{WE}$ ) is LOW.

The CY6116A and CY6117A utilize a die coat to insure alpha immunity.

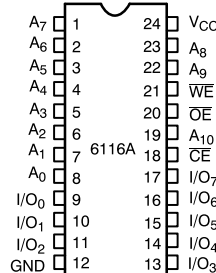
### Logic Block Diagram



6116A-1

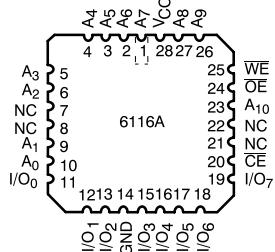
### Pin Configurations

#### DIP/SOJ Top View



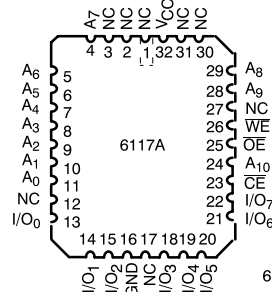
6116A-2

#### LCC Top View



6116A-3

#### LCC Top View



6116A-4

### Selection Guide

|                                |            | 6116A-20<br>6117A-20 | 6116A-25<br>6117A-25 | 6116A-35<br>6117A-35 | 6116A-45<br>6117A-45 | 6116A-55<br>6117A-55 |
|--------------------------------|------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| Maximum Access Time (ns)       |            | 20                   | 25                   | 35                   | 45                   | 55                   |
| Maximum Operating Current (mA) | Commercial | 100                  | 100                  | 100                  | 100                  | 80                   |
|                                | Military   |                      | 125                  | 100                  | 100                  | 100                  |
| Maximum Standby Current (mA)   | Commercial | 40/20                | 20                   | 20                   | 20                   | 20                   |
|                                | Military   |                      | 40                   | 20                   | 20                   | 20                   |



# CY6116A CY6117A

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
Ambient Temperature with  
Power Applied .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
Supply Voltage to Ground Potential  
(Pin 24 to Pin 12) .....  $-0.5\text{V}$  to  $+7.0\text{V}$   
DC Voltage Applied to Outputs  
in High Z State .....  $-0.5\text{V}$  to  $+7.0\text{V}$   
DC Input Voltage .....  $-3.0\text{V}$  to  $+7.0\text{V}$   
Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage .....  $>2001\text{V}$   
(per MIL-STD-883, Method 3015)

Latch-Up Current .....  $>200\text{ mA}$

## Operating Range

| Range                   | Ambient Temperature                             | V <sub>CC</sub>      |
|-------------------------|-------------------------------------------------|----------------------|
| Commercial              | $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$    | $5\text{V} \pm 10\%$ |
| Military <sup>[1]</sup> | $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | $5\text{V} \pm 10\%$ |

## Electrical Characteristics Over the Operating Range<sup>[2]</sup>

| Parameter        | Description                                                       | Test Conditions                                                                                                                                                                 | 6116A–20<br>6117A–20 |                 | 6116A–25, 35, 45<br>6117A–25, 35, 45 |                 | 6116A–55<br>6117A–55 |                 | Unit          |
|------------------|-------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----------------|--------------------------------------|-----------------|----------------------|-----------------|---------------|
|                  |                                                                   |                                                                                                                                                                                 | Min.                 | Max.            | Min.                                 | Max.            | Min.                 | Max.            |               |
| V <sub>OH</sub>  | Output HIGH Voltage                                               | V <sub>CC</sub> = Min., I <sub>OH</sub> = $-4.0\text{ mA}$                                                                                                                      | 2.4                  |                 | 2.4                                  |                 | 2.4                  |                 | V             |
| V <sub>OL</sub>  | Output LOW Voltage                                                | V <sub>CC</sub> = Min., I <sub>OL</sub> = $8.0\text{ mA}$                                                                                                                       |                      | 0.4             |                                      | 0.4             |                      | 0.4             | V             |
| V <sub>IH</sub>  | Input HIGH Voltage                                                |                                                                                                                                                                                 | 2.2                  | V <sub>CC</sub> | 2.2                                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | V             |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[3]</sup>                                  |                                                                                                                                                                                 | $-0.5$               | 0.8             | $-0.5$                               | 0.8             | $-0.5$               | 0.8             | V             |
| I <sub>IX</sub>  | Input Load Current                                                | $\text{GND} \leq V_I \leq V_{CC}$                                                                                                                                               | $-10$                | $+10$           | $-10$                                | $+10$           | $-10$                | $+10$           | $\mu\text{A}$ |
| I <sub>OZ</sub>  | Output Leakage Current                                            | $\text{GND} \leq V_I \leq V_{CC}$ ,<br>Output Disabled                                                                                                                          | $-10$                | $+10$           | $-10$                                | $+10$           | $-10$                | $+10$           | $\mu\text{A}$ |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[4]</sup>                       | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                                                                                                                                  |                      | $-300$          |                                      | $-300$          |                      | $-300$          | mA            |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current                          | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA<br>f = f <sub>MAX</sub> = 1/trc                                                                                               | Com'l                |                 |                                      | 100             |                      | 80              | mA            |
|                  |                                                                   |                                                                                                                                                                                 | Mil                  | 25              |                                      |                 | 125                  | 100             |               |
|                  |                                                                   |                                                                                                                                                                                 |                      | 35, 45          |                                      |                 | 100                  |                 |               |
| I <sub>SB1</sub> | Automatic $\overline{\text{CE}}$ Power-Down Current – TTL Inputs  | Max. V <sub>CC</sub> ,<br>$\overline{\text{CE}} \geq V_{IH}$<br>f = f <sub>MAX</sub>                                                                                            | Com'l                |                 |                                      | 40              |                      | 20              | mA            |
|                  |                                                                   |                                                                                                                                                                                 | Mil                  | 25              |                                      |                 | 40                   | 20              |               |
|                  |                                                                   |                                                                                                                                                                                 |                      | 35, 45, 55      |                                      |                 | 20                   |                 |               |
| I <sub>SB2</sub> | Automatic $\overline{\text{CE}}$ Power-Down Current – CMOS Inputs | Max. V <sub>CC</sub> ,<br>$\overline{\text{CE}} \geq V_{IH} - 0.3\text{V}$ ,<br>V <sub>IN</sub> $\geq V_{CC} - 0.3\text{V}$<br>or V <sub>IN</sub> $\leq 0.3\text{V}$ ,<br>f = 0 | Com'l                |                 |                                      | 20              |                      | 20              | mA            |
|                  |                                                                   |                                                                                                                                                                                 | Mil                  |                 |                                      |                 | 20                   | 20              |               |

## Capacitance<sup>[5]</sup>

| Parameter        | Description        | Test Conditions                                                              | Max. | Unit |
|------------------|--------------------|------------------------------------------------------------------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = $25^{\circ}\text{C}$ , f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 10   | pF   |
| C <sub>OUT</sub> | Output Capacitance |                                                                              | 10   | pF   |

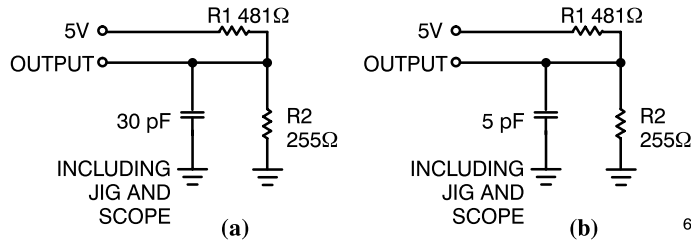
### Notes:

1. T<sub>A</sub> is the “instant on” case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V<sub>IL</sub> (min.) =  $-3.0\text{V}$  for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.



# CY6116A CY6117A

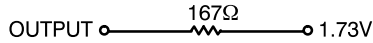
## AC Test Loads and Waveforms



6116A-5

6116A-6

Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics Over the Operating Range<sup>[2, 6]</sup>

| Parameter                  | Description                                      | 6116A-20<br>6117A-20 |      | 6116A-25<br>6117A-25 |      | 6116A-35<br>6117A-35 |      | 6116A-45<br>6117A-45 |      | 6116A-55<br>6117A-55 |      | Unit |
|----------------------------|--------------------------------------------------|----------------------|------|----------------------|------|----------------------|------|----------------------|------|----------------------|------|------|
|                            |                                                  | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |      |
| READ CYCLE                 |                                                  |                      |      |                      |      |                      |      |                      |      |                      |      |      |
| t <sub>RC</sub>            | Read Cycle Time                                  | 20                   |      | 25                   |      | 35                   |      | 45                   |      | 55                   |      | ns   |
| t <sub>AA</sub>            | Address to Data Valid                            |                      | 20   |                      | 25   |                      | 35   |                      | 45   |                      | 55   | ns   |
| t <sub>OHA</sub>           | Data Hold from Address Change                    | 5                    |      | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns   |
| t <sub>ACE</sub>           | $\overline{CE}$ LOW to Data Valid                |                      | 20   |                      | 25   |                      | 35   |                      | 45   |                      | 55   | ns   |
| t <sub>DOE</sub>           | $\overline{OE}$ LOW to Data Valid                |                      | 10   |                      | 12   |                      | 15   |                      | 20   |                      | 25   | ns   |
| t <sub>LZOE</sub>          | $\overline{OE}$ LOW to Low Z                     | 3                    |      | 3                    |      | 3                    |      | 3                    |      | 3                    |      | ns   |
| t <sub>HZOE</sub>          | $\overline{OE}$ HIGH to High Z <sup>[7]</sup>    |                      | 8    |                      | 10   |                      | 12   |                      | 15   |                      | 20   | ns   |
| t <sub>LZCE</sub>          | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 5                    |      | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns   |
| t <sub>HZCE</sub>          | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |                      | 8    |                      | 10   |                      | 15   |                      | 15   |                      | 20   | ns   |
| t <sub>PU</sub>            | $\overline{CE}$ LOW to Power-Up                  | 0                    |      | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns   |
| t <sub>PD</sub>            | $\overline{CE}$ HIGH to Power-Down               |                      | 20   |                      | 20   |                      | 20   |                      | 25   |                      | 25   | ns   |
| WRITE CYCLE <sup>[9]</sup> |                                                  |                      |      |                      |      |                      |      |                      |      |                      |      |      |
| t <sub>WC</sub>            | Write Cycle Time                                 | 20                   |      | 20                   |      | 25                   |      | 40                   |      | 50                   |      | ns   |
| t <sub>SCE</sub>           | $\overline{CE}$ LOW to Write End                 | 15                   |      | 20                   |      | 25                   |      | 30                   |      | 40                   |      | ns   |
| t <sub>AW</sub>            | Address Set-Up to Write End                      | 15                   |      | 20                   |      | 25                   |      | 30                   |      | 40                   |      | ns   |
| t <sub>HA</sub>            | Address Hold from Write End                      | 0                    |      | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns   |
| t <sub>SA</sub>            | Address Set-Up to Write Start                    | 0                    |      | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns   |
| t <sub>PWE</sub>           | $\overline{WE}$ Pulse Width                      | 15                   |      | 15                   |      | 20                   |      | 20                   |      | 25                   |      | ns   |
| t <sub>SD</sub>            | Data Set-Up to Write End                         | 10                   |      | 10                   |      | 15                   |      | 15                   |      | 25                   |      | ns   |
| t <sub>HD</sub>            | Data Hold from Write End                         | 0                    |      | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns   |
| t <sub>HZWE</sub>          | $\overline{WE}$ LOW to High Z                    |                      | 7    |                      | 7    |                      | 10   |                      | 15   |                      | 20   | ns   |
| t <sub>LZWE</sub>          | $\overline{WE}$ HIGH to Low Z                    | 5                    |      | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns   |

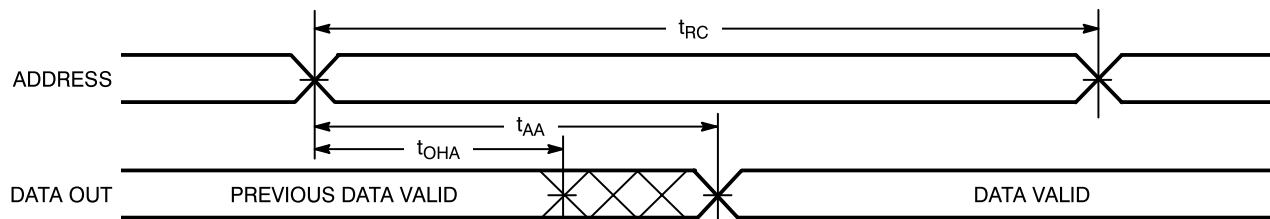
### Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



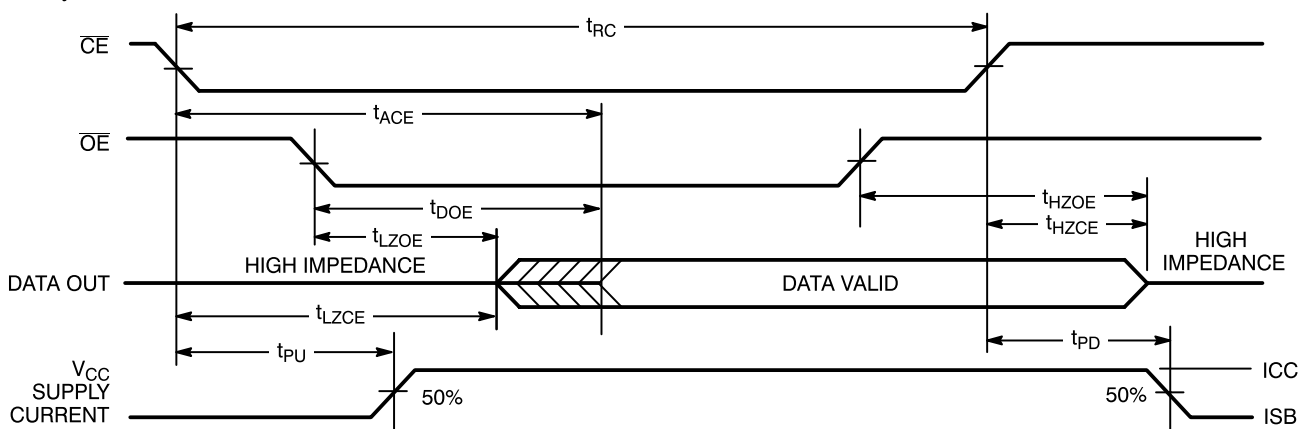
## Switching Waveforms

### Read Cycle No. 1<sup>[10, 11]</sup>



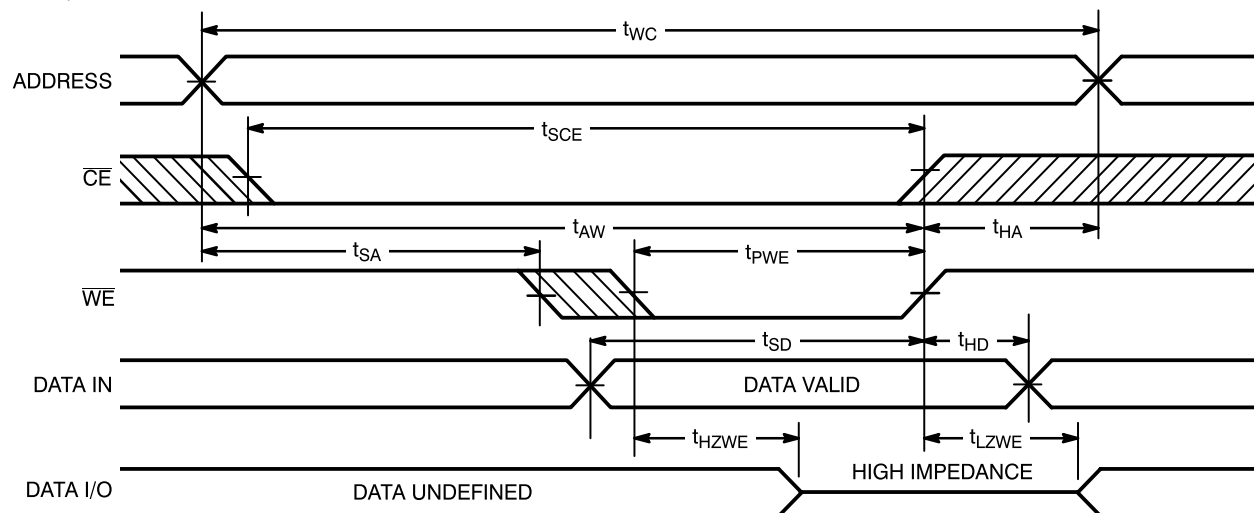
6116A-7

### Read Cycle No. 2<sup>[10, 12]</sup>



6116A-8

### Write Cycle No. 1 ( $\overline{WE}$ Controlled)<sup>[9, 13]</sup>



6116A-9

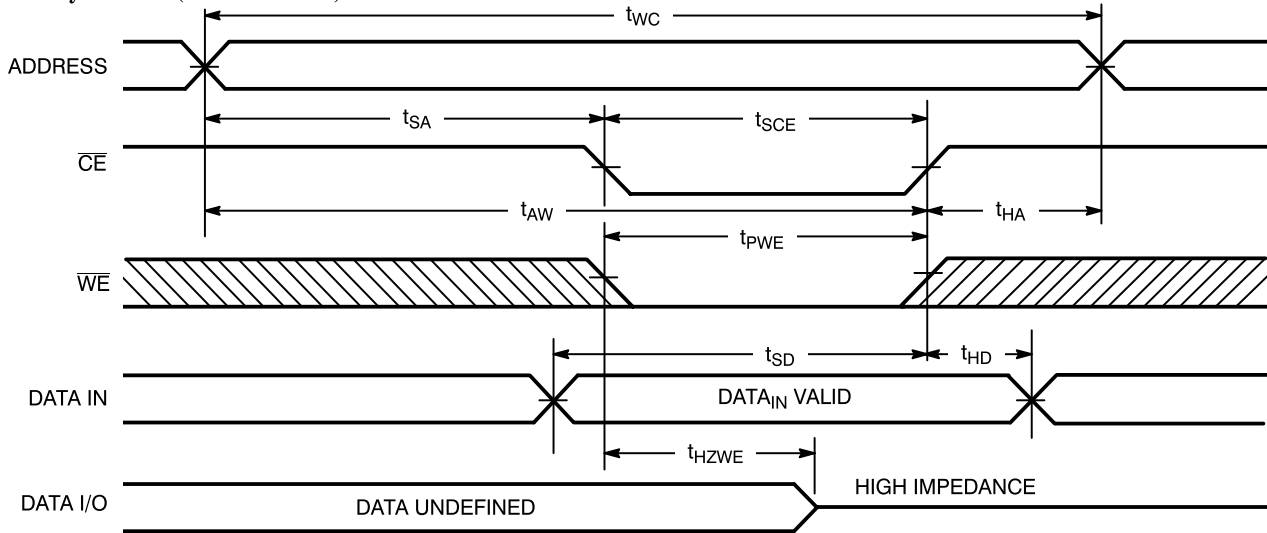
#### Notes:

10.  $\overline{WE}$  is HIGH for read cycle.
11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. Data I/O pins enter high-impedance state, as shown, when  $\overline{OE}$  is held LOW during write.



## Switching Waveforms (continued)

### Write Cycle No. 2 ( $\overline{\text{CE}}$ Controlled)<sup>[9, 13, 14]</sup>



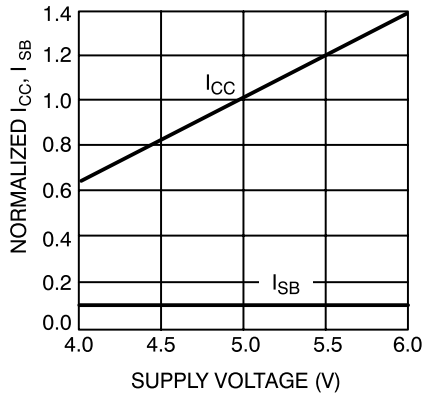
6116A-10

#### Note:

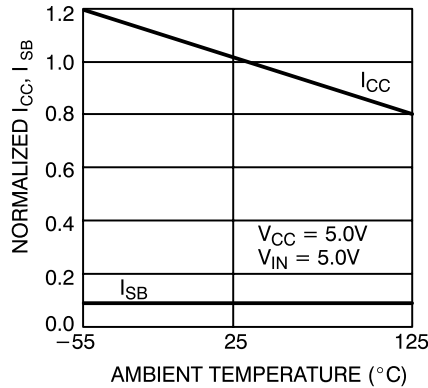
14. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.

## Typical DC and AC Characteristics

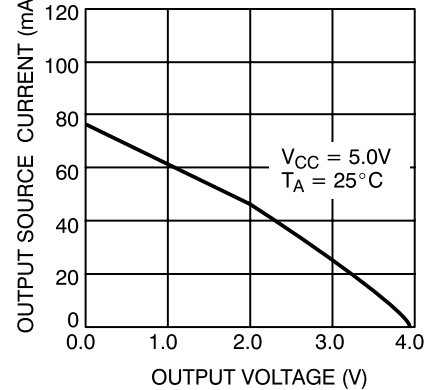
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



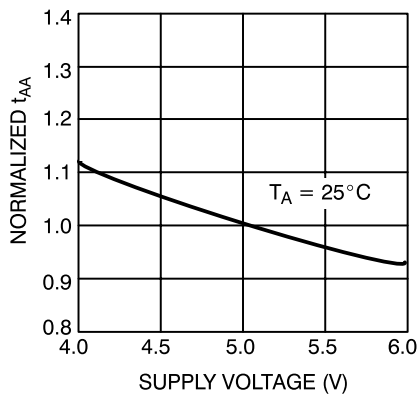
**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



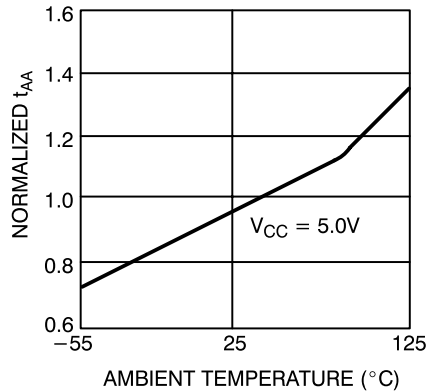
**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**



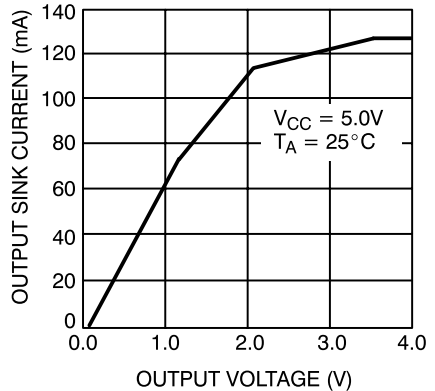
**NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**



**NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE**



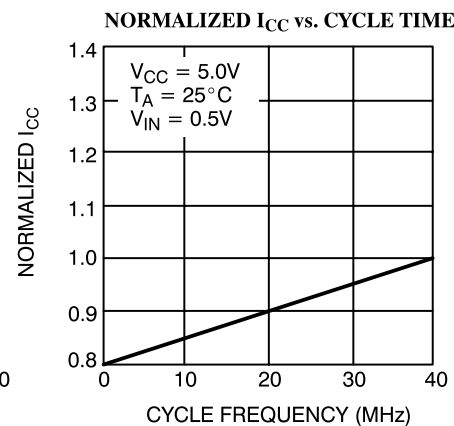
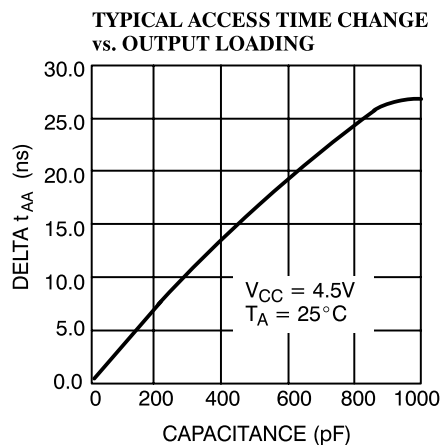
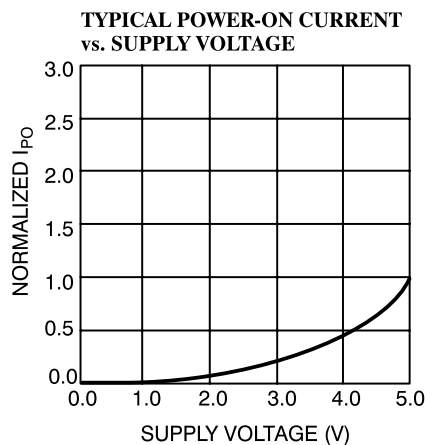
**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**





**CY6116A**  
**CY6117A**

## Typical DC and AC Characteristics (continued)



## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type                    | Operating Range |
|------------|---------------|--------------|---------------------------------|-----------------|
| 20         | CY6116A-20PC  | P11          | 28-Lead (300-Mil) Molded DIP    | Commercial      |
| 25         | CY6116A-25PC  | P11          | 28-Lead (300-Mil) Molded DIP    | Commercial      |
|            | CY6116A-25DMB | D12          | 24-Lead (600-Mil) CerDIP        | Military        |
|            | CY6116A-25LMB | L64          | 28-Square Leadless Chip Carrier |                 |
| 35         | CY6116A-35PC  | P11          | 28-Lead (300-Mil) Molded DIP    | Commercial      |
|            | CY6116A-35DMB | D12          | 24-Lead (600-Mil) CerDIP        | Military        |
|            | CY6116A-35LMB | L64          | 28-Square Leadless Chip Carrier |                 |
| 45         | CY6116A-45PC  | P11          | 28-Lead (300-Mil) Molded DIP    | Commercial      |
|            | CY6116A-45DMB | D12          | 24-Lead (600-Mil) CerDIP        | Military        |
|            | CY6116A-45LMB | L64          | 28-Square Leadless Chip Carrier |                 |
| 55         | CY6116A-55PC  | P11          | 28-Lead (300-Mil) Molded DIP    | Commercial      |
|            | CY6116A-55DMB | D12          | 24-Lead (600-Mil) CerDIP        | Military        |
|            | CY6116A-55LMB | L64          | 28-Square Leadless Chip Carrier |                 |

| Speed (ns) | Ordering Code | Package Name | Package Type                             | Operating Range |
|------------|---------------|--------------|------------------------------------------|-----------------|
| 35         | CY6117A-35LMB | L55          | 32-Pin Rectangular Leadless Chip Carrier | Military        |
| 45         | CY6117A-45LMB | L55          | 32-Pin Rectangular Leadless Chip Carrier | Military        |
| 55         | CY6117A-55LMB | L55          | 32-Pin Rectangular Leadless Chip Carrier | Military        |



## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameter            | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1, 2, 3   |
| V <sub>OL</sub>      | 1, 2, 3   |
| V <sub>IH</sub>      | 1, 2, 3   |
| V <sub>IL</sub> Max. | 1, 2, 3   |
| I <sub>IX</sub>      | 1, 2, 3   |
| I <sub>OZ</sub>      | 1, 2, 3   |
| I <sub>CC</sub>      | 1, 2, 3   |
| I <sub>SB</sub>      | 1, 2, 3   |

#### Switching Characteristics

| Parameter          | Subgroups       |
|--------------------|-----------------|
| <b>READ CYCLE</b>  |                 |
| t <sub>RC</sub>    | 7, 8, 9, 10, 11 |
| t <sub>AA</sub>    | 7, 8, 9, 10, 11 |
| t <sub>OHA</sub>   | 7, 8, 9, 10, 11 |
| t <sub>ACE</sub>   | 7, 8, 9, 10, 11 |
| t <sub>DOE</sub>   | 7, 8, 9, 10, 11 |
| <b>WRITE CYCLE</b> |                 |
| t <sub>WC</sub>    | 7, 8, 9, 10, 11 |
| t <sub>SCE</sub>   | 7, 8, 9, 10, 11 |
| t <sub>AW</sub>    | 7, 8, 9, 10, 11 |
| t <sub>HA</sub>    | 7, 8, 9, 10, 11 |
| t <sub>SA</sub>    | 7, 8, 9, 10, 11 |
| t <sub>PWE</sub>   | 7, 8, 9, 10, 11 |
| t <sub>SD</sub>    | 7, 8, 9, 10, 11 |
| t <sub>HD</sub>    | 7, 8, 9, 10, 11 |

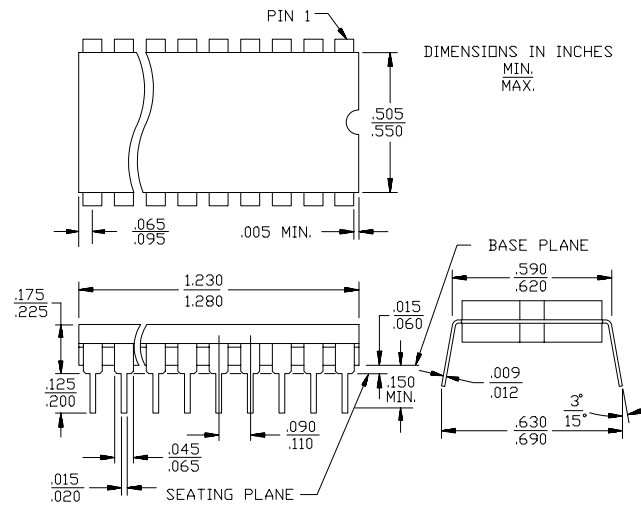
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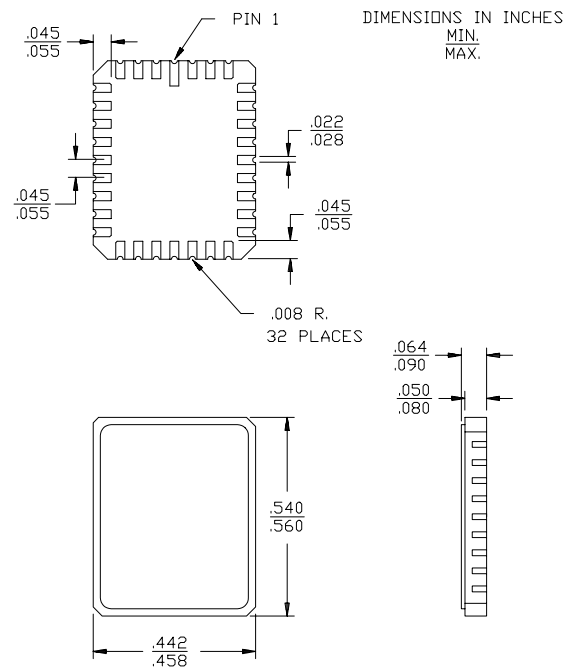
**CY6116A**  
**CY6117A**

## Package Diagrams

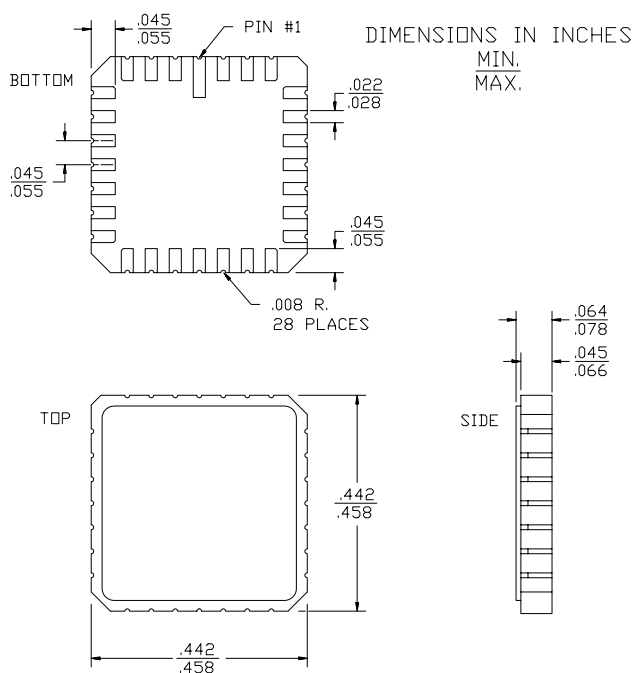
**24-Lead (600-Mil) CerDIP D12**  
MIL-STD-1835 D-3 Config. A



**32-Pin Rectangular Leadless Chip Carrier L55**  
MIL-STD-1835 C-12



**28-Square Leadless Chip Carrier L64**  
MIL-STD-1835 C-4







**CY6116A**  
**CY6117A**

**Package Diagrams (continued)**

**24-Lead (600-Mil) Molded DIP P11**

