FEATURES

- 5-phase dual output PWM Controller
- Phases are flexibly assigned between Loops 1 & 2
- Intel® VR12, AMD® SVI/G34 & Memory modes
- Switching frequency from 200kHz to 1.2MHz per phase
- Efficiency Shaping Features including Variable Gate Drive and Dynamic Phase Control
- Programmable 1-phase or 2-phase for Light Loads Adaptive Transient Algorithm (ATA) on both loops minimizes output bulk capacitors and system cost
- Auto-Phase Detection with auto-compensation
- Per-Loop Fault Protection: OVP, UVP, OCP, OTP, CFP
- I2C/SMBus/PMBus system interface for telemetry
- Non-Volatile Memory (NVM) for custom configuration
- Compatible with Active Tri-Level (ATL) and 3.3V tri-state Drivers
- +3.3V supply voltage; 0ºC to 85ºC ambient operation
- Pb-Free, RoHS, 6x6 40 pin QFN package

APPLICATIONS

- Intel ® VR12 & AMD® SVI & PVI based systems
- DDR Memory with Vtt tracking
- Overclocked & Gaming platforms

DESCRIPTION

The IR3541 is a dual-loop, digital multi-phase buck controller that drives up to 5 phases. The IR3541 is fully Intel® VR12 and AMD® SVI compliant on both loops and provides a Vtt tracking function for DDR memory.

The IR3541 includes Variable Gate Drive to optimize the MOSFET gate drive voltage as a function of real-time load current. Dynamic Phase Control adds/drops active phases based upon load current. The IR3541 can be configured to enter 1-phase operation and active diode emulation mode automatically or by command.

The Adaptive Transient Algorithm (ATA), minimizes output bulk capacitors. In addition, a coupled inductor mode, with phases added/dropped in pairs, enables further improvement in transient response and form factor.

The I2C/PMBus interface can communicate with up to 16 IR3541 based VR loops. Device configuration and fault parameters are easily defined using the IR Intuitive Power Designer (IPD) GUI and stored in on-chip NVM.

The IR3541 provides extensive OVP, UVP, OCP and OTP fault protection and includes thermistor based temperature sensing with VRHOT signal.

The IR3541 also includes numerous features like register diagnostics for fast design cycles and platform differentiation, truly simplifying VRD design and enabling fastest time-to-market with its “set-and-forget” methodology.

BASIC APPLICATION

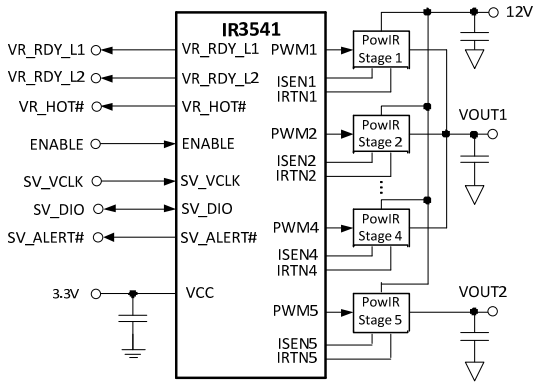


Figure 1: IR3541 Basic Application Circuit

PIN DIAGRAM

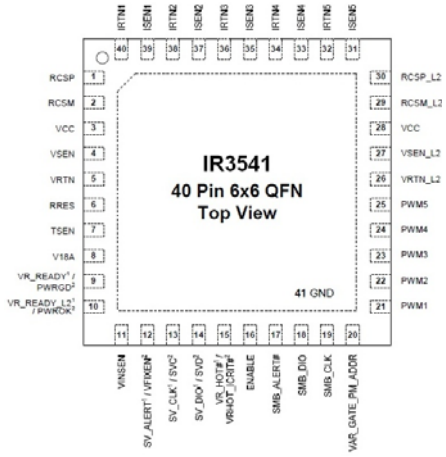
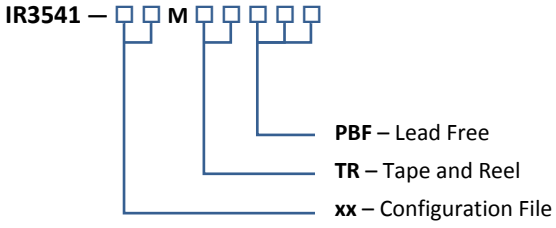


Figure 2: IR3541 Package Top View

ORDERING INFORMATION



Package	Tape & Reel Qty	Part Number
QFN	100	**IR3541-xxMPBF**
QFN	3000	**IR3541-xxMTRPBF**

Notes: For unprogrammed/default parts, use configuration file 00. Unprogrammed parts will not start up until programmed in order to ensure a safe power up.

FUNCTIONAL BLOCK DIAGRAM

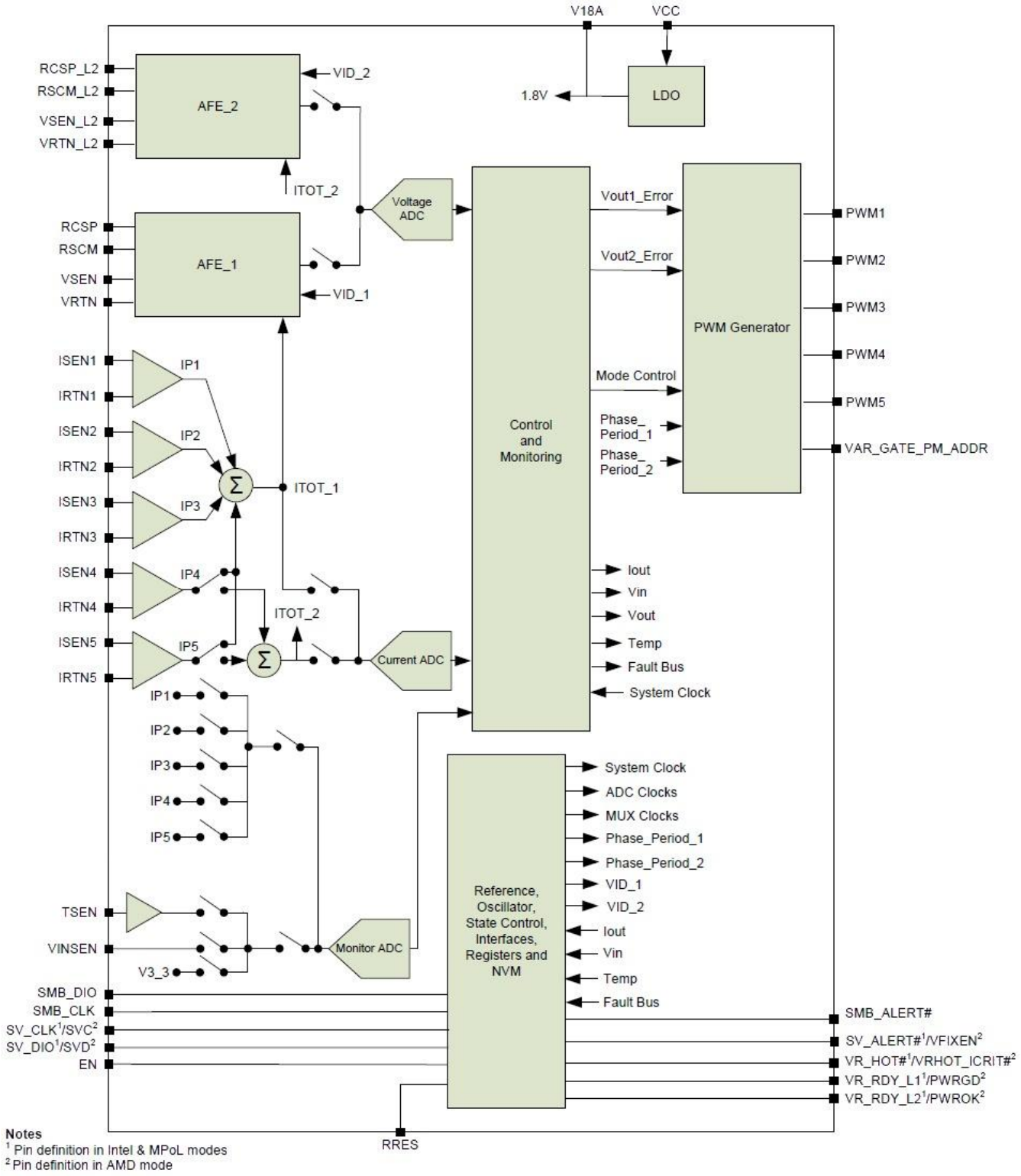
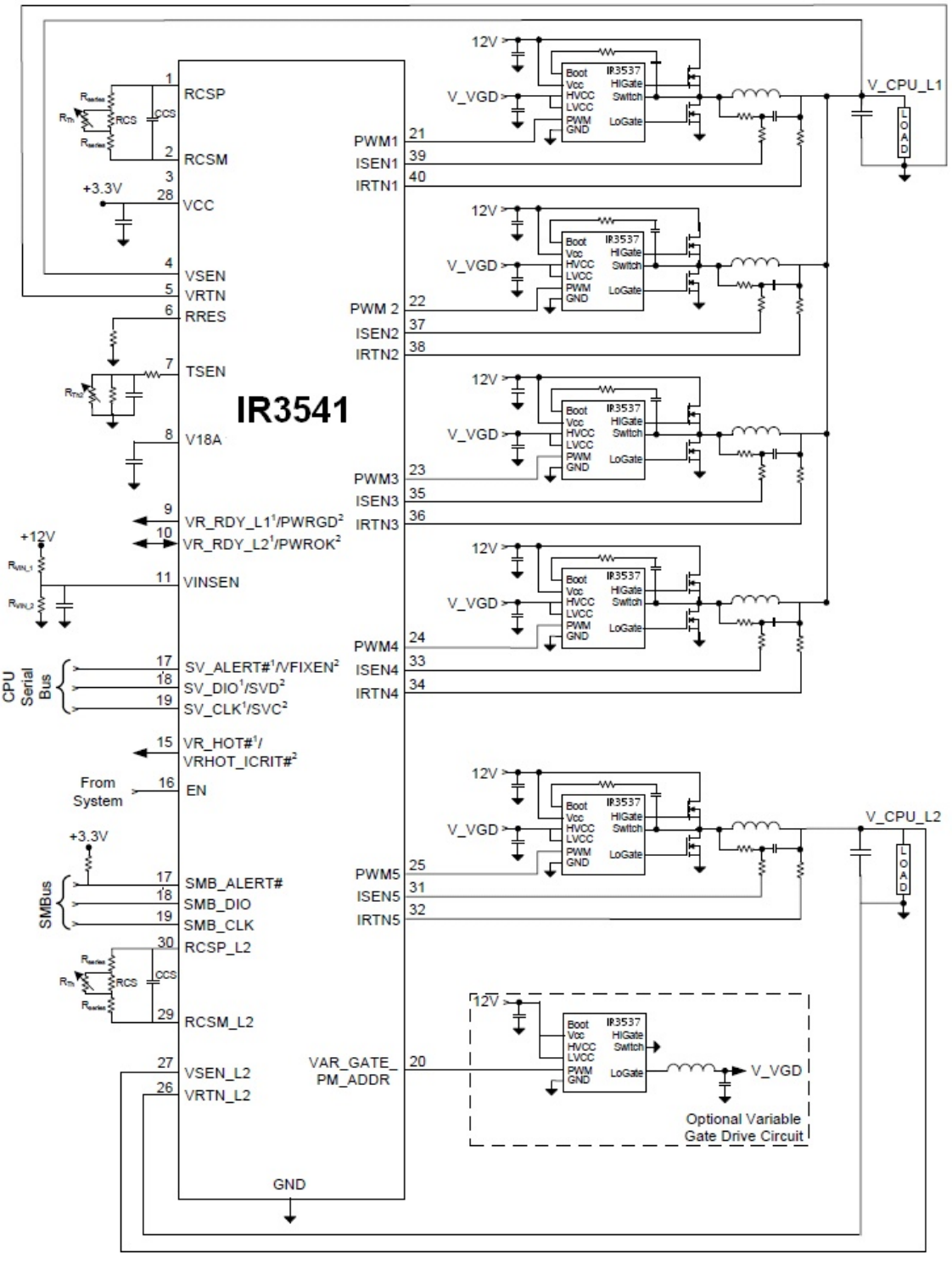


Figure 3: IR3541 Functional Block Diagram

TYPICAL APPLICATIONS BLOCK DIAGRAMS



Notes
[1] Pin definition in Intel & MPoL modes
[2] Pin definition in AMD mode

Figure 4: Dual-Loop DRV using IR3541 Controller and IR3537 MOSFET drivers in 4+1, Intel Mode configuration

PIN DESCRIPTIONS

PIN #	PIN NAME	TYPE	PIN DESCRIPTION	
1	RCSP	A [O]	**Resistor Current Sense Positive Loop#1**. This pin is connected to an external network to set the loadline slope, bandwidth and temperature compensation for Loop #1	
2	RCSM	A [O]	**Resistor Current Sense Minus Loop#1**. This pin is connected to an external network to set the loadline slope, bandwidth and temperature compensation for Loop #1	
3	VCC	A [P]	**Input supply voltage.** 3.3V supply to power the device	
4	VSEN	A [I]	**Voltage Sense Input Loop#1**. This pin is connected directly to the VR output voltage of Loop #1 at the load and should be routed differentially with VRTN.	
5	VRTN	A [I]	**Voltage Sense Return Input Loop#1.** This pin is connected directly to Loop#1 ground at the load and should be routed differentially with VSEN.	
6	RRES	A [B]	**Current Reference Resistor.** A 1% resistor is connected to this pin to set an internal precision current reference	
7	TSEN	D [I]	**NTC Temperature Sense Input.** An NTC network is connected to this pin to measure temperature for VRHOT. Refer to Figure 43 for details.	
8	V18A	A [O]	**1.8V Decoupling.** Two capacitors on this pin provide decoupling for the internal 1.8V supply.	
9	VR_RDY_L1 / PWRGD	D [O]	***Intel/MPoL mode*** **Voltage Regulator Ready Output (Loop #1).** Open-drain output that asserts high when the VR has completed soft-start to Loop #1 VID. It is pulled up to an external voltage rail	***AMD mode*** **Power Good Output.** Open-drain output that is asserted when both Loop 1 and Loop 2 are in regulation.
10	VR_RDY_L2 / PWROK	D [O] / D [I]	***Intel/MPoL mode*** **Voltage Regulator Ready Output (Loop #2).** Open-drain output that asserts high when the VR has completed soft-start to Loop #2 VID. It is pulled up to an external voltage rail.	***AMD mode*** **Power OK Input.** An input that when low indicates to return to the Boot Voltage and when high indicates to use the SVI bus.
11	VINSEN	D [I]	**+12V Voltage Sense Input.** This is used to detect a valid 12V supply voltage and measure the input voltage to the VR.	
12	SV_ALERT# / VFIXEN	D [O] / D [I]	***Intel/MPoL mode*** **VR12 Serial VID ALERT#.** SVID ALERT# is pulled low by the IR3541 (SVID Slave) to alert the CPU (SVID Master) of new VR12 Status, typically a VR Settled, Icc Max or Temp Max alert. The IR3541 is always an SVID Slave device.	***AMD mode*** **Fixed Voltage Enable.** Is an input that when asserted active high, overrides the serial VID to force a fixed output voltage. Tie low to disable.
13	SV_CLK / SVC	D[I]	***Intel/MPoL mode*** **VR12 Serial VID Clock Input.** Clock input driven by the CPU Master.	***AMD mode*** **SVI Serial VID Clock Input.** Clock input driven by the CPU Master.
14	SV_DIO / SVD	D[B]	***Intel/MPoL mode*** **VR12 Serial VID Data I/O.** Is a bi-directional serial line over which the CPU Master issues commands to controller/s slave/s	***AMD mode*** **SVI Serial VID Data I/O.** Is a bi-directional serial line over which the CPU Master issues commands to controller/s slave/s
15	VR_HOT# / VRHOT_ICRIT#	D [O]	***Intel/MPoL mode*** **VR HOT# Output.** Thermal alert that asserts active low when parameter Temp Max is exceeded. Assertion is not a fault and the PWM continues to regulate.	***AMD SVI mode*** **VR HOT_ICRIT# Output.** Active low pin that can be programmed to assert when parameter Temp Max or Max Current is exceeded. Assertion is not a fault and the PWM continues to regulate.

PIN #	PIN NAME	TYPE	PIN DESCRIPTION
16	EN	D [I]	**VR Enable Input.** ENABLE is an active high system input to power-on the regulator, provided Vin and Vcc are present. ENABLE is not pulled up on the controller. When ENABLE is pulled low, the controller de-asserts VR READY and shuts down the regulator.
17	SMB_ALERT#	D [B]	**SMBus ALERT#.** SMBus/PMBus ALERT# is pulled low to alert the SMBus Master, to query SMBus status of IR3541. The IR3541 is always a SMBus Slave device.
18	SMB_DIO	D [B]	**Serial Data Line I/O.** I2C/SMBus/PMBus bi-directional serial data line
19	SMB_CLK	D [I]	**Serial Clock Line Input.** I2C/SMBus/PMBus clock input. The IR3541 SMBus interface is rated to 400 KHz.
20	VAR_GATE_PM_ADDR	D [O]	**Variable Gate Drive PWM Output or I2C/SMBus PMBus Address.** Variable Gate Drive is a PWM output that may be used to power MOSFET Drivers. This pin can be configured as inverted or non-inverted. Alternatively, the pin can be programmed in NVM to be an address offset pin for the I2C/SMBus/PMBus addresses. A resistor to ground defines the offset.
21-25	PWM1 – PWM5	D [O]	**Phase 1-5 Pulse Width Modulation Outputs.** PWM signal pin which is connected to the input of an external MOSFET gate driver. Flexible phasing allows PWM1-PWM5 to be assigned to Loop #1 (5+0 configuration) and PWM5 and PWM4 to be assigned to loop 2 (3+2 configuration). Refer to Flexible Phasing section for unused/disabled phases. The power-up state is high-impedance until ENABLE goes active.
26	VRTN_L2	A [I]	**Voltage Sense Return Input Loop#2.** This pin is connected directly to Loop#2 ground at the load and should be routed differentially with VSEN_L2.
27	VSEN_L2	A [I]	**Voltage Sense Input Loop#2**. This pin is connected directly to the VR output voltage of Loop #2 at the load and should be routed differentially with VRTN_L2.
28	VCC	A [P]	**Input supply voltage.** 3.3V supply to power the device
29	RCSM_L2	A [O]	**Resistor Current Sense Minus Loop#2**. This pin is connected to an external network to set the loadline slope, bandwidth and temperature compensation for Loop #2.
30	RCSP_L2	A [O]	**Resistor Current Sense Positive Loop#2**. This pin is connected to an external network to set the loadline slope, bandwidth and temperature compensation for Loop #2.
31	ISEN 5	A [I]	**Phase 5 Current Sense Input.** Phase 5 sensed current input (+)
32	IRTN 5	A [I]	**Phase 5 Current Sense Return Input.** Phase 5 sensed current input return (-)
33	ISEN 4	A [I]	**Phase 4 Current Sense Input.** Phase 4 sensed current input (+)
34	IRTN 4	A [I]	**Phase 4 Current Sense Return Input.** Phase 4 sensed current input return (-)
35	ISEN 3	A [I]	**Phase 3 Current Sense Input.** Phase 3 sensed current input (+)
36	IRTN 3	A [I]	**Phase 3 Current Sense Return Input.** Phase 3 sensed current input return (-)
37	ISEN 2	A [I]	**Phase 2 Current Sense Input.** Phase 2 sensed current input (+)
38	IRTN 2	A [I]	**Phase 2 Current Sense Return Input.** Phase 2 sensed current input return (-)
39	ISEN 1	A [I]	**Phase 1 Current Sense Input.** Phase 1 sensed current input (+)
40	IRTN 1	A [I]	**Phase 1 Current Sense Return Input.** Phase 1 sensed current input return (-)
41 (PAD)	GND		**Ground.** Ground reference for the IC. The large metal pad on the bottom of the IR3541 must be connected to Ground.

Note 1: A - Analog; D – Digital; [I] – Input; [O] – Output; [B] – Bi-directional; [P] – Power

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC)	GND-0.3V to 4.0V
RCSPx, RCSMx	0 to 2.2 V
VSEN, VSEN_L2, VRTN, VRTN_L2, ISENx, IRTNx	GND-0.2V to 2.7V
RRES, V18A, , TSEN, TSEN2, VINSEN	GND-0.2V to 2.2V
SV_CLK/SVC, SV_DIO/SVD, SV_ALERT#/VFIXEN	GND-0.3V to VCC
PWMx, VAR_GATE	GND-0.3V to VCC
VR_RDY_L1/PWRGD, VR_RDY_L2/PWROK, EN	GND-0.3V to VCC
VRHOT#/VRHOT_ICRIT#	GND-0.3V to VCC
SMB_DIO, SMB_CLK, SMB_ALERT#	GND-0.3V to 5.5V
ESD RATING	
Human Body Model	2000V
Machine Model	200V
Charge Device Model	1000V
THERMAL INFORMATION	
Thermal Resistance (θ_{JA} & θ_{JC})	29°C/W & 3°C/W
Maximum Operating Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300°C

Notes 1: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Caution: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

Recommended Operating Ambient Temperature Range	0°C to 85°C
Recommended Supply Voltage Range	+2.97V to +3.6V

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply	**VCC/GND**					
Supply voltage	V_{cc}		2.97	3.3	3.6	V
Supply current	I_{vcc}	No PWM switching		120		mA
3.3V UVLO turn on threshold				2.80		V
3.3V UVLO turn off threshold				2.64		V
Input voltage (+12V) sense input	**VINSEN**					
Input impedance				1		MΩ
Input range	V12	With 14:1 divider	0	0.8	1.1	V
12V UVLO turn on threshold		With 14:1 divider	10	10.2	10.4	V
12V UVLO turn off threshold		With 14:1 divider		9		V
Reference Voltage and DAC						
Boot Voltage Range[1]		Intel/MPoL Mode	0		1.52	V
		AMD Mode	0.0125		1.55	V
System Accuracy		VID = 1.0V–1.6V	-0.5		0.5	%VID
System Accuracy		VID = 0.5 –1.0V	-7.0		7.0	mV
System Accuracy		VID = 0.25 –0.5V	-8		8	mV
External reference resistor	**RRES**	1% external bias resistor		7.5		kΩ
Oscillator & PWM Generator						
Internal oscillator				192		MHz
Frequency Accuracy			-2.0		2.0	%
PWM Frequency Range			200		1200	kHz
PWM frequency step size (refer to Fig.20)				0.8-30		kHz
PWM resolution					160	ps
NTC Temperature Sense	**TSEN1,2**					
Output Current		For TSEN = 0 to 1.2V	97	100	103	µA
Accuracy		at 100°C (ideal NTC)	97		103	°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Digital inputs – Low Vth type 1	**EN (Intel/MPoLMode)**					
Input high voltage			0.7			V
Input low voltage					0.35	V
Input leakage current		Vpad=0 to 2V			±1	µA
Digital inputs – Low Vth type 2	**SV_CLK, SV_DIO**					
Input high voltage			0.65			V
Input low voltage					0.45	V
Hysteresis				95		mV
Input leakage current		Vpad=0 to 2V			±1	µA
Digital inputs – Low Vth type 3	**VFIXEN, PWROK**					
Input high voltage			0.9			V
Input low voltage					0.6	V
Input leakage current		Vpad=0 to 2V			±1	µA
Digital inputs - LVTTL	**SMB_DIO, SMB_CLK, EN (AMD Mode)**					
Input voltage high			2.1			V
Input voltage low					0.8	V
Input leakage		Vpad=0 to 3.6V			±1	µA
Remote voltage sense inputs	**VSEN, VRTN, VSEN_L2, VRTN_L2**					
VSENx Input current		VCPU = 0.5V to 1.5V		-250 to +250		uA
VRTNx input current				-500		uA
Differential Input voltage range		VRTN= ±100mV	0.0		2.6	V
VRTN Input CM voltage			-100		100	mV
Remote current sense inputs	**ISEN/IRTN 1-5**					
Voltage range			0.0		2.6	V
Bias current				200		nA
Open-Drain outputs - 4mA drive	**VR_RDY/PWRGD, VR_RDY_L2, SMB_DIO, SMB_ALERT**					
Output low voltage		4mA			0.3	V
Output leakage		Vpad=0 to 3.6V			±1	µA
Open-Drain outputs - 20mA drive	**SV_DIO, SV_ALERT, VR_HOT_ICRIT#**					
Output low voltage		I=20mA			0.26	V
On resistance		I=20mA	7	9	13	Ω
Tri-state leakage	I_{leak}	Vpad=0 to 3.6V			±1	µA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
PWM I/O	**PWM1 – PWM5, VAR_GATE**					
Output low voltage (Tri-state mode)		I=-4mA			0.4	V
Output high voltage (Tri-State mode)		I=+4mA	2.9			V
Output low voltage (IR ATL mode)		I=-4mA			0.4	V
Output high voltage (IR ATL mode)		I=+4mA	1.4		2	V
Active Tri-State Level (IR ATL mode)		I=+4mA	2.9			V
Tri-state leakage		ATS_EN=0, Vpad = 0 to Vcc			±1	µA
Load					60	pF
Rise/Fall time					20	ns
PWM auto-detect inputs (when 3.3V Vcc is applied)						
Input voltage high			1.3			V
Input voltage low					0.5	V
Input leakage					±1	µA
I2C / PMBus & Reporting						
Bus Speed				100	400	kHz
Iout & Vout filter				3.66		Hz
Iout & Vout Update rate				2.93		kHz
12V Vin & Temperature filter				1.3		kHz
12V Vin & Temperature update rate				62.5		kHz
12V Vin range reporting[1]			0		15	V
12V accuracy reporting		With 1% resistors	-3		3	%
12V resolution reporting				31		mV
Vout range reporting[1]					2.2	V
Vout accuracy reporting		No load-line	-0.5		0.5	%
Vout resolution reporting		Vout < 2V		2		mV
Iout range reporting[1]		Per phase	0		62	A
Iout accuracy reporting		Maximum load, all phase active (based on DCR, NTC and # active phases)		5		%
Iout resolution reporting		Iout < 256A		0.25		A
Temperature range reporting[1]			0		125	°C
Temperature accuracy reporting		At 100°C	-3		3	%
Temperature resolution reporting				1		°C
Variable Gate Drive						
Frequency				500		kHz
Output Voltage range[1]			4.0		12	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Load line (programmable)[1]			0		+12.5	mΩ
Fault Protection						
OVP threshold during Start-up (until output reaches 1V)				1.248		V
OVP Operating threshold		Relative to VID+load line		200		mV
OVP filter delay				160		ns
Output UVP threshold		Relative to VID+load line		-248		mV
OCP range (per phase) [1]			0		62	A
OCP System accuracy		System excluding DCR/sense resistor	-5		+5	%
OCP filter bandwidth				30		kHz
VR_HOT range[1]			64		127	°C
OTP range[1]			VR_HOT level		64 to 135	°C
I_CRITICAL filter bandwidth		Very Slow setting		3.66		Hz
		Slow setting		30.3		
Dynamic Phase Control						
Current filter bandwidth		For Phase drop		1		kHz
Timing Information						
Automatic Configuration from NVM[1]	t_3-t_2 in Figure 6	3.3V ready to end of configuration			1	ms
Automatic trim time[1]	t_4-t_3 in Figure 6				4	ms
EN Delay (to ramp start)				3		us
VID Delay (to ramp start)		Loop bandwidth dependent		5		us
Pwr_Rdy_L1/L2 & PwrGD delay		after reaching Boot voltage		20		us

Notes:

[1] Guaranteed by design

GENERAL DESCRIPTION

The IR3541 is a flexible, dual-loop, digital multiphase PWM buck controller optimized to convert a 12V input supply to the core voltage required by Intel and AMD performance microprocessors and DDR memory. It is easily configurable for 1-5 phase operation on Loop #1 and 0-2 phase operation on Loop #2. The IR3541 supports the same switching frequency on each loop. It is designed to meet the steady state and transient power requirements of high performance AMD and Intel processors.

The unique partitioning of analog and digital circuits within the IR3541 provides the user with easy configuration capability while maintaining the required accuracy and performance. Access to on-chip non-volatile memory (NVM) to store the IR3541 configuration parameters enables power supply designers to optimize their designs without changing external components.

The IR3541 controls two independent output voltages. Each voltage is controlled in an identical fashion, so that the user can configure and optimize each control loop individually. Unless otherwise described, the following functions are performed on the IR3541 on each control loop independently.

OPERATING MODES

The IR3541 can be used for Intel VR12 designs, AMD SVI designs and DDR Memory designs without significant changes to the external components (Bill of Materials). The required mode is selected in NVM and the pin-out, VID table and relevant functions are automatically configured. This greatly reduces time-to-market and eliminates the need to manage and inventory 3 different PWM controllers.

DIGITAL CONTROLLER & PWM

A linear Proportional-Integral-Derivative (PID) digital controller provides the loop compensation for system regulation. The digitized error voltage from the high-speed voltage error ADC is processed by the digital compensator. The digital PWM generator uses the outputs of the PID and the phase current balance control signals to determine the pulse width for each phase on each loop. The PWM generator has enough resolution to ensure that there are no limit cycles. The compensator coefficients are user configurable to enable optimized system response. The compensation algorithm uses a PID with two additional programmable poles. This provides the digital equivalent of a Type III analog compensator.

ADAPTIVE TRANSIENT ALGORITHM (ATA)

Dynamic load step-up and load step-down transients require fast system response to maintain the output voltage within specification limits. This is achieved by a unique adaptive non-linear transient control loop based on a proprietary algorithm.

NON-VOLATILE MEMORY

The non-volatile memory (NVM) stores the device configuration. At power-up, NVM contents are transferred to registers for access during operation. NVM allows customization during both design and high-volume manufacturing. NVM integrity is verified by cyclic redundancy code (CRC) checking on each power up. The controller will not start in the event of a CRC error.

Using NVM to configure basic device parameters such as frequency and boot voltage represents a significant size and component saving compared to traditional analog methods.

INTERNAL OSCILLATOR

The IR3541 has a single 192MHz internal oscillator that generates all the internal system clock frequencies required for proper device function. The oscillator frequency is factory trimmed for precision and has extremely low jitter (Figure 5) even in light-load mode (Figure 6). The single internal oscillator is used to set the same switching frequency on each loop.

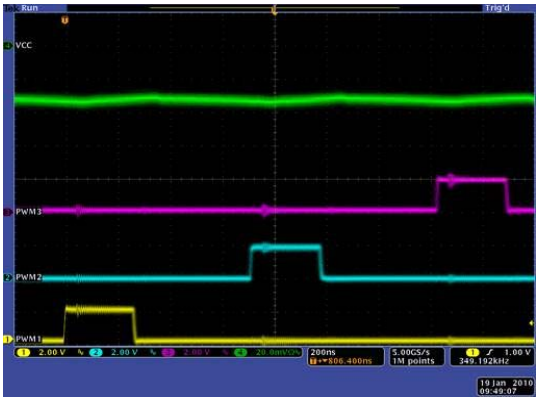


Figure 5: Persistence plot of a 3Φ, 50A system

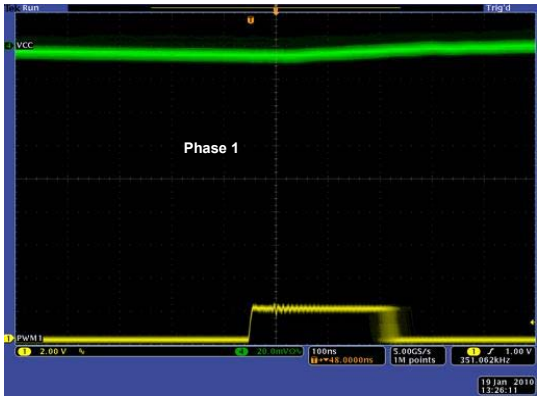


Figure 6: Persistence plot in 1Φ, 10A

HIGH-PRECISION VOLTAGE REFERENCE

The internal high-precision voltage reference supplies the required reference voltages to the VID DACs, ADCs and other analog circuits. This factory trimmed reference is guaranteed over temperature and manufacturing variations.

HIGH PRECISION CURRENT REFERENCE

An on-chip precision current reference is derived using an off-chip precision resistor connected to the RRES pin of the IR3541. RRES must be a 7.5kΩ, 1% tolerance resistor, placed very close to the controller pin to minimize parasitics.

VOLTAGE SENSE

An error voltage is generated from the difference between the target voltage, defined by the VID and loadline (if implemented), and the differential, remotely sensed, output voltage. For each loop, the error voltage is digitized by a high-speed, high-precision ADC. An anti-alias filter provides the necessary high frequency noise rejection. The gain and offset of the voltage sense circuitry for each loop is factory trimmed to deliver the required accuracy.

CURRENT SENSE

Lossless inductor DCR or precision resistor current sensing is used to accurately measure individual phase currents. Using a simple off-chip thermistor, resistor and capacitor network for each loop, a thermally compensated loadline is generated to meet the given power system requirement. A filtered voltage, which is a function of the total load current and the target loadline resistance, is summed into each voltage sense path to accomplish the Active Voltage Positioning (AVP) function.

VID DECODER

The VID decoder receives a VID code from the CPU that is converted to an internal code representing the VID voltage. This block also outputs the signal for VR disable if a VID shutdown code has been received. The VID code is 8 bits in Intel/MPoL modes, 7 bits in AMD SVI.

MOSFET DRIVER AND POWIRSTAGE COMPATIBILITY

The output PWM signals of the IR3541 are designed for compatibility with the IR3537 family of active tri-level (ATL) MOSFET drivers. IR3537 drivers have a fast disable capability which enables any phase to be turned off on-the-fly. It supports power-saving control modes, improved transient response, and superior on the fly phase dropping without having to route multiple output disable (ODB or SMOD) signals.

In addition, the IR3541 provides the flexibility to configure PWM levels to operate with external MOSFET drivers or PowIRstage devices that support Industry standard +3.3V tri-state signaling.

I2C & PMBUS INTERFACE

An I2C/SMBus/PMBus interface is used to communicate with the IR3541. This two-wire serial interface consists of clock, data signals and operates as fast as 400kHz. The bus provide read and write access to the internal registers for configuration and monitoring of operating parameters. Registers can also be used to program on-chip non-volatile memory (NVM) to store operating parameters.

To ensure operation with multiple devices on the bus, an exclusive address for the IR3541 is programmed into NVM.

The IR3541 supports the packet error checking (PEC) protocol and a number of PMBus commands to monitor voltages and currents. Refer to the PMBus section on page 40.

INTUITIVE POWER DESIGNER (IPD) GUI

The IPD GUI provides the designer with a comprehensive design environment that includes screens to calculate VR efficiency and DC error budget, design the thermal compensation networks and feedback loops, and produce calculated Bode plots and output impedance plots. The IPD environment is a key utility for design optimization, debug, and validation of designs that saves designer significant time, allowing faster time-to-market (TTM).

The IPD also allows real-time design optimization and real-time monitoring of key parameters such as output current and power, input current and power, efficiency, phase currents, temperature, and faults.

The Intuitive Power Designer (IPD) GUI allows access to the system configuration settings for switching frequency, MOSFET driver compatibility, soft start rate, VID table, PSI, loop compensation, transient control system parameters, input under-voltage, output over-voltage, output under-voltage, output over-current and over-temperature.

PROGRAMMING

Once a design is complete, the IPD produces a complete configuration file.

The configuration file can be re-coded into an I2C/PMBus Master (e.g. a Test System) and loaded into the IR3541 using the bus protocols described on page 40. The IR3541 has a special in-circuit programming mode that allows the NVM to be loaded at board test in mass production without powering on the entire board.

REAL-TIME MONITORING

The IR3541 can be accessed through the use of PMBus Command codes (described on page 40) to read the real time status of the VR system including input voltage, output voltage, input and output current, input and output power, efficiency, and temperature.

THEORY OF OPERATION

OPERATING MODE

The IR3541 changes its pin-out and functionality based on the user-selected operating mode, allowing 1 device to be used for multiple applications without significant BoM changes. This greatly reduces the user's design cycles and time-to-market.

The pin-out, VID table and functionality for each operating mode are completely configured by a simple selection in NVM as shown in Table 1.

TABLE 1: MODE SELECTION

Intel VR12
AMD SVI
MPoL Tracking

INTEL MODE

In Intel mode, the IR3541 configures its pins to be fully compliant with the Intel VR12 specification.

AMD SVI/PVI MODES

In AMD SVI mode, the IR3541 configures its pins to be fully compliant with the AMD SVI specification.

MPOL MODE

In MPoL mode, the IR3541 configures Loop 2 VID code to be 50% of Loop 1. Communication with and control of the IR3541 may occur either through the SVID interface where an Intel SVID Master is present or alternatively through the I2C/SMBus/PMBus interface for non-Intel applications.

DEVICE POWER-ON AND INITIALIZATION

The IR3541 is powered from a 3.3V DC supply. Figure 7 shows the timing diagram during device initialization. An internal LDO generates a 1.8V rail to power the control logic within the device. During initial startup, the 1.8V rail follows the rising 3.3V supply voltage, proportional to an internal resistor tree. The internal oscillator becomes active at t1 as the 1.8V rail is ramping up. Until soft-start begins, the IR3541 PWM outputs are disabled in a high impedance state to ensure that the system comes up in a known state.

The controller comes out of power-on reset (POR) at t2 when the 3.3V supply is high enough for the internal bias central to generate 1.8V. At this time the controller will detect the populated phases by sensing the voltage on the PWM pins. If the voltage is less than the Auto Phase Detect threshold (unused PWMs are grounded), the controller assumes the phase is unpopulated. This Auto Phase Detect feature can be disabled. Once the phase detection is complete the contents of the NVM are transferred to the registers by time t3 and the automatic trim routines are complete by time t4. The register settings and number of phases define the controller performance specific to the VR configuration - including trim settings, soft start ramp rate, boot voltage and PWM signal compatibility with the MOSFET driver.

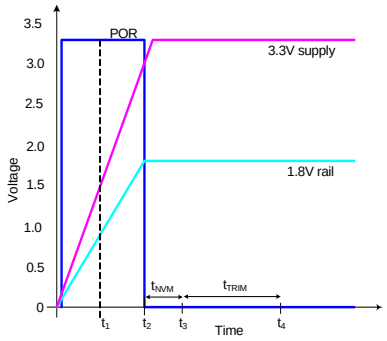


Figure 7: Controller startup and initialization

Once the registers are loaded from NVM, the I2C/PMBus interface can be used to re-configure the registers to suit the specific VR design requirements.

NVM PROGRAM CHECK

The IR3541 is shipped with a default configuration. Thus, to prevent an unprogrammed part from being enabled in a circuit, the IR3541 contains a protection circuit which disables the IR3541 until it is programmed by the user.

SUPPLY VOLTAGE

The controller is powered by the 3.3V supply rail. Once initialization of the device is complete, steady and stable supply voltage rails and a VR enable signal (EN) are required to set the controller into an active state. A high EN signal is required to enable the PWM signals and begin the soft start sequence after the 3.3V and 12V supply rails are determined to be within the defined operating bands. The recommended decoupling for the 3.3V is shown in Figure 8. The Vcc pins should have 0.1µF X7R type ceramic capacitors placed as close as possible to the package.

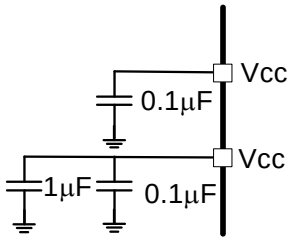


Figure 8: Vcc 3.3V decoupling

The V18A pin must have a 4.7µF, X5R type decoupling capacitor connected close to the package as shown in Figure 9 and a 0.47uF for additional immunity.

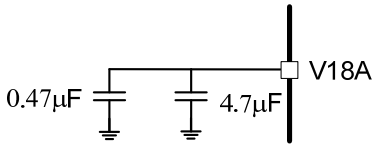


Figure 9: V18A decoupling

The 12V supply voltage on the VINSEN pin is compared against a fixed threshold. Once the rising 12V voltage crosses the turn-on threshold, EN is asserted and all PWM outputs become active.

The 12V supply voltage is valid until it declines below its turn-off level.

A 14:1 attenuation network is connected to the VINSEN pin as shown in Figure 10. Recommended values for a 12V system are R_{VIN_1} = 13kΩ and R_{VIN_2} = 1kΩ, with a 1% tolerance or better. C_{VINSEN} is usually not required or may be populated up to a maximum of 10nF for noise suppression.

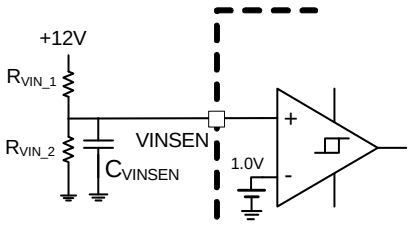


Figure 10: 12V resistor divider network

POWER-ON SEQUENCING

The VR power-on sequence is initiated when all of the following conditions are satisfied:

- IR3541 Vcc (+3.3V rail) > VCC UVLO
- Input Voltage (+12V rail) > Vin UVLO
- ENABLE is HIGH
- VR has no Over-current, Over-voltage or Under-voltage faults on either rail.
- NVM transfer to configuration registers occurred without parity error

Once the above conditions are cleared, start-up behavior is controlled by the operating mode.

MPoL MODE

The IR3541 follows startup and timing requirements as shown in Figure 11 and Table 2. When the power-on sequence is initiated, and with VBOOT set to > 0V, both rails will ramp to their configured voltages and assert VR_RDY_L1 and VR_RDY_L2. The slew rates for both loops are set independently per Table 18. If tracking is required during the slew, then care must be taken to ensure that the Loop 2 slew rate is set to ½ of the Loop 1 slew rate. Typical MPoL start-up and shut-down waveforms are shown in Figure 12 and Figure 13.

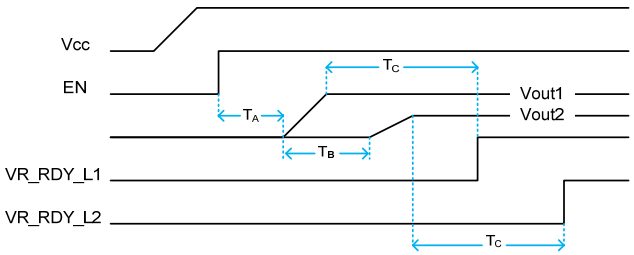


Figure 11: MPoL start-up

TABLE 2: MPoL START-UP TIMING

Time	Description	Min	Typ	Max
T_A	VR EN to Loop 1 ramp start		3us	
T_B	Loop 2 delay		Table3	
T_C	Voltage Ramp complete to VR_RDY_L1/L2			1us

Figure 12: MPoL tracking start-up

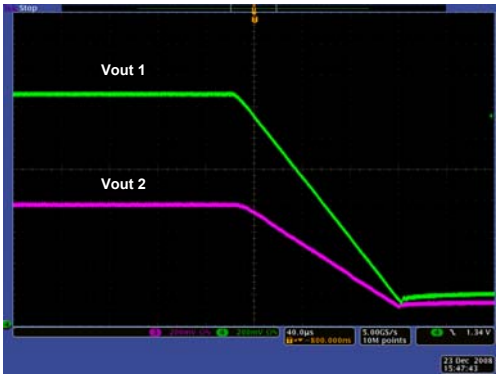


Figure 13: MPoL tracking shut-down

In MPoL mode, Loop 2 start-up can be delayed relative to Loop 1 according to Table 3.

TABLE 3: MPoL LOOP 2 START-UP DELAY

Loop 2 delay
0 – 678.3us in 2.66us steps

INTEL MODE

When the power-on sequence is initiated, and with Vboot set to > 0V, both rails will ramp to their configured boot voltages and assert VR_READY_L1 and VR_READY_L2. The slew rate to VBOOT is programmed per Table 18.

If Vboot>0V on both loops, then both loops will ramp at the same time. If Vboot= 0V, the VR will stay at 0V and will not soft-start until the CPU issues a VID command to the appropriate loop.

Intel Boot Voltage

The IR3541 Vboot voltage is fully programmable in NVM to the range shown in Table 4. Table 12 shows the Intel/MPoL VID table.

TABLE 4: VBOOT RANGE

Loop	Boot Voltage
Loop 1	Per Intel/MPoL VID table
Loop 2	Per Intel/MPoL VID table

Intel Catastrophic Failure Protection (CFP)

In Server computer systems, the CFP signal is commonly used to immediately shut down the input supply when an OVP occurs. The IR3541 can be configured to generate this signal by re-configuration of the SMB_ALERT# pin through NVM settings.

Intel SVID Interface

The IR3541 implements a fully compliant VR12 Serial VID (SVID) interface. This is a three-wire interface between a VR12 compliant processor and a VR that consists of clock, data and alert# signals.

The IR3541 architecture is based upon a digital core and hence lends itself very well to digital communications. As such, the IR3541 implements all the required SVID registers and commands. The IR3541 also implements all the optional commands and registers with only a very few exceptions. The Intel CPU is able to detect and recognize the extra functionality that the IR3541 provides and thus gives the Intel VR12 CPU unparalleled ability to monitor and optimize its power.

The SVID address of the IR3541 is programmed in NVM.

Intel Offsets

In addition to the mandatory features of the SVID bus, the IR3541 provides optional volatile SVID registers which allow the user to offset the reporting on the SVID interface as detailed in Table 5.

TABLE 5: SVID OFFSET REGISTERS

Parameter	Memory	Range	Step Size
Output Voltage	R/W	-128 to +127	1 VID code
Output Current	NVM	-4A to +3.75A	0.25A
Temperature	R/W	-32°C to +31°C	1°C

Intel IMON Scaling

Current measurements reported to the Intel processor must be skewed so as not to under-report current. This ensures that the processor will not exceed the thermal design point and maximum current capability of the system. Typical VR controllers use a fixed offset or scale factor. Rather than providing a fixed scaling factor, the IR3541 contains a user-programmable scale factor (Table 6 and Figure 14). The programmable scale factor, together with a programmable current offset, allow the user to match the IMON scaling to the design's VRTOB (Voltage Regulator Tolerance Band) calculation. This provides the most accurate current reporting across the entire load range and maximizes the performance of Intel turbo and normal when compared with other VR12 voltage regulators.

TABLE 6: IMON SCALE FACTOR

RANGE	94% to 106%
STEP SIZE	2% steps

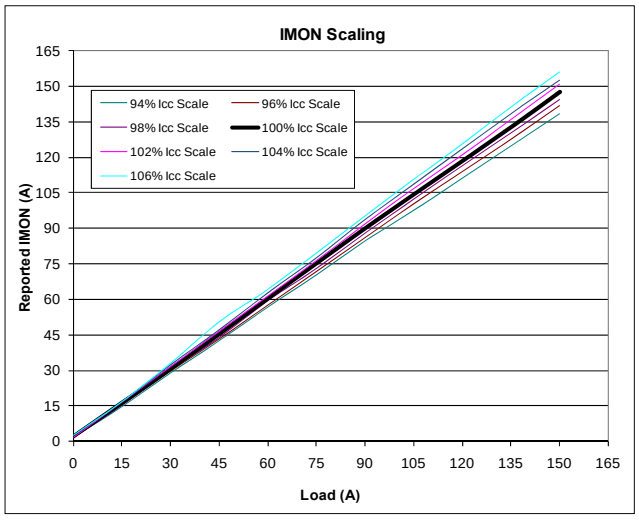


Figure 14: Imon Scaling

AMD SVI MODE

When the power-on sequence is initiated, both rails will ramp to the configured Vboot voltage and assert PWRGD. The soft-start occurs at the Slew rate selected in Table 18, typically 2.5mV/us.

The boot voltage is decoded from the SVC and SVD levels when the EN pin is asserted high as shown in Table 7. This value is latched and will be re-used in the event of a soft reset (de-assertion and re-assertion of PwrOK). Note, Vcc must be stable for a minimum 5ms delay before the IC is enabled to ensure that the Boot voltage is decoded from the SVI correctly.

TABLE 7: AMD SVI BOOT TABLE

Boot Voltage	SVC	SVD
1.1V	0	0
1.0V	0	1
0.9V	1	0
0.8V	1	1

Alternatively, the AMD boot voltage can be set by an NVM register instead of decoding the SVI signals as shown in Table 8.

TABLE 8: AMD BOOT OPTIONS

NVM Boot Register	Boot Location
Bit[7]=low	Decode from SVI per Table 7
Bit[7]=high	Use NVM Boot Register bits [6:0]

AMD PwrOK

The IR3541 regulates to the boot voltage whenever PwrOK is low. When PwrOK is asserted high, the IR3541 responds to commands sent over the SVI interface.

AMD CBOUT Crowbar Output

In Server computer systems, CBOUT signal is commonly used to immediately shut down the input supply when an OVP or OTP occurs. The ir3541 can be configured to generate this signal by re-configuration of the SMB_ALERT# pin through NVM settings.

AMD VFIXEN Hardware Override

The IR3541 allows the SVI interface to be bypassed in the event of CPU SVI communication breakdown. Asserting VFIXEN active high, enables VFIX mode and sets the output voltage according to Table 9. VFIXEN must be tied low to disable.

TABLE 9: VFIXEN CODING

VFIX Voltage	SVC	SVD
1.4V	0	0
1.2V	0	1
1.0V	1	0
0.8V	1	1

AMD SVI Interface

The IR3541 implements a fully compliant AMD Serial VID interface (SVI). This is a two-wire interface between an SVI compliant processor and a VR and consists of clock and data signals using the SMBus "Send Byte" protocol.

AMD PSI_L flag

The PSI_L signal is contained within the SVI command, and when asserted, indicates that the processor is in a low power state (<20A). The IR3541 can be programmed to drop down to 1 or 2 phase operation in this state.

AMD VID Offset

The IR3541 provides a method to offset the VID voltage either negative or positive by a fixed value. The offset is programmed in multiples of 6.25mV steps. Table 10 shows the programmable range. Note that applying an offset will reduce the range of the available VID table by the amount of the offset.

TABLE 10: AMD SVI VID OFFSET

	VID Offset	
	Register value	**Offset**
Minimum	-8	-50mV
No offset	0	0mV
Maximum	+7	+43.75mV

AMD Socket G34 Support & I-spike Support

The IR3541 has been specifically designed to support the G34 socket and advanced AMD CPUs which requires a loadline of typically 1.3mΩ, VID offset of typically 35mV and provision to account for a large current spike (Idd-spike) above the Thermal Design Point (TDP) of the system so long as it lasts for a short time. The IR3541 implements this by allowing the user to set the OCP level to accommodate the current spike and by either programming the I_CRITICAL threshold to limit the average current or OTP threshold to ensure the TDP is protected.

HIGH SPEED BUS UTILITIES

Both Intel and AMD employ high speed serial buses to communicate information between the processor and the voltage regulator. High speed buses in the vicinity of high voltage and high current switching requires careful design to maintain signal integrity. However, the high voltage switching nodes with high frequency ringing found in VRs, can couple noise on to the communications lines (Figures 15 and 16).

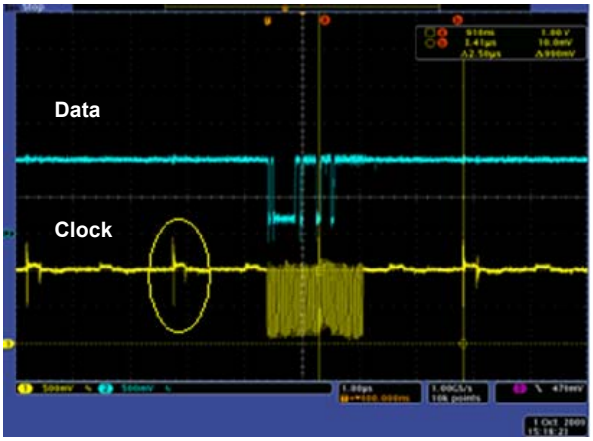


Figure 15: High speed bus picking up regulator switching noise

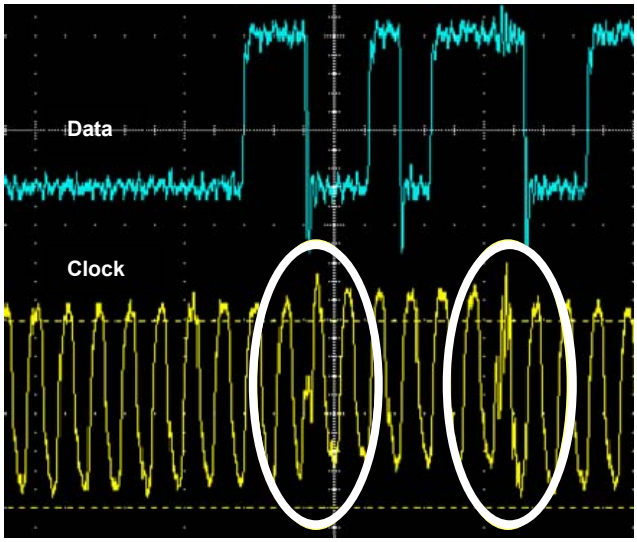


Figure 16: Noise Corruption in the Clock Line

In the event that a board layout has poor signal integrity or unanticipated data skew, the IR3541 includes utilities (Table 11) to improve bus data integrity. These utilities allow the designer to tune the bus I/O on the IR3541 to achieve high quality communications with poor layouts, avoiding extra board spins.

TABLE 11: HIGH SPEED BUS UTILITIES

Utility	Range
Programmable Low Pass Filter	35MHz - 1591MHz
Programmable Glitch Rejection	1.2ns – 5ns
Programmable Clock to Data skew	1.24ns – 3.94ns
Programmable Timeout period	0 – 10.6us

Figure 17 shows how noise in the bus can cause errors and finally Figure 18 demonstrates that enabling the appropriate bus utility setting cleans up the noise.

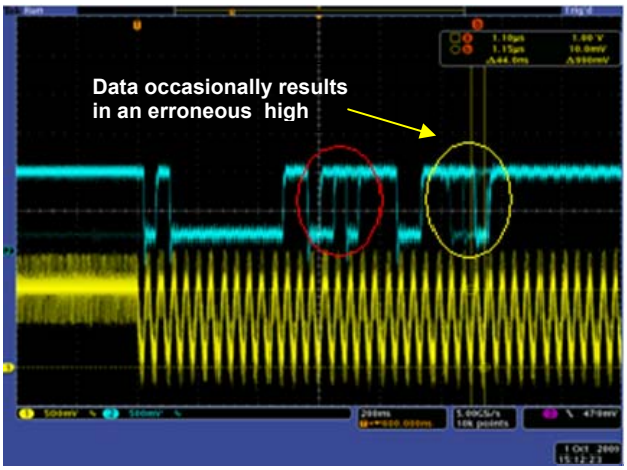


Figure 17: Data Corruption without IR Utilities

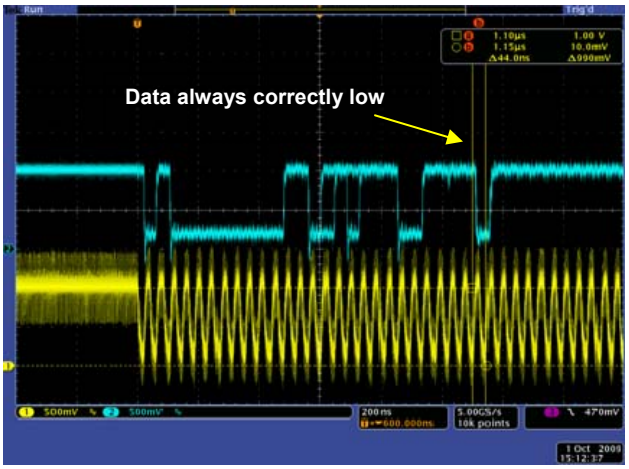


Figure 18: Robust Communication with IR Utilities

VID VOLTAGE & TABLES

The IR3541 contains 2 different VID tables to facilitate operation with different generations of Intel and AMD CPUs. The correct VID table is automatically selected when the Operating Mode is selected In NVM. The Intel/MPoL VIDs are shown in Table 12 and AMD SVI VIDs in Tables 13.

Figure 19 shows typical VID voltage performance over temperature.

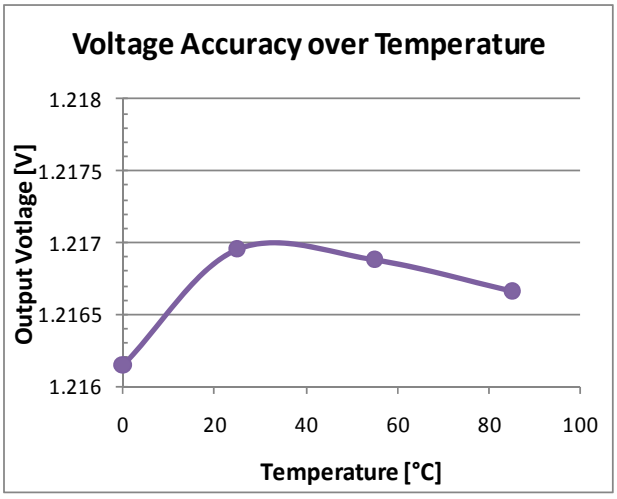


Figure 19: Typical Voltage Accuracy over Temperature

TABLE 12: INTEL/MPOL VID TABLE

VID (Hex)	Voltage	VID (Hex)	Voltage	VID (Hex)	Voltage	VID (Hex)	Voltage	VID (Hex)	Voltage
00	0.000	34	0.505	68	0.765	9C	1.025	D0	1.285
01	0.250	35	0.510	69	0.770	9D	1.030	D1	1.290
02	0.255	36	0.515	6A	0.775	9E	1.035	D2	1.295
03	0.260	37	0.520	6B	0.780	9F	1.040	D3	1.300
04	0.265	38	0.525	6C	0.785	A0	1.045	D4	1.305
05	0.270	39	0.530	6D	0.790	A1	1.050	D5	1.310
06	0.275	3A	0.535	6E	0.795	A2	1.055	D6	1.315
07	0.280	3B	0.540	6F	0.800	A3	1.060	D7	1.320
08	0.285	3C	0.545	70	0.805	A4	1.065	D8	1.325
09	0.290	3D	0.550	71	0.810	A5	1.070	D9	1.330
0A	0.295	3E	0.555	72	0.815	A6	1.075	DA	1.335
0B	0.300	3F	0.560	73	0.820	A7	1.080	DB	1.340
0C	0.305	40	0.565	74	0.825	A8	1.085	DC	1.345
0D	0.310	41	0.570	75	0.830	A9	1.090	DD	1.350
0E	0.315	42	0.575	76	0.835	AA	1.095	DE	1.355
0F	0.320	43	0.580	77	0.840	AB	1.100	DF	1.360
10	0.325	44	0.585	78	0.845	AC	1.105	E0	1.365
11	0.330	45	0.590	79	0.850	AD	1.110	E1	1.370
12	0.335	46	0.595	7A	0.855	AE	1.115	E2	1.375
13	0.340	47	0.600	7B	0.860	AF	1.120	E3	1.380
14	0.345	48	0.605	7C	0.865	B0	1.125	E4	1.385
15	0.350	49	0.610	7D	0.870	B1	1.130	E5	1.390
16	0.355	4A	0.615	7E	0.875	B2	1.135	E6	1.395
17	0.360	4B	0.620	7F	0.880	B3	1.140	E7	1.400
18	0.365	4C	0.625	80	0.885	B4	1.145	E8	1.405
19	0.370	4D	0.630	81	0.890	B5	1.150	E9	1.410
1A	0.375	4E	0.635	82	0.895	B6	1.155	EA	1.415
1B	0.380	4F	0.640	83	0.900	B7	1.160	EB	1.420
1C	0.385	50	0.645	84	0.905	B8	1.165	EC	1.425
1D	0.390	51	0.650	85	0.910	B9	1.170	ED	1.430
1E	0.395	52	0.655	86	0.915	BA	1.175	EE	1.435
1F	0.400	53	0.660	87	0.920	BB	1.180	EF	1.440
20	0.405	54	0.665	88	0.925	BC	1.185	F0	1.445
21	0.410	55	0.670	89	0.930	BD	1.190	F1	1.450
22	0.415	56	0.675	8A	0.935	BE	1.195	F2	1.455
23	0.420	57	0.680	8B	0.940	BF	1.200	F3	1.460
24	0.425	58	0.685	8C	0.945	C0	1.205	F4	1.465
25	0.430	59	0.690	8D	0.950	C1	1.210	F5	1.470
26	0.435	5A	0.695	8E	0.955	C2	1.215	F6	1.475

VID (Hex)	Voltage	VID (Hex)	Voltage	VID (Hex)	Voltage	VID (Hex)	Voltage	VID (Hex)	Voltage
27	0.440	5B	0.700	8F	0.960	C3	1.220	F7	1.480
28	0.445	5C	0.705	90	0.965	C4	1.225	F8	1.485
29	0.450	5D	0.710	91	0.970	C5	1.230	F9	1.490
2A	0.455	5E	0.715	92	0.975	C6	1.235	FA	1.495
2B	0.460	5F	0.720	93	0.980	C7	1.240	FB	1.500
2C	0.465	60	0.725	94	0.985	C8	1.245	FC	1.505
2D	0.470	61	0.730	95	0.990	C9	1.250	FD	1.510
2E	0.475	62	0.735	96	0.995	CA	1.255	FE	1.515
2F	0.480	63	0.740	97	1.000	CB	1.260	FF	1.520
30	0.485	64	0.745	98	1.005	CC	1.265		
31	0.490	65	0.750	99	1.010	CD	1.270		
32	0.495	66	0.755	9A	1.015	CE	1.275		
33	0.500	67	0.760	9B	1.020	CF	1.280		

TABLE 13: AMD SVI VID TABLE

VID CODE	VOLTAGE	VID CODE	VOLTAGE	VID CODE	VOLTAGE
00h	1.5500V	30h	0.9500V	60h	0.3500V
01h	1.5375V	31h	0.9375V	61h	0.3375V
02h	1.5250V	32h	0.9250V	62h	0.3250V
03h	1.5125V	33h	0.9125V	63h	0.3125V
04h	1.5000V	34h	0.9000V	64h	0.3000V
05h	1.4875V	35h	0.8875V	65h	0.2875V
06h	1.4750V	36h	0.8750V	66h	0.2750V
07h	1.4625V	37h	0.8625V	67h	0.2625V
08h	1.4500V	38h	0.8500V	68h	0.2500V
09h	1.4375V	39h	0.8375V	69h	0.2375V
0Ah	1.4250V	3Ah	0.8250V	6Ah	0.2250V
0Bh	1.4125V	3Bh	0.8125V	6Bh	0.2125V
0Ch	1.4000V	3Ch	0.8000V	6Ch	0.2000V
0Dh	1.3875V	3Dh	0.7875V	6Dh	0.1875V
0Eh	1.3750V	3Eh	0.7750V	6Eh	0.1750V
0Fh	1.3625V	3Fh	0.7625V	6Fh	0.1625V
10h	1.3500V	40h	0.7500V	70h	0.1500V
11h	1.3375V	41h	0.7375V	71h	0.1375V
12h	1.3250V	42h	0.7250V	72h	0.1250V
13h	1.3125V	43h	0.7125V	73h	0.1125V
14h	1.3000V	44h	0.7000V	74h	0.1000V
15h	1.2875V	45h	0.6875V	75h	0.0875V
16h	1.2750V	46h	0.6750V	76h	0.0750V
17h	1.2625V	47h	0.6625V	77h	0.0625V
18h	1.2500V	48h	0.6500V	78h	0.0500V
19h	1.2375V	49h	0.6375V	79h	0.0375V
1Ah	1.2250V	4Ah	0.6250V	7Ah	0.0250V
1Bh	1.2125V	4Bh	0.6125V	7Bh	0.0125V
1Ch	1.2000V	4Ch	0.6000V	7Ch	OFF
1Dh	1.1875V	4Dh	0.5875V	7Dh	OFF
1Eh	1.1750V	4Eh	0.5750V	7Eh	OFF
1Fh	1.1625V	4Fh	0.5625V	7Fh	OFF
20h	1.1500V	50h	0.5500V		
21h	1.1375V	51h	0.5375V		
22h	1.1250V	52h	0.5250V		
23h	1.1125V	53h	0.5125V		
24h	1.1000V	54h	0.5000V		
25h	1.0875V	55h	0.4875V		
26h	1.0750V	56h	0.4750V		
27h	1.0625V	57h	0.4625V		
28h	1.0500V	58h	0.4500V		
29h	1.0375V	59h	0.4375V		
2Ah	1.0250V	5Ah	0.4250V		
2Bh	1.0125V	5Bh	0.4125V		
2Ch	1.0000V	5Ch	0.4000V		
2Dh	0.9875V	5Dh	0.3875V		
2Eh	0.9750V	5Eh	0.3750V		
2Fh	0.9625V	5Fh	0.3625V		

FLEXIBLE PHASING

The IR3541 is configurable to operate up to five phases, which can be flexibly assigned to two loops as shown in Table 14. The phase of the PWM outputs is automatically adjusted to optimize phase interleaving for minimum output ripple. Phase interleaving results in a ripple frequency that is the product of the switching frequency times the number of phases. A high ripple frequency results in reduced ripple voltage and output filter capacitance requirements.

Unused Phases

Phases are disabled based upon the configuration shown in Table 14. Note that loop phases are disabled in reverse order e.g. in 2+1 mode, phases 4 & 3 are disabled. Disabled PWM outputs should be left floating.

In addition, the IR3541 detects the number of populated phases at start-up by comparing the voltage on the PWM pin against the phase detection threshold. Unused PWM outputs should be grounded so that their voltage is below the threshold (phase is disabled). The IR3541 will automatically adjust the phase configuration to operate with the populated phases (up to the configuration allowed by the settings in Table 14). As an example, a 3+1 configuration can have phase 3 PWM left unconnected to operate in 2+1 mode. Typical PWM pulse phase relationships are shown in Figure 20.

TABLE 14: FLEXIBLE DUAL-LOOP PHASE SELECTION

ACTIVE PHASES		
Config	**PWMx Loop #1**	**PWMy Loop #2**
1+0	1	-
1+1	1	**5**
2+0	1-2 (180º)	-
2+1	1-2 (180º)	**5**
2+2	1-2 (180º)	**4-5 (180º)**
3+0	1-3 (120º)	-
3+1	1-3 (120º)	**5**
3+2	1-3 (120º)	**4-5 (180º)**
4+0	1-4 (90º)	-
4+1	1-4 (90º)	**5**
5+0	1-5 (72º)	-

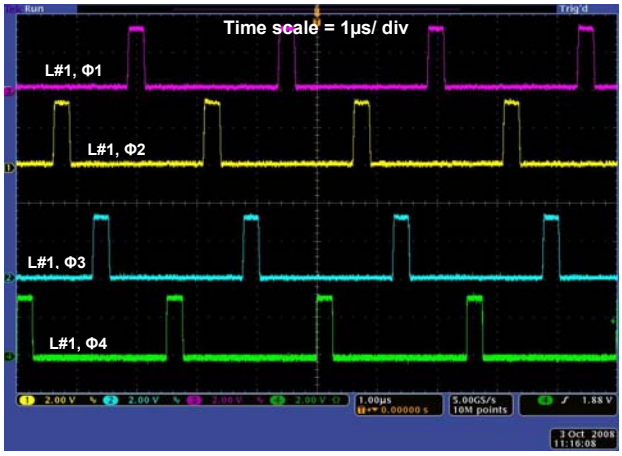


Figure 20: 4 phase PWM interleaved operation

SWITCHING FREQUENCY

The phase switching frequency (Fsw) of the IR3541 is set by a user configurable register. The IR3541 provides fine granularity as shown in Figure 21. The IR3541 oscillator is factory trimmed to guarantee absolute accuracy and very low jitter compared to analog controllers.

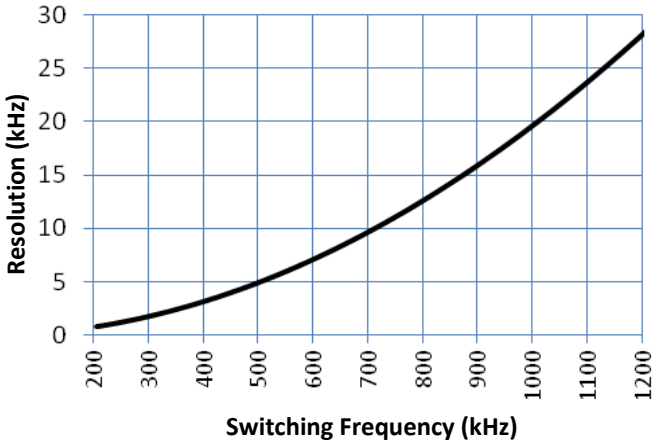


Figure 21: Switching Frequency Resolution

MOSFET DRIVER AND POWIRSTAGE SELECTION

The PWM signals from the active phases of the IR3541 are designed to operate with Active Tri-Level (ATL) type or industry standard tri-state type drivers or PowIRstage devices. ATL drivers are preferred because they have a fast phase disable capability with only a single control signal to the driver. The fast disable capability of the IR driver can be used to enhance transient response when used with the non-linear transient control. The user selects tri-state type drivers with 1.8V PWM voltage level (for IR3537) or 3.3V PWM level as shown in Table 15. The logic operation for these two types of tri-state drivers is depicted in Figures 22 and 23. The driver mode configuration is stored in the NVM.

In addition, the IR3541 provides the flexibility to configure PWM levels to operate with external MOSFET drivers or PowIRstage devices that support +3.3V tri-state signaling. The IR3541, when in 3.3V tri-state mode, floats the outputs so that the voltage level is determined by an external voltage divider which is typically inside the driver MOSFET. Sometimes external resistors are added to improve the speed of the PWM signal going into tri-state.

Note that the PWM outputs are tri-stated whenever the controller is disabled (EN=low) and the shut-down ramp has completed and before the soft-start ramp is initiated

TABLE 15: DRIVER LOGIC LEVEL SELECTION

Tri-level PWM voltage
3.3V (Tri-state)
1.8V (IR Active Tri-Level)

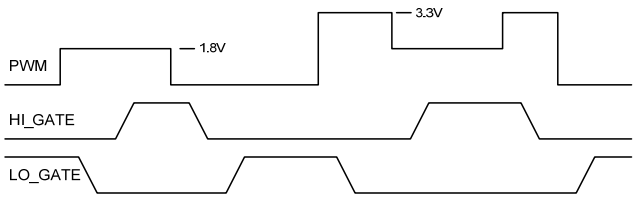


Figure 22: 1.8V Active Tri-level (ATL) Logic Levels

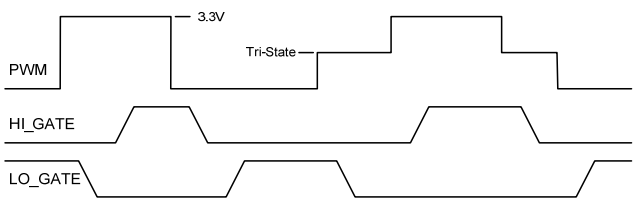


Figure 23: 3.3V Tri-state Driver logic levels

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The IR3541 VSEN and VRTN pins for each loop are connected to the load sense pins of each output voltage to provide true differential remote voltage sensing with high common-mode rejection. Each loop has a high bandwidth error amplifier which generates the error voltage between this remote sense voltage and the target voltage. The error voltage is digitized by a fast, high precision ADC.

As shown in Figure 24, the VSEN and VRTN inputs have a 2KΩ pull-up to an internal 1V rail. This causes some current flow in the VSEN and VRTN lines so external impedance should be kept to a minimum to avoid creating an offset in the sensed output voltage.

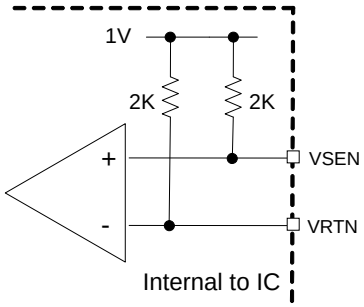


Figure 24: Output Voltage sensing impedance

CURRENT SENSING

The IR3541 provides per phase current sensing to support accurate Adaptive Voltage Positioning (AVP), current balancing, and over-current protection. The differential current sense scheme supports both lossless inductor DCR and per phase precision resistor current sensing techniques.

For DCR sensing, a suitable resistor-capacitor network of R_{sen} and C_{sen} is connected across the inductor in each phase as shown in Figure 25. The time constant of this RC network is set to equal the inductor time constant (L/DCR) such that the voltage across the capacitor C_{sen} is equal to the voltage across the inductor DCR.

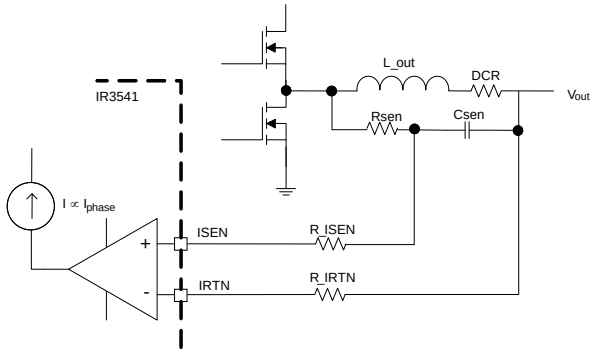


Figure 25: DCR Current Sensing

A current proportional to the inductor current in each phase is generated and used for per phase current balancing. The individual phase current signals are summed to arrive at the total current. The phase currents and total current are quantized by the monitor ADC and used to implement the current monitoring and OCP features. The total current is also summed with the VID DAC output to implement the AVP function (see Figure 3).

The recommended value for C_{sen} is a 100nF NPO type capacitor. For an assumed operating temperature higher than ambient, T_{op}, the R_{sen} resistor can be calculated by

$$R_{sen} = \frac{L\_out}{C_{sen} * L\_DCR\,@\,25^{o}C * [1 + 0.00393 * (T_{op} - 25)]}$$

Identical resistors (R_ISEN and R_IRTN) are connected to the ISEN and IRTN pins of each phase for the best common mode rejection. The required value is:

R_ISEN, R_IRTN = 301Ω, 1% resistor

These components must be placed close to the IR3541 pins.

CURRENT BALANCING & OFFSET

The IR3541 provides accurate digital phase current balancing in any phase configuration. Current balancing equalizes the current across all the phases. This improves efficiency, prevents hotspots and reduces the possibility of inductor saturation.

The sensed currents for each phase are converted to a voltage and are multiplexed into the monitor ADC. The digitized phase currents are low-pass filtered and passed through a proprietary current balance algorithm to equalize them as shown in Figure 26.

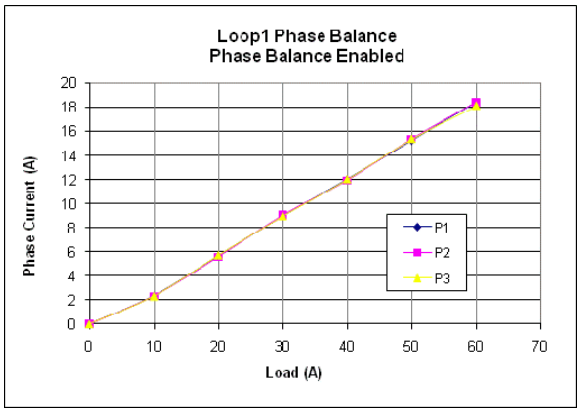


Figure 26: Typical Phase Current Balance (3-phases enabled)

A unique high-speed active phase current balance operates during load transients to eliminate current imbalance that can result from a load current oscillating near the switching frequency. The phase pulse widths are compared and the largest pulse is skipped if its pulse width exceeds an internally set threshold relative to the smallest phase (Figure 27). This ensures that the phases remain balanced during high frequency load transients.

Figure 27: High Speed Phase Balance for a 10A→109A 245kHz load-step

In addition, the IR3541 allows the user to offset phase currents to optimize the thermal solution. A positive gain can be applied to a particular phase to create a current offset, which proportional to load current, relative to the other phases. The increase in current relative to a non-programmed phase is given by:

$$PhaseX\ \ Current\ \ Gain = \frac{1}{1 - \frac{PhaseX\ \_Gain}{64}}$$

The Phase Current gain is programmed as shown in Table 16. Figure 28 shows the current difference versus the imbalance setting between phase one and the other five phases of a six-phase VR.

TABLE 16: PHASE CURRENT GAIN (OFFSET)

Settings Range	0 to 15
Average Gain step	2%
Maximum gain	30%

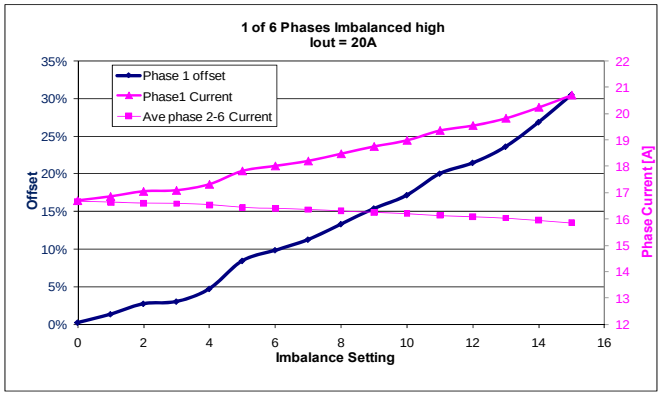


Figure 28: Phase 1 Current Imbalance

CURRENT CALIBRATION

For optimizing the current measurement accuracy of a design or even individual boards, the IR3541 contains a register in NVM which can store a user-programmed Total Current Offset to zero the no-load current reading. Refer to Table 37 for input and output current calibration registers.

LOAD LINE

The IR3541 enables the implementation of accurate, temperature compensated load lines on both loops. The load line is set by an external resistor R_{CS}, as shown in Figure 30 and the nominal value must also be stored in NVM. The stored value provides the IR3541 with the scaling factor for the digital computation of the total current to determine the OCP threshold PMBus current reporting. The load line ranges for IR3541 are shown in Table 17.

TABLE 17: LOAD LINE SETTINGS

	Loop #1	Loop #2
Minimum	0.0 mΩ	0.0 mΩ
Maximum	3.175 mΩ	6.375 mΩ
Resolution	0.025 mΩ	0.025 mΩ

Figure 29 shows a typical 0.8mΩ loadline measurement with minimum and maximum error ranges. The IR accuracy lies well within common processor requirements.

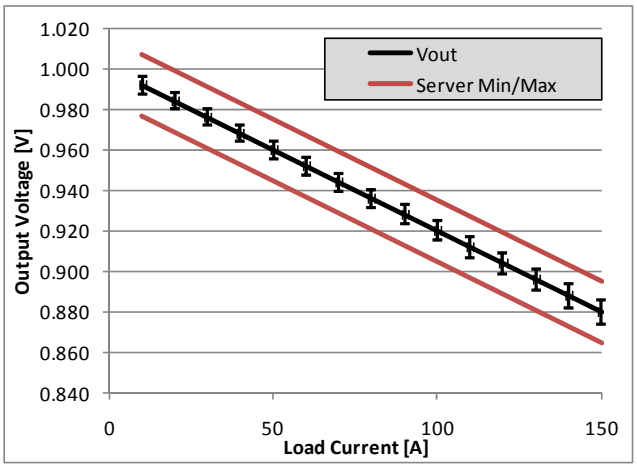


Figure 29: Load Line Measurements

For each loop, the sensed current from all the active phases is summed and applied to a resistor network across the RSCP and RCSM pins. This generates a precise proportional voltage which is summed with the sensed output voltage and VID DAC reference to form the error voltage. Also part of the network shown in Figure 30 is thermistor, R_{Th}. For proper loadline temperature compensation, the thermistor is placed near the phase one inductor to accurately sense the VR temperature.

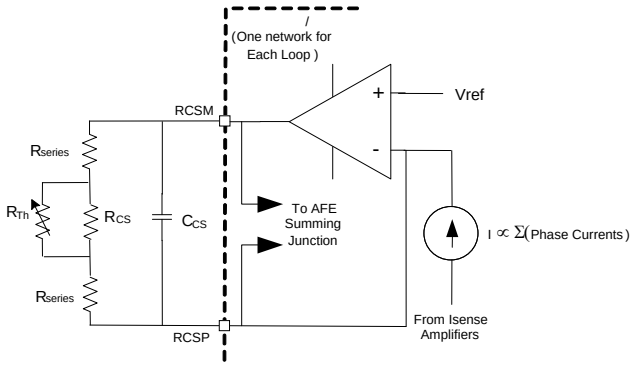


Figure 30: Load Line & Thermal Compensation

The resistor R_{CS} is calculated using the follow procedure. First the designer calculates the $R_{CSeffective}$ or the total effective parallel resistance across the RSCP and RCSM pins. It is defined by,

$$R_{CS\,effective} = 6 \times R\_ISEN \times \frac{R_{LL}}{DCR}$$

Where R_{LL} is the desired loadline; typically 1.0mΩ, DCR is DC resistance of the phase inductor, and R_ISEN is the series resistor across the inductor sense circuit. The required value for R_ISEN is a 301 Ω, 1% tolerance. Then the designer chooses a suitable NTC thermistor. Thermistor R_{th} is typically selected to have the lowest thermal coefficient and tightest tolerance in a standard available package. A typical value for the NTC will be 10kΩ, 1%.

Then the designer calculates R_{CS} using the following equation:

$$R_{CS} = \frac{1}{\frac{1}{R_{CSeffective} - 2 \times R_{series}} - \frac{1}{R_{Th}}}$$

R_{series} is selected to achieve minimum loadline error over temperature. The IR IPD provides a graphical tool that allows the user to easily calculate the resistor values for minimum error.

The capacitor C_{CS} is defined by the following equation:

$$C_{CS} = \frac{1}{2 \times \pi \times RCSeffective \times f_{AVP}}$$

where f_{AVP} is the user selectable current sense AVP bandwidth. The best bandwidth is typically in the range 500kHz to 1MHz.

Setting 0mΩ Loadline

The load line is turned off by setting a digital bit in the IR3541 register map. This is a separate bit from the load line settings for each loop.

Even though the loadline is disabled digitally, the resistors and loadline register should be set such that the load line is at least 3 times the value of low ohmic DCR inductors (<0.5mΩ) or 1 times the DCR value for high ohmic inductors (>0.5mΩ), e.g. if the inductor(s) DCR is 0.3mΩ, a notional 0.9 mΩ load line should be set. For accurate current measurement and OCP threshold with the loadline disabled, the loadline register must be set to the same value as the loadline set with the external resistor network. With loadline disabled, the thermistor and Ccs capacitor must still be installed to ensure accuracy of the current measurement.

DIGITAL FEEDBACK LOOP & PWM

The IR3541 uses a digital feedback loop to minimize the requirement for output decoupling and maintain a tightly regulated output voltage. The error between the target and the output voltage is digitized. This error voltage is then passed through a low pass filter to smooth ripple and then passed through a PID (Proportional Integral Derivative) compensator followed by an additional single pole filter. The loop compensation parameters K_p (proportional coefficient), K_I (integral coefficient), and K_D (derivative coefficient) and low-pass filter pole locations are user configurable to optimize the VR design for the chosen external components.

The IR3541 significantly reduces design time because the loop coefficients need to be calculated only once. Simply enable any number of phases and design the compensation coefficients. The IR3541 will intelligently scale the coefficients automatically as phases dynamically add and drop to maintain optimum stability (Figure 31).

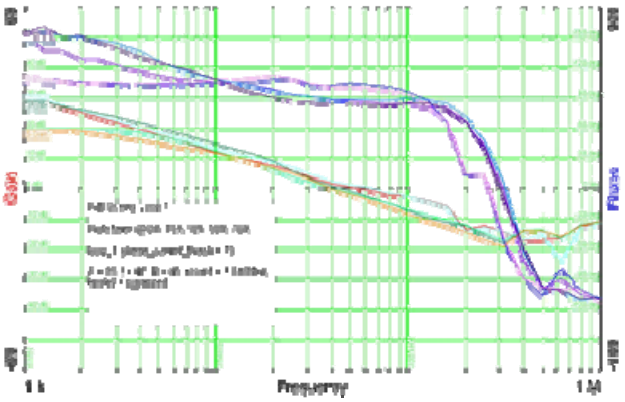


Figure 31: Stability with Phase Add/Drop

Each of the proportional, integral and derivative terms is a 6-bit value stored in NVM that is decoded by the IC's digital code. This allows the designer to set the converter bandwidth and phase margin to the desired values.

The compensator transfer function is defined as

$$(Kp + \frac{Ki}{s} + Kd \bullet s) \bullet \left(\frac{1}{1 + {}^{s}/_{\omega p_1}} \right) \bullet \left(\frac{1}{1 + {}^{s}/_{\omega p_2}} \right)$$

where ωp_1 and ωp_2 are configurable poles typically positioned to filter noise and ripple and roll off the high-frequency gain that the K_D term creates.

The outputs of the compensator and the phase current balance block are fed into a digital PWM pulse generator to generate the PWM pulses for the active phases. The digital PWM generator has a native time resolution of 625ps which is combined with digital dithering to provide an effective PWM resolution of 156.25ps. This ensures that there is no limit cycling when operating at the highest switching frequency.

ADAPTIVE TRANSIENT ALGORITHM (ATA)

The IR3541 Adaptive Transient Algorithm (ATA) is a high speed non-linear control technique that allows compliance with CPU voltage transient load regulation requirements with minimum output bulk capacitance for reduced system cost.

A high-speed digitizer measures both the magnitude and slope of the error signal to predict the load current transient. This prediction is used to control the pulse widths and the phase relationships of the PWM pulses. The ATA bypasses the PID control momentarily during load transients to achieve very wideband closed loop control and smoothly transitions back to PID control during steady state load conditions. Figure 32 illustrates the transient performance improvement provided by the ATA showing the clear reduction in undershoot and overshoot. Figure 33 is a close up of a load-step illustrating the fast reaction time of ATA and how the algorithm changes the pulse phase relationships. ATA can be disabled if desired.

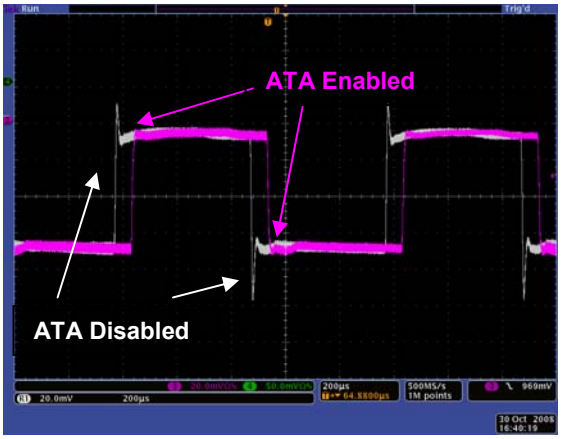


Figure 32: ATA. 5A to 70A 1KHz Load step

Figure 33: Load step with ATA enabled (L=215nH, Fsw=400kHz)

During a load transient overshoot, the ATA can also be programmed to turn off the low-side MOSFETS instead of holding them on. This forces the load current to flow through the larger forward voltage of the FET body diode and helps to reduce the overshoot created during a load release (Figure 34).

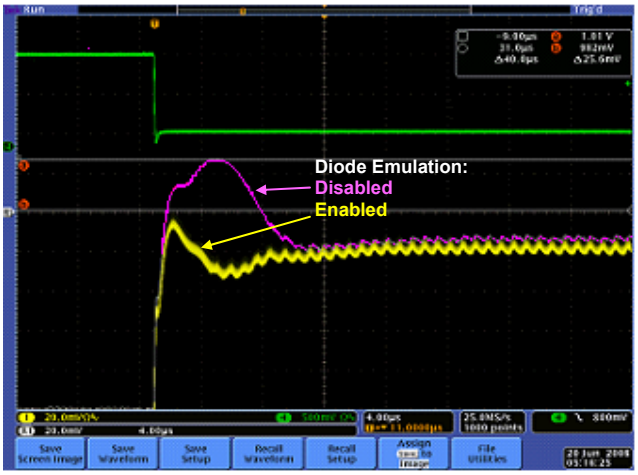


Figure 34: Diode emulation during a load-release

DYNAMIC VID SLEW RATE

The default slew rate is 2.5mV. The IR3541 provides the VR designer with 8 slew rates up to 12.5mV/us by selecting a notional 'FAST' slew rate and then applying a ½ or ¼ multiplier as shown in Table 18. Note that the Fast Slew Rate up to 25mV/us is accessible in Intel mode only.

TABLE 18: SLEW RATES

	FAST rate	½ Multiplier	¼ Multiplier
mV/us	10	5.0	2.50
	15	7.5	3.75
	20	10	5.00
	25	12.5	6.25

IR EFFICIENCY SHAPING

In addition to CPU-specified Power States, the IR3541 features Efficiency Shaping Technology that enables VR designers to cost-effectively maximize system efficiency. Efficiency Shaping Technology consists of two techniques – Variable Gate Drive and Dynamic Phase Control. These can be used individually or in combination to achieve the best VR efficiency at a given cost point.

VARIABLE GATE DRIVE (VGD)

The IR3541 monitors the load current of loop 1 and creates a feed-forward corrected PWM pulse on the VAR_GATE pin that can be used to create a gate drive voltage that varies optimally with load current. This approach can significantly improve VR efficiency. The VAR_GATE output together with a IR3537 driver (see Figure 4) can be used to generate the gate drive voltage for the MOSFET drivers using information from Loop 1 load current only.

The user can adjust the gate drive voltage slope (V/A) and the minimum gate drive voltage. The IR3541 intelligently resets the gate drive voltage each time a phase is added or dropped for maximum efficiency (Figure 35).

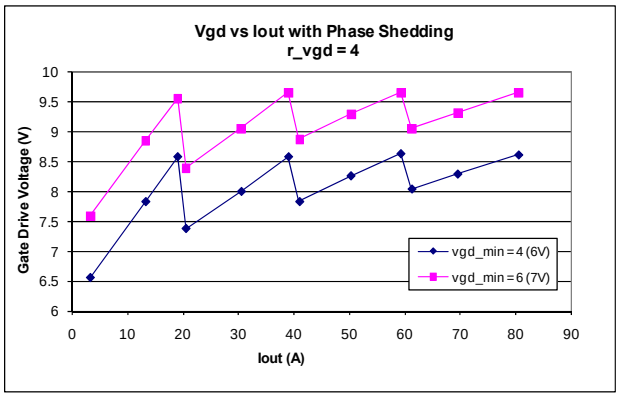


Figure 35: Variable Gate Drive configurability

An external circuit consisting of an IR driver, inductor, and filter capacitor (see Figure 4) can be used to generate an external variable gate drive voltage using the VAR_GATE pin. When using an IR3537 driver, the VAR_GATE signal should be configured as inverted for the most cost effective solution. Table 19 outlines the VGD parameters.

TABLE 19: VGD CONFIGURATION

Function
VGD Polarity
Minimum Drive (*Vmin*) (*Vgd_min=4V + Vgd_min/2*)
VGD Load line (*Rvgd*) (1/32, 2/32 .. 8/32mΩ)
NOTE: VGD tri-state Driver type is set by the main PWM output driver type

The Gate Drive voltage is calculated as:

$$V_{GD} = V_{GD\_Min} + I_{Phase\,1} \times R_{VGD}$$

POWER-SAVING STATES

The IR3541 uses Power States to set the operating mode. These are summarized in Table 20.

TABLE 20: POWER STATES

Power State	Mode	Recommended Current
PS0	Full Power	Maximum
PS1	Light Load 1-2Φ	<20A
PS2	1Φ Active Discontinuous	<5A
PS3	1Φ Passive Discontinuous	<1A

The Power States may be commanded through the I2C/PMBus, SVID interface or the IR3541 can autonomously step through the Power States based upon the regulator conditions summarized in Table 21.

TABLE 21: POWER STATE ENTRY/EXIT

	Command Mode	Auto Mode
PS1 Entry	a) Command	n/a if Phase Shed enabled
PS1 Exit	a) Command to PS0 b) DVID to PS0 c) Current limit to PS0	n/a if Phase Shed enabled
PS2 Entry	a) Command	a) reverse current in 1Φ
PS2 Exit	a) Command to PS0 b) DVID to PS0 c) Current limit to PS0	a) $F_{sw} > F_{sw\_desired}$ to PS0 b) DVID to PS0 c) Current limit to PS0
PS3 Entry	a) Command	n/a
PS3 Exit	a) Command to PS0 b) DVID to PS0 Current limit to PS0	n/a

DYNAMIC PHASE CONTROL (DPC) IN PS0, PS1

IR3541 optionally supports the ability to autonomously adjust the number of phases with load current, thus optimizing efficiency over a wide range of loads. This function can be enabled or disabled through a NVM setting (Table 22).

TABLE 22: DPC THRESHOLD

Function
DPC Enable/per phase Threshold (0 to 62A) in 2A steps

As shown in Figure 36 (loop 1, 4-phase example shown), the designer can configure the VR to dynamically add or shed phases as the load current varies. Both control loops of the IR3541 have the DPC feature.

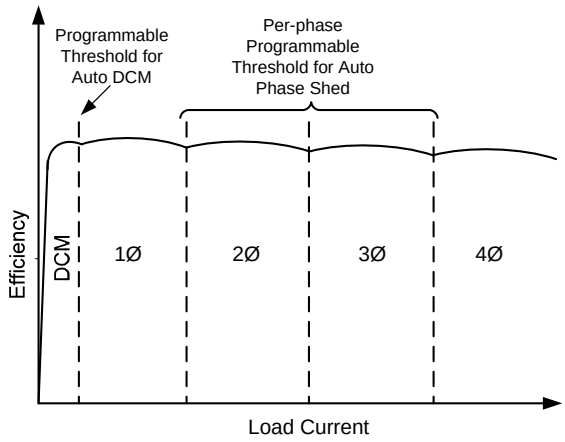


Figure 36: Dynamic Phase Control Regions

The IR3541 Dynamic Phase Control reduces the number of phases (Figure 37) based upon monitoring both filtered total current and error voltage over the DPC filter window. Monitoring the error voltage ensures that the VR will not drop phases during large load oscillations.

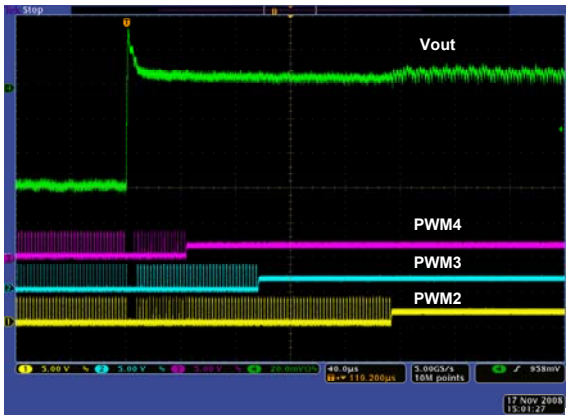


Figure 37: Phase Shed 4Φ→1Φ

During a large load step and based upon the error voltage, the controller instantly goes to the maximum programmed number of phases and will remain there for the DPC filter delay after which phases will be dropped depending on the load current. Dynamic Phase Control (DPC) algorithms are designed to meet Intel and AMD specifications even if the

VR experiences a large load transient when operating with a lower number of phases. The ATA circuitry ensures that the idle phases are activated with optimum timing during a load step (Figure 38).

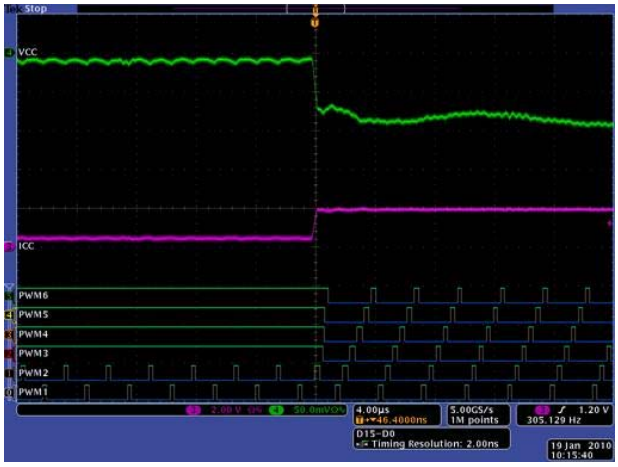


Figure 38: Phase Add 1Φ→6Φ (20A→126A)

Current limit and current balancing circuits remain active during ATA events to prevent inductor saturation and maintain even distribution of current across the active phases.

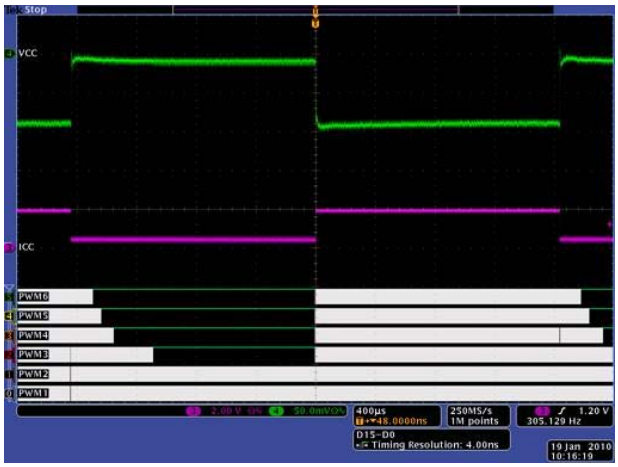


Figure 39: Wide view of Phase Shed/Add

Loop coefficients are automatically scaled to the number of active phases to ensure stability at all load currents (Figure 31). This truly simplifies compensation.

The add/drop points for each phase can be set in 2A increments from 0 to 62A per phase with a fixed 4A hysteresis. This results in a uniform per-phase current density as the load increases or decreases.

$$\text{Add Phase}: \quad \text{if } I_{OUT} > \#\text{ActivePhases} \times \text{DPC}_{threshold}$$

$$\text{Drop Phase}: \quad \text{if } I_{OUT} < \#\text{ActivePhases} \times \text{DPC}_{threshold} - 4\text{A}$$

As shown in Figure 40, DPC enabled VRs provide light and medium load efficiency improvements and together with VGD, true load-adaptive power savings can be realized (Figure 41).

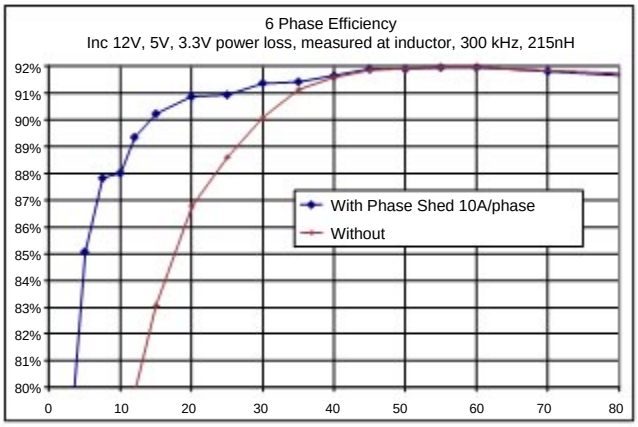


Figure 40: Typical 1.2V Efficiency with DPC

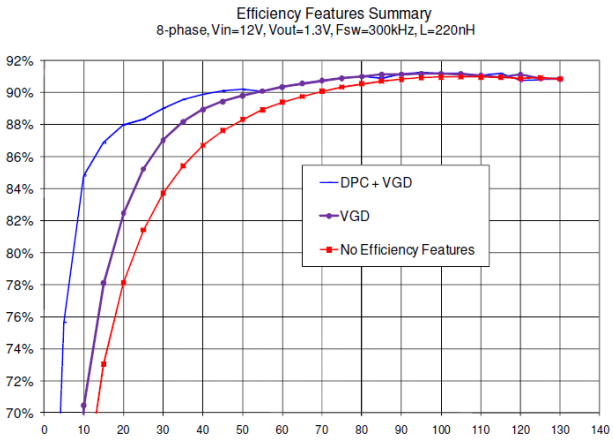


Figure 41: Efficiency with DPC & VGD

DISCONTINUOUS MODE OPERATION PS2, PS3

Under very light loads, efficiency can become dominated by MOSFET switching losses. In PS2/PS3 mode, the IR3541 operates as a constant on-time controller where the user sets the desired peak-to-peak ripple by programming an error threshold and an on-time duration (Table 23). Note that PS2 and PS3 modes are equivalent.

TABLE 23: PS2/PS3 MODE CONSTANT ON-TIME CONTROL

NVM Register	Function
de_thresh	Sets the error voltage at which an on-time pulse is started in 2mV steps
Pulse_width_de	Sets the duration of the on-time pulse in 40ns steps. Note that this also sets the off-time in 160ns steps

In PS2 mode (Active Discontinuous Mode), internal circuitry determines when the inductor current declines to zero on a cycle-by-cycle basis and shuts off the low-side MOSFET at the appropriate time in each cycle. This reduces conduction losses and also lowers the switching frequency resulting in improved efficiency because the inductor and low-side MOSFET are not sinking power from the output capacitors at light loads.

FAULTS & PROTECTION

The comprehensive fault coverage of the IR3541 protects the VR against a variety of fault conditions. Faults are user configurable through the IR IPD which also displays the fault status. There are two types of fault monitoring registers. In addition to real-time fault registers, there are "sticky" fault registers that can only be cleared with a PMBus command or 3.3V power cycle. These will indicate if any fault has occurred since the last power cycle, even if the fault has cleared itself and the VR has resumed normal operation. Table 24 lists the available faults.

TABLE 24: STICKY & NON-STICKY FAULTS

Register Type	Faults
Sticky	OTP, OCP, OVP, UVP, 12V UVLO, 3.3V UVLO, VID shutdown, Bad Parity
Non-Sticky	

The controller has two programmable modes for determining how the controller responds to faults on the two loops. In combined mode, an over-current or under-voltage fault on either loop will trigger the programmed response on both loops. In individual mode, a loop will respond only to its own over-current or under-voltage fault independent from the other loop. Input under-voltage on 3.3V or 12V supplies, over-voltage on either loop or an over-temperature fault will always shut down both loops. The fault capability is summarized in Table 25.

TABLE 25: STATUS & FAULT REGISTERS

Function
Combined/Individual OCP & UVP Fault mode
Sticky Fail codes
Non-sticky Fail codes
Status Word
Communications/Memory/Logic Fault

Output Over-voltage Protection (OVP)

If the output voltage exceeds a fixed threshold above the VID set-point, the IR3541 detects an output over-voltage fault and latches on the low-side MOSFETs to limit the output voltage rise based on the settings in Table 26.

TABLE 26: OVP ACTION

OVP Action
Low-side MOSFET latched on
Low-side MOSFET on until Output<0.3V

Under OVP conditions, the low-side MOSFETs can be configured to remain latched indefinitely or remain latched on until the output voltage falls below the threshold at which time the low-side MOSFETs are released. This release mode can reduce or prevent undershoot of the output voltage. In the release mode, if the output voltage rises above the OVP level the low side MOSFET's will again be turned on until Vout drops below the release threshold level. Note that OVP is disabled during DVID down to prevent false triggering. During soft-start, OVP is triggered at the fixed soft-start level.

Over-current protection (OCP)

The IR3541 provides a user defined output over-current protection limit up to a maximum value of 62A per phase per loop. For example, with 4 phases, the OCP maximum would be 62A*4 phases = 248A.

The controller action in OCP is configurable as shown in Table 27.

TABLE 27: OCP & UVP MODE SELECTION

OCP/UVP Behavior Mode
Per phase OCP Threshold (0 to 62A)
Shutdown immediately (cycle power or enable to restart)
Hiccup 7X before Shutdown
Hiccup indefinitely

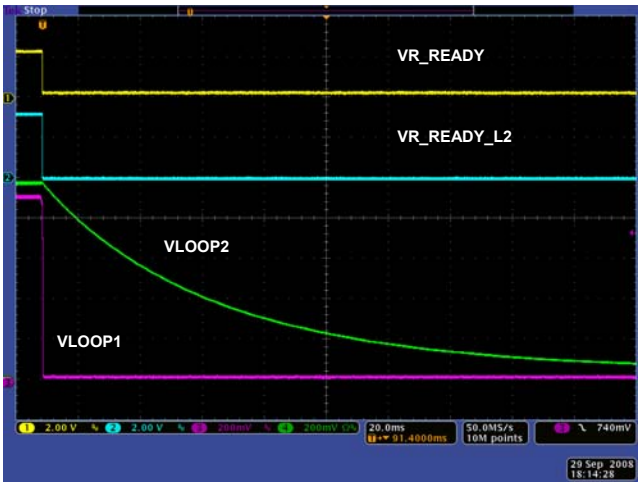


Figure 42: Loop 1 OCP configured to shut down both loops

Output Under-voltage Protection (UVP)

The IR3541 detects an output under-voltage condition if the sensed voltage at the CPU is below the UVP threshold as defined by the VID setting and loadline. Upon detecting an output under-voltage condition, the IR3541 responds in the same manner as the OCP, according to the setting selected in Table 27.

VR_HOT and Over Temperature Protection (OTP)

The IR3541 provides a temperature measurement capability at the TSEN pin that is used for over temperature protection, VR_HOT flag and temperature monitoring on Loop 1. The temperature is measured with an NTC network that can be positioned close to thermal hot spot. The thresholds are programmable in 1°C increments as shown in Table 28. If the measured temperature exceeds the OTP threshold, the IR3541 will latch off the VR (cycle system power to restart).

TABLE 28: VR_HOT & OTP

Function
VR_HOT polarity
VR_HOT threshold (64°C to 127°C)
OTP threshold (VR_HOT + 0°C to 32°C) max 135°C

The IR3541 includes a pre-programmed look-up table that is optimized for the recommended NTC options shown in Table 29. The NTC network is connected to the TSEN pin as shown in Figure 43. A 0.01uF capacitor is recommended to filter noise.

TABLE 29: NTC TEMPERATURE SENSE RANGE

NTC	Value	$R_{parallel}$
Murata NCP15WB473F03RC or Panasonic ERT-J0EP473J	47KΩ	13KΩ

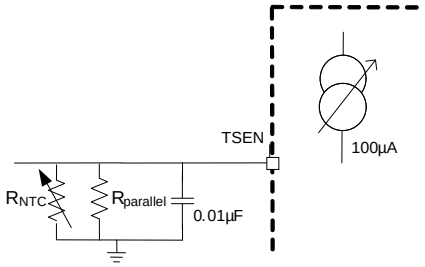


Figure 43: Temperature Sense NTC Network

I_CRITICAL/VRHOT FLAG (AMD MODE ONLY)

The IR3541 VRHOT pin in AMD mode can be optionally reprogrammed to assert when a user programmed critical current level is exceeded. Assertion is not a fault and the PWM continues to regulate. I_CRITICAL monitors a long term averaged output current which is a useful indicator of average operating current and thermal operation.
The user can select between 2 I_CRITICAL filter bandwidths (Table 30).

TABLE 30: I_CRITICAL BANDWIDTH OPTIONS

Slow
Very Slow

Refer to electrical table for filter values

For advanced AMD I-spike enabled processors, the I_CRITICAL can be used to provide a slow current limit in conjunction with the OCP level providing a fast current limit to protect against the maximum spike level.

The I_CRITICAL current level can be programmed in NVM and if set, the I_CRITICAL function replaces the VRHOT1 function on the pin (Table 31). I_CRITICAL on VRHOT1 represents both loop1 and loop2.

TABLE 31: I_CRITICAL FUNCTION

I_CRITICAL register	VRHOT_ICRIT# pin Function
0A	VRHOT loop 1
4A-252A in 4A steps	I_CRITICAL loop1 and loop 2

The default hysteresis for I_CRITICAL is 5%, however this can be disabled by the user.

I_CRITICAL can be easily used to disable the controller, if required, by using the circuit in Figure 44.

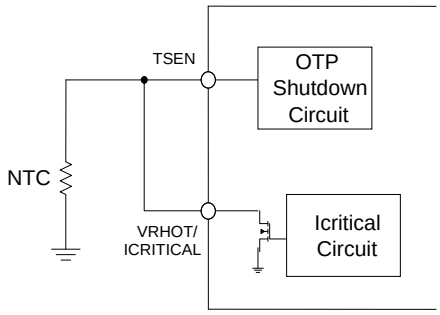


Figure 44: Using I_CRITICAL to shut down the VR

COUPLED INDUCTOR OPERATION

Coupled inductors provide excellent transient response and low ripple. The IR3541 can be enabled to operate with coupled inductors (Table 32) on a loop with an even number of phases.

TABLE 32: COUPLED INDUCTOR MODE

Function
Coupled Inductor Enable/Disable

The IR3541 allows phase shedding/adding in Coupled Inductor mode thereby improving the efficiency over standard Coupled Inductor implementations. Each pair of coupled phases runs at 180° apart (Figure 45).

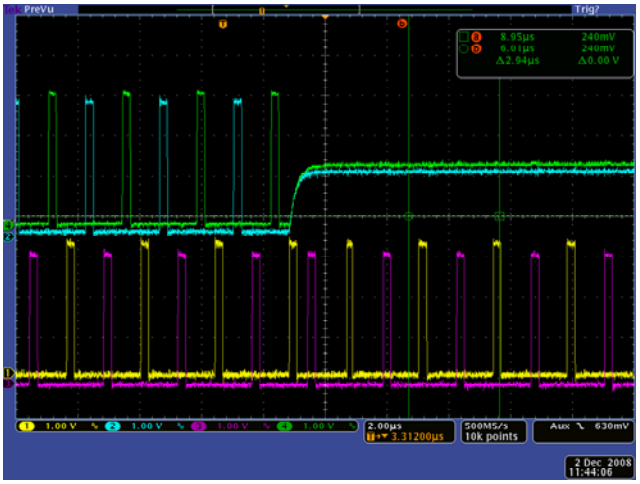


Figure 45: Coupled Inductor Phase Shed 4Φ→2Φ

Phases are added/dropped in pairs and Table 33 shows the required pairings. The Phase Shedding Threshold is set according to Table 22. In addition, at very light loads, Diode Emulation can be enabled in which case the VR runs in single phase with one side of the coupled inductor undriven (Figure 46). Under this condition, the effective inductance is lower.

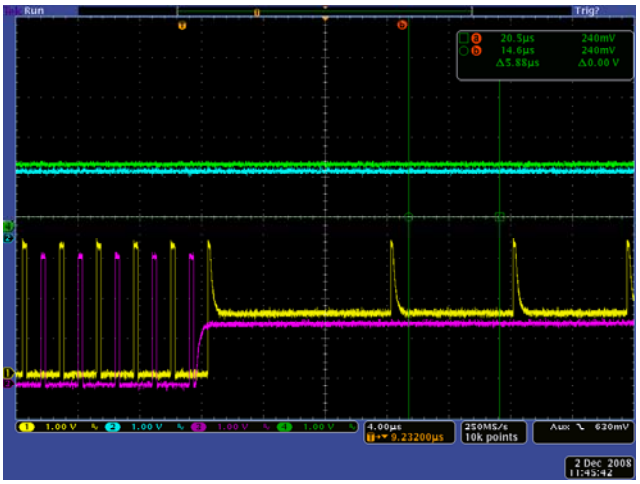


Figure 46: Coupled Inductor Phase Shed 2Φ→1Φ

TABLE 33: COUPLED INDUCTOR PHASE PAIRINGS

Loop Configuration	Phase Pairs	
	Loop #1	**Loop #2**
2+1	1-2	n/a
3+2	n/a	4,5
4+1	1-3, 2-4	n/a

I2C/PMBUS COMMUNICATION

The IR3541 simultaneously supports I2C/SMBus/PMBus through the use of exclusive addressing. The I2C/SMBus/PMBus address for the IR3541 is programmed NVM bits (PM_Addr<3:0> in Table 34) Optionally, the IR3541 can enable an address resistor offset as shown in Table 35 and Table 36 (note that a 0.01uF capacitor is required across the resistor per Figure 47). This means that a motherboard PMBus master may communicate with typically up to 8 dual loops, or if used as single loop controllers, as many as 16 IR3541-based VRs. Note that a single I2C address operates both loops whereas Table 34 sets the PMBus address of Loop 1, while Loop 2 is offset higher by the *Chip_Addr_Offset* register which is volatile and defaults to 1.

$$PMaddress_{Loop\,2} = PMaddress_{Loop\,1} + Chip\_Addr\_Offset$$

Once the address of the IR3541 is set, it is locked to protect it from being overridden.

Additionally, the I2C address can be set to any value by writing the desired address to a volatile register I2C_addr<6:0>. When this address is set to zero, the I2C address is taken from Table 34.

For unprogrammed devices, the PMBus address can be temporarily forced by Setting EN=VR_HOT=low.

TABLE 34: I2C/PMBUS ADDRESSING IN NVM

Register Setting PM_Addr<3:0>	Controller I2C 7bit Address	Loop 1 PMBus 7bit Address
1111	37 hex	**77 hex**
1110	36 hex	**76 hex**
1101	35 hex	**75 hex**
1100	34 hex	**74 hex**
1011	33 hex	**73 hex**
1010	32 hex	**72 hex**
1001	31 hex	**71 hex**
1000	30 hex	**70 hex**
0111	2F hex	**47 hex**
0110	2E hex	**46 hex**
0101	2D hex	**45 hex**
0100	2C hex	**44 hex**
0011	2B hex	**43 hex**
0010	2A hex	**42 hex**
0001	29 hex	**41 hex**
0000	28 hex	**40 hex**
I2C_Addr<6:0> is non-zero	I2C_addr<6:0>	**n/a**
EN=VrHOT=low	0A hex	**0D hex**

TABLE 35: PM_ADDR ENABLE

Enable_Addr_Pin NVM bit	Pin 20 Function
0	VAR_GATE
1	PM_ADDR

TABLE 36: PM_ADDR RESISTOR OFFSET

PM_ADDR Resistor	I2C/SMBus/PMBus Address Offset
0.953kΩ	+0
1.78kΩ	+1
2.49kΩ	+2
3.48kΩ	+3
4.32kΩ	+4
5.23kΩ	+5
6.19kΩ	+6
7.15kΩ	+7
8.25kΩ	+8
9.31kΩ	+9
10.5kΩ	+10
11.8kΩ	+11

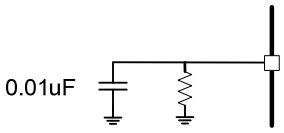


Figure 47: PM_ADDR components

REAL-TIME PMBUS MONITORING FUNCTIONS

IR3541 provides real-time accurate measurement of input voltage, output current and temperature over the PMBus interface. The PMBus data is provided in a linear format with an 11-bit mantissa and 5-bit exponent (Figure 61). Output voltage is calculated based upon the VID setting and loadline and the result is reported through the PMBus dependent upon the user-configurable VOUT_MODE setting.

I2C REPORTING

The same PMBus measurements are accessible by I2C. But since the data is 2 bytes long, each byte must be accessed with separate commands illustrated by the following pseudo-code:

High byte= I2C_ReadByte(Slave Address, Loop 1 Iout high byte register address)
Low byte= I2C_ReadByte(Slave Address, Loop 1 Iout low byte register address)

ACCURACY OPTIMIZATION REGISTERS

The IR3541 provides excellent factory-trimmed chip accuracy. In addition, the designer has calibration capability that can be used to optimize accuracy for a given design. This can be done by determining the average offsets across a sample of boards and using these figures in the generic NVM configuration (design optimization) or by individual board programming at production (calibration). Irrespective of the method chosen, the IR3541 provides a number of NVM registers to fine tune the accuracy of the reported measurements (Table 37). This allows the system designer to minimize board level inaccuracies by design or at In-Circuit Test or similar manufacturing steps (Figures 48,49 and 50).

TABLE 37: ACCURACY OPTIMIZATION REGISTERS

Nvm register	Function
I_{IN} Fixed Offset	Offsets the input current in 1/32A steps e.g. driver Icc which can be 5-8mA per driver
I_{IN} Per Phase Offset	Offsets the input current dependent upon the number of active phases in 1/128A steps e.g. the drive current for the MOSFET's. This current increases every time a new phase is added
I_{OUT} Current Offset	Offsets the output current from -4A to +3.75A in 0.25A steps
Vout Offset	Offsets the output voltage -40mV to +35mV in 5mV steps (Intel mode) or -50mV to + 43.75mV in 6.25mV steps
Temperature Offset (volatile)	Offsets the temperature in 1°C steps e.g. to compensate for offset between the hottest component and the NTC sensing location. **Not stored in NVM, must be written to IC at every start-up**

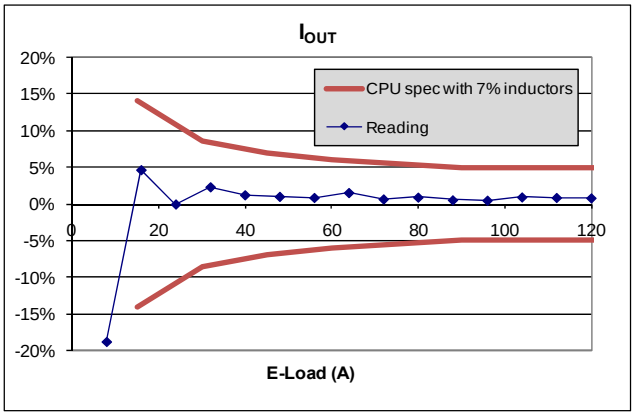


Figure 48: PMBus I_{OUT} Error using 10% DCR inductors, with phase shedding

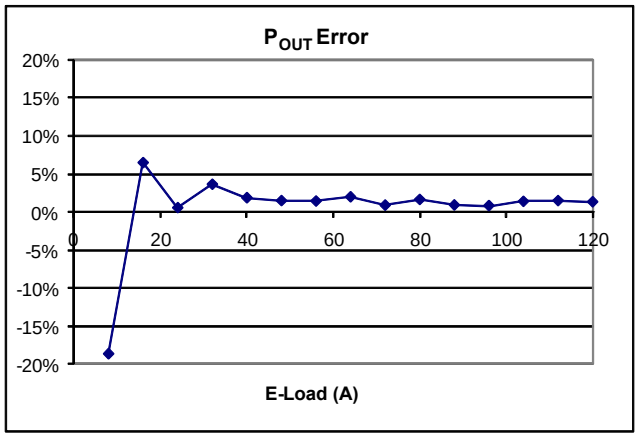


Figure 49: PMBus P_{OUT} Error using 10% DCR inductors

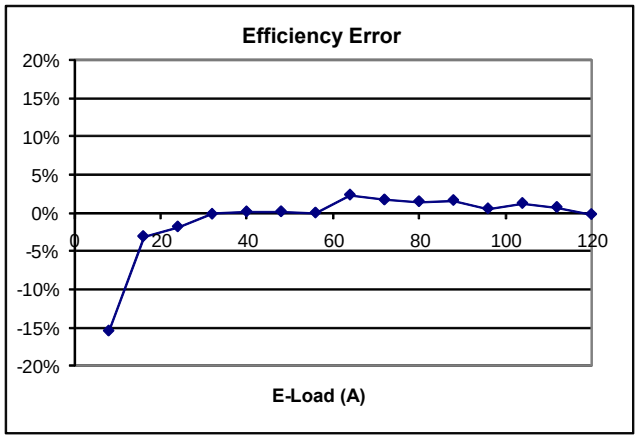


Figure 50: PMBus Efficiency using 10% DCR inductors

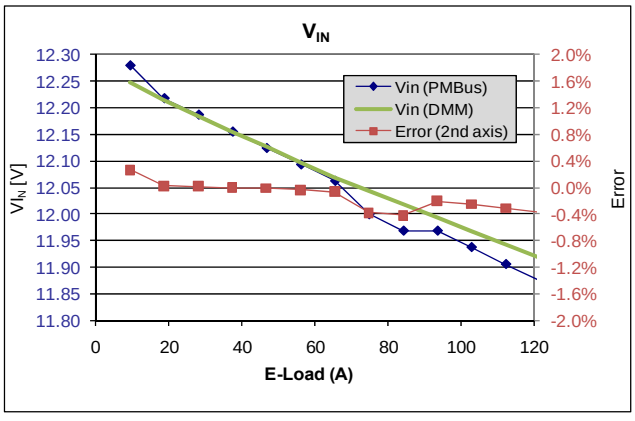


Figure 51: PMBus Input Voltage Measurements

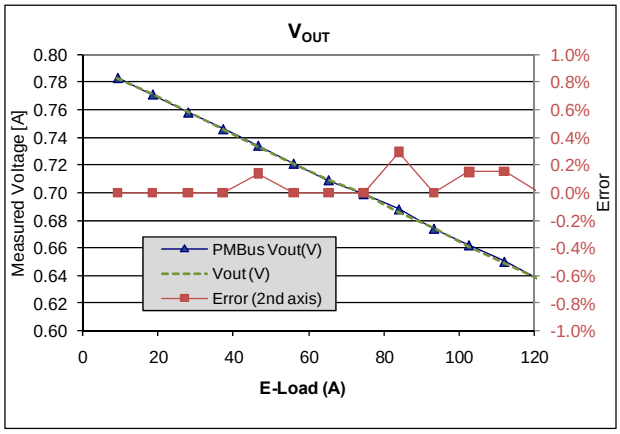


Figure 52: PMBus Output Voltage Measurements

GAMER MODE & MARGINING

IR3541 supports a PMBus gamer command for flexible over-clocking over an extended VID range. System firmware can use this command to enable and disable "Gamer Mode". When Gamer mode is enabled, the CPU output voltage transitions from CPU VID to Gamer VID.

The Gamer VID is represented as a 9-bit word given by the formula:

$$V_{Gamer} = (VID + 1) \times Stepsize \quad for\ VID = 1\ to\ 383$$
$$V_{Gamer}MAX = 1.9V \quad for\ Intel / MPol\ \&\ 2.3V \quad for\ AMD$$
$$where\ Stepsize = 5mV\ (Intel / MPoL)\ or\ 6.25mV\ (AMD)$$

The designer may also configure a maximum Vout (Table 39) to protect the VR from exceeding the programmed voltage regardless of the commanded VID and offset.

The Gamer command may be used to set the controller to either override or track CPU DVID commands. In Override mode, the IR3541 sets the output voltage defined by the Gamer VID and ignores the VIDs from the CPU. In Track mode, the output voltage is initially set to the Gamer VID and any subsequent changes to the CPU VID cause the same offset changes in the Gamer VID.

The IR3541 Gamer command also provides overclockers the ability to minimize droop by digitally scaling the loadline to 75%, 50% or 25% of the nominal value.

In Gamer mode, the Intel SVID output current information to the CPU is rescaled by 50% to prevent the CPU from throttling. For protection purposes, the VRHOT# circuit functions as normal to thermal throttle the CPU if the VR overheats.

A summary of the PMBus Gamer command is shown in Table 38.

TABLE 38: GAMER COMMAND FORMAT

Bits	Function
15-13	Reserved. Always set to "001"b
12	Gamer Mode Enable/Disable
11	VID Follow or VID Override Mode
10:9	Loadline scale 100%, 50%, 75%, 25%
8:0	Gamer VID[8:0]

TABLE 39: VMAX

Register Value	Vmax (Intel/MPoL mode)	Vmax (AMD mode)
0	0.64V	0.80V
1	0.73V	0.91V
2	0.81V	1.02V
3	0.90V	1.13V
4	0.99V	1.24V
5	1.08V	1.35V
6	1.17V	1.46V
7	1.25V	1.57V
8	1.34V	1.68V
9	1.43V	1.79V
10	1.52V	1.90V
11	1.61V	2.01V
12	1.69V	2.12V
13	1.78V	2.23V
14	1.87V	2.38V
15	1.96V	2.45V

Intel SVID Gamer Behavior

The Intel CPU relies upon voltage and current reporting to determine the optimum power-state and operating point. Therefore, Gamer mode must continue to provide information on the SVID interface, essentially to prevent the Intel CPU from acting upon the actual Gamer mode voltage and current. To facilitate this, the IR3541 performs the following actions:

- SVID current is reported as 50% of the actual current
- SVID voltage is reported as last SVID commanded voltage + 7%

Margining

The Gamer command can also be used to easily margin the output voltage up and down for testing system level dependencies.

Gamer Mode Recovery

Raising the CPU voltage to achieve higher performance or lowering the CPU to save power can result in a system crash. The IR3541 contains a safety mechanism whereby the Gamer mode is immediately disabled any time that the ENABLE pin is driven low (typically by a system restart). This ensures that the CPU starts at the proper boot VID.

I2C VOLTAGE & POWER-STATE OVERRIDE

The IR3541 provides an I2C alternative method to using SMBus/PMBus commands to override the output voltage and power-state settings (Table 40). This is useful when the system designer does not have access to SMBus Process Call protocol which is required for IR's Gamer Command. Note that only the standard 8 bit VID is available. The I2C method requires direct reading/writing of IR registers, please refer to the IR3541 Register Map User Note for detailed information.

TABLE 40: I2C VOLTAGE & POWER-STATE REGISTERS

Function	Register Address/bit
Loop 1 VID override enable	D0[6]
Loop 1 Power-state override enable	D0[5]
Loop 1 override Power-state setting	D0[1:0]
Loop 1 override VID setting	D1[7:0]
Loop 1 Loadline Scale	D5[1:0]
Loop 2 VID override enable	D2[6]
Loop 2 Power-state override enable	D2[5]
Loop 2 override Power-state setting	D2[1:0]
Loop 2 override VID setting	D3[7:0]
Loop 2 Loadline Scale	D5[5:4]

I2C PROTOCOLS

All registers may be accessed using either I2C or PMBus protocols. I2C allows the use of a simple format whereas PMBus provides error checking capability. Figure 53 shows the I2C format employed by the IR3541.

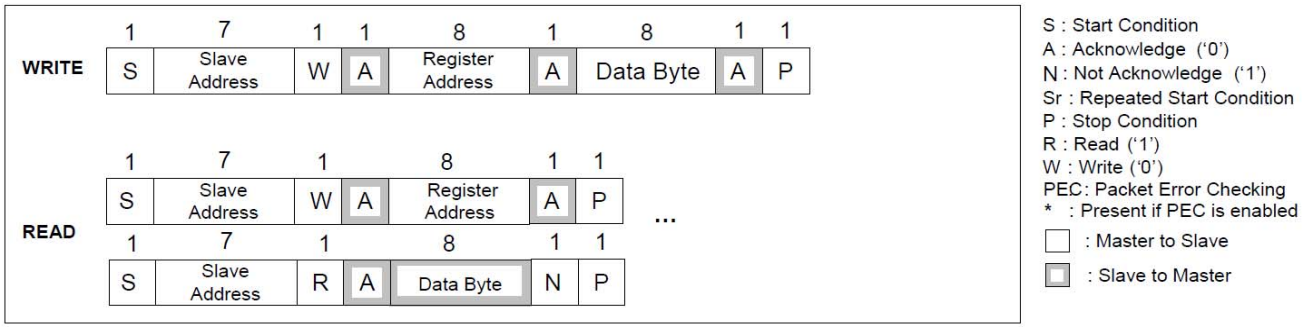


Figure 53: I2C Format

SMBUS/PMBUS PROTOCOLS

To access IR configuration and monitoring registers, 4 different protocols are required:

- the SMBus Read/Write Byte/Word protocol with/without PEC (for status and monitoring)
- the SMBus Send Byte protocol with/without PEC (for CLEAR_FAULTS only)
- the SMBus Block Read protocol for accessing Model and Revision information
- the SMBus Process call (for accessing IR3541 configuration registers)

An explanation of which command codes and protocols are required to access them is given in Table 41.

In addition, the IR3541 supports

- Alert Response Address (ARA)
- Bus timeout (10ms)
- Group Command for writing to many VRs within one command

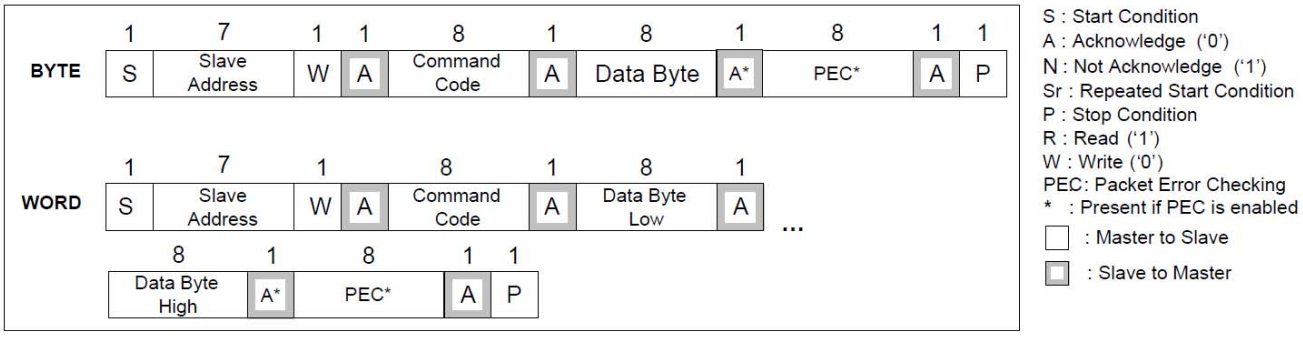


Figure 54: SMBus Write Byte/Word

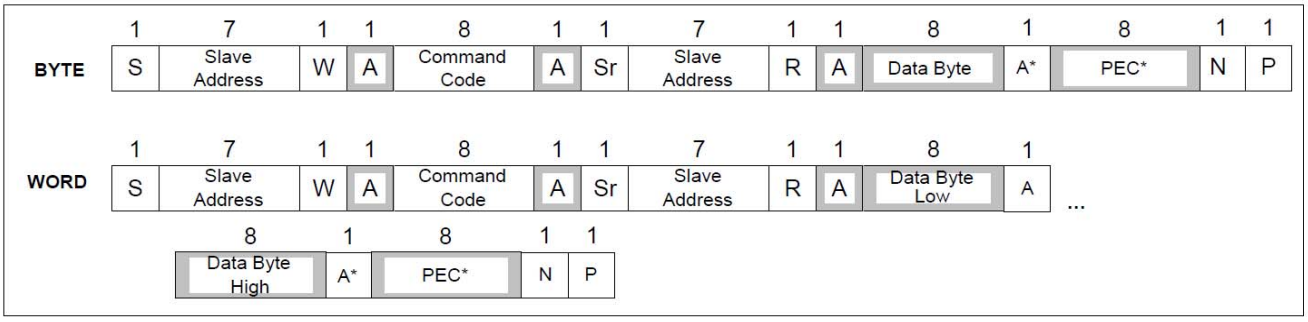


Figure 55: SMBus Read Byte/Word

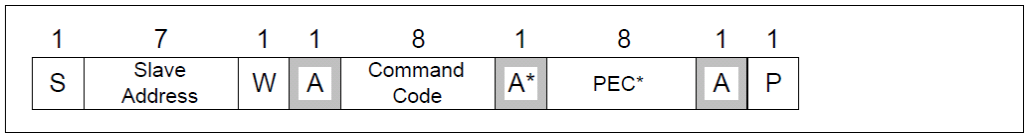


Figure 56: SMBus Send Byte

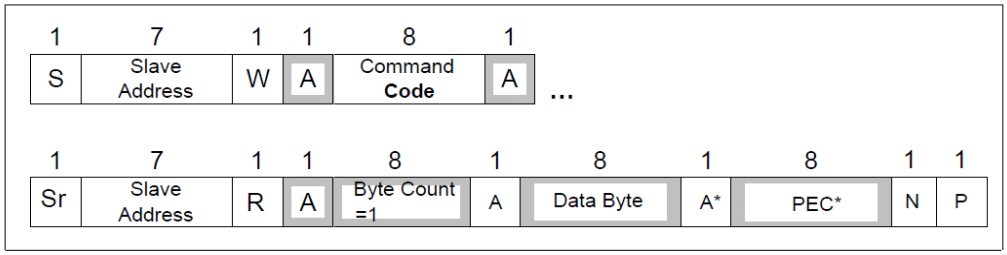


Figure 57: SMBus Block Read with Byte Count=1

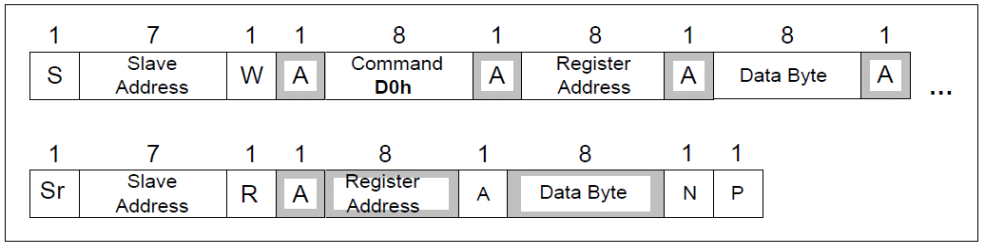


Figure 58: SMBus Process Call to Write an IR register

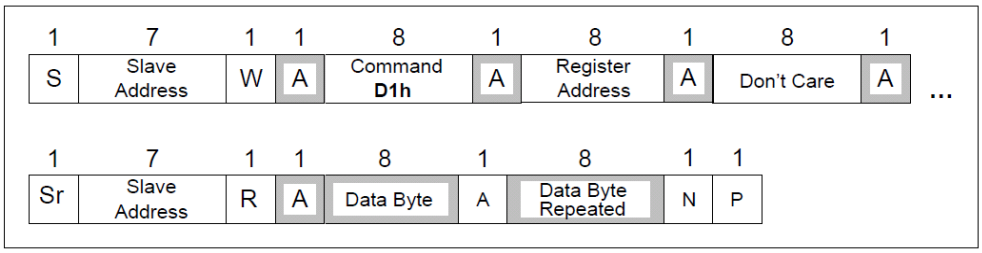


Figure 59: SMBus Process Call to Read an IR register

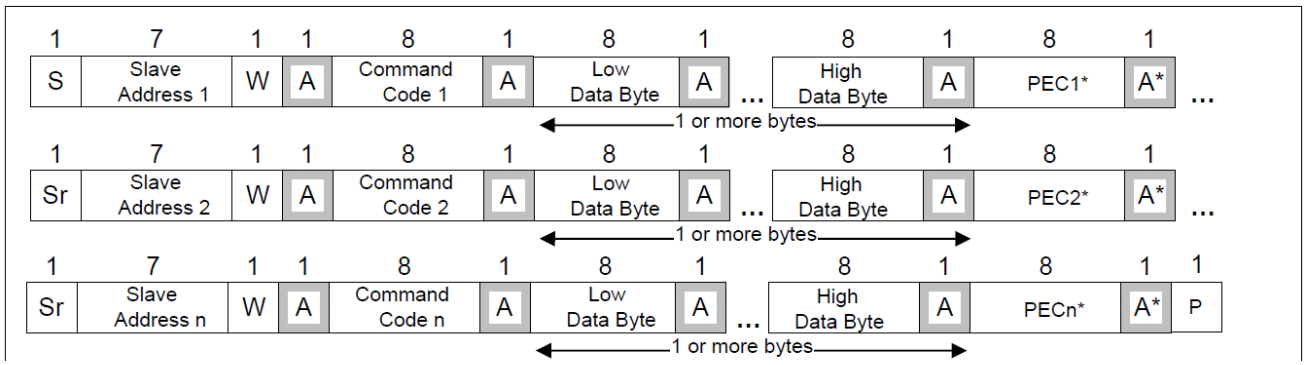


Figure 60: Group Command

TABLE 41: PMBUS COMMANDS

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
OPERATION	Read/Write Byte	01h	Enables or disables IR3541 and controls margining
ON_OFF_CONFIG	Read/Write Byte	02h	Configures the response to the EN pin and OPERATION command
CLEAR FAULTS	Send Byte	03h	Clear contents of Fault registers
CAPABILITY	Read Byte	19h	Returns 1010xxxx to indicate Packet Error Checking is supported and Maximum bus speed is 400kHz
VOUT_MODE	Read/Write Byte	20h	Sets the VOUT format to Linear, Direct or VID for the READ_VOUT, VOUT_MARGIN_LOW, VOUT_MARGIN_HIGH commands The default is LINEAR mode with exponent -11. **LINEAR Mode**: exponent of 1 to -16 is supported **DIRECT Mode**: coefficients are b=0, m=2048, R=0 **VID Mode**: only '1Fh' manufacturer specific VID table is supported, others will be rejected
VOUT_MARGIN_HIGH	Read/Write Word	25h	Sets the high voltage when commanded by OPERATION
VOUT_MARGIN_LOW	Read/Write Word	26h	Sets the low voltage when commanded by OPERATION
STATUS_BYTE	Read Byte	78h	Returns 1 byte where the bit meanings are Bit <7> device busy fault Bit <6> output off (due to fault or enable) Bit <5> Output over-voltage fault Bit <4> Output over-current fault Bit <3> Input Under-voltage fault Bit <2> Temperature fault Bit <1> Communication/Memory/Logic fault Bit <0>: Reserved
STATUS_WORD	Read Word	79h	Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings Bit <7> Output high or low fault Bit <6> Output over-current fault Bit <5> Input under-voltage fault Bit <4> Reserved Bit <3> Loop is not ready Bit <2:0> Reserved
STATUS_TEMPERATURE	Read Byte	7Dh	Returns Over Temperature warning (VRHOT level) and Over Temperature fault (OTP level). Does not report under temperature warning/fault.
STATUS_CML	Read Byte	7Eh	Returns 1 byte where the bit meanings are Bit <7> Command not Supported Bit <6> Reserved Bit <5> PEC fault Bit <4:0> Reserved
READ_VIN	Read Word	88h	Returns the input voltage in Volts[1]
READ_IIN	Read Word	89h	Returns the input current in Amperes[1]
READ_VOUT	Read Word	8Bh	Returns the output voltage in the format set by VOUT_MODE
READ_IOUT	Read Word	8Ch	Returns the output current in Amperes [1]

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION
READ_TEMPERATURE_1	Read Word	8Dh	Returns the addressed loop NTC temperature in degrees Celsius [1]
READ_TEMPERATURE_2	Read Word	8Eh	Returns the **other loop** NTC temperature in degrees Celsius [1]
READ_POUT	Read Word	96h	Returns the output power in Watts[1]
READ_PIN	Read Word	97h	Returns the input power in Watts[1]
PMBUS_REVISION	Read Byte	98h	Reports PMBus Part I rev 1.1 & PMBUs Part II rev 1.2(draft)
MFR_MODEL	Block Read, byte count=1	9Ah	Returns a 1 byte code representing the model: 1 = IR3541
MFR_REVISION	Block Read, byte count=1	9Bh	Returns 1 unsigned byte whose value is the revision number. Eg '0000 0011b' is revision 3.
WRITE_REGISTER_PROCESS_CALL	Process Call	D0h	Write to configuration registers
READ_REGISTER_PROCESS_CALL	Process Call	D1h	Read from configuration & status registers
GAMER COMMAND	Write Word	D2h	Enables/disables Gamer Mode and associated options
SET_REGISTER_ADDRESS	Write Byte	D3h	Sets the register address for reading/writing
READ_REGISTER_BYTE	Read Byte	D4h	Reads 1 byte from the previously set register address
WRITE_REGISTER_BYTE	Write Word	D5h	Writes 1 byte to the previously set register address
READ_EFFICIENCY	Read Word	D7h	Reports the efficiency in % [1]

[1]Note on PMBus: Linear Data Format is used

LINEAR DATA FORMAT

Monitored parameters use the Linear Data Format (Figure 61) encoding into 1 Word (2 bytes), where

$$Value = Y \times 2^{N}$$

Note N and Y are "signed" values. If, VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16 bit unsigned number.

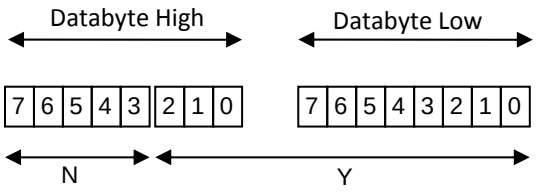


Figure 61: Linear Data Format

MARKING INFORMATION

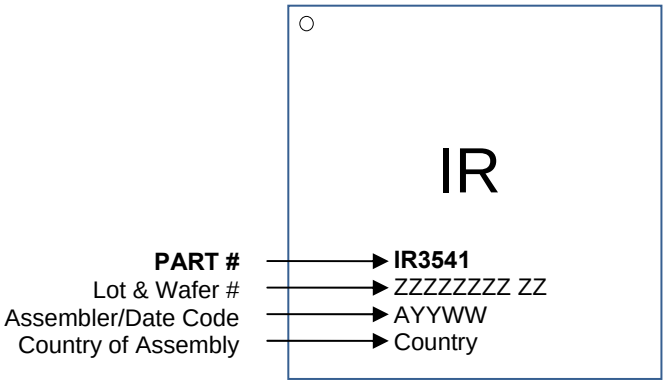


Figure 62: Marking Information

PACKAGE INFORMATION

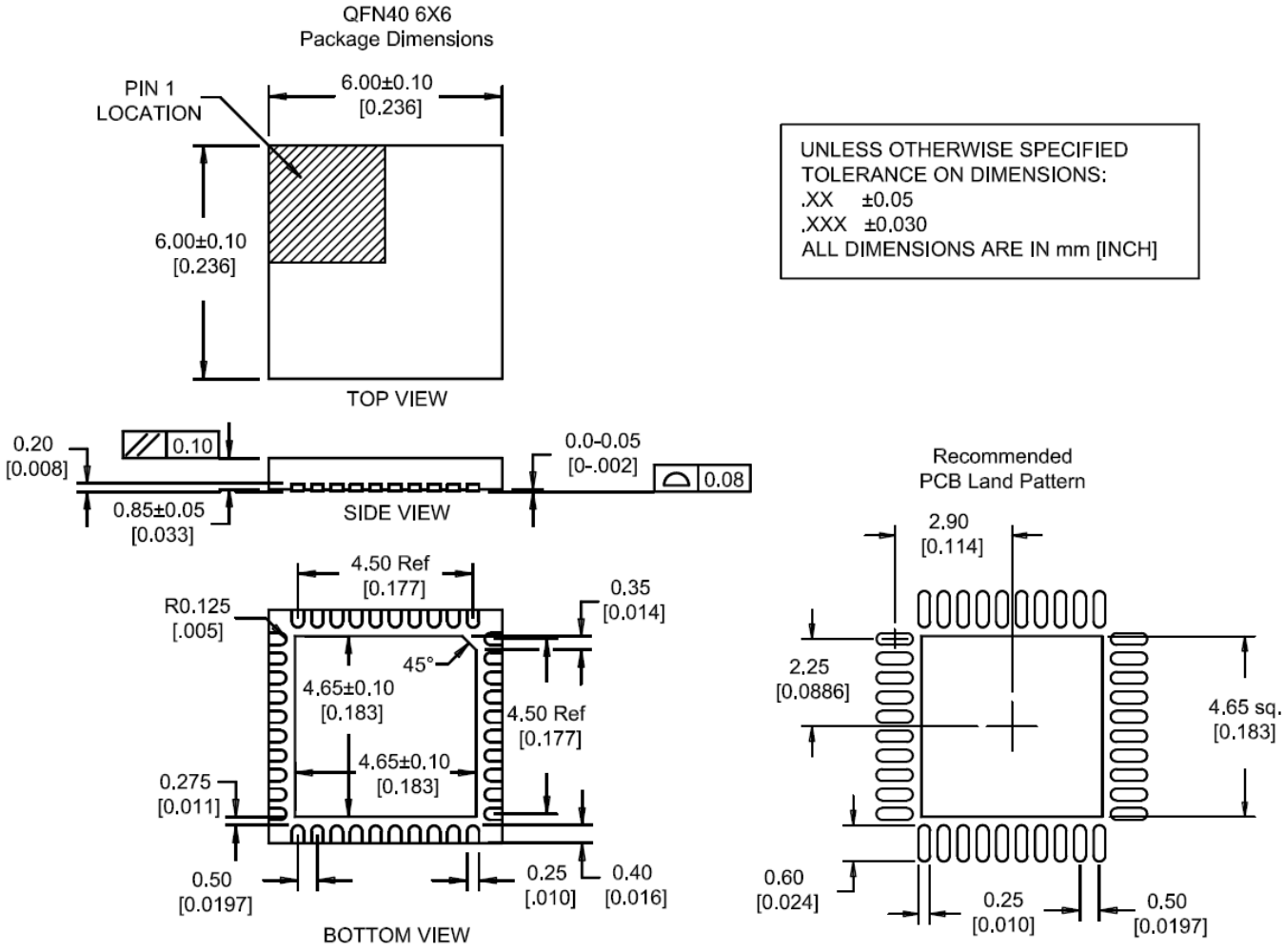


Figure 63: QFN 6x6mm, 40 pin (IR3541)

Data and specifications subject to change without notice.
This product will be designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
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