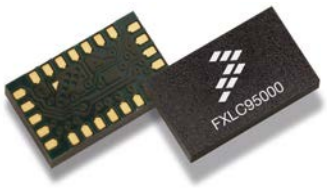
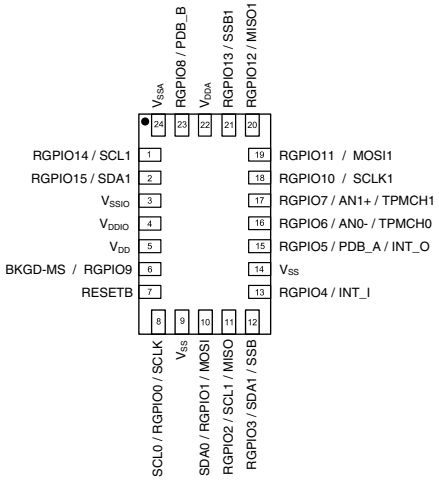
Xtrinsic FXLC95000CL Intelligent, Motion-Sensing Platform

FXLC95000CL



24-LEAD LGA
3 mm by 5 mm by 1 mm
Case 2208-01

Top View



Pin Connections

The FXLC95000CL Intelligent, Motion-Sensing Platform is a breakthrough device with the integration of a 3-axis MEMS accelerometer and a 32-bit ColdFire MCU that enables autonomous, high-precision sensing solutions with local computing and sensors management capability in an open, easy to use, architecture.

The FXLC95000CL hardware is user-programmable to create an intelligent high-precision, flexible, motion-sensing platform. The user's firmware, together with the hardware device, can make system-level decisions required for sophisticated applications, such as gesture recognition, pedometer, and e-compass tilt compensation and calibration.

The FXLC95000 platform can act as an intelligent sensing hub and a highly configurable decision engine. Using the Master I^2C or SPI module, the FXLC95000 platform can manage secondary sensors such as pressure sensors, magnetometers, and gyroscopes. The embedded microcontroller allows sensor integration, initialization, calibration, data compensation, and computation functions to be added to the platform, thereby off-loading those functions from the host processor. Total system power consumption is significantly reduced because the application processor stays powered down for longer periods of time.

The FXLC95000CL device is programmed and configured with CodeWarrior Development Studio for Microcontroller (Eclipse IDE). This standard, integrated development environment (IDE) enables customers to quickly implement custom embedded algorithms and features to exactly match their application needs.

Hardware Features

- 3-axis low noise accelerometer
  - ±2 *g*, ±4 *g*, ±8 *g* configurable dynamic ranges available
  - Up to 16-bit resolution
- 32-bit MCU
  - Coldfire V1 CPU with MAC hardware unit
  - 128K Flash, 16K RAM, 16K ROM
  - 10-, 12-, 14-, and 16-bit, trimmed analog-to-digital converter (ADC) data formats available
  - Master and slave, I^2C and SPI serial connectivity modules
  - Sleep and low power modes to enable local power

- Wide operating voltage and temperature range
  - 1.71 to 3.6 V I/O supply voltage
  - –40ºC to +85ºC operating temperature range
- Small package footprint
  - 3 mm x 5 mm x 1 mm 24-pin LGA package

Ordering Information

Part number	Temperature range	Package description	Shipping
FXLC95000CLR1	–40°C to +85°C	LGA-24	Tape and reel

Table of Contents

1 Typical Applications

This low-power intelligent sensor platform is optimized for a variety of applications.

- Mobile phones/PMP/PDA/Digital cameras
- E-Compass applications with tilt compensation
- Smartbooks/e-readers/netbooks/laptops
- Pedometers
- Gaming and toys
- Virtual-reality, 3D position feedback
- Personal navigation devices (PNDs)
- Activity monitoring in medical and fitness applications
- Security
- Fleet monitoring and tracking
- Power tools and small appliances

2 Software Support

The Xtrinsic Intelligent Sensing Framework (ISF) is a software framework built on top of Freescale's MQX real time operating system (RTOS). ISF offers an open programming model with library support for FXLC95000CL devices. The flexibility of this open programming model allows the FXLC95000CL to be delivered ready to accept a customer's choice of firmware images. A number of pre-built firmware images are available for download from the Freescale website, or, using CodeWarrior and ISF, a customer may create their own custom firmware image incorporating sensor processing algorithms of their own design.

Sensor Adapter libraries for a number of additional Freescale sensors are also available for download enabling the FXLC95000CL to become a sensor hub.

3 Related Documentation

The FXLC95000CL device's features and operations are described in a variety of reference manuals, user guides, and application notes.

To find the most-current versions of these documents:

1. Go to the Freescale homepage at freescale.com.
2. In the Keyword search box at the top of the page, enter the device number FXLC95000CL.
3. In the Refine Your Result pane on the left, click on the Documentation link.

4 General Description

4.1 Functional overview

The FXLC95000CL platform consists of a three-axis, MEMS accelerometer and a mixed-signal ASIC with an integrated, 32-bit CPU. The mixed-signal ASIC can be utilized to measure and condition the outputs of the MEMS accelerometer, internal temperature sensor, or a differential analog signal from an external device.

These measured values can be read at different sample rates through a subscription mechanism in the Intelligent Sensing Framework (ISF) and/or utilized internally by firmware for the FXLC95000CL device (Freescale supplied or user-written).

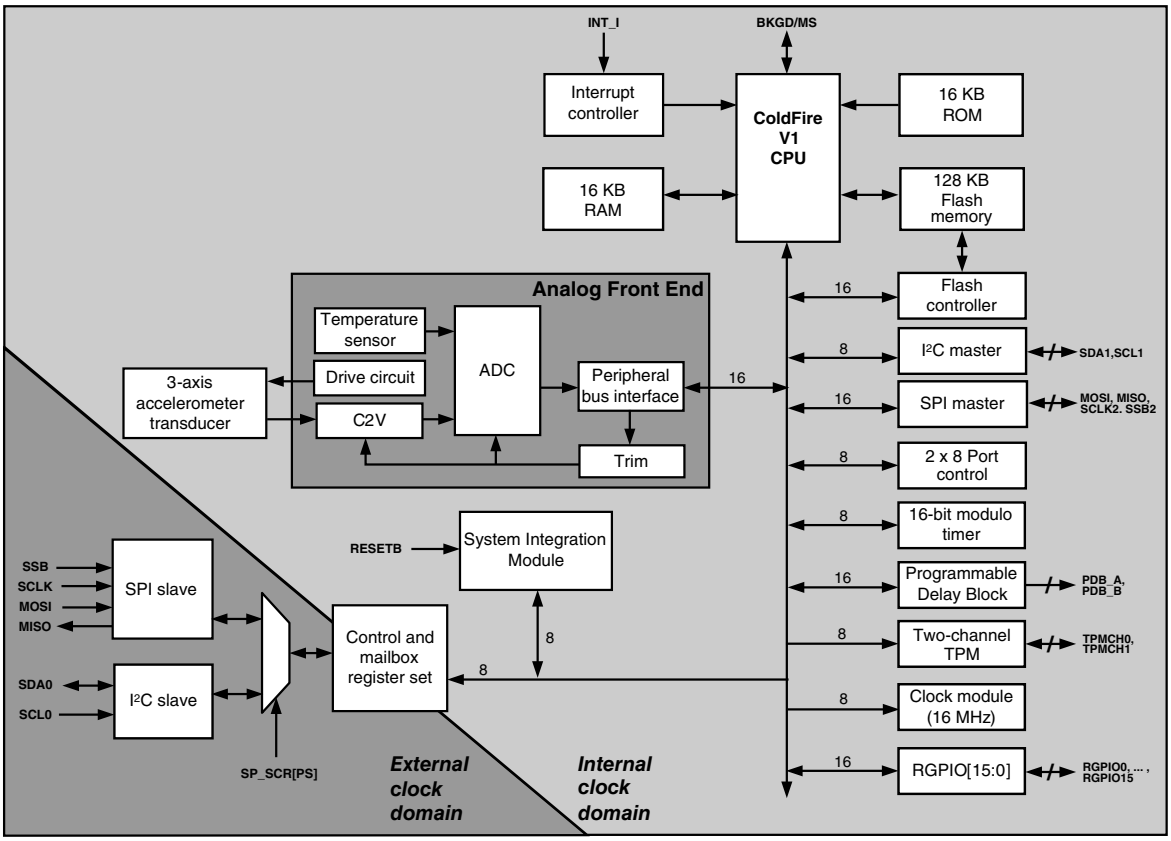


Figure 1. Block diagram of the FXLC95000CL

A block level view of the FXLC95000CL platform is shown in Figure 1 and can be summarized at a high level as an analog/mixed mode subsystem associated with a digital engine.

The analog sub-system is composed of:

- A 3-axis MEMS transducer
- An Analog Front End (AFE) with:
  - A capacitance-to-voltage converter
  - An analog-to-digital converter
  - A temperature sensor

The digital sub-system is composed of:

- A 32-bit, ColdFire V1 CPU with Background Debug Module (BDM)
- Memory: RAM, ROM, and flash
- Rapid General Purpose Input/Output (RGPIO) port control logic
- Timer functions:
  - Modulo Timer Module (MTIM16)
  - Programmable Delay Timer (PDB)
  - General-Purpose Timer/Pulse-Width Modulation Module (TPM)

- I^2C master interface
- Queued SPI master interface (This interface has both send and receive FIFOs of size 16 bit wordlength and 4 words depth each. No DMA.)
- I^2C or SPI slave interface
- System Integration Module (SIM)
- Clock-generation module

The slave interfaces (either SPI or I^2C) operate independently of the ColdFire CPU subsystem. This allows the host processor to access the slave interface at any time, including while the FXLC95000CL's CPU is in low-power, deep-sleep mode. Host access can be set to trigger a FXLC95000CL CPU wakeup.

4.1.1 ROM content and usage

There are several classes of functions stored in ROM:

- A Boot program, including ROM-based slave port command interpreter.
- A collection of utilities which can be invoked via the ROM-based slave port command interpreter.
- ROM functions which are callable from user code using the call_trap() function.

For a detailed description of these items, refer to the FXLC95000CL Hardware Reference Manual ROM chapter.

The FXLC95000CL device boots from a standard routine in ROM. This boot function is responsible for a number of initialization steps (in particular the state of GPIO8 pin is checked in order to select either I^2C or SPI interface as serial communication Slave port), before transferring control if desired to user code in flash memory (when the Boot from Flash bit-field has been set).

The ROM contains a simple command interpreter capable of running a number of ROM-based utility and test functions. These ROM-based functions support flash memory programming and erasing, the protection of flash, the device Reset, and the reading of device information. They also provide useful error codes.

The FXLC95000CL platform is supplied with a fully erased flash memory. Users can take advantage of the ROM-based flash controller and slave port command-line interpreter to communicate with a virgin device and program custom firmware into the flash array.

4.2 Pinout

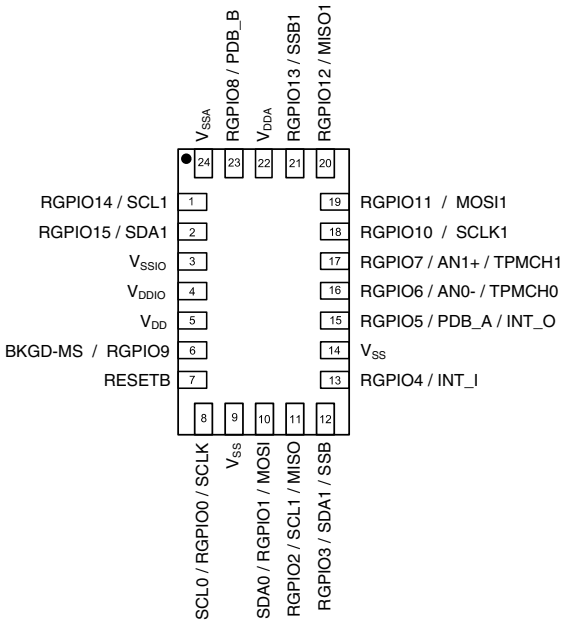


Figure 2. Device pinout (top view)

Table 1. Pin functions

Pin #	Default Pin Function[1]	Pin Function #2	Pin Function #3	Description
1	SCL1[2]	RGPIO14		Master I²C Clock / RGPIO14
2	SDA1[3]	RGPIO15		Master I²C Data / RGPIO15
3	V_{SSIO}			I/O ground
4	V_{DDIO}			I/O power supply
5	V_{DD}			Digital power supply
6	BKGD/MS	RGPIO9		Background debug - Mode select / RGPIO9
7	RESETB[4]			Active low reset with internal, pullup resistor
8	SCL0	RGPIO0	SCLK	Serial clock for slave I²C / RGPIO0 / Serial clock for slave SPI
9	V_{SS}			Digital ground
10	SDA0	RGPIO1	MOSI	Serial data for slave I²C / RGPIO1 / SPI Master Output Slave Input
11	RGPIO2	SCL1	MISO	RGPIO2 / Serial clock for master I²C / SPI Master Input Slave Output
12	RGPIO3	SDA1	SSB	RGPIO3 / Serial data for master I²C / SPI slave select
13	RGPIO4	INT_I		RGPIO4 / Interrupt input
14	V_{SS}			Must be connected to GND externally
15	RGPIO5	PDB_A	INT_O	RGPIO5 / PDB_A / Interrupt output

Table continues on the next page...

Table 1. Pin functions (continued)

Pin #	Default Pin Function[1]	Pin Function #2	Pin Function #3	Description
16	RGPIO6	AN0-	TPMCH0	RGPIO6 / ADC Input 0 / TPM Channel 0
17	RGPIO7	AN1+	TPMCH1	RGPIO7 / ADC Input 1 / TPM Channel 1
18	SCLK1	RGPIO10		master queued SPI clock / RGPIO10
19	MOSI1	RGPIO11		master queued SPI Master Output Slave Input / RGPIO11
20	MISO1	RGPIO12		master queued SPI Master Input Slave Output / RGPIO12
21	SSB1	RGPIO13		master queued SPI slave select / RGPIO13
22	V_{DDA}			Analog power
23[5]	RGPIO8	PDB_B		RGPIO8 / PDB_B
24	V_{SSA}			Analog ground

1. Default Pin Function 1 represents the reset state of the device. Pin functions may be changed via the SIM pin mux-control registers. Drive strength and pullup controls are programmed by the port control registers.
2. SCL1 is available for use on pin (RGPIO14) only when SIM_PMCR1[A2] is not equal to "01". That setting would enable it for pin 11 (RGPIO2).
3. SDA1 is available for use on pin (RGPIO15) only when SIM_PMCR1[A3] is not equal to "01". That setting would enable it for pin 12 (RGPIO3).
4. RESETB defaults to input only, but can be configured as an open-drain, bidirectional pin.
5. GPIO8/PDB_B = LOW at startup indicates that SPI should be used as slave instead of the I^2C module.

4.2.1 Pin function description

Descriptions of the pin functions available on this device are provided in this section.

Sixteen of the device pins are multiplexed with Rapid GPIO (RGPIO) functions. The Default Pin Function column of Table 1 lists which function is active when the device exits the reset state. User firmware can use the Pin Mux Control registers in the System Integration Module (SIM) to change pin assignments for these pins after reset.

V_{DDIO} and V_{SSIO}

I/O power and ground. V_{DDIO} ranges from 1.71V to 3.6V for this device. The device will not load the I^2C bus if V_{DDIO} is not connected. Parasitic paths to supply this power domain from other pins is not recommended.

V_{DD} and V_{SS}

Digital power and ground. V_{DD} is nominally 1.8V for this device. Parasitic paths to supply this power domain from other pins is not recommended.

V_{DDA} and V_{SSA}

Analog power and ground. V_{DDA} is nominally 1.8V for this device. It is recommended that this supply voltage be filtered to remove any digital noise that may be present on the supply.

RESETB

The RESETB pin is an open-drain, bidirectional pin. At power up, it is configured strictly as an input pin. Setting RCSR[DR] (Reset Control & Status Register "Drive Reset" bit) to one will cause the RESET function to become bidirectional. Using this feature, FXLC95000CL can reset external devices whenever it is reset for any purpose other than power-on-reset.

Slave I^2C: SDA0, SCL0

Slave I^2C data and clock signals. FXLC95000CL may be controlled via this serial port or via the slave SPI interface. At reset, SDA0 and SCL0 are open-drain, bidirectional in input mode, with the pullup resistor disabled.

Master I^2C: SDA1, SCL1

Master I^2C data and clock signals. Because the FXLC95000CL contains a 32-bit ColdFire V1 CPU, it is fully capable of mastering other devices in the system via this serial port.

State at reset: active. SCL1 and SDA1 are configured on pins 1 and 2, respectively. The alternate functionality on these pins is RGPIO14 and RGPIO15.

Analog-to-Digital Conversion: AN0, AN1

The on-chip ADC can be used to perform a differential analog-to-digital conversion based upon the voltage present across pins AN0(-) and AN1(+). Conversions for these pins are at the same Sample Data Rate (SDR) as the MEMS transducer signals.

State at reset: Inactive. AN[1:0] are secondary functions on RGPIO[7:6], which own the pins at reset.

Rapid General Purpose I/O: RGPIO[15:0]

The ColdFire V1 CPU has a feature called "Rapid GPIO" or RGPIO. This is a 16-bit input/output port with single-cycle write, set, clear, and toggle functions available to the CPU. The FXLC95000CL brings out all 16 bits of that port as pins of the device.

State at reset:

- RGPIO[15:14]: inactive. SDA1 and SCL1 own the pin at reset.

- RGPIO[13:10, 8:2]: Pin mux registers for these bits are configured as RGPIO. Pullups are disabled. RGPIO functionality can be enabled via RGPIO_ENB[13:10, 8:2].
- RGPIO[9]: Inactive. BKGD/MS owns the pin at reset
- RGPIO[1:0]: inactive. SDA0 and SCL0 own the pin at reset.

Configuration details:

- RGPIO[15:14] are configured as Master I^2C port at reset when RGPIO_ENB[15:14]=00 and PMCR[A3]=PMCR[A2]=00 or 10. They can only be configured as RGPIO when PMCR[A3]=PMCR[A2]=01. RGPIO_ENB[15:14] must also be set to 11 for them to assume RGPIO functionality.
- RGPIO_ENB[13:10] are used to configure RGPIO[13:10].
- Pin function selections are made via the SIM pin mux registers for RGPIO[9:0].

Interrupts: INT_I

This input pin may be used to wake the CPU from a deep-sleep mode. It can be programmed to trigger on either rising or falling edge or high or low level. This pin operates as a level 7 (high priority) interrupt.

Interrupts: INT_O

RGPIO5 (pin 11) can be configured to function as an interrupt output pin. This interrupt can be asserted via software when a command response packet has been stored on the slave port mailboxes and is ready for the host to read. The host will see the interrupt and can read the data from the FXLC95000CL platform. The FXLC95000CL will automatically clear the interrupt once it recognizes that the response packet is being transmitted. This clearing action occurs while the packet is being read and prevents the host from falsely recognizing the same interrupt after the packet read is complete.

State at reset: Pin muxing is set to RGPIO5 mode.

Debug/Mode Control: BKGD/MS

At power-up, this pin operates as Mode Select. If low during power-up, the CPU will boot into debug halt mode. If high, the CPU will boot normally and run code. After power-on reset, this pin operates as a bidirectional, single-wire Background Debug port. CodeWarrior uses the Background Debug port to download code into on-chip RAM and flash, and for debugging that code using breakpoints and single stepping.

State at reset: Mode Select (MS).

MS = 1'b0, at exit from reset → boot to debug halt mode.

MS = 1'b1, at exit from reset → boot to run mode.

State after reset: BKGD. The BKGD pin is a bidirectional, pseudo-open-drain pin used for communications with a debug environment.

Programmable Delay Block: PDB_A, PDB_B

These are the two outputs of the programmable delay block (PDB). Normally, the PDB is used to schedule internal events at some fixed interval(s) relative to start of either the analog or digital phase. By bringing the PDB outputs to these pins, it becomes possible for the FXLC95000CL to initiate some external event, also relative to start of analog or digital phase. For more information, refer to the FXLC95000CL Hardware Reference Manual.

Timer: TPMCH0 and TPMCH1

These pins are the outputs for a general modulo 16 timer and general input/output capture (TPM) and pulse width modulation (PWM) functions.

Slave SPI Interface: SCLK, MOSI, MISO, SSB

Slave SPI clock, master-output slave-input, master-input slave-output, and slave-select signals. The FXLC95000CL may be controlled via this serial port or via the slave I^2C interface.

State at reset: In reset, these pins are configured according to I^2C and RGPIO[3:2] functions listed above. The pin may be reconfigured for SPI use as part of the boot process.

Master SPI Interface: SCLK1, MOSI1, MISO1, SSB1

Master SPI clock, master-output slave-input, master-input slave-output, and slave-select signals.

State at reset: In reset, these pins are configured as RGPIO[13:10] functions listed above.

4.3 System connections

The FXLC95000CL platform offers the choice of connecting to a host processor through either an I^2C or SPI interface. It can also act as a master controller for I^2C or SPI peripherals and analog sensors.

4.3.1 Power supply considerations

- An internal circuit powered by V_{DDA} provides the FXLC95000CL with a power-on-reset signal. For this signal to be properly recognized, it is important that V_{DD} is powered up before or simultaneously with V_{DDA}.
- The voltage potential difference between V_{DD} and V_{DDA} must not exceed ±0.1 V. The simplest way to accomplish this is to power both pins from the same voltage source.
- When using the same voltage source, some digital noise might reach the analog section. To prevent this, connect a small inductor or ferrite bead in serial with both the V_{DDA} and V_{SSA} traces. Additionally, two ceramic capacitors (of approximately 1 µF, and 100 nF, respectively) can be used to efficiently bypass the power and ground of both digital and analog supply rails.
- V_{DDIO} must rise up before or simultaneously with V_{DDA}/V_{DD}.

4.3.2 General connections and layout recommendations

- Provide a low-impedance path from the board power supply to each power pin (VDD, VDDA, and VDDIO) on the device and from the board ground to each ground pin (VSS, VSSA, and VSSIO).
- The minimum bypass requirement is to place 0.01 – 0.1 µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the VDD/VSS pairs, including VDDA/ VSSA. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads, associated printed circuit traces, and vias that connect to the chip VDD and VSS (GND) pins are as short as possible.
- Bypass the power and ground. It is suggested that a high-frequency bypass capacitor be placed close to and on each power pin. Bulk capacitance also is suggested, with it evenly distributed around the power and ground planes of the board.
- Take special care to minimize noise levels on the VDDA and VSSA pins. An isolation circuit consisting of a Ferrite Bead and capacitors is suggested, to ensure that the voltage supplying the analog input is noise free.
- Use separate power planes for VDD and VDDA and separate ground planes for VSS and VSSA. Connect the separate analog and digital power and ground planes as close as possible to power supply outputs. If both analog circuit and digital circuit are powered by the same power supply, it is advisable to connect a small inductor or ferrite bead in serial with both VDDA and VSSA traces.

- It is highly desirable to physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. It is also desirable to place an analog ground trace around an analog signal trace to isolate it from digital traces.
- If in-circuit debug capability is desired, provide an interface to the BKGD/MS pin.
- Select resistors R2 and R3 in Figure 3 to match requirements stated in the I^2C standard. An example value of 4.7kΩ is appropriate for the configuration shown.
- Use the PCB footprint, solder mask, and solder stencil shown in Footprint and pattern information.

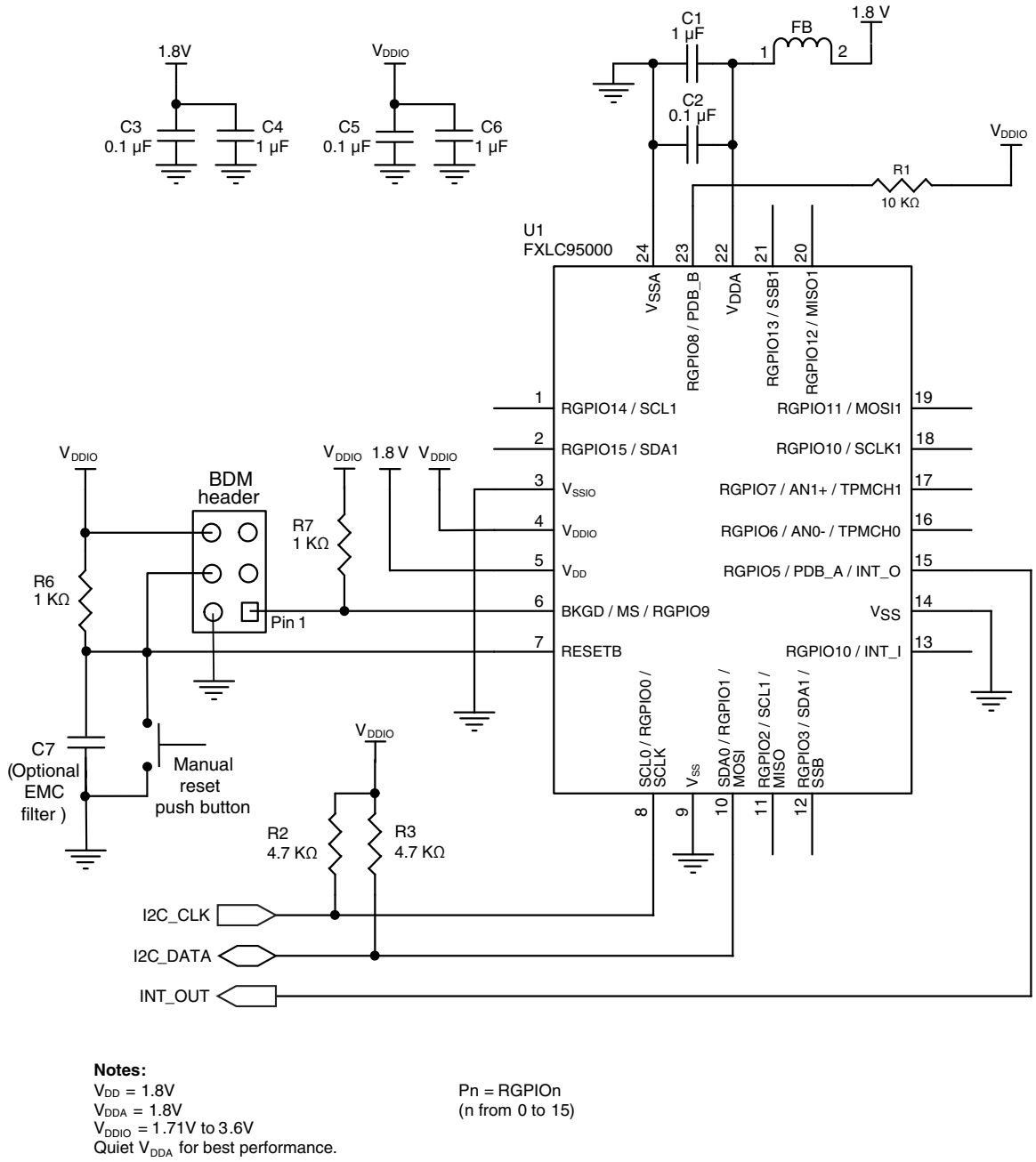
4.3.3 I^2C reset considerations

If there is a reset during a slave I^2C read transaction, then the slave device state machine will hang the bus, because it is waiting for the master clock. The host-driven reset signal provides an external way to reset the I^2C state machine.

4.3.4 FXLC95000CL as an intelligent slave

I^2C pullup resistors, a ferrite bead, and a few bypass capacitors are all that are required to attach this device to a host platform. The basic configuration of the I^2C interface is shown in Figure 3.

The voltage level on pin 23 (RGPIO8) selects the slave-port format: I^2C or SPI. The RGPIO pins can also be programmed to generate interrupts to the host platform, in response to the occurrence of application events. In this case, the pins should be routed to the external interrupt pins of the host processor.

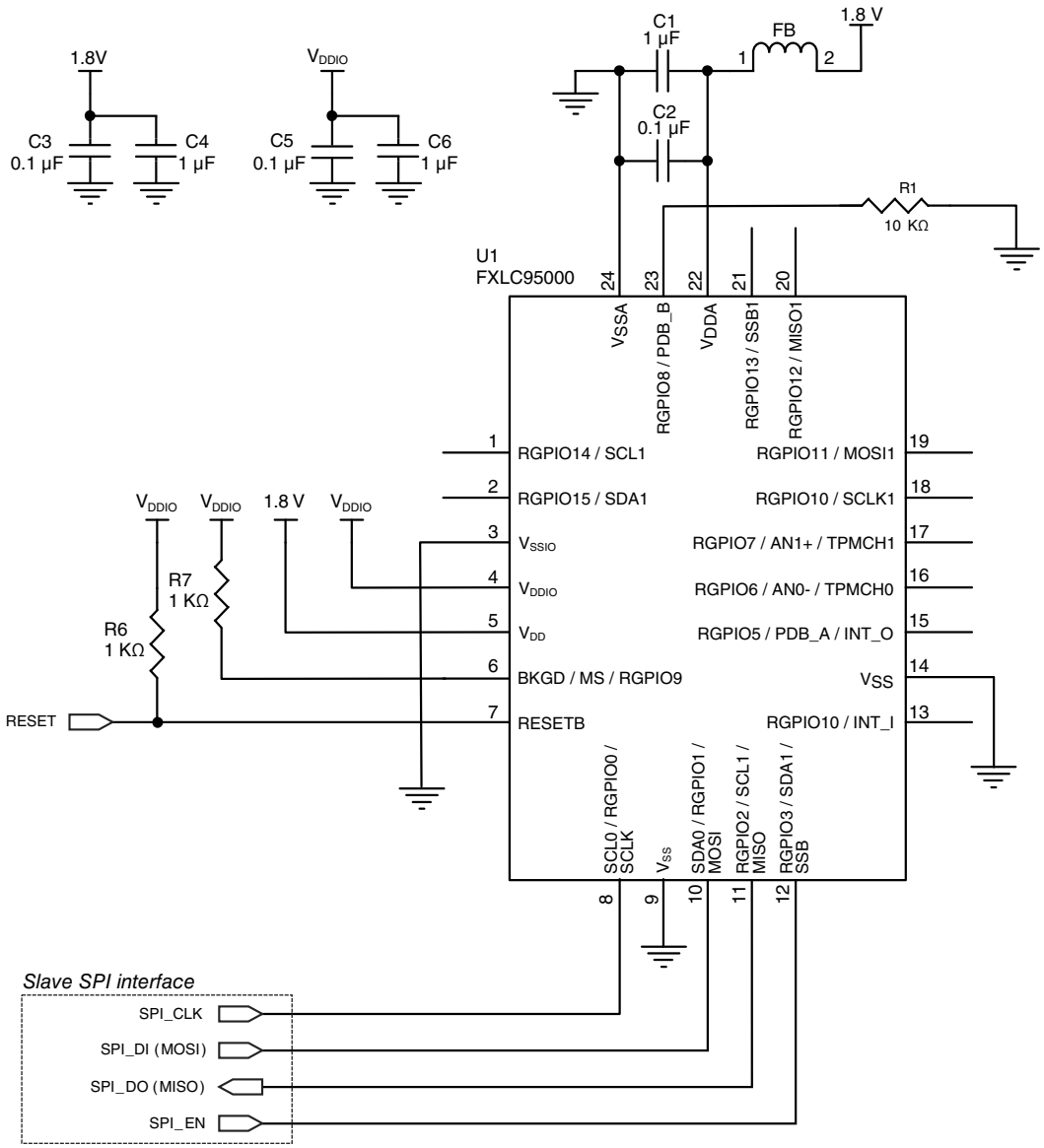


Notes:
V_{DD} = 1.8V
V_{DDA} = 1.8V
V_{DDIO} = 1.71V to 3.6V
Quiet V_{DDA} for best performance.

Pn = RGPIOn
(n from 0 to 15)

Figure 3. FXLC95000CL as a slave (I^2C interface)

The basic configuration of the SPI interface is shown in Figure 4. The RGPIO pins can also be programmed to generate interrupts to the host platform, in response to the occurrence of application events. In this case, the pins should be routed to the external interrupt pins of the host processor.



Notes:
V_{DD} = 1.8V
V_{DDA} = 1.8V
V_{DDIO} = 1.7V to 3.6V
Quiet V_{DDA} for best performance .

Slave interface select
1 = I^2C
2 = SPI

Figure 4. FXLC95000CL as a slave (SPI interface)

4.3.5 FXLC95000CL as a sensor hub

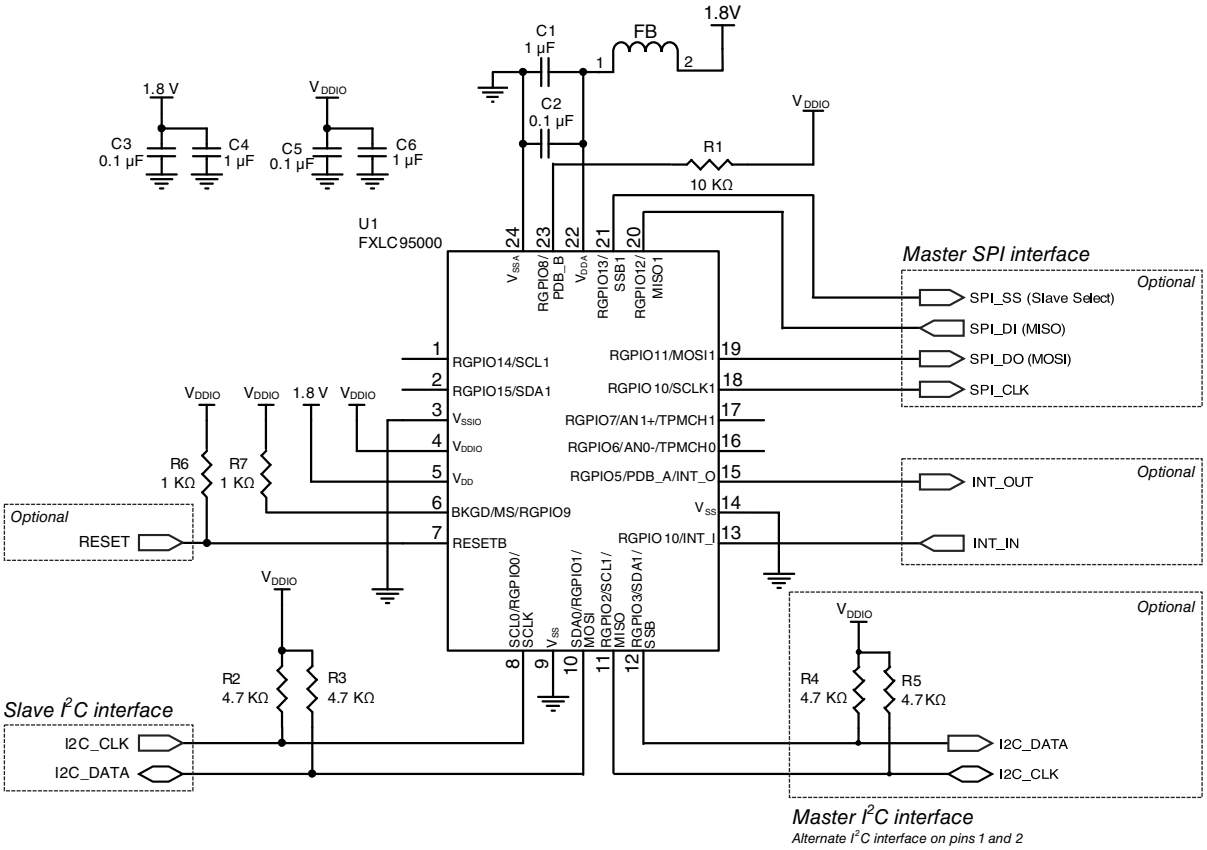
The FXLC95000CL device includes a 32-bit ColdFire V1 CPU associated with an ample amount of RAM and flash memory, a master I^2C and SPI bus, and external differential analog inputs. These are the key hardware components that transform FXLC95000CL into an efficient and versatile sensor hub. The FXLC95000CL Xtrinsic

Intelligent Sensing Platform can interface and manage almost any type of sensor, digital or analog, such as pressure sensors, magnetometers, gyroscopes, and humidity sensors. The system supports external sensors interfacing to FXLC95000CL concurrently, via a combination of master SPI and master I^2C interfaces, and external differential analog inputs.

Besides FXLC95000CL rich connectivity, the 32-bit core and hardware Multiply Accumulator (MAC) provide the processing power to collect, manipulate and fuse all sensors measurement locally and make appropriate decisions to optimize overall system power consumption.

For example, FXLC95000CL can be programmed to operate effectively as a power controller for handheld units by enabling the host platform to put itself to sleep, with confidence that the FXLC95000CL will issue a wake-up request when an external event requires the host's attention. Figure 5 shows the FXLC95000CL being used in this sensor hub configuration. Note the simple connections. Only a few bypass capacitors, a ferrite bead, and pullup resistors for the I^2C buses are required.

- Slave I^2C interface is dedicated to communication with the host processor. Interrupt output line INT_O can be involved as well.
- Master SPI, Master I^2C, AN0/AN1 and interrupt input line INT_I are available to interface a variety of external sensors



Notes:

V_{DD} = 1.8 V
V_{DDA} = 1.8 V
V_{DDIO} = 1.7 V to 3.6 V
Quiet V_{DDA} for best performance.

Slave interface select
1 = I^2C
2 = SPI

Figure 5. FXLC95000CL as a sensor hub (I^2C interface)

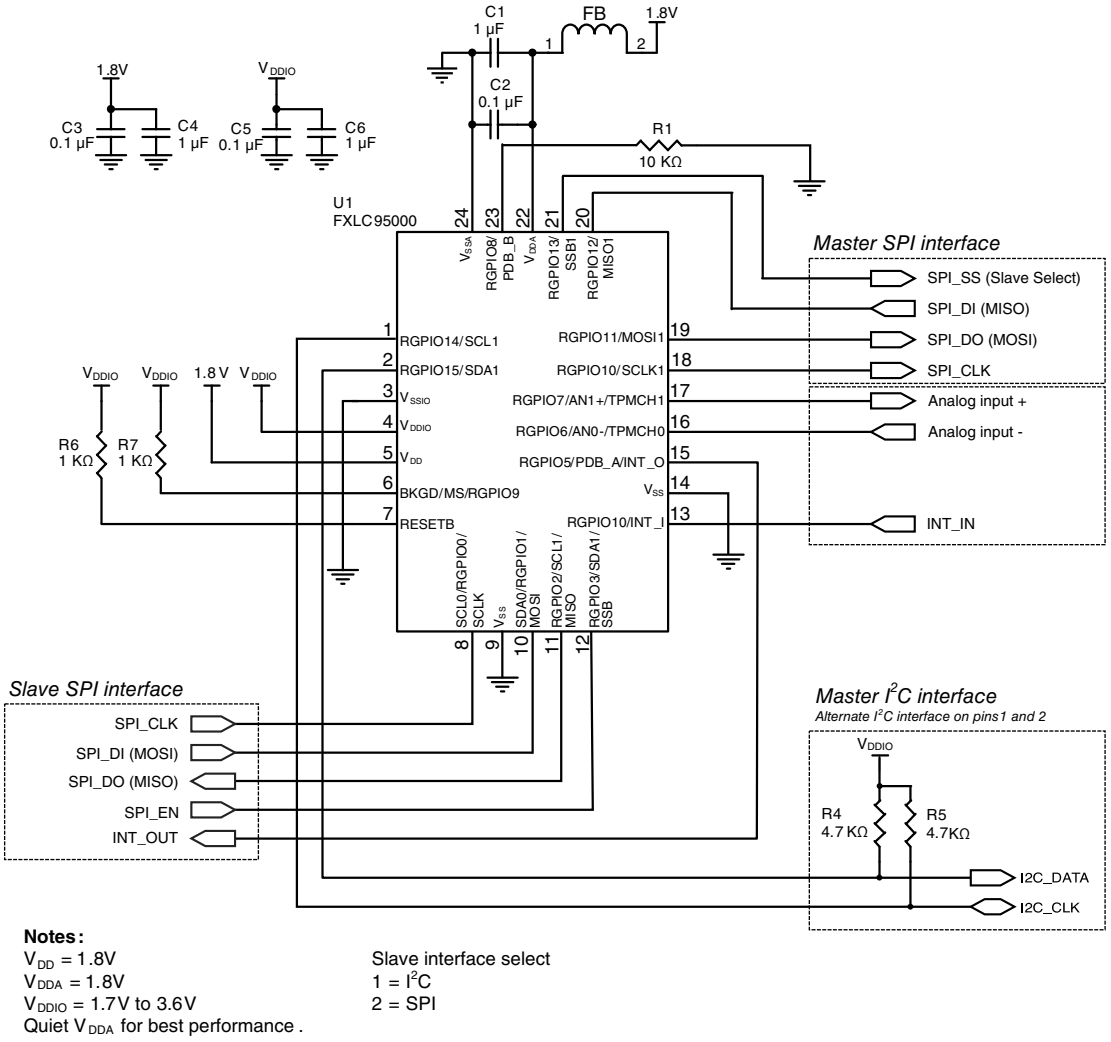


Figure 6. FXLC95000CL as a sensor hub (SPI interface)

4.4 Sensing direction and output response

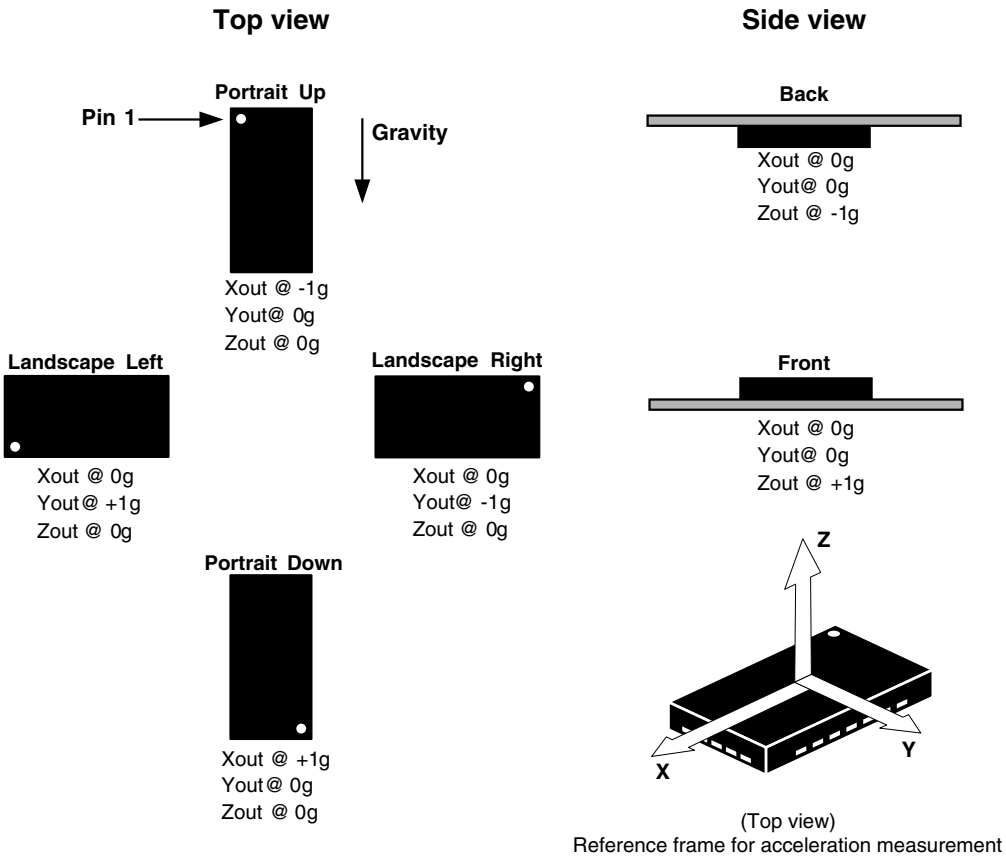


Figure 7. Sensing direction and output response

Table 2. ± 1 *g* field-measured results

g range	Full Scale[1]	± 1g[1]
± 2 *g*	± 32,767	± 16,384
± 4 *g*	± 32,767	± 8192
± 8 *g*	± 32,767	± 4095

1. Measured data in counts (16-bit word) after trimming.

5 Mechanical and Electrical Specifications

This section contains electrical specification tables and reference timing diagrams for the FXLC95000CL platform, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

5.1 Definitions

cross-axis sensitivity	The proportionality constant that relates a variation of accelerometer output to cross acceleration. This sensitivity varies with the direction of cross acceleration and is primarily due to misalignment.
deep-sleep mode	The device's lowest power state, when the system clock is stopped and the device performs no functions. In this mode, only a few exception events can wake the device.
full range	The maximum level of acceleration supported by the accelerometer's output signal, typically specified in ±*g*. For example, the output of an accelerometer program in ±2 *g* mode will be linear when subjected to accelerations within ±2 *g*. If the acceleration is larger than ±2 *g*, the output will not be linear and may rail.
hardware compensated	Sensor modules on this device include hardware correction factors for gain and offset errors which are calibrated during factory test using a least-squares fit of the raw sensor data.
nonlinearity	A measurement of deviation from perfect sensitivity. Ideally, the relationship between input and output is linear and described by the sensitivity of the device.
pin group	Device pins are clustered into a number of logical pin groupings in order to simplify and standardize electrical data sheet parameters. Pin groups are defined in Table 6.
sensitivity	Describes the gain of the sensor and can be determined by applying a 1 *g* acceleration to it, such as the earth's gravitational field. The sensitivity of the sensor can be determined by subtracting the -1 *g* acceleration value from the +1 *g* acceleration value and dividing by two.
software compensated	In addition to the first-order hardware gain and offset calibration features, Freescale implements advanced, nonlinear calibration functions to improve sensor performance.
warm-up time	The time—from the initial application of power—for a sensor to reach specified performance under specified operating conditions.
zero-g offset	Describes the deviation of an actual output signal from the ideal output signal, if no acceleration is present. The expected ideal output signal, in this case, would be zero. A deviation from ideal value is called zero-g offset. Offset is, to some extent, a result of stress on the MEMS sensor and, therefore, the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress.

5.2 Absolute maximum ratings

Absolute maximum ratings are stress ratings only and functional operation at the maximum ratings is not guaranteed. Stress beyond the limits specified here may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 3. Absolute maximum ratings

Rating	Symbol	Condition	Minimum	Maximum	Unit
Digital supply voltage	V_{DD}	—	–0.3	2.0	V
Analog supply voltage	V_{DDA}	—	–0.3	2.0	V
I/O buffer supply voltage	V_{DDIO}	—	–0.1	4.0	V
Voltage difference V_{DD} to V_{DDA}	$V_{DDA} – V_{DD}$	—	–0.1	0.1	V
Voltage difference V_{SS} to V_{SSA}	$V_{SSA} – V_{SS}$	—	–0.1	0.1	V
Input voltage	V_{In}	—	–0.3	V_{DDIO} + 0.3	V
Input/Output pin clamp current	I_C	—	–20	20	mA
Output voltage range	V_{OUTOD}	Open-drain mode	–0.3	V_{DDIO} + 0.3	V
Storage temperature	T_{STG}	—	–40	+125	°C
Mechanical shock	SH	—	—	5k	*g*
Drop test	DR	Drop onto concrete slab	—	1.8	m

Table 4. ESD and latch-up protection characteristics

Rating	Symbol	Min	Max	Unit
Human body model (HBM)	V_{HBM}	±2000	—	V
Machine model (MM)	V_{MM}	±200	—	V
Charge device model (CDM)	V_{CDM}	±500	—	V
Latch-up current at T = 85 °C	I_{LU}	±100	—	mA

Caution

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

Caution

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

5.3 Operating conditions

Table 5. Nominal operating conditions

Rating	Symbol	Min	Typ	Max	Unit
Digital supply voltage	V_{DD}	1.71	1.8	1.89	V
Analog supply voltage	V_{DDA}	1.71	1.8	1.89	V
I/O buffer supply voltage	V_{DDIO}	1.71	3.3	3.6	V
Input voltage high	V_{IH}	0.7 * V_{DDIO}	—	V_{DDIO} + 0.1	V
Input voltage low	V_{IL}	V_{SS} – 0.3	—	0.3 * V_{DDIO}	V
Operating temperature	T_A	–40	25	85	°C

5.4 General DC characteristics

Table 6. DC characteristics

Characteristic	Symbol	Condition(s)[1]	Min	Typ	Max	Unit
Output voltage high Low drive strength High drive strength	V_{OH}	Pin Groups 1 and 3[2, 3] ILOAD = –2 mA ILOAD = –3 mA	V_{DD} – 0.5	—	—	V
Output voltage low Low drive strength High drive strength	V_{OL}	Pin Groups 1 and 3[2, 3] ILOAD = 2 mA ILOAD = 3 mA	—	—	0.5	V
Total package output low current Max total I_{OL} for all pins	I_{OHT}	—	—	—	24	mA
Total package output high current Max total I_{OH} for all pins	I_{OHT}	—	—	—	24	mA
Hi-Z (off state) leakage current	$\|I_{OZ}\|$	Pin Group 3 input resistors disabled[3] V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
Pullup resistor (Pins RESETB and BKGD/MS)	R_{PU}	When enabled	17.5	—	52.5	KΩ
Power-on-reset voltage	V_{POR}	—	—	1.50	—	V
Power-on-reset hysteresis	$V_{POR-hys}$	—	—	100	—	mV
Input pin capacitance	C_{IN}	—	—	7	—	pF
Output pin capacitance	C_{OUT}	—	—	7	—	pF

1. All conditions at nominal supply: V_{DD} = V_{DDA} = 1.8 V and V_{DDIO} = 3.3 V.
2. Pin Group 1 = RESETB.
3. Pin Group 3 = RGPIO[15:0].

5.5 Supply current characteristics

Table 7. Supply current characteristics

Characteristic	Symbol	Condition(s)[1]	Min	Typ	Max	Unit
Supply current in $STOP_{NC}$ mode[2]	I_{DD-SNC}	Internal clocks disabled	—	2	—	µA
Supply current in $STOP_{SC}$ mode[3]	I_{DD-SSC}	Intenal clock in slow speed mode	—	15	—	µA
Supply current in RUN mode[4]	I_{DD-R}	Internal clock in fast mode	—	5.4	—	mA

1. All conditions at nominal supply: V_{DD} = V_{DDA} = 1.8 V and V_{DDIO} = 3.3 V.
2. $STOP_{NC}$: Stop mode, no clock.
3. $STOP_{SC}$: Stop mode, slow clock.
4. RUN: Normal fast mode. Total current with the analog section active, 16 bits ADC resolution selected, MAC unit used, and all peripheral clocks enabled.

5.6 Accelerometer transducer mechanical characteristics

Table 8. Accelerometer characteristics

Characteristic	Symbol	Condition(s)[1]	Min	Typ	Max	Unit
Full range	A_{FR}	±2 *g*	—	±2	—	*g*
		±4 *g*	—	±4	—	
		±8 *g*	—	±8	—	
Sensitivity/resolution (16 bits ADC resolution) (after trimming)	A_{SENS}	±2 *g*	—	0.061	—	mg/LSB
		±4 *g*	—	0.122	—	
		±8 *g*	—	0.244	—	
Zero-g level offset accuracy (pre-board mount)	OFF_{PBM}	±2 *g*	–100	—	+100	mg
		±4 *g*				
		±8 *g*				
Nonlinearity Best fit straight line	A_{NL}	±2 *g*	—	±0.25	—	% A_{FR}
		±4 *g*	—	±0.5	—	
		±8 *g*	—	±1	—	
Sensitivity change versus temperature	TC_{SA}	±2 *g*	—	±0.17	—	%/°C
Zero-g level change versus temperature[2]	TC_{Off}	—	—	±0.2	—	mg/°C
Zero-g level offset accuracy (post-board mount)	OFF_{BM}	±2 *g*	–100	—	+100	mg
		±4 *g*				
		±8 *g*				
Output data bandwidth	BW	—	—	ODR/2[3]	—	Hz
Noise density	Noise	±2*g*, ODR=488Hz, 4xoversampling[4]	—	100	—	µg/sqrt(Hz)
			—	3.12	—	mg (RMS)

Table continues on the next page...

Table 8. Accelerometer characteristics (continued)

Characteristic	Symbol	Condition(s)[1]	Min	Typ	Max	Unit
		±8*g*, ODR=488Hz, 4xoversampling[4]	—	120	—	µg/sqrt(Hz)
			—	3.75	—	mg (RMS)
Cross-axis sensitivity	—	—	–5	—	5	%

1. All conditions at nominal supply: V_{DD} = V_{DDA} = 1.8V and V_{DDIO} = 3.3V.
2. Relative to 25°C.
3. ODR: Output Data Rate or the sampled data rate of the system.
4. Performance specification is with CPU being inactive during sensor data acquisition

5.7 Temperature sensor characteristics

Table 9. Temperature sensor characteristics

Characteristic	Symbol	Condition(s)[1]	Min	Typ	Max	Unit
Full scale range	T_{FSR}	—	–40	—	+85	°C
Sensitivity	TSENS	16 bit data word	—	0.0025	—	°C/LSB
Non-linearity	T_{NL}	—	—	±2.4	—	% FSR

1. All conditions at nominal supply: V_{DD} = V_{DDA} = 1.8 V and V_{DDIO} = 3.3 V.

5.8 ADC characteristics

Table 10. ADC characteristics

Characteristic	Symbol	Condition(s)[1]	Min	Typ	Max	Unit
External input voltage	V_{AI}	Voltage at AN0 or AN1	0.2	—	1.1	V
External differential input voltage[2]	V_{ADI}	AN1 – AN0	–0.9	—	0.9	V
Full-scale range	V_{FS}	—	—	1.8	—	V
Programmable resolution	R_{ES}	—	10	14	16	bits
Conversion Time @ 14 bits resolution (three-sample frame, XYZ)	t_c	—	—	207	—	µs
Integral nonlinearity	INL	Full scale	—	±15	—	LSB
Differential nonlinearity	DNL	—	—	±2	—	LSB
Input leakage	I_{IA}	—	—	—	±2	µA
Total capacitance	C_{in}	—	—	7	—	pF
Series resistance	R_{in}	—	—	6	—	kΩ

1. All conditions at nominal supply: V_{DD} = V_{DDA} = 1.8 V, V_{DDIO} = 3.3 V, and R_{ES} = 14 unless otherwise noted.
2. The external ADC input pins go through a buffer line that is powered by V_{DDIO}. Noise on the V_{DDIO} line degrades the external ADC signal.

5.8.1 ADC Sample Rates

The system clock is 16 MHz with the first sample rate generated by dividing the system clock by 4096 (16 MHz / 4096 = 3906.25 Hz). Subsequent sample rates are all a sequence of divide-by-two.

The FXLC95000CL platform's internal frame timer supports the following sample rates (frames per second (fps)):

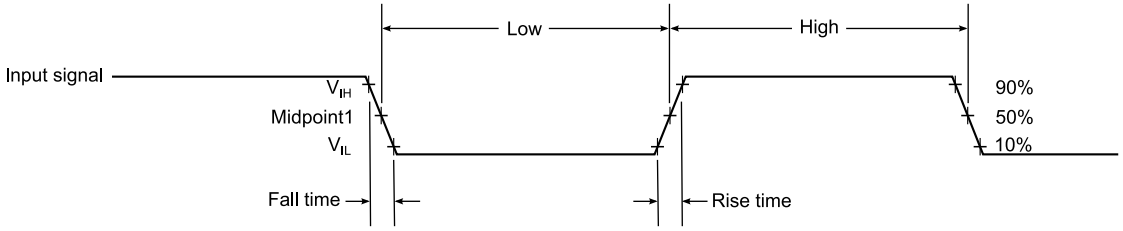
3906.25 fps
1953.13 fps
976.56 fps
488.28 fps
244.14 fps
122.07 fps
61.04 fps
30.52 fps
15.26 fps
7.63 fps
3.81 fps
1.91 fps
0.95 fps
0.48 fps
0.24 fps

Notes

- At the fastest sampling rate of 3906.25 Hz, there is not enough time to complete the ADC conversions' highest-bit resolution, so only 10-,12-,and 14-bit resolutions are available at that rate. All of the ADC resolutions (10-,12-, 14-, and 16-bit) are available at all other sample rates.
- Freescale's Intelligent Sensor Framework (ISF) uses the software-triggered sample mode, using the MTIM16 timer to set the sample period. This allows the specification of sample periods to microsecond resolution.

5.9 AC electrical characteristics

Tests are conducted using the input levels specified in Table 5. Unless otherwise specified, propagation delays are measured from one 50% point to the next 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 8.



Note: The midpoint in $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 8. Input signal measurement references

Figure 9 shows the definitions of the following signal states:

- Data Active state, when a bus or signal is driven, and enters a low impedance state
- Data Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

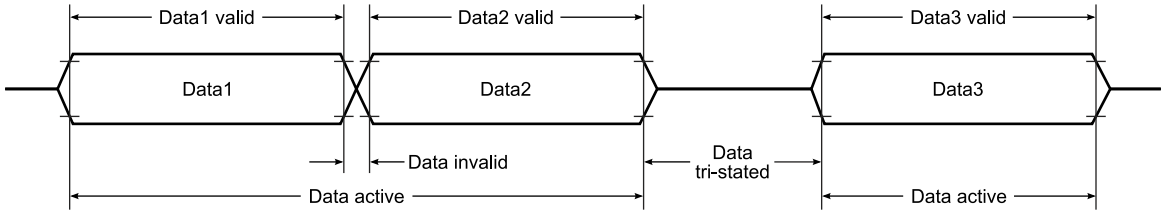


Figure 9. Signal states

5.10 General timing control

Table 11. General timing characteristics

Characteristic	Symbol	Condition(s)[1]	Min	Typ	Max	Unit
V_{DD} rise time	T_{rvdd}	10% to 90%	—	—	1	ms
POR release delay[2]	T_{POR}	Power-up	0.35	—	1.5	ms

Table continues on the next page...

Table 11. General timing characteristics (continued)

Characteristic	Symbol	Condition(s)[1]	Min	Typ	Max	Unit
Warm-up time	T_{WU}	From STOP with No Clock	—	7	—	sample periods
Frequency of operation	F_{OPH}	Full-speed clock	—	16	—	MHz
	F_{OPL}	Slow-speed clock	—	62.5	—	KHz
System clock period	t_{CYCH}	Full-speed clock	—	62.5	—	ns
	t_{CYCL}	Slow-speed clock	—	16	—	µs
Full/Slow clock ratio	—	—	—	256	—	
Oscillator frequency absolute accuracy @ 25°C	—	Full-speed clock	–5	—	+5	%
Oscillator frequency variation over temperature (–40°C to 85°C vs. ambient)	—	Slow-speed clock	–6	—	+6	%
Minimum RESET Assertion Duration	t_{RA}	—	4T[3]	—	—	—

1. All conditions at nominal supply: $V_{DD} = V_{DDA} = 1.8$ V and $V_{DDIO} = 3.3$ V.
2. Time measured from $V_{DD} = V_{POR}$ until the internal reset signal is released.
3. T = Period of one system clock cycle. In full-speed mode, T is nominally 62.5 ns. In slow-speed mode, T is nominally 16 µs.

5.11 Interfaces

The FXLC95000CL may be controlled via its included slave I²C module that can be active 100% of the time. The FXLC95000 also includes a master I²C that should be used only when the system clock is running at full speed. The master interface is intended to be used to communicate with other, external sensors.

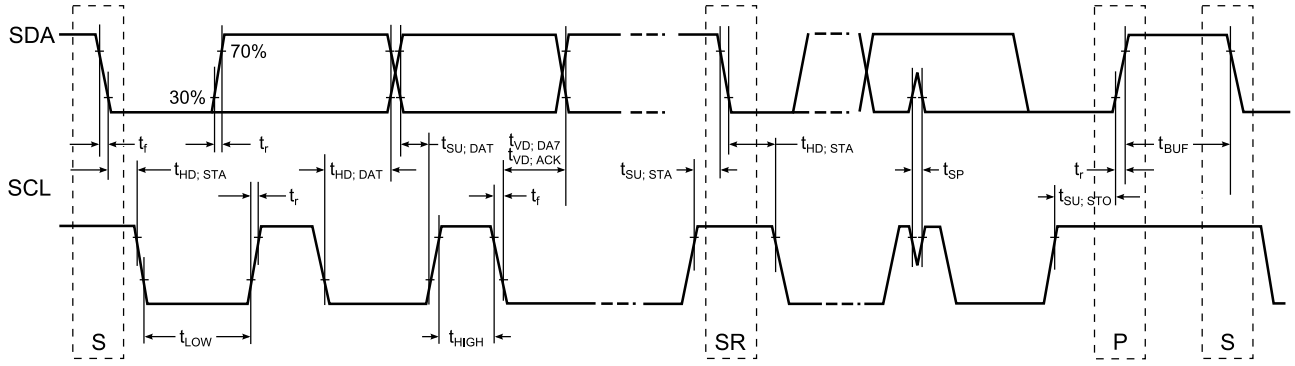


Figure 10. I²C standard and fast-mode timing

5.11.1 Slave I²C

Table 12. I²C speed ranges

Mode	Max Baud Rate (f_{SCL})	Minimum Bit Time	Minimum SCL Low (t_{LOW})	Minimum SCL High (t_{HIGH})	Min Data Set-up Time ($t_{SU;\ DAT}$)	Min/Max Data Hold Time ($t_{HD;\ DAT}$)
Standard	100 KHz	10 µs	4.7 µs	4 µs	250 ns	0 µs/3.45 µs[1]
Fast	400 KHz	2.5 µs	1.3 µs	0.6 µs	100 ns	0 µs/0.9 µs[1]
Fast +	1 MHz	1 µs	500 ns	260 ns	50 ns	0 µs/0.45 µs[1]
High-speed supported	2.0 MHz	0.5 µs	200 ns	200 ns	10 ns	0 ns/70 ns (100 pf)[2]

1. The maximum $t_{HD;DAT}$ must be at least a transmission time less than $t_{VD;DAT}$ or $t_{VD;ACK}$. For details, see the I²C standard.
2. Timing met with IFE = 0, DS = 1, and SE = 1. For more information, refer to Port Control Registers in the FXLC95000CL Hardware Reference Manual.

5.11.2 Master I²C Timing

The master I²C should only be used when the system clock is running at full speed. Do not attempt to use the master I²C across frames in which a portion of the time is spent in low-speed mode.

Table 13. Master I²C timing

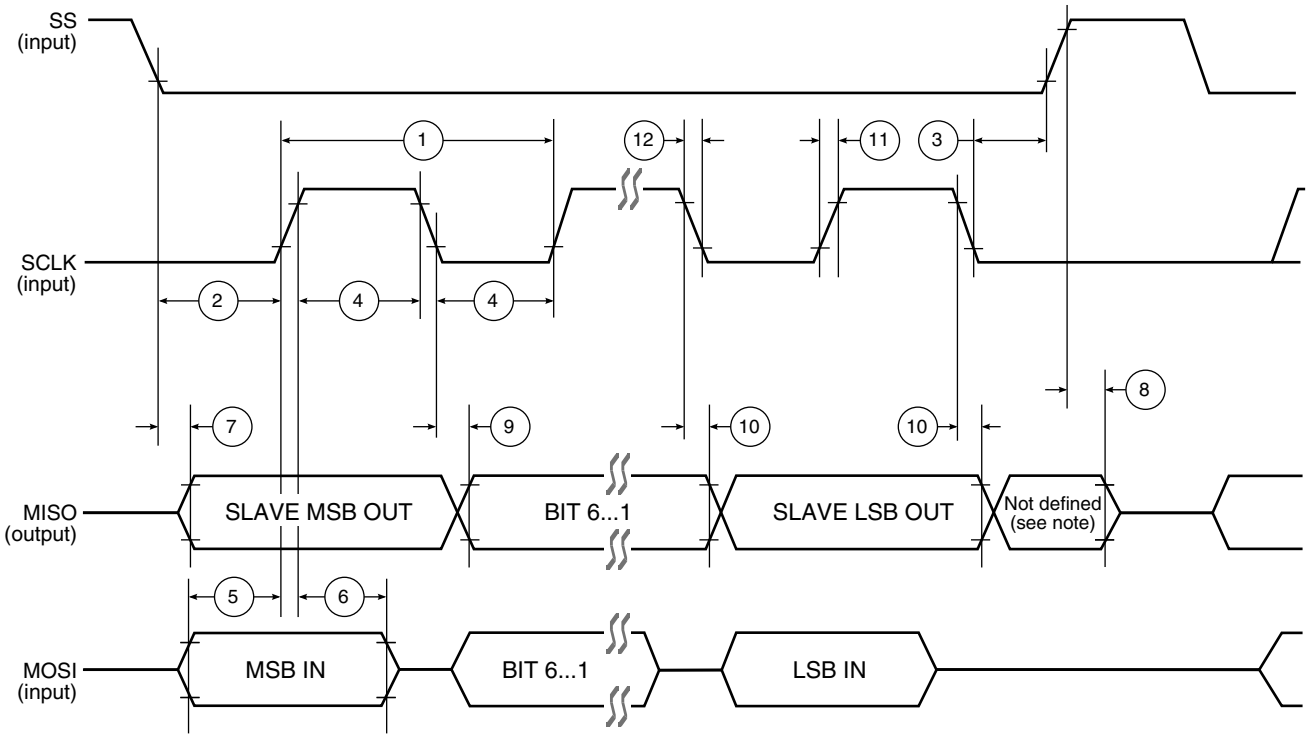
Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7	—	0.6	—	µs
Data Hold Time for I²C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	0[1]	0.9[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250	—	100[3, 4]	—	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	µs

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum $t_{HD;\ DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

3. Set-up time in slave-transmitter mode is 1 system-clock period (16 MHz = 62.5 ns). There is no FIFO on the I^2C.
4. A fast-mode, I^2C bus device can be used in a standard mode I^2C bus system, but the requirement $t_{SU;\,DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. According to the standard mode, I^2C bus specification, if such a device stretches the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + t_{SU}; DAT = 1000 + 250 = 1250 ns before the SCL line is released.

5.11.3 SPI interfaces (slave and master)

Figure 11 and Table 14 describe the timing requirements for the SPI system.



Note:
Not defined—normally the MSB of the character just received.

Figure 11. Slave and master SPI timing

Table 14. Slave and master SPI timing

Drawing Number	Function	Symbol	Min	Max	Unit
—	Operating frequency	f_{op}	0	$F_{OPH}/4$	Hz
1	SCLK period	t_{SCLK}	4	—	t_{CYCH}
2	Enable lead time	t_{Lead}	0.5	—	t_{CYCH}
3	Enable lag time	t_{Lag}	0.5	—	t_{CYCH}
4	Clock (SCLK) high or low time	t_{WSCLK}	200	—	ns

Table continues on the next page...

Table 14. Slave and master SPI timing (continued)

Drawing Number	Function	Symbol	Min	Max	Unit
5	Data set-up time (inputs)	t_{SU}	15	—	ns
6	Data hold time (inputs)	t_{HI}	25	—	ns
7	Access time	t_a	—	25	ns
8	MISO Disable Time	t_{dis}	—	25	ns
9	Data valid (after SCLK edge)	t_v	—	25	ns
10	Data hold time (outputs)	t_{HO}	0	—	ns
11	Rise time				
	Input	t_{RI}	—	25	ns
	Output	t_{RO}	—	25	ns
12	Fall time				
	Input	t_{FI}	—	25	ns
	Output	t_{FO}	—	25	ns

5.12 Flash parameters

The FXLC95000CL platform has 128 KB of internal flash memory. There are ROM functions that allow the erasing and programming of the flash memory. A chip supply voltage of 1.8 V is sufficient for the flash programming voltage.

The smallest block of memory that can be written is four bytes and those four bytes must be aligned on a four byte boundary. The largest block of memory that can be programmed is 256 bytes and the block must start at a 256-byte boundary.

Flash programming blocks must start on a 4-byte boundary and cannot cross a 256-byte page boundary.

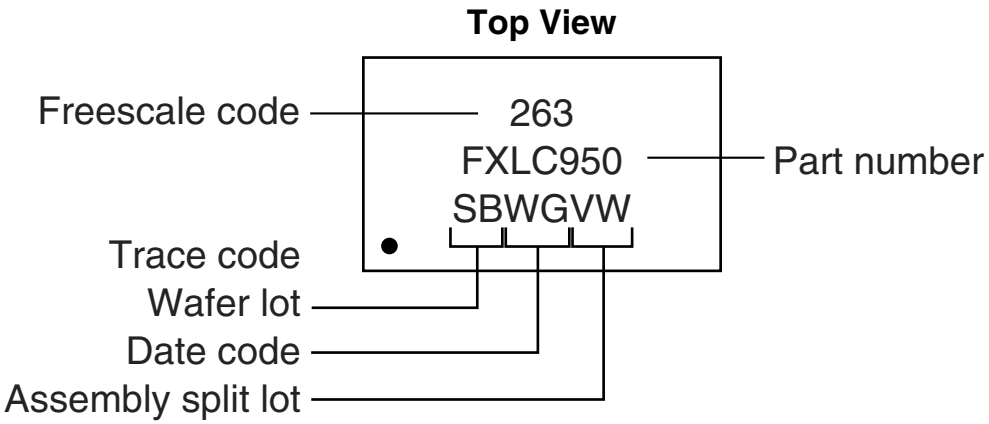
Table 15. Flash parameters

Parameter	Value
Word depth	32,768
Row size	256 bytes
Page erase size (Erase block size)	4 rows = 1024 bytes
Maximum page programming size	1 row = 256 bytes
Minimum word programming size	4 bytes
Memory organization	32,768 × 32 bits = 128 KB total
Endurance	20,000 cycles minimum
Data retention	> 100 years at room temperature

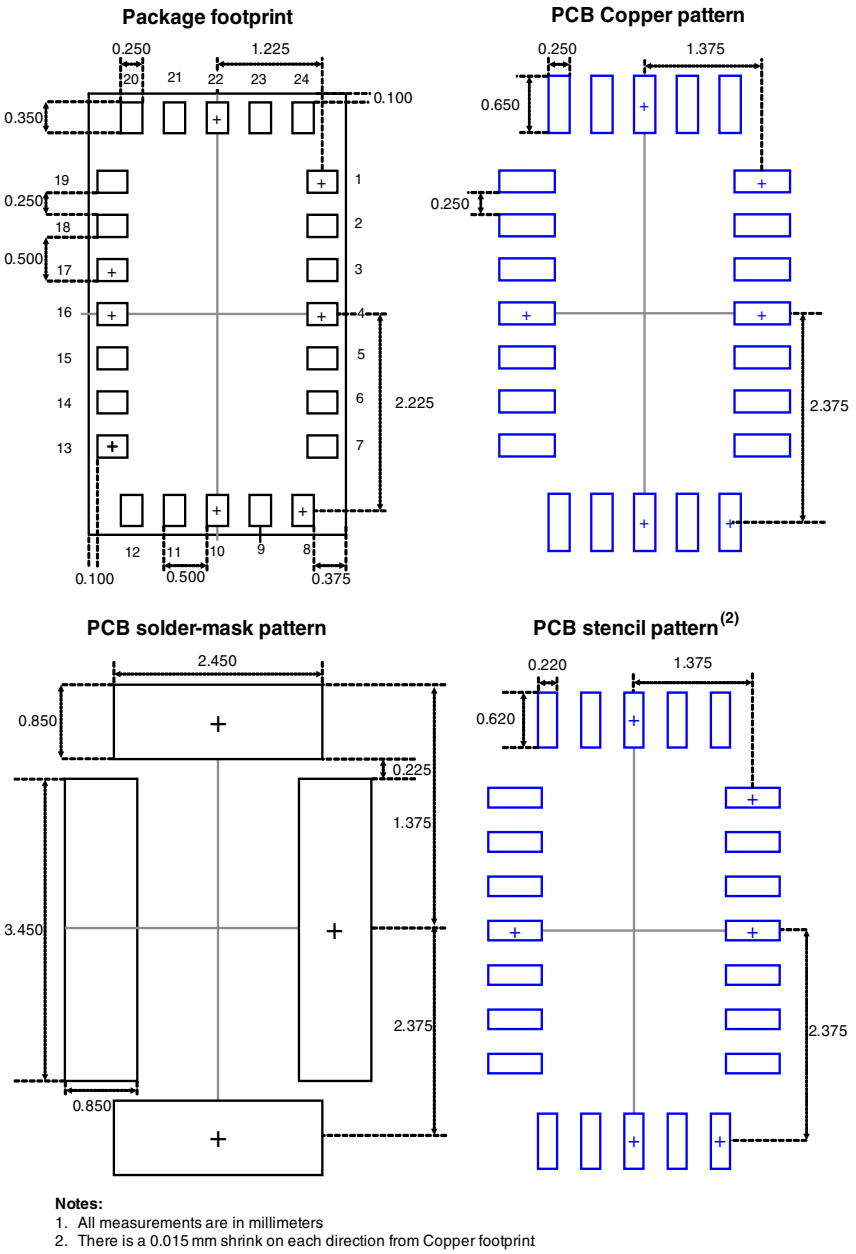
6 Package Information

The FXLC95000CL is contained in a 24 pin, 3 mm by 5 mm by 1 mm LGA package.

6.1 Product Identification Markings

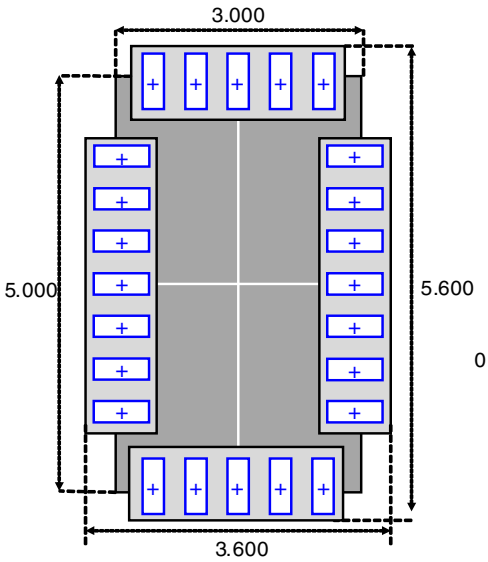


6.2 Footprint and pattern information

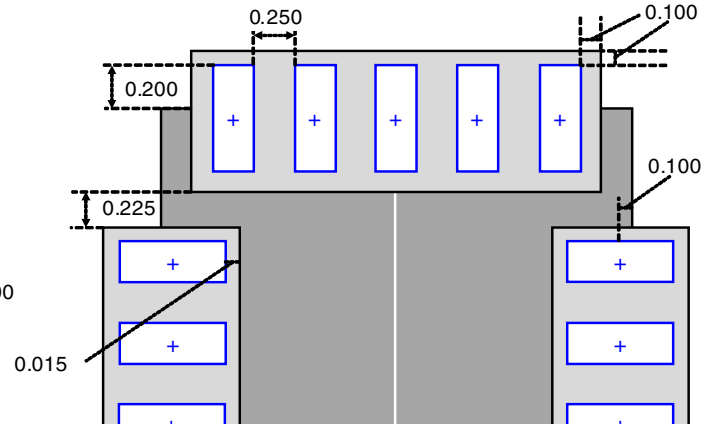


Notes:
1. All measurements are in millimeters
2. There is a 0.015 mm shrink on each direction from Copper footprint

Overlay drawing



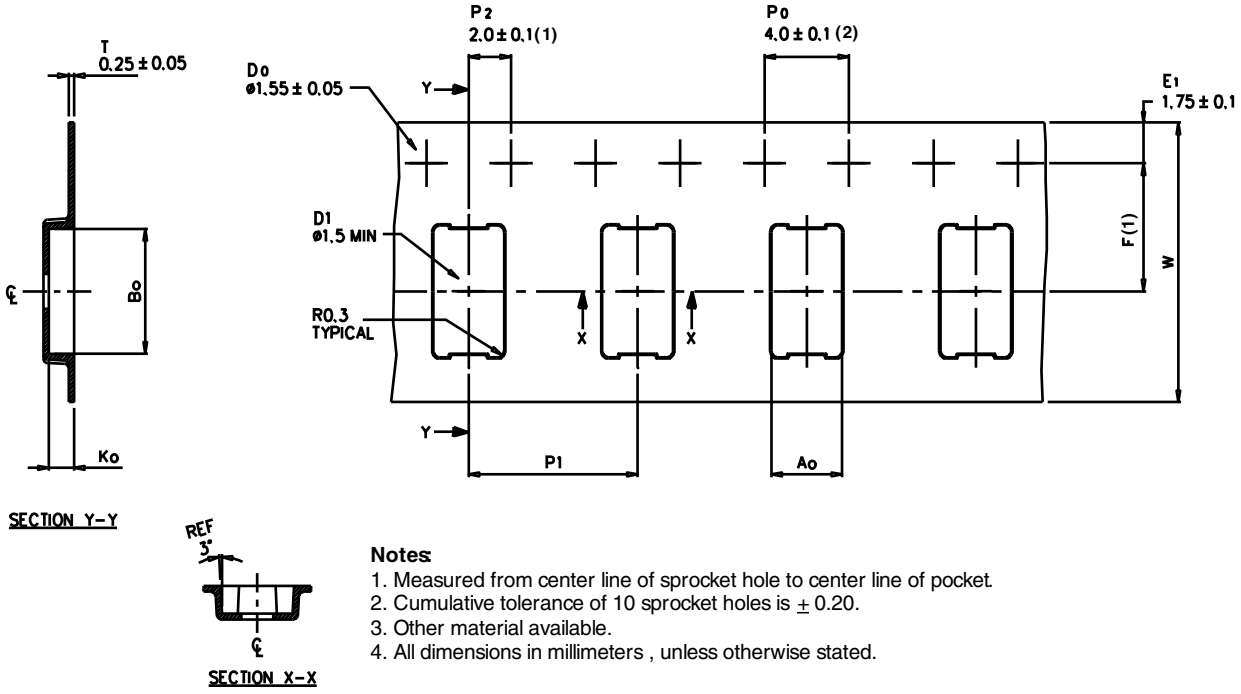
Zoom-in drawing



Note:
All measurements are in millimeters

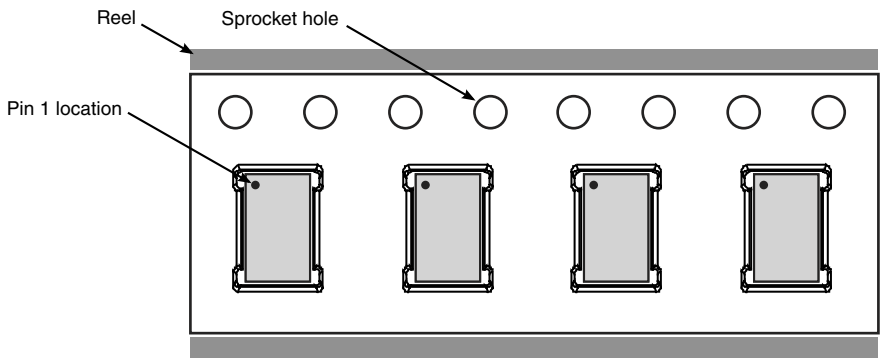
6.3 Tape and reel information

6.3.1 Tape dimensions

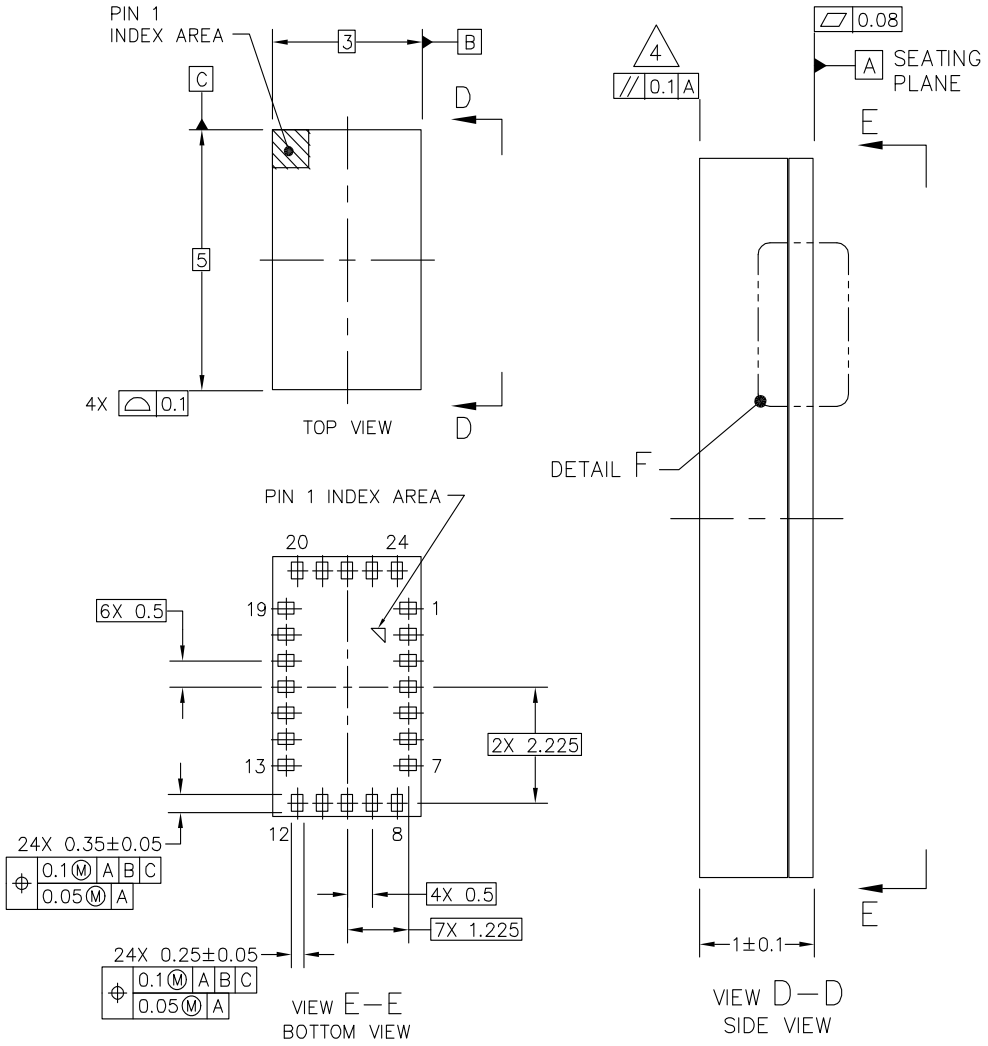


Notes:
1. Measured from center line of sprocket hole to center line of pocket.
2. Cumulative tolerance of 10 sprocket holes is ± 0.20.
3. Other material available.
4. All dimensions in millimeters , unless otherwise stated.

6.3.2 Device orientation



6.4 Package dimensions



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSION APPLIES TO ALL LEADS.
4. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Case 2208-01, Issue O, 24-lead LGA

7 Revision History

Revision number	Revision date	Description
1.0	May 2013	**Initial Public Release**
1.1	August 2013	• Changed Zero-g level change versus temperature (TC_{Off}) specification in Table 8 • Added RMS noise specification for ±2 *g* and ±8 *g* in Table 8 • Removed footnote in Table 9 • Restated non-linearity in different units (% FSR) in Table 9
1.2	August 2013	• Changed Zero-g level change versus temperature (TC_{Off}) specification in Table 8. • Changed Sensitivity TSENS specification in Table 9.

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Revision 1.2, 8/2013