File Number **2314**

IRFD110, IRFD111, IRFD112, IRFD113

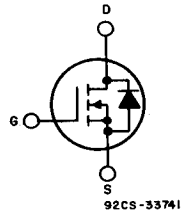
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

0.8 A and 1 A, 60 V - 100 V
$r_{DS(on)}$ = 0.6 Ω and 0.8 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

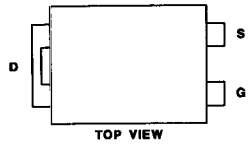


TERMINAL DIAGRAM

The IRFD110, IRFD111, IRFD112, and IRFD113 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-pin DIP package.

TERMINAL DESIGNATION



4-PIN DIP

ABSOLUTE MAXIMUM RATINGS

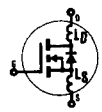
	Parameter	IRFD110	IRFD111	IRFD112	IRFD113	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	100	60	100	60	V
I_D @ T_A = 25°C	Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM}	Pulsed Drain Current	8.0	8.0	6.4	6.4	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_A = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100 μH				A
		8.0	8.0	6.4	6.4	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFD110, IRFD111, IRFD112, IRFD113

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD110, 2	100	–	–	V	V_{GS} = 0V
		IRFD111, 3	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate - Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate - Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD110, 1	1.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFD112, 3	0.8	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD110, 1	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 0.8A
		IRFD112, 3	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.2	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.8A
C_{iss}	Input Capacitance	ALL	–	135	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	80	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.8A, Z_o ≈ 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.0	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. *See Fig. 17 for test circuit. (Gate charge is essentially* independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	3.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	11	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measure from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	*Measured from the* source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD110, 1	–	–	1.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD112, 3	–	–	0.8	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD110, 1	–	–	8.0	A	
		IRFD112, 3	–	–	6.4	A	
V_{SD}	Diode Forward Voltage ②	IRFD110, 1	–	–	2.5	V	T_A = 25°C, I_S = 1.0A, V_{GS} = 0V
		IRFD112, 3	–	–	2.0	V	T_A = 25°C, I_S = 0.8A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	100	–	ns	T_J = 150°C, I_F = 1.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	0.2	–	μC	T_J = 150°C, I_F = 1.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

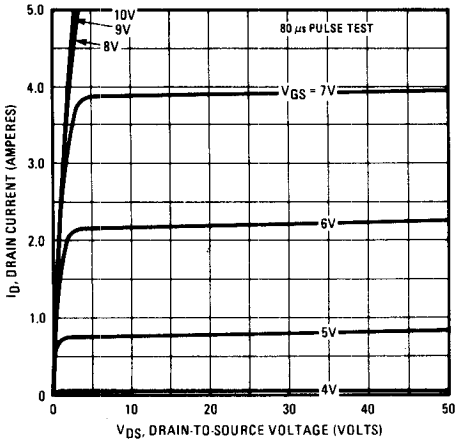


Fig. 1 – Typical Output Characteristics

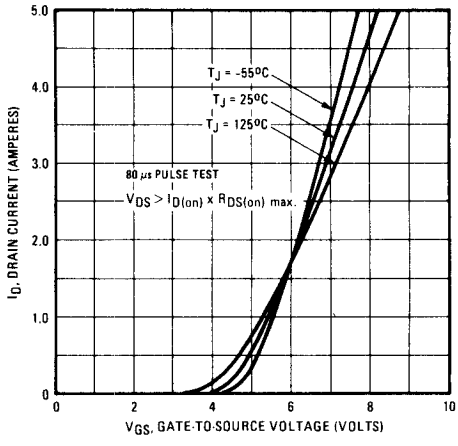


Fig. 2 – Typical Transfer Characteristics

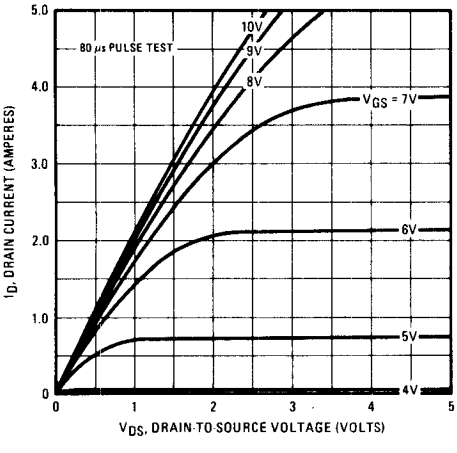


Fig. 3 – Typical Saturation Characteristics

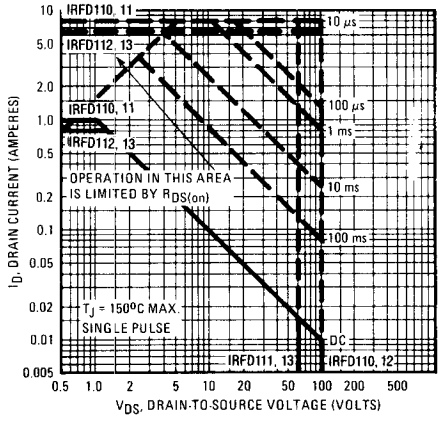


Fig. 4 – Maximum Safe Operating Area

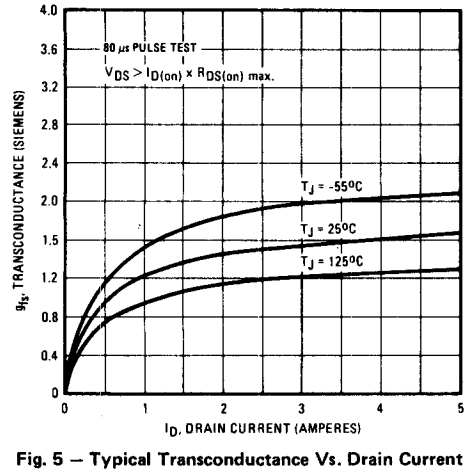


Fig. 5 – Typical Transconductance Vs. Drain Current

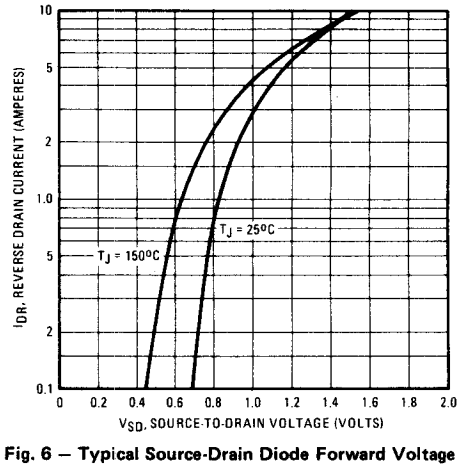


Fig. 6 – Typical Source-Drain Diode Forward Voltage

IRFD110, IRFD111, IRFD112, IRFD113

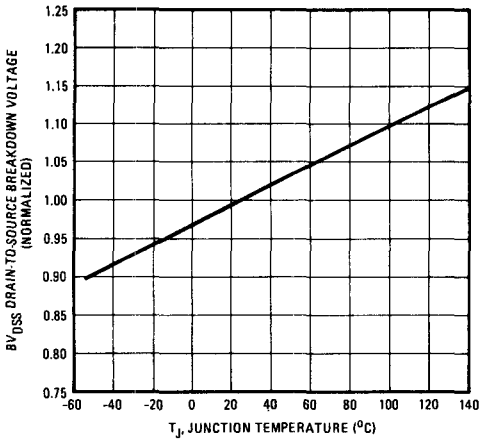


Fig. 7 — Breakdown Voltage Vs. Temperature

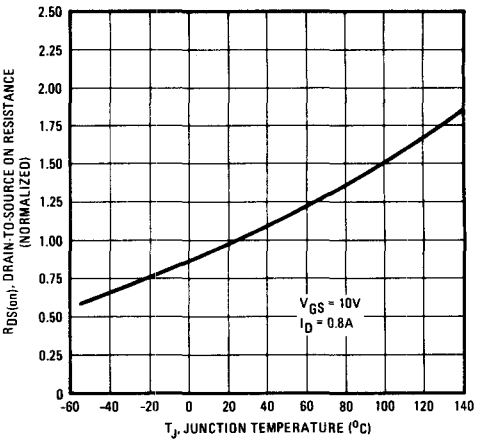


Fig. 8 — Normalized On-Resistance Vs. Temperature

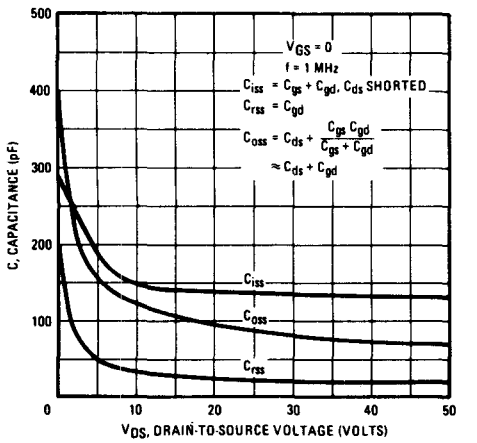


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

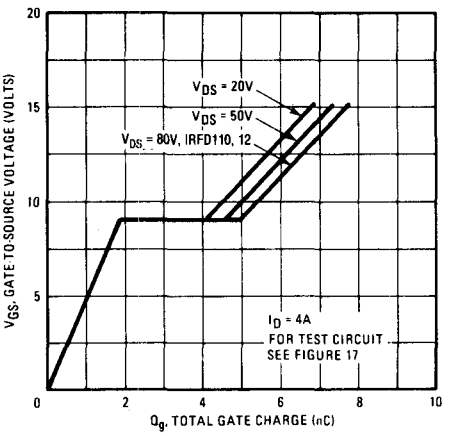


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

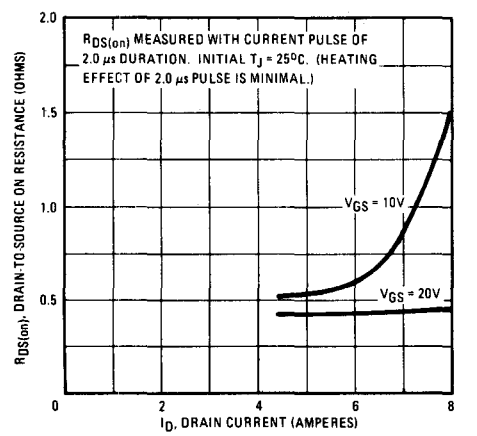


Fig. 11 — Typical On-Resistance Vs. Drain Current

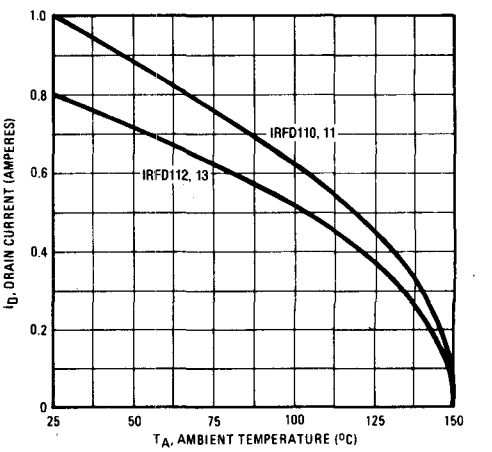


Fig. 12 — Maximum Drain Current Vs. Case Temperature

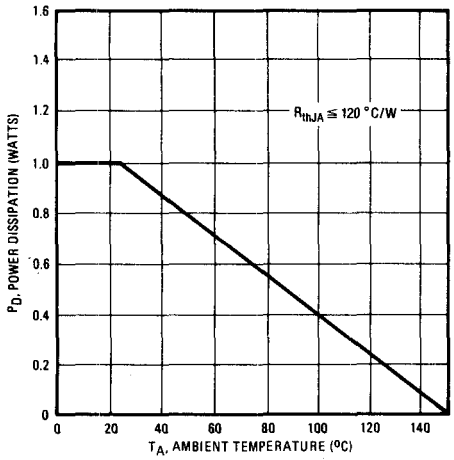


Fig. 13 – Power Vs. Temperature Derating Curve

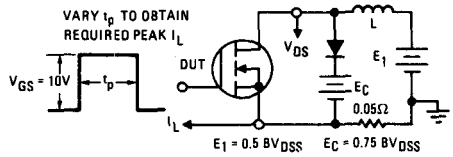


Fig. 14 – Clamped Inductive Test Circuit

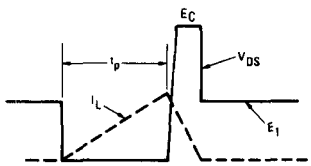


Fig. 15 – Clamped Inductive Waveforms

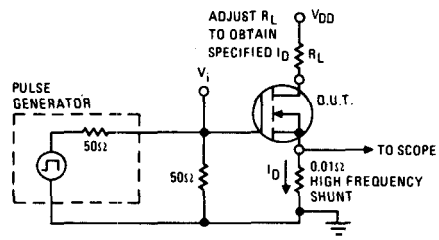


Fig. 16 – Switching Time Test Circuit

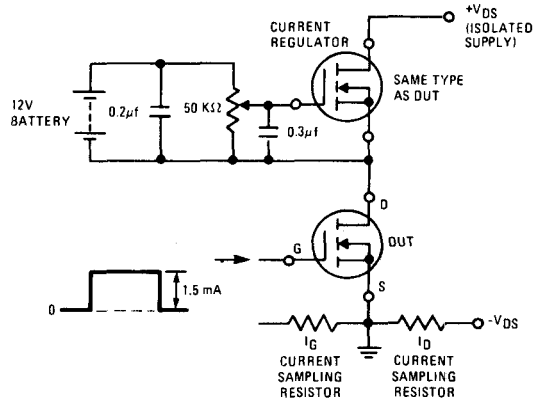


Fig. 17 – Gate Charge Test Circuit