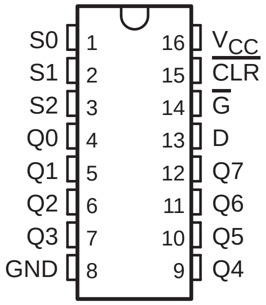
# SN54ALS259, SN74ALS259
# 8-BIT ADDRESSABLE LATCHES

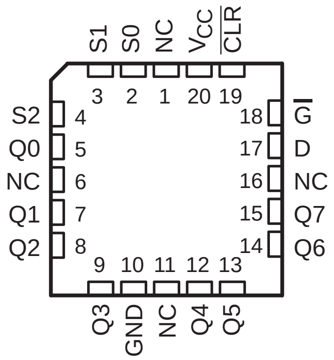
SDAS217A − DECEMBER 1982 − REVISED DECEMBER 1994

- **8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage**
- **Asynchronous Parallel Clear**
- **Active-High Decoder**
- **Enable/Disable Input Simplifies Expansion**
- **Expandable for n-Bit Applications**
- **Four Distinct Functional Modes**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54ALS259 . . . J PACKAGE**
**SN74ALS259 . . . D OR N PACKAGE**
**(TOP VIEW)**



**SN54ALS259 . . . FK PACKAGE**
**(TOP VIEW)**



NC − No internal connection

## description

These 8-bit addressable latches are designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{\text{CLR}}$) and enable ($\overline{\text{G}}$) inputs as shown in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch follows the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, $\overline{\text{G}}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output follows the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54ALS259 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS259 is characterized for operation from 0°C to 70°C.

### Function Tables

**FUNCTION**

| INPUTS | | OUTPUT OF ADDRESSED LATCH | EACH OTHER OUTPUT | FUNCTION |
|---|---|---|---|---|
| $\overline{\text{CLR}}$ | $\overline{\text{G}}$ | | | |
| H | L | D | $Q_{iO}$ | Addressable latch |
| H | H | $Q_{iO}$ | $Q_{iO}$ | Memory |
| L | L | D | L | 8-line demultiplexer |
| L | H | L | L | Clear |

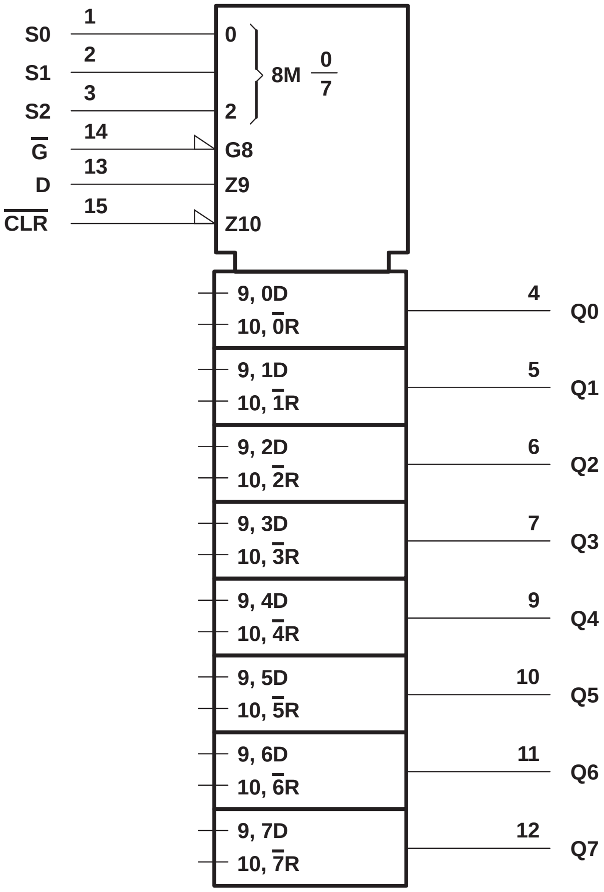
D = the level at the data input.
$Q_{iO}$ = the level of $Q_i$ (i = Q, 1, . . . 7 as appropriate) before the indicated steady-state input conditions were established.

## Function Tables (Continued)

**LATCH SELECTION**

| SELECT INPUTS | | | LATCH ADDRESSED |
|---|---|---|---|
| S2 | S1 | S0 | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

## logic symbol†



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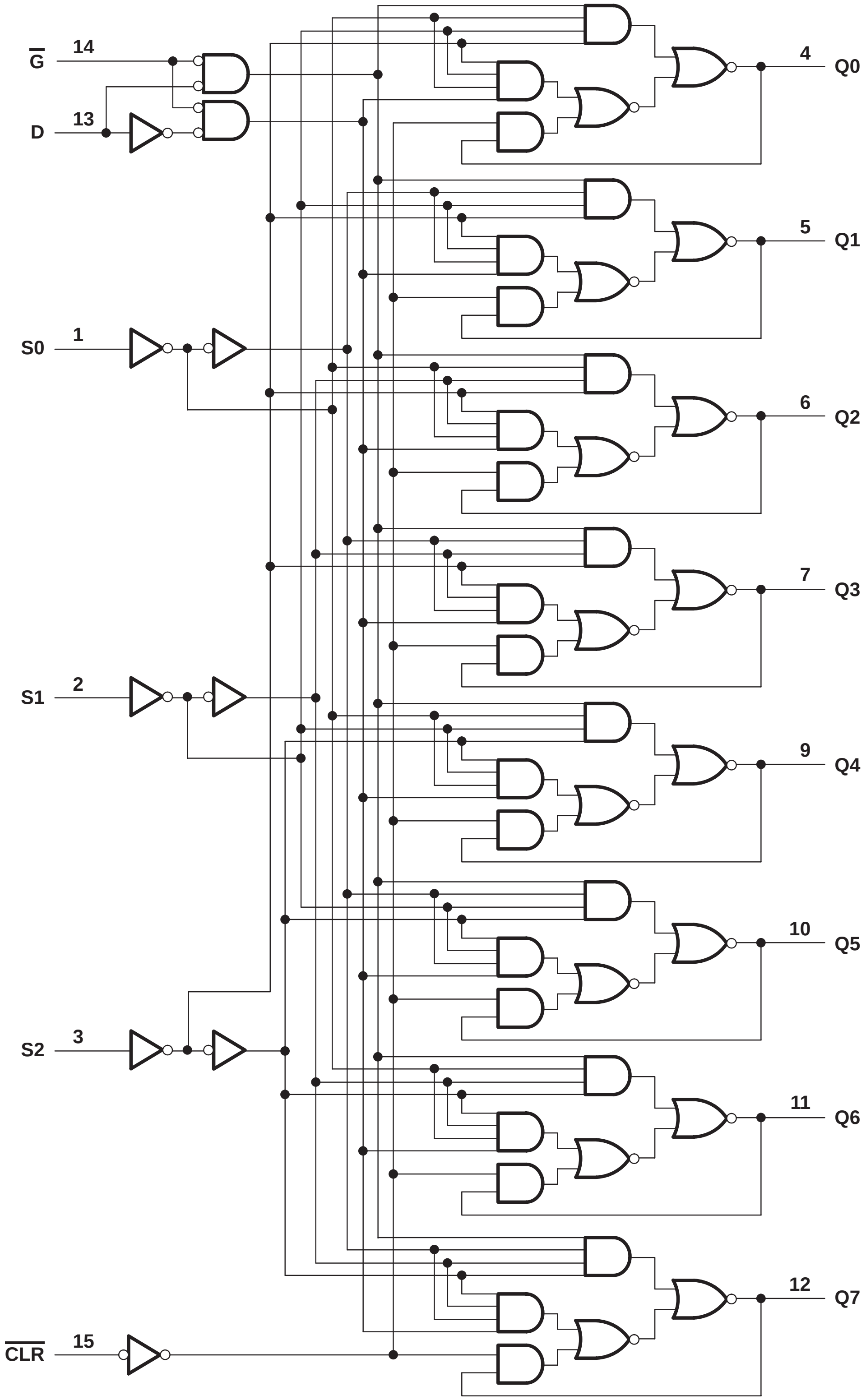
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

### logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, $V_{CC}$ . . . . . . . . . . 7 V
Input voltage, $V_I$ . . . . . . . . . . 7 V
Operating free-air temperature range, $T_A$: SN54ALS259 . . . . . . . . . . −55°C to 125°C
SN74ALS259 . . . . . . . . . . 0°C to 70°C
Storage temperature range . . . . . . . . . . −65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | SN54ALS259 | | | SN74ALS259 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 8 | mA |
| $t_w$ | Pulse duration | $\overline{G}$ low | 20 | | | 15 | | | ns |
| | | $\overline{CLR}$ low | 10 | | | 10 | | | |
| $t_{su}$ | Setup time | Data before $\overline{G}$↑ | 20 | | | 15 | | | ns |
| | | Address before $\overline{G}$↑ | 20 | | | 15 | | | |
| $t_h$ | Hold time | Data after $\overline{G}$↑ | 0 | | | 0 | | | ns |
| | | Address after $\overline{G}$↑ | 0 | | | 0 | | | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54ALS259 | | | SN74ALS259 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP[‡] | MAX | MIN | TYP[‡] | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$ − 2 | | | $V_{CC}$ − 2 | | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.1 | | | −0.1 | mA |
| $I_O$[§] | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −20 | | −112 | −30 | | −112 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | | | 14 | 22 | | 14 | 22 | mA |

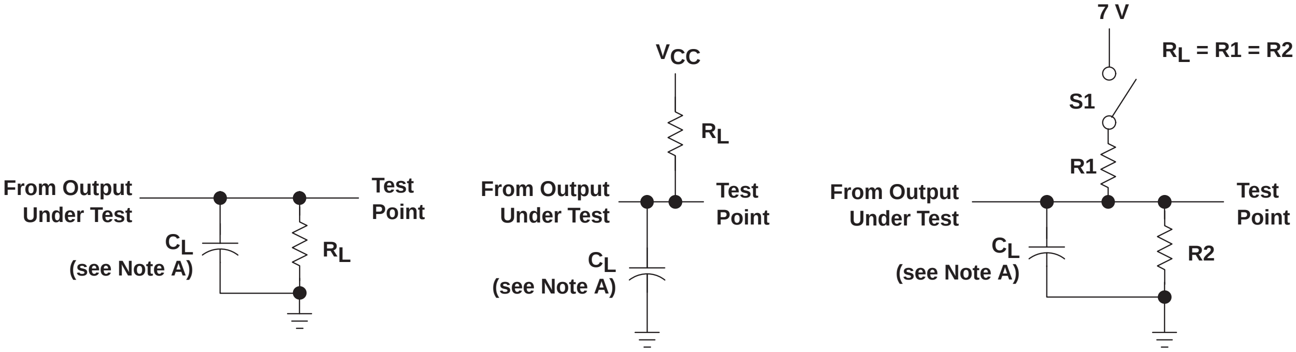
[‡] All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54ALS259 | | SN74ALS259 | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{PHL}$ | $\overline{\text{CLR}}$ | Any Q | 2 | 15 | 2 | 12 | ns |
| $t_{PLH}$ | Data | Any Q | 4 | 22 | 4 | 19 | ns |
| $t_{PHL}$ | | | 2 | 15 | 2 | 12 | |
| $t_{PLH}$ | Address | Any Q | 4 | 26 | 4 | 22 | ns |
| $t_{PHL}$ | | | 2 | 15 | 2 | 12 | |
| $t_{PLH}$ | Execute | Any Q | 4 | 22 | 4 | 20 | ns |
| $t_{PHL}$ | | | 2 | 16 | 2 | 13 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

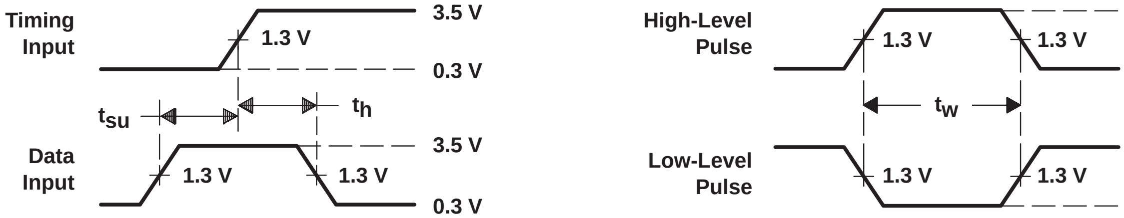
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

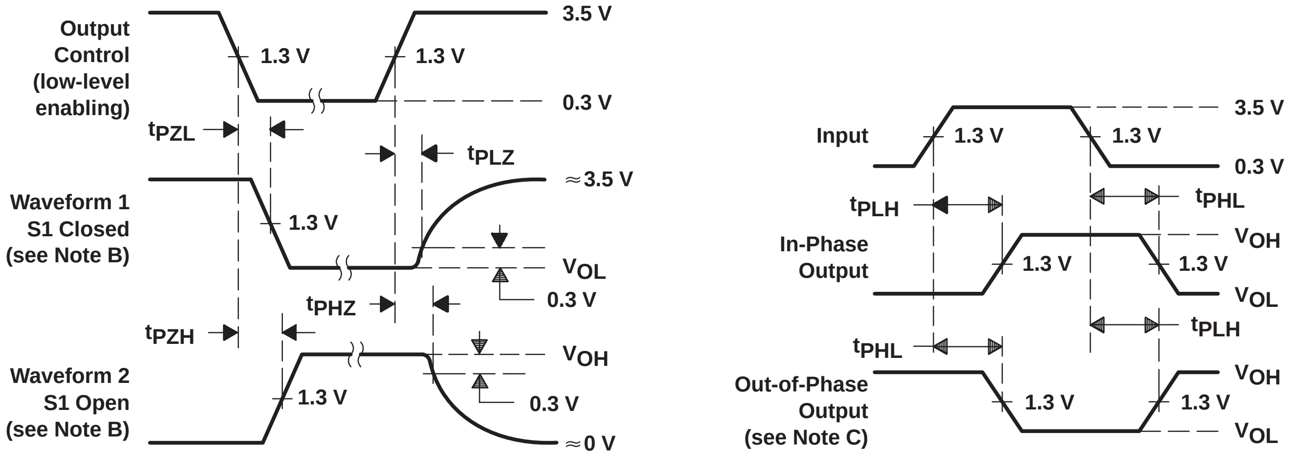
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-8874101EA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8874101EA<br>SNJ54ALS259J |
| SN54ALS259J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54ALS259J |
| SN54ALS259J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54ALS259J |
| SN74ALS259D | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | 0 to 70 | ALS259 |
| SN74ALS259DR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS259 |
| SN74ALS259DR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS259 |
| SN74ALS259N | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS259N |
| SN74ALS259N.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS259N |
| SNJ54ALS259J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8874101EA<br>SNJ54ALS259J |
| SNJ54ALS259J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8874101EA<br>SNJ54ALS259J |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF SN54ALS259, SN74ALS259 :**

- Catalog : SN74ALS259

- Military : SN54ALS259

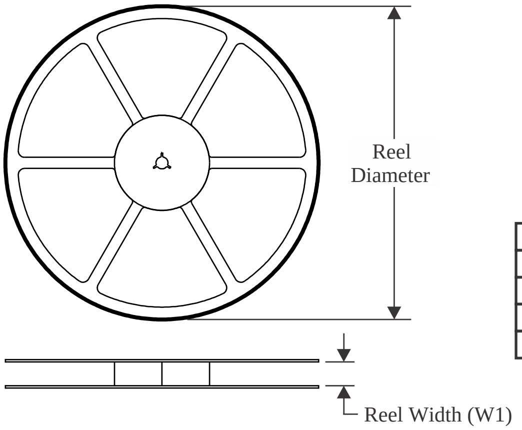
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

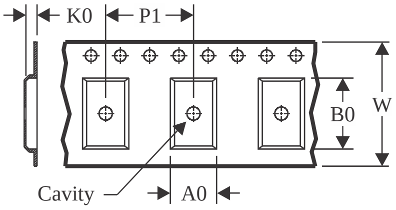
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

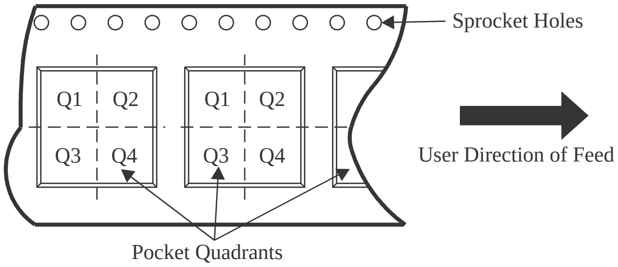


TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

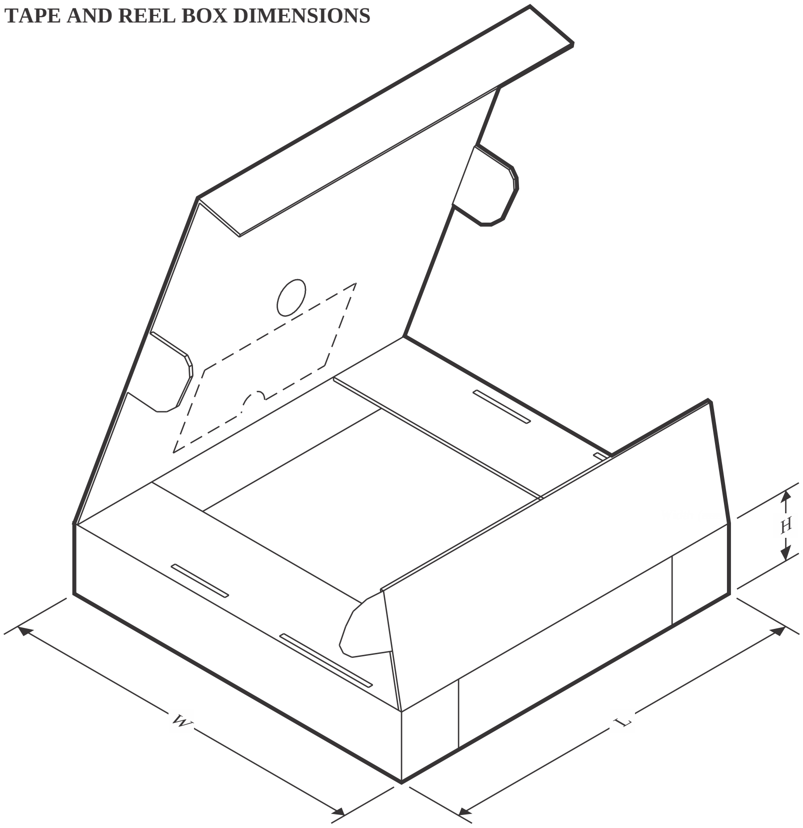
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALS259DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

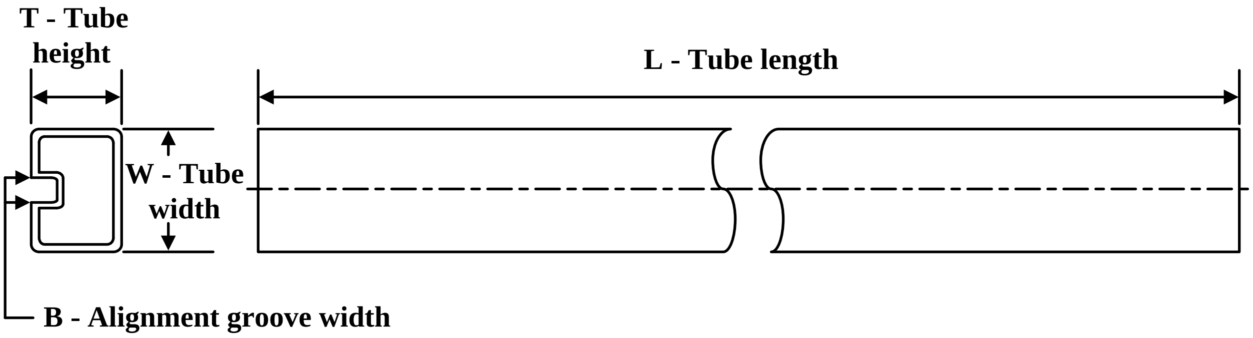
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ALS259DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |

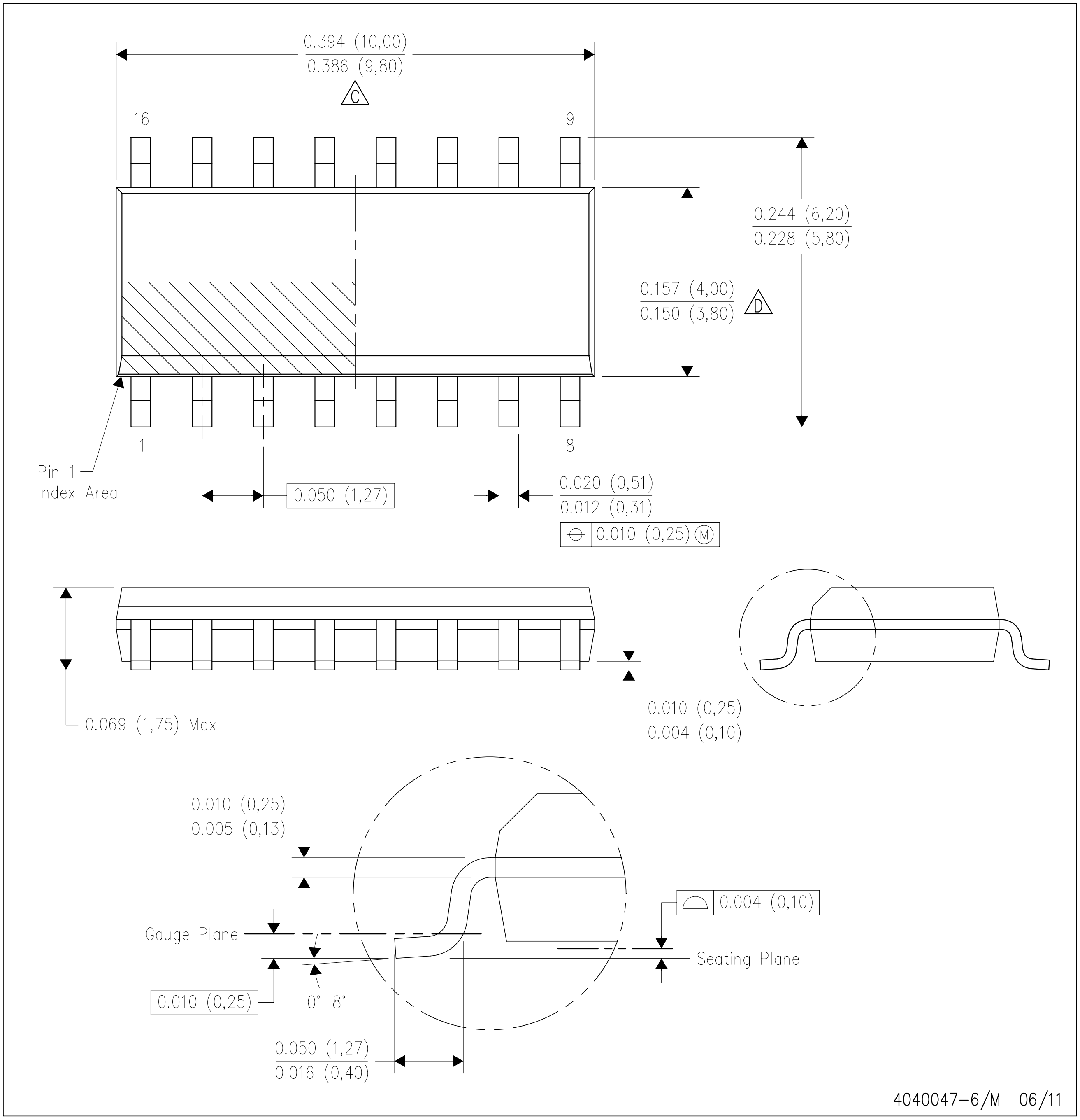
## TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74ALS259N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS259N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS259N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS259N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

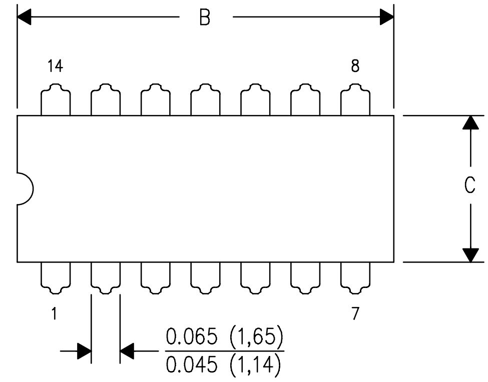
## D (R-PDSO-G16) PLASTIC SMALL OUTLINE



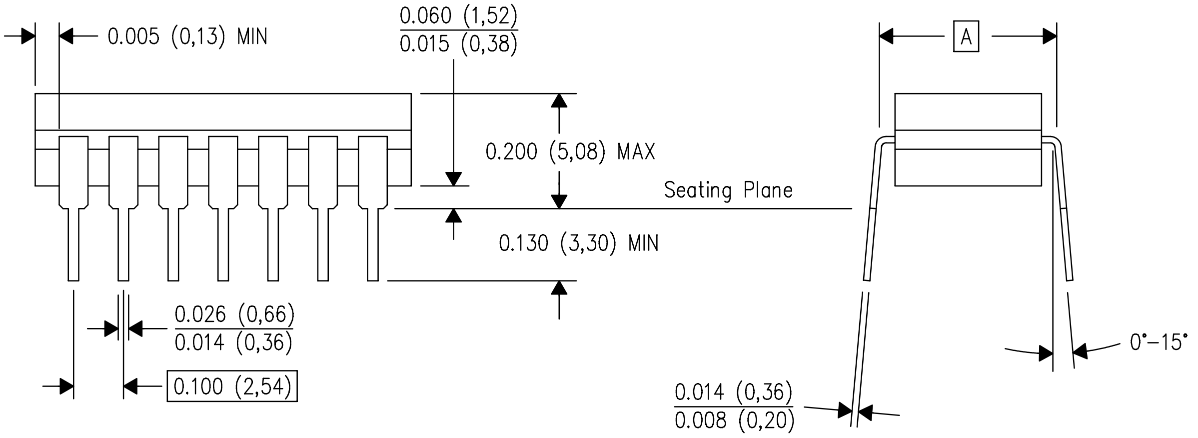
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

# J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX | 0.785<br>(19,94) | .840<br>(21,34) | 0.960<br>(24,38) | 1.060<br>(26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300<br>(7,62) | 0.300<br>(7,62) | 0.310<br>(7,87) | 0.300<br>(7,62) |
| C MIN | 0.245<br>(6,22) | 0.245<br>(6,22) | 0.220<br>(5,59) | 0.245<br>(6,22) |



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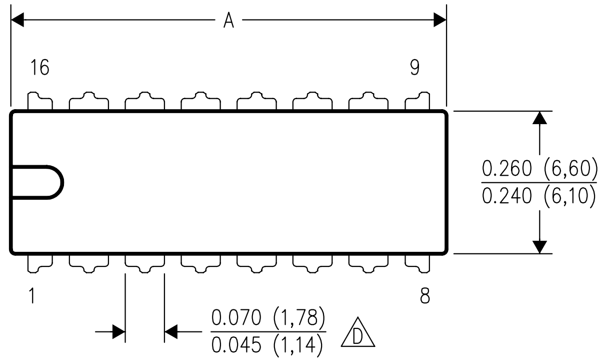
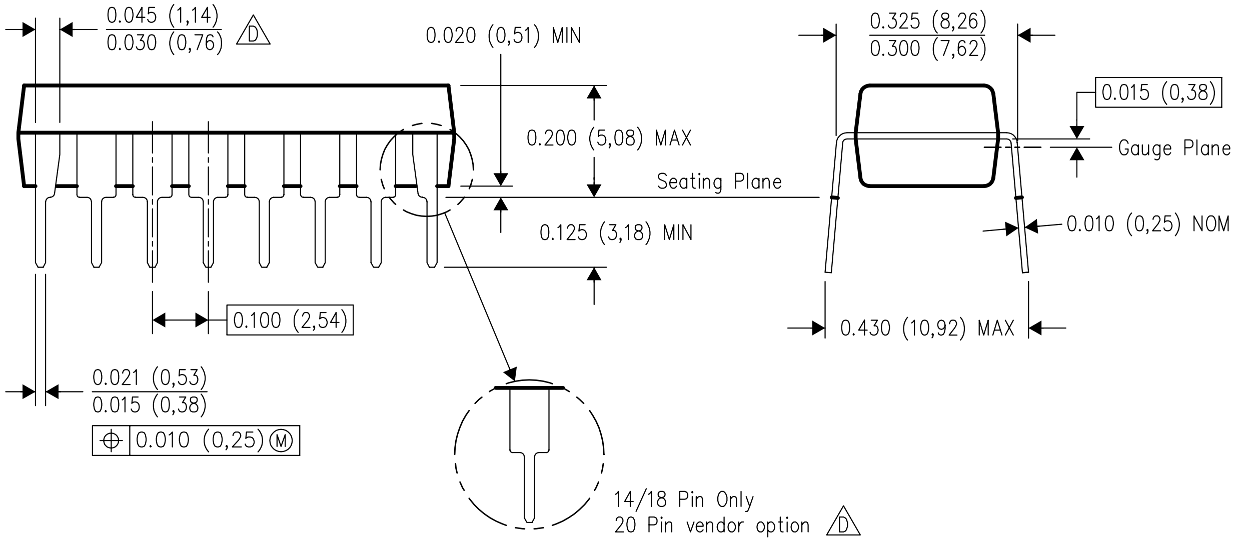
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



| PINS ** / DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| Ⓒ MS–001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Ⓒ Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- Ⓓ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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