CSD16340Q3 25-V N-Channel NexFET™ Power MOSFET

1 Features

- Optimized for 5 V Gate Drive
- Resistance Rated at V_{GS} =2.5 V
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

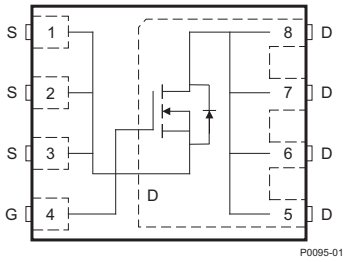
2 Applications

- Point of Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Control or Synchronous FET Applications

3 Description

This 25 V, 3.8 mΩ, 3.3 × 3.3 mm SON NexFET™ power MOSFET is designed to minimize losses in power conversion and optimized for 5 V gate drive applications.

Top View



Product Summary

T_A = 25°C		VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge Total (4.5 V)	6.5		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.2		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V	6.1	mΩ
		V_{GS} = 4.5 V	4.3	mΩ
		V_{GS} = 8 V	3.8	mΩ
V_{th}	Threshold Voltage	0.85		V

Ordering Information(1)

Device	Media	Qty	Package	Ship
CSD16340Q3	13-Inch Reel	2500	SON 3.3 x 3.3 mm Plastic Package	Tape and Reel
CSD16340Q3T	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

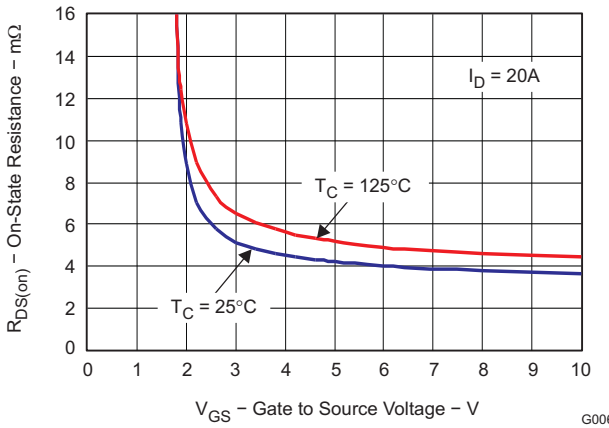
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	+10 / –8	V
I_D	Continuous Drain Current, T_C = 25°C	60	A
	Continuous Drain Current(1)	21	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	115	A
P_D	Power Dissipation(1)	3	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 40 A, L = 0.1 mH, R_G = 25 Ω	80	mJ

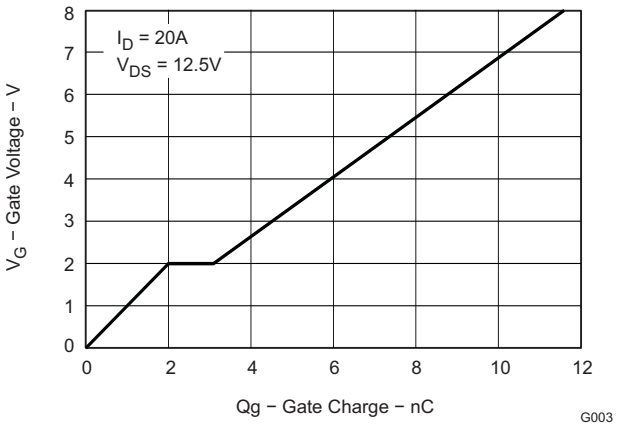
(1) Typical $R_{\theta JA}$ = 39°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300 µs, duty cycle ≤2%

$R_{DS(on)}$ vs V_{GS}



Gate Charge



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4 Revision History

Changes from Revision D (November 2011) to Revision E — **Page**

- Added 7" reel to Ordering Information ... 1
- Updated Mechanical Information ... 9

Changes from Revision C (June 2011) to Revision D — **Page**

- Replaced the THERMAL CHARACTERISTICS table with the new Thermal Information Table ... 4
- Replaced Figure 10 - Maximum Safe Operating Area ... 6

Changes from Revision B (September 2010) to Revision C — **Page**

- Deleted the Package Marking Information section ... 9

Changes from Revision A (January 2010) to Revision B — **Page**

- Changed Figure 2, reversed the order of the V_{GS} labels ... 5

Changes from Original (December 2009) to Revision A — **Page**

- Changed Q_g in the PRODUCT SUMMARY table from: 6.8 To 6.5 nC ... 1

5 Specifications

5.1 Electrical Characteristics

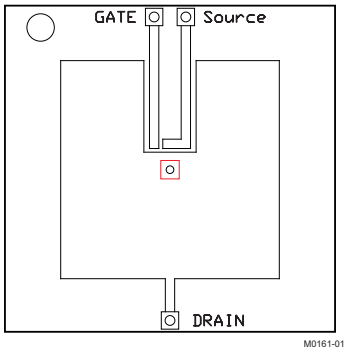
(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = 250 µA	25			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 20 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = +10/–8 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	0.6	0.85	1.1	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V, I_{DS} = 20 A		6.1	7.8	mΩ
		V_{GS} = 4.5 V, I_{DS} = 20 A		4.3	5.5	mΩ
		V_{GS} = 8 V, I_{DS} = 20 A		3.8	4.5	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 20 A		121		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		1050	1350	pF
C_{OSS}	Output Capacitance			730	950	pF
C_{RSS}	Reverse Transfer Capacitance			53	69	pF
R_g	Series Gate Resistance			1.5	3	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 12.5 V, I_D = 20 A		6.5	9.2	nC
Q_{gd}	Gate Charge Gate-to-Drain			1.2		nC
Q_{gs}	Gate Charge Gate-to-Source			2.1		nC
Qg(th)	Gate Charge at V_{th}			1		nC
Q_{OSS}	Output Charge	V_{DS} = 13 V, V_{GS} = 0 V		15		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 20 A, R_G = 2 Ω		4.8		ns
t_r	Rise Time			16.1		ns
$t_{d(off)}$	Turn Off Delay Time			13.8		ns
t_f	Fall Time			5.2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = 20 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 13 V, I_F = 20 A, di/dt = 300 A/µs		14.5		nC
t_{rr}	Reverse Recovery Time			20		ns

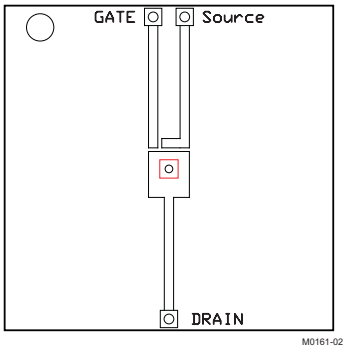
5.2 Thermal Information

THERMAL METRIC[1][2]		CSD16340Q3 Q3 (8 PINS)	UNITS
θ_{JA}	Junction-to-Ambient Thermal Resistance	42.0	°C/W
θ_{JCtop}	Junction-to-Case (top) Thermal Resistance	20.6	
θ_{JB}	Junction-to-Board Thermal Resistance	8.8	
ψ_{JT}	Junction-to-Top Characterization Parameter	0.3	
ψ_{JB}	Junction-to-Board Characterization Parameter	8.7	
θ_{JCbot}	Junction-to-Case (bottom) Thermal Resistance	0.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.



Max $R_{\theta JA}$ = 58°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 162°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

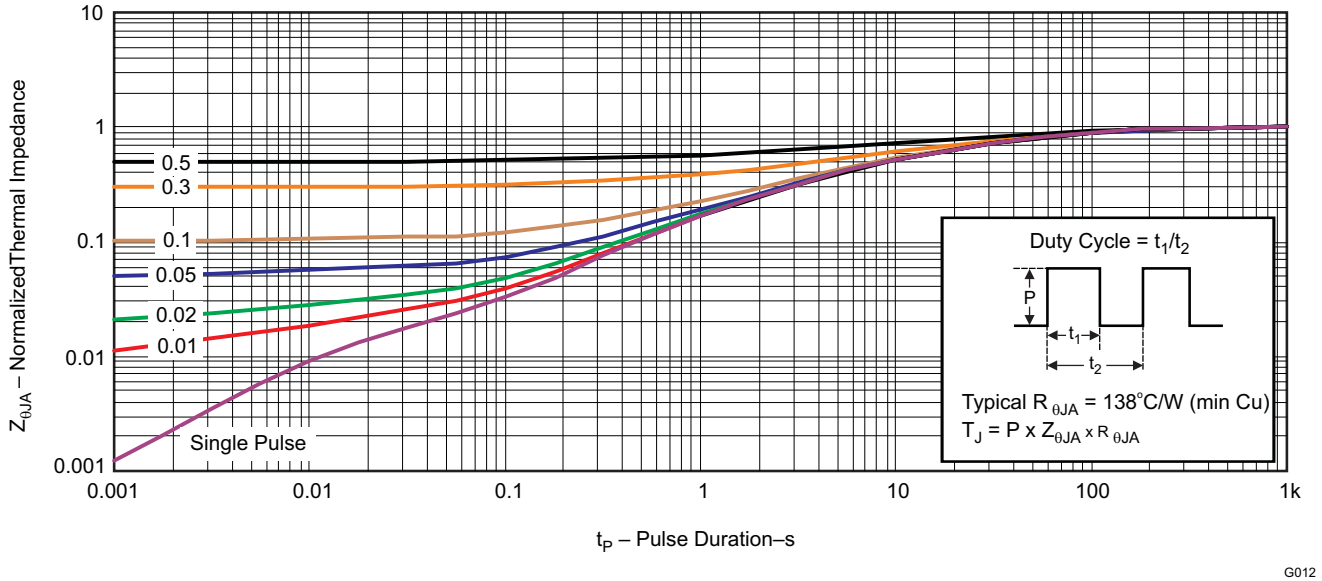


Figure 1. Transient Thermal Impedance

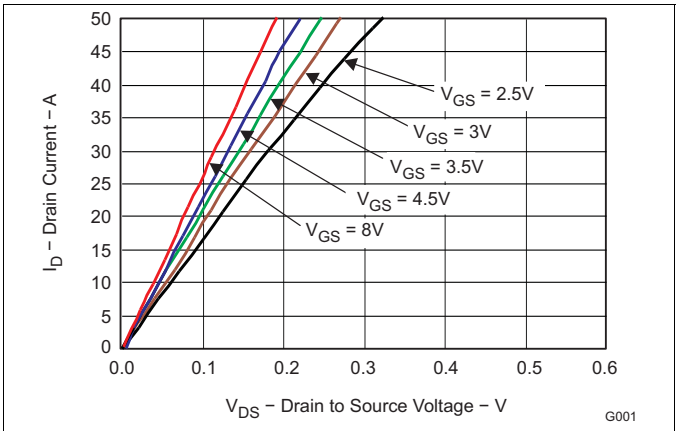


Figure 2. Saturation Characteristics

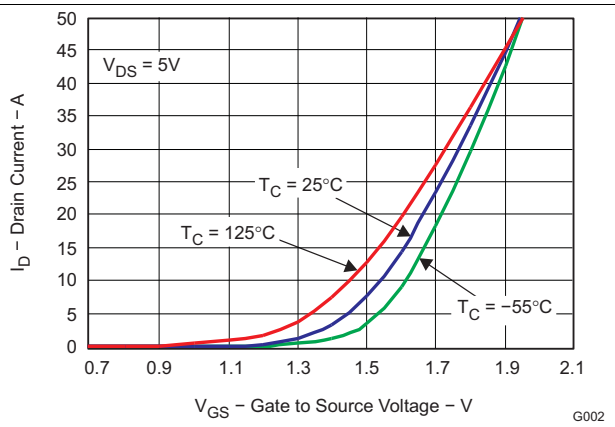


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

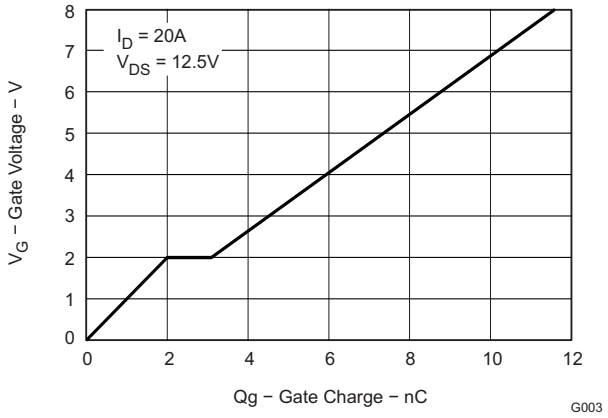


Figure 4. Gate Charge

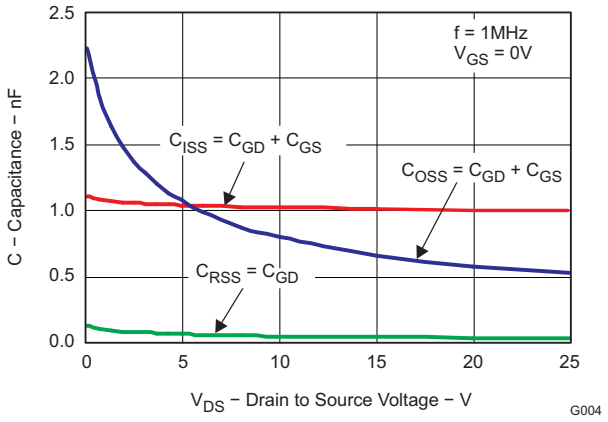


Figure 5. Capacitance

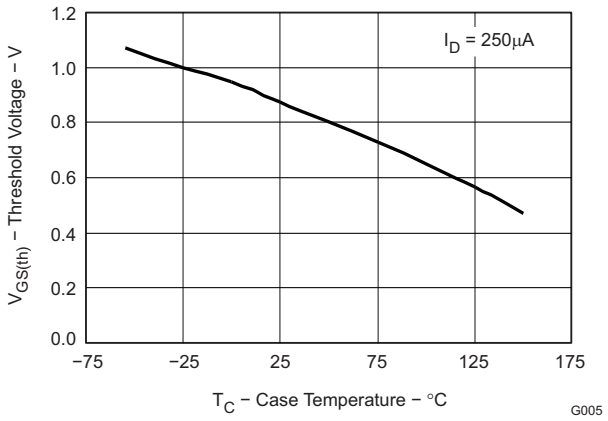


Figure 6. Threshold Voltage vs Temperature

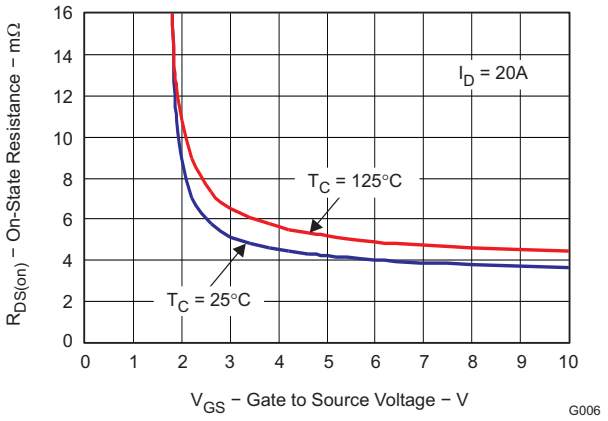


Figure 7. On-Resistance vs Gate Voltage

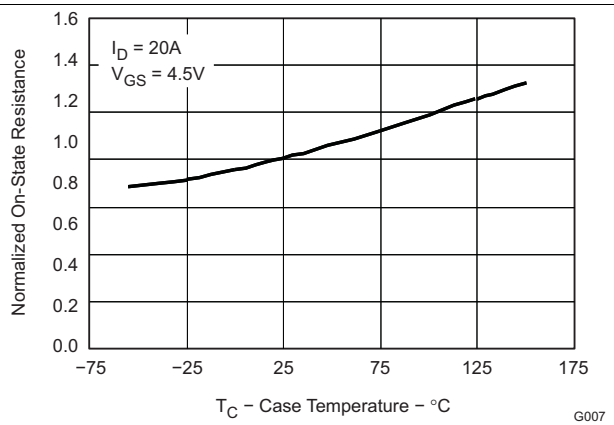


Figure 8. Normalized On Resistance vs Temperature

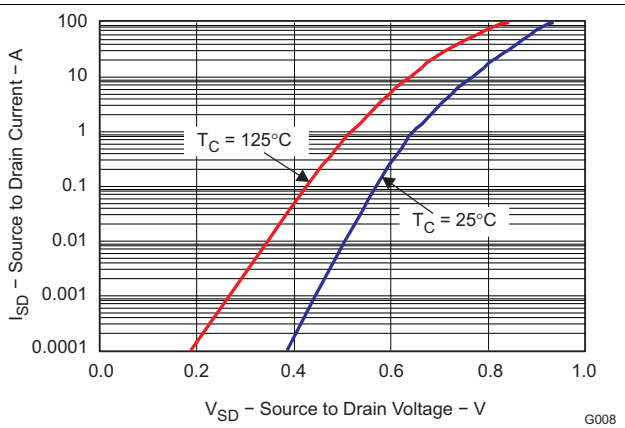


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

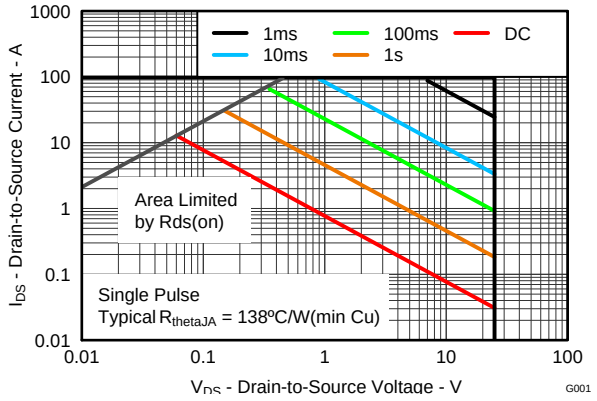


Figure 10. Maximum Safe Operating Area

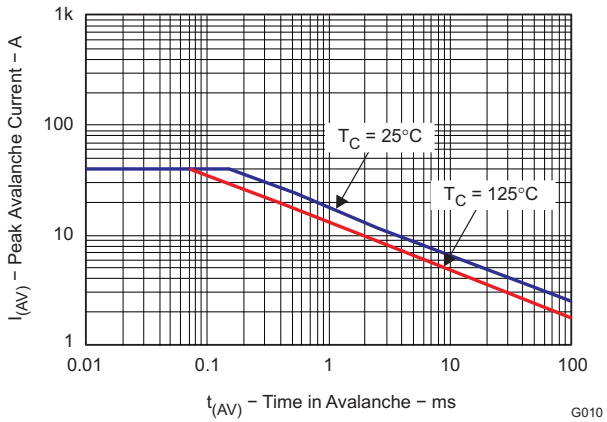


Figure 11. Single Pulse Unclamped Inductive Switching

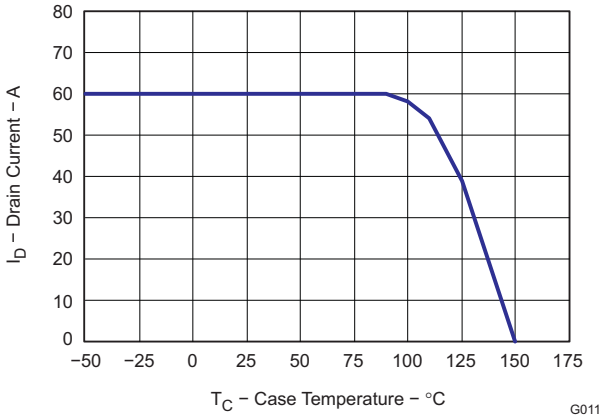


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

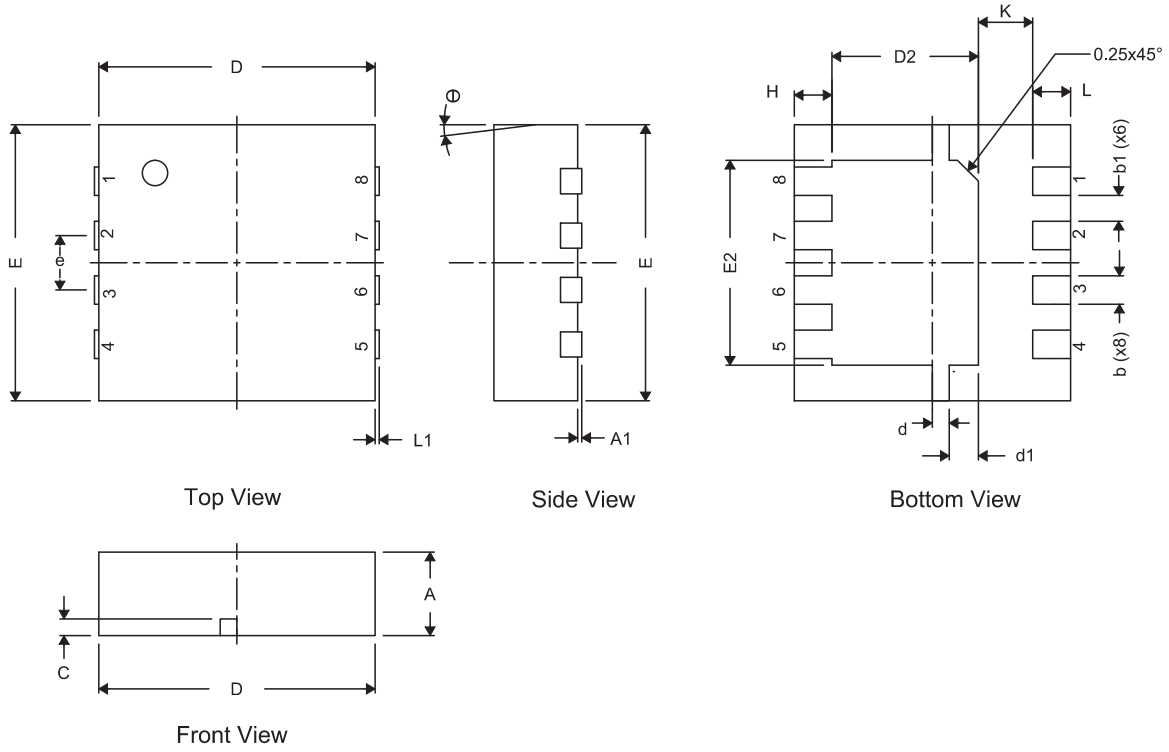
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

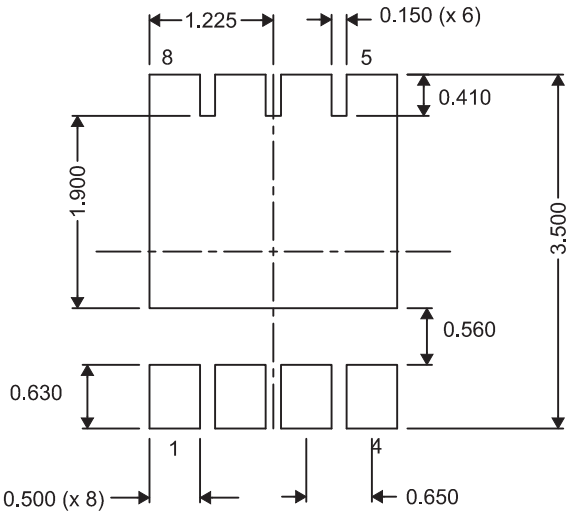
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



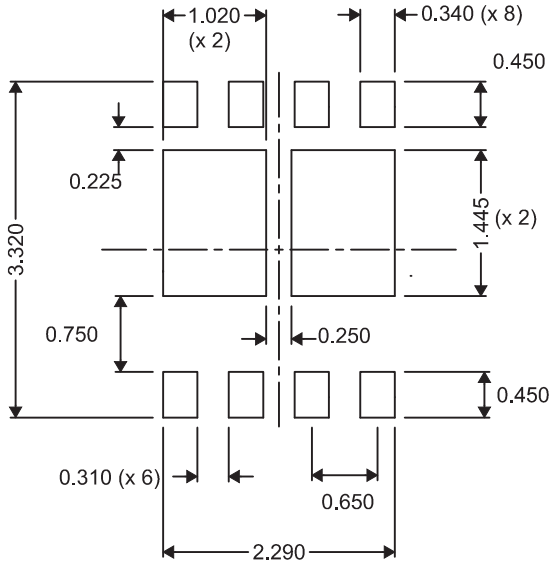
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1		0.310 NOM			0.012 NOM	
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e		0.650 TYP			0.026	
H	0.35	0.450	0.550	0.014	0.018	0.022
K		0.650 TYP			0.026 TYP	
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



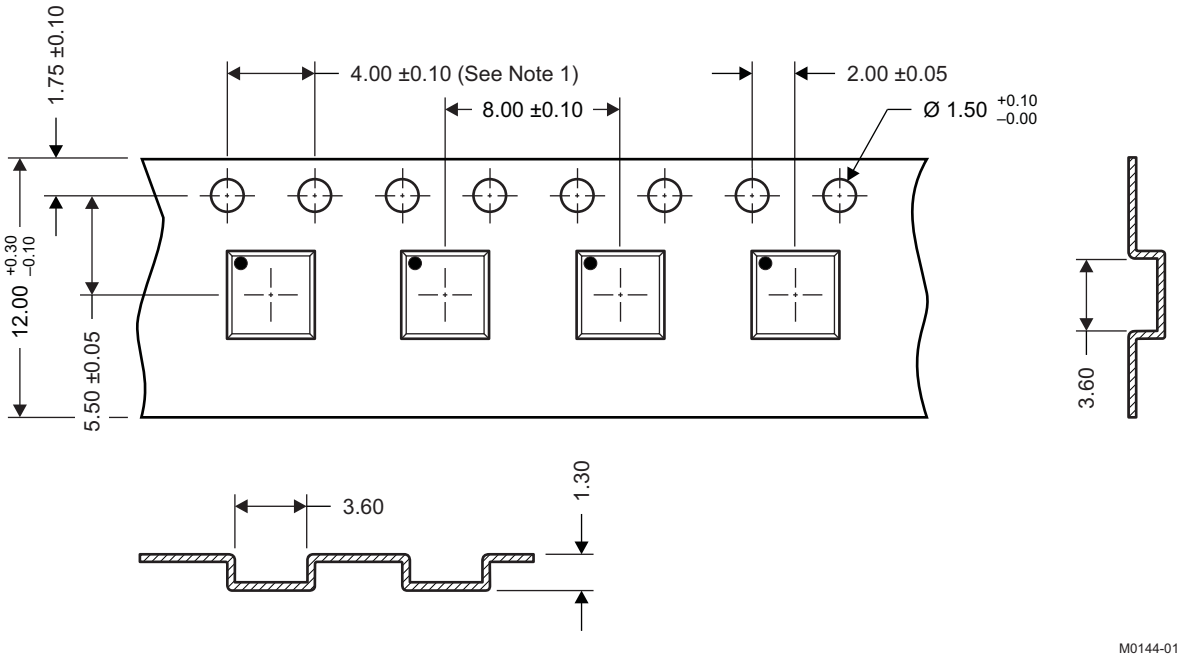
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ±0.05 mm
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16340Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 150	CSD16340	Samples
CSD16340Q3T	ACTIVE	VSON-CLIP	DQG	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 150	CSD16340	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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