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PCI to SD Memory Card / SmartMedia™  
Interface Controller  
**TC6371AF**

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Outline

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Rev. 1.8    2002-01-22

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**TOSHIBA CORPORATION**

## Revision history

TITLE: TC6371AF Specification

| REV NO. | DATE      | CONTENTS                                                                                                                                                                                    | Parts                             | REVISED    | APP'D    |
|---------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|------------|----------|
| 1.00    | '00-09-08 | Issued                                                                                                                                                                                      |                                   | S.Ueta     | T.Takada |
| 1.01    | '01-03-26 | Mentioned '5.2.PCI Interface DC Characteristics'.<br>Mentioned '5.3.1.PCI clock AC characteristics'.                                                                                        | Page 34<br>Page 40                | T.Murakami | T.Takada |
| 1.02    | '01-04-02 | Symbol 'Topr' is raised to 70°C from 60°C<br>Ta is changed to '0-70°C' from '0-60°C'                                                                                                        | Page 33<br>Page 35-52             | S.Ueta     | T.Takada |
| 1.03    | '01-04-18 | Recommended resistance of SDCD3 line is changed to 100 KΩPull-up from 510 KΩPull-down.<br>Added 4.11 item                                                                                   | Page 32<br><br>Page 33            | S.Ueta     | T.Takada |
| 1.04    | '01-04-25 | Low active signals are unified as #xxxx.<br>(ex. SDCD#→#SDCD)<br>Modified recommended resistance of SDCD3-0 and SDCMD case of MMC not supported.<br>(100KΩ→47KΩ)                            | Page 32                           | S.Ueta     | T.Takada |
| 1.1     | '01-05-17 | Modified a comment of [4.7 SUSPEND State ].<br>Modified recommended resistance of SDCD2-0 and SDCMD case of MMC not supported.<br>(47KΩ→100KΩ)<br>Added Current Dissipation Characteristics | Page 26<br>Page 32<br><br>Page 41 | S.Ueta     | T.Takada |
| 1.2     | '01-07-20 | Added [4.12 Processing Unused<br>Interface External Pins].<br>Modified recommended resistance of #SDCD and SDWP. (100KΩ→10KΩ)                                                               | Page 34-35<br><br>Page 32         | S.Ueta     | T.Takada |
| 1.3     | '01-08-17 | Added [6 Package outline].                                                                                                                                                                  | Page 56                           | S.Ueta     | T.Takada |
| 1.4     | '01-08-31 | Added SmartMedia DC spec. for #SMLOCK, #SMEJCT and #SMLED.                                                                                                                                  | Page 38                           | S.Ueta     | T.Takada |
| 1.5     | '01-09-03 | To be slimed files.                                                                                                                                                                         |                                   | S.Ueta     | T.Takada |
| 1.6     | '01-10-02 | Added the comment regarding Subsystem Vendor ID and Subsystem Device ID.                                                                                                                    | Page17,19                         | S.Ueta     | T.Takada |
| 1.61    | '01-11-09 | Corrected the written.                                                                                                                                                                      | Page17,19<br>(red letters)        | S.Ueta     | T.Takada |
| 1.62    | '01-11-26 | Corrected the written.                                                                                                                                                                      | Page27<br>(red letters)           | S.Ueta     | T.Takada |
| 1.7     | '02-01-09 | Regarding serial rom I/F, specified that only 4K bits serial rom be supported.<br>Added #SMLED signal specification.                                                                        | Page5<br>(red letters)<br>Page36  | S.Ueta     | T.Takada |
| 1.8     | '02-01-22 | Modified the explanation of CLK32 signal.<br><br>Added GPIO interface specification.                                                                                                        | Page21<br>(red letters)<br>Page36 | S.Ueta     | T.Takada |
|         |           |                                                                                                                                                                                             |                                   |            |          |

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## 1 Outline

The TC6371AF is an SD memory card/SmartMedia™ controller LSI with a 32-bit PCI bus interface. This product conforms to SD memory card physical layer specifications as well as to SmartMedia™ electrical and physical format specifications.

The TC6371AF can also be used with all power supplies for memory card interfaces. When the memory card is inserted, TC6371AF automatically detects the card type and the power supply in use. In addition to supporting a CLKRUN function and advanced configuration power interface (ACPI), the TC6371AF supports a PCI power management-compliant PME, giving the product fully developed power management functions that allow it to minimize the system's power dissipation.

With such features as subsystem ID and subsystem vendor ID supplied from external serial ROM, the TC6371AF can be used as a PCI card or CardBus card LSI.

### 1.1 Chip Specifications

- 0.35-μm CMOS process
- Number of gates: 80,000 approx.
- 0.4-mm pitch, 128-pin QFP package (LQFP128-P-1414B)

### 1.2 Low power dissipation

- Conforms to PCI power management specifications (Supports #PME \*)
- Supports CLOCKRUN (mobile PC/PCI)
- Internal gate clock design

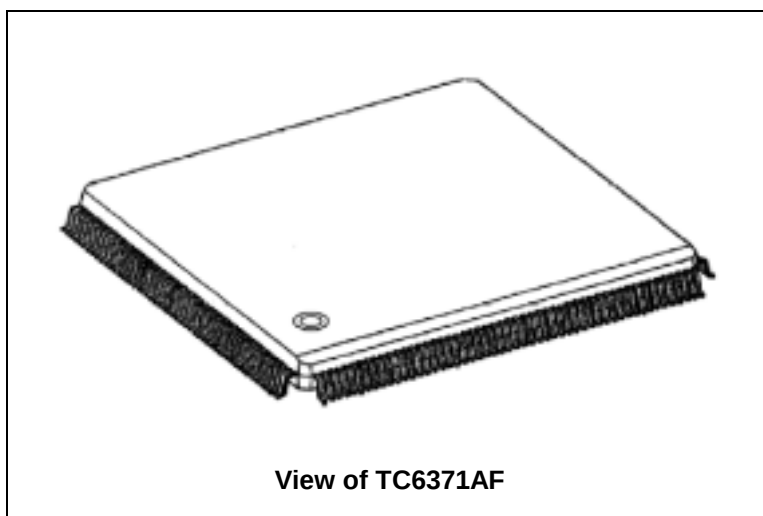
### 1.3 General Specifications

- Conforms to PCI power management specification revision 1.1
- Conforms to PCI local bus specification revision 2.2 \*
- Supports remote wakeup feature (#PME-compliant) \*\*
- Supports PCI interrupts (INT)
- Supports PCI CLKRUN
- Supports suspend state
- Supports Plug & Play
- Operating frequency: PCI (33 MHz max)
- Supports LSI MIC2563 which controls power supply
- Supports subsystem ID and subsystem vendor ID from 4k bits EEPROM (3-line serial ROM interface) (Only 4K bits EEPROM supports)
- Supports 3.3-V PCI interface
- Conforms to SD memory card physical layer specifications (ver. 1.0)
  - Operating frequency 16 MHz max
  - Offers Multimedia card read/write
  - Supports 3.3 V
  - Offers multi-block write/read
- Conforms to SmartMedia™ electrical specifications (ver. 1.20) and physical format specifications (ver. 1.20), supporting:
  - Supports 3.3-V SmartMedia™ (5.0 V not supported)
  - Supports hardware ECC

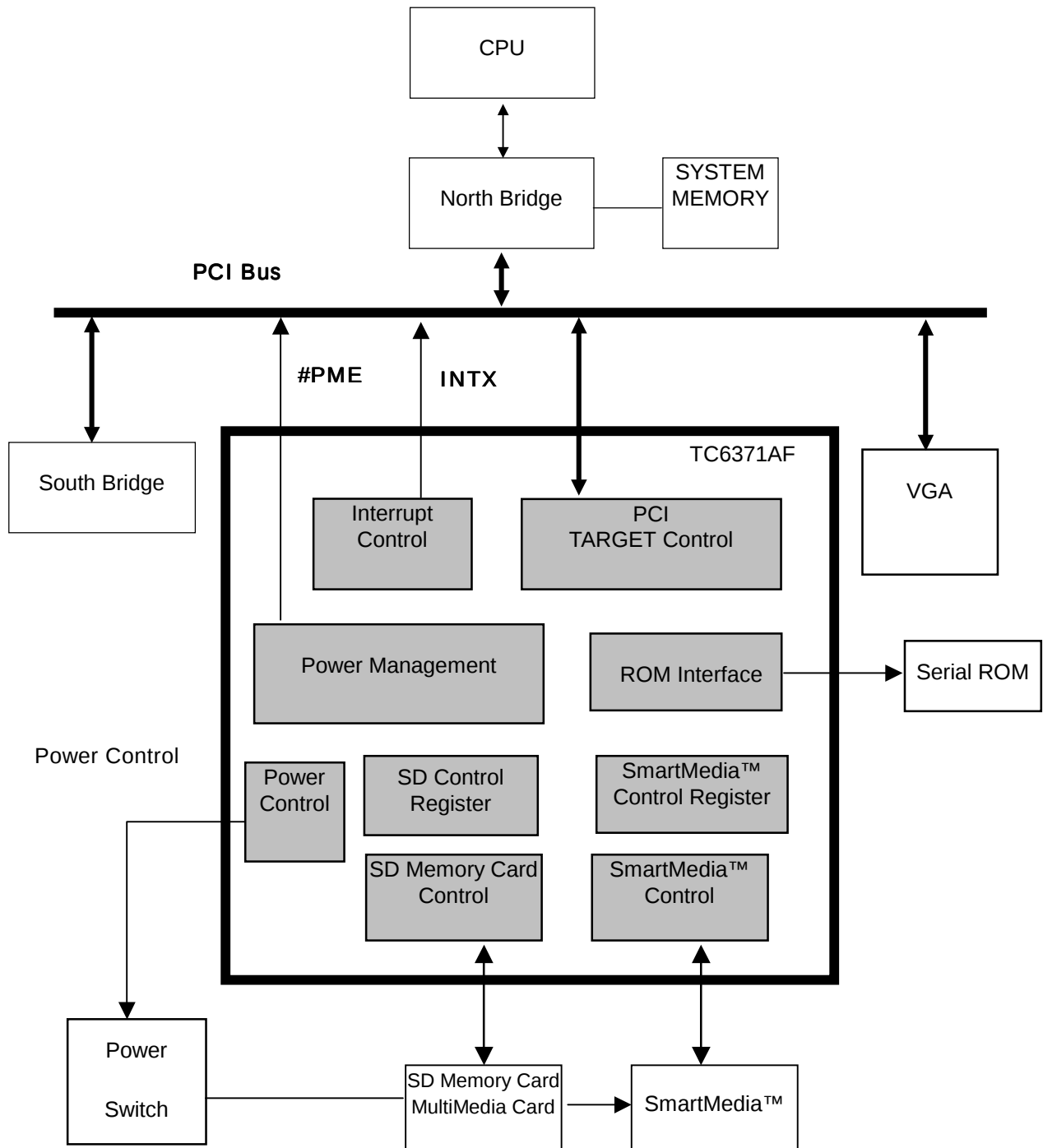
\* The minimum input voltage level of "PCICLK" "#PCIRST" shall not exceed 0.7 times of Vcc. Vih(min) = 0.7 \* Vcc

\*\* As of January, 2002, the SD/MMC/SmartMedia™ driver does not perform any functions by enabling #PME.

SmartMedia™ is a registered trademark of Toshiba Corporation.



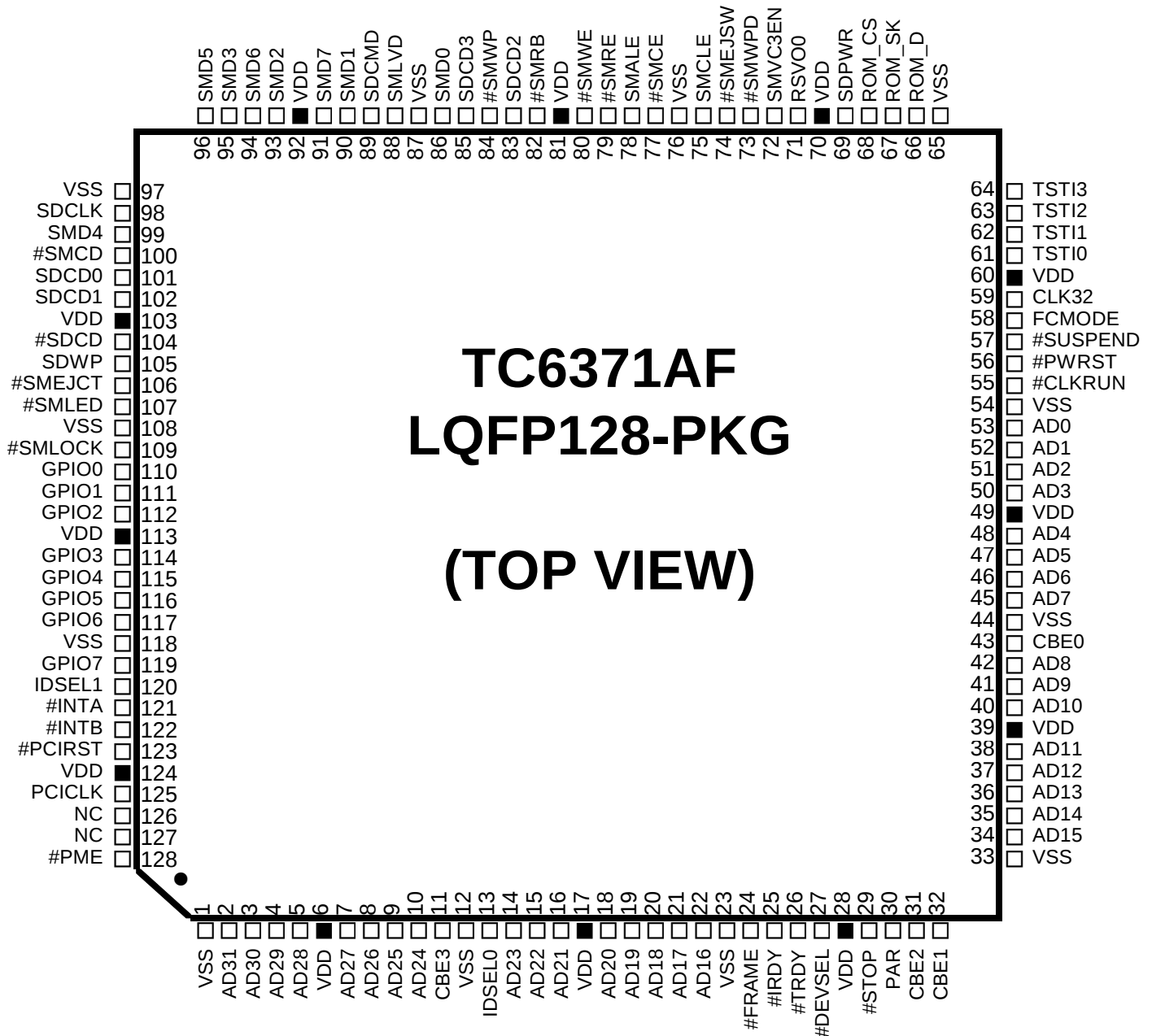
## 2 Block diagram



### 3 Signals

#### 3.1 Pin Assignments

QFP128 Matrix Diagram



## 3.2 Pin Signals

### PCI Interface (50-Pin)

| NAME  | Pin | IO | VCC (V) | FUNCTION                                                                                                                                                                                               |
|-------|-----|----|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AD31  | 2   | IO | 3.3     | PCI address/data bus                                                                                                                                                                                   |
| AD30  | 3   |    |         |                                                                                                                                                                                                        |
| AD29  | 4   |    |         |                                                                                                                                                                                                        |
| AD28  | 5   |    |         |                                                                                                                                                                                                        |
| AD27  | 7   |    |         |                                                                                                                                                                                                        |
| AD26  | 8   |    |         |                                                                                                                                                                                                        |
| AD25  | 9   |    |         |                                                                                                                                                                                                        |
| AD24  | 10  |    |         |                                                                                                                                                                                                        |
| AD23  | 14  |    |         |                                                                                                                                                                                                        |
| AD22  | 15  |    |         |                                                                                                                                                                                                        |
| AD21  | 16  |    |         |                                                                                                                                                                                                        |
| AD20  | 18  |    |         |                                                                                                                                                                                                        |
| AD19  | 19  |    |         |                                                                                                                                                                                                        |
| AD18  | 20  |    |         |                                                                                                                                                                                                        |
| AD17  | 21  |    |         |                                                                                                                                                                                                        |
| AD16  | 22  |    |         |                                                                                                                                                                                                        |
| AD15  | 34  |    |         |                                                                                                                                                                                                        |
| AD14  | 35  |    |         |                                                                                                                                                                                                        |
| AD13  | 36  |    |         |                                                                                                                                                                                                        |
| AD12  | 37  |    |         |                                                                                                                                                                                                        |
| AD11  | 38  |    |         |                                                                                                                                                                                                        |
| AD10  | 40  |    |         |                                                                                                                                                                                                        |
| AD9   | 41  |    |         |                                                                                                                                                                                                        |
| AD8   | 42  |    |         |                                                                                                                                                                                                        |
| AD7   | 45  |    |         |                                                                                                                                                                                                        |
| AD6   | 46  |    |         |                                                                                                                                                                                                        |
| AD5   | 47  |    |         |                                                                                                                                                                                                        |
| AD4   | 48  |    |         |                                                                                                                                                                                                        |
| AD3   | 50  |    |         |                                                                                                                                                                                                        |
| AD2   | 51  |    |         |                                                                                                                                                                                                        |
| AD1   | 52  |    |         |                                                                                                                                                                                                        |
| AD0   | 53  |    |         |                                                                                                                                                                                                        |
| #CBE3 | 11  | IO | 3.3     | PCI bus command/byte enable. Specifies bus commands at the PCI cycle address phase. Specifies the byte enable that indicates which byte lane of the 32 bits to use for sending data at the data phase. |
| #CBE2 | 31  |    |         |                                                                                                                                                                                                        |
| #CBE1 | 32  |    |         |                                                                                                                                                                                                        |
| #CBE0 | 43  |    |         |                                                                                                                                                                                                        |
| PAR   | 30  | O  | 3.3     | PCI bus parity. Parity bit for even-number parity checks on the PCI address/data bus and bus command line.                                                                                             |

**Pin Signals (Continued)****PCI Interface (Continued)**

| NAME    | Pin | IO           | VCC (V) | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                  |
|---------|-----|--------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #FRAME  | 24  | I            | 3.3     | PCI cycle frame. Driven by the initiator, this signal indicates that the bus cycle is in progress. When the signal is asserted, address and bus command output starts. When de-asserted, the signal indicates that the next data transfer phase is the final data transfer.                                                                                                               |
| #IRDY   | 25  | I            | 3.3     | Enables PCI initiator. Indicates that the initiator is ready for data transfer. The R/W data are transferred when signal asserted.                                                                                                                                                                                                                                                        |
| #TRDY   | 26  | O            | 3.3     | Enables PCI target. Indicates that the target is ready for data transfer. The R/W data are transferred when signal asserted.                                                                                                                                                                                                                                                              |
| #STOP   | 29  | O            | 3.3     | Terminates the PCI cycle. The target uses this signal to ask the initiator to terminate processing that is currently in progress. Supports three types of termination: retry/disconnect/target abort.                                                                                                                                                                                     |
| IDSEL0  | 13  | I            | 3.3     | Selects the PCI bus initialization device (ID). Asserted to specify the TC6371AF as the target device during a configuration access. This signal is used for SD card controller functions. When the FCMODE pin is set to H, this signal is used for the SD card/SmartMedia™ controller multifunction device feature.                                                                      |
| IDSEL1  | 120 | I            | 3.3     | Selects the PCI bus initialization device (ID). Asserted when the TC6371AF is specified as the target device during configuration access. This signal is used for SmartMedia™ controller functions. When the FCMODE pin is set to H, the TC6371AF operates as a multifunction device using IDSEL0 and therefore this signal does not function. (In Multifunction mode, pull up this pin.) |
| #CLKRUN | 55  | IO           | 3.3     | Runs the PCI clock. Can request a stop or slowdown of the PCI clock.                                                                                                                                                                                                                                                                                                                      |
| #DEVSEL | 27  | O            | 3.3     | Selects the PCI device. Asserted by the TC6371AF in response to bus access.                                                                                                                                                                                                                                                                                                               |
| PCICLK  | 125 | I            | 3.3     | PCI bus clock. Inputs a 33-MHz clock. All processing on the PCI bus is on the PCICLK rising edge.                                                                                                                                                                                                                                                                                         |
| #PCIRST | 123 | I            | 3.3     | Resets PCI bus. Asserted when power is turned on and or when system has been reset.                                                                                                                                                                                                                                                                                                       |
| #INTA   | 121 | O<br>(OD) *1 | 3.3     | PCI interrupt INTA.                                                                                                                                                                                                                                                                                                                                                                       |
| #INTB   | 122 | O<br>(OD) *1 | 3.3     | PCI interrupt INTB.                                                                                                                                                                                                                                                                                                                                                                       |
| #PME    | 128 | O<br>(OD) *1 | 3.3     | #PME interrupt signal                                                                                                                                                                                                                                                                                                                                                                     |

\*1: Level cannot be converted.

**Pin Signals (Continued)****SD Card Interface (8 pins)**

| NAME  | Pin | IO | VCC (V) | FUNCTION                                                   |
|-------|-----|----|---------|------------------------------------------------------------|
| SDCD3 | 85  | IO | 3.3     | SD card data bus                                           |
| SDCD2 | 83  |    |         |                                                            |
| SDCD1 | 102 |    |         |                                                            |
| SDCD0 | 101 |    |         |                                                            |
| SDCMD | 89  | IO | 3.3     | SD command                                                 |
| SDCLK | 98  | O  | 3.3     | SD card clock                                              |
| #SDCD | 104 | I  | 3.3     | SD card detection                                          |
| SDWP  | 105 | I  | 3.3     | SD card write-protect.<br>When H, SD card write-protected. |

**SD Card Power Supply Controller (One pin)**

| NAME  | Pin | IO | VCC (V) | FUNCTION                                               |
|-------|-----|----|---------|--------------------------------------------------------|
| SDPWR | 69  | O  | 3.3     | Controls SD card power supply.<br>3.3-V enable signal. |

**Pin Signals (Continued)****SmartMedia™ Interface (22 pins)**

| NAME    | Pin | IO         | VCC (V) | FUNCTION                                                                                                                                                                                                                                  |
|---------|-----|------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SMD7    | 91  | IO         | 3.3     | Data                                                                                                                                                                                                                                      |
| SMD6    | 94  |            |         |                                                                                                                                                                                                                                           |
| SMD5    | 96  |            |         |                                                                                                                                                                                                                                           |
| SMD4    | 99  |            |         |                                                                                                                                                                                                                                           |
| SMD3    | 95  |            |         |                                                                                                                                                                                                                                           |
| SMD2    | 93  |            |         |                                                                                                                                                                                                                                           |
| SMD1    | 90  |            |         |                                                                                                                                                                                                                                           |
| SMD0    | 86  |            |         |                                                                                                                                                                                                                                           |
| SMCLE   | 75  | O (3state) |         | Enables the command latch.                                                                                                                                                                                                                |
| SMALE   | 78  | O (3state) |         | Enables the address latch.                                                                                                                                                                                                                |
| #SMCE   | 77  | O (3state) |         | Enables the chip.                                                                                                                                                                                                                         |
| #SMWE   | 80  | O (3state) |         | Enables a write.                                                                                                                                                                                                                          |
| #SMRE   | 79  | O (3state) |         | Enables a read.                                                                                                                                                                                                                           |
| #SMWP   | 84  | O (3state) |         | Protects against write.                                                                                                                                                                                                                   |
| #SMRB   | 82  | I          |         | Busy                                                                                                                                                                                                                                      |
| #SMCD   | 100 | I          |         | Detects card.                                                                                                                                                                                                                             |
| SMLVD   | 88  | I          |         | Detects low voltage.                                                                                                                                                                                                                      |
| #SMWPD  | 73  | I          |         | Write-protection seal<br>When L, a write-protected media is inserted.                                                                                                                                                                     |
| #SMEJSW | 74  | I          |         | Ejects request.<br>When H, a media is inserted. When L, no media is inserted.<br>Changes detection control to one where L indicates a media is inserted by setting bit 7 of the SmartMedia™ host controller's configuration register 63h. |
| #SMLED  | 107 | O (OD) *1  |         | Turns on the LED.                                                                                                                                                                                                                         |
| #SMLOCK | 109 | O (OD) *1  |         | Lock mode                                                                                                                                                                                                                                 |
| #SMEJCT | 106 | O (OD) *1  |         | Eject response                                                                                                                                                                                                                            |

\*1: Level cannot be converted.

**SmartMedia™ Power Supply Control (2 pins)**

| NAME    | Pin | IO | VCC (V) | FUNCTION                                                |
|---------|-----|----|---------|---------------------------------------------------------|
| SMVC3EN | 72  | O  | 3.3     | Parallel power supply control. VCC 3.3 V enable signal. |
| RSVO0   | 71  | O  | 3.3     | Leave pin open.                                         |

**Pin Signals (Continued)****System Interface (4 pins)**

| NAME     | Pin | IO | VCC (V) | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------|-----|----|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK32    | 59  | I  | 3.3     | Detects card or allow interruptions when PCICLK stops.                                                                                                                                                                                                                                                                                                                                                                               |
| #PWRST   | 56  | I  | 3.3     | Power-on reset signal input.                                                                                                                                                                                                                                                                                                                                                                                                         |
| #SUSPEND | 57  | I  | 3.3     | When #SUSPEND is Low, prevents throughput of data input from the SD card and SmartMedia™. Control signals output from TC6371AF are controlled at non-active level.                                                                                                                                                                                                                                                                   |
| FCMODE   | 58  | I  | 3.3     | Function mode signal.<br>When the FCMODE pin is set to L, the TC6371AF operates as a single-function PCI device. (IDSEL0 is used for the SD card controller functions, IDSEL1 for the SmartMedia™ functions.)<br>When the FCMODE pin is set to H, TC6371AF operates as a multifunction device. (Only IDSEL0 is valid. FUNCTION0 controls the SD card controller functions; FUNCTION1 controls the SmartMedia™ controller functions.) |

**Serial ROM Interface (3 pins)**

| NAME   | Pin | IO | VCC (V) | FUNCTION                                                                                                                                                                                                                   |
|--------|-----|----|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ROM_CS | 68  | O  | 3.3     | Serial ROM interface: Chip selection<br>Connect to serial ROM chip select (CS) pin.<br>Set TSTI[3-0] to be "0010" when the serial ROM interface applied.<br>Leave the pin open when the serial ROM interface not applied,. |
| ROM_SK | 67  | O  | 3.3     | Serial ROM interface: Clock<br>Connect to serial ROM clock pin (SK).<br>Leave the pin open when the serial ROM interface not applied.                                                                                      |
| ROM_D  | 66  | IO | 3.3     | Serial ROM interface: Data<br>Connect to the serial ROM data input/output pin.<br>Pull up the pin with a 100-kΩ resistor when the serial ROM interface not applied.                                                        |

## GPIO Interface (8 pins)

| NAME  | Pin | IO | VCC (V) | FUNCTION                                                                                                                                                                                        |
|-------|-----|----|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO0 | 110 | IO | 3.3     | General-purpose port 0.<br>Pull up this pin.                                                                                                                                                    |
| GPIO1 | 111 | IO | 3.3     | General-purpose port 1.<br>Pull up this pin.                                                                                                                                                    |
| GPIO2 | 112 | IO | 3.3     | General-purpose port 2.<br>Set to Low when 8-bit ROM selected or set to High when 16-bit ROM selected in ROM interface mode.<br>Pull up this pin .when the serial ROM interface is not applied, |
| GPIO3 | 114 | IO | 3.3     | General-purpose port 3.<br>Pull up this pin.                                                                                                                                                    |
| GPIO4 | 115 | I  | 3.3     | General-purpose port 4.<br>Set to Low.                                                                                                                                                          |
| GPIO5 | 116 | I  | 3.3     | General-purpose port 5.<br>Set to High.                                                                                                                                                         |
| GPIO6 | 117 | I  | 3.3     | General-purpose port 6.<br>Set to Low.                                                                                                                                                          |
| GPIO7 | 119 | I  | 3.3     | General-purpose port 7.<br>Set to Low.                                                                                                                                                          |

**Pin Signals (Continued)****Test Pins (4 pins)**

| NAME  | Pin | IO | VCC (V) | FUNCTION                                                                                                                                                             |
|-------|-----|----|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TSTI0 | 61  | I  | 3.3     | Test mode signals 3, 2, 1, 0<br>Used in Test mode.<br>Set TSTI[3-0] to "0000" in normal operating mode. Set TSTI[3-0] to "0010" when using the serial ROM interface. |
| TSTI1 | 62  |    |         |                                                                                                                                                                      |
| TSTI2 | 63  |    |         |                                                                                                                                                                      |
| TSTI3 | 64  |    |         |                                                                                                                                                                      |

**3.3 Power Supply, GND, and NC Pins (26)**

| NAME | Pin                                              | FUNCTION       |
|------|--------------------------------------------------|----------------|
| VSS  | 1, 12, 23, 33, 44, 54, 65, 76, 87, 97, 108, 118  | GND            |
| VDD  | 6, 17, 28, 39, 49, 60, 70, 81, 92, 103, 113, 124 | 3.3V           |
| NC   | 126, 127                                         | Not connected. |

**3.4 Interface Pin Summary**

| Interface                        |                  | Number of pins | Remarks                                                           |
|----------------------------------|------------------|----------------|-------------------------------------------------------------------|
| PCI                              |                  | 50             |                                                                   |
| SD card                          |                  | 8              |                                                                   |
| SD card power supply control     |                  | 1              |                                                                   |
| SmartMedia™                      |                  | 22             |                                                                   |
| SmartMedia™ power supply control |                  | 2              |                                                                   |
| System                           |                  | 19             | System interface, Serial ROM interface, GPIO interface, TEST pins |
|                                  | <b>Sub total</b> | 103            |                                                                   |
| Power supply                     |                  | 12             |                                                                   |
| GND                              |                  | 12             |                                                                   |
| Not connected (NC)               |                  | 2              | Leave open.                                                       |
|                                  | <b>Total</b>     | 128            |                                                                   |

## 4 Description of Functions

### 4.1 PCI Device Interface

- Address decode timing Medium
- Delayed transaction Supported
- LOCK# Not supported
- PERR#, SERR# Not supported
- Resource space

#### 4.1.1 Resource Space

The TC6371AF has the following resource space:

- SD host controller configuration register space
- SD control register space
- SmartMedia™ host controller configuration register space
- SmartMedia™ control register space

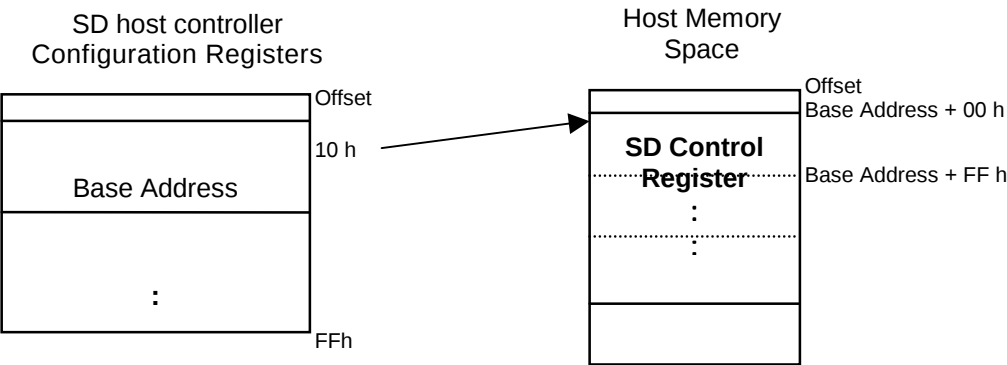
SD host controller /SmartMedia™ host controller configuration register space

The configuration space of the host controllers is set by external pins IDSEL0, IDSEL1, and FCMODE.

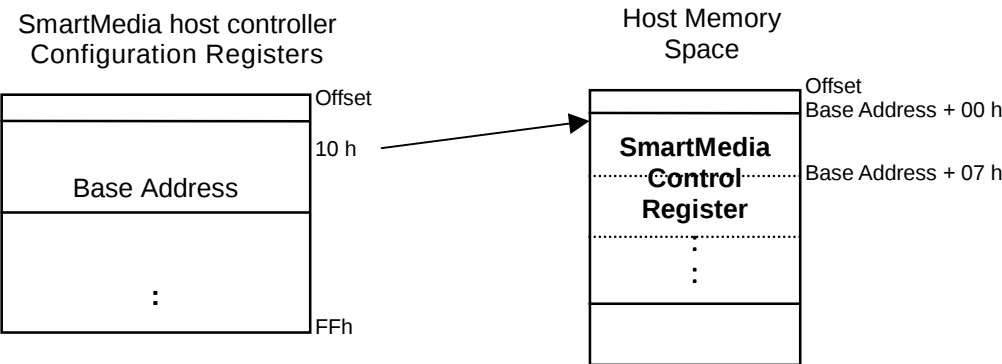
| FCMODE pin                | SD host controller<br>configuration register space                            | SmartMedia™ host controller<br>configuration register space                   |
|---------------------------|-------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
| 0<br>Single-function mode | Determined by IDSEL0<br>Header-type 00h                                       | Determined by IDSEL1<br>Header-type 00h                                       |
| 1<br>Multifunction mode   | Determined by IDSEL0<br>FUNCTION No. 0<br>Header-type 80h<br>IDSEL1 pulled up | Determined by IDSEL0<br>FUNCTION No. 1<br>Header-type 80h<br>IDSEL1 pulled up |

Note: When using only either the SD host controller function or the SmartMedia™ host controller function in systems using the TC6371AF, set Single-Function mode and mask the configuration space of the host controller you don't need.

- SD Control Register Space  
Use the base address register (config offset: 10h) of the SD host controller's configuration register for accessing the resources in the SD control register space. This allows you to set the SD control register space to any memory space. However, the SD control register space cannot be set to I/O resource space.



- SmartMedia™ Control Register Space  
Use the base address register (config offset: 10h) of the SmartMedia™ host controller's configuration register for accessing the resources in the SmartMedia™ control register space. This allows you to set SmartMedia™ control register space to any memory or I/O space.



## 4.2 Register Map

The TC6371AF incorporates an SD host controller registers and a SmartMedia™ host controller registers.

- SD host controller configuration register
- SD control register
- SmartMedia™ host controller configuration register
- SmartMedia™ control register

### 4.2.1 SD Host Controller Configuration Register

| 31                                  | 23                                          | 15                                      | 07                    | 00 | Port    |
|-------------------------------------|---------------------------------------------|-----------------------------------------|-----------------------|----|---------|
| Device ID (0803h)                   |                                             | Vendor ID (1179h)                       |                       |    | 00h     |
| Status (0210h)                      |                                             | Command (0000h)                         |                       |    | 04h     |
| Class Code (088000h)                |                                             |                                         | Revision ID (02h)     |    | 08h     |
|                                     | Header Type                                 |                                         | Cache Line Size       |    | 0Ch     |
| SD Card Register Base Address       |                                             |                                         |                       |    | 10h     |
|                                     |                                             |                                         |                       |    | 14h-27h |
|                                     |                                             |                                         | CISPT                 |    | 28h     |
| Subsystem Device ID (0001h) *1      |                                             | Subsystem Vendor ID (1179h) *1          |                       |    | 2Ch     |
|                                     |                                             |                                         |                       |    | 30h     |
|                                     |                                             |                                         | Capability Pointer    |    | 34h     |
|                                     |                                             |                                         |                       |    | 38h     |
|                                     |                                             | Interrupt Pin                           | Interrupt Line        |    | 3Ch     |
|                                     | SD Clock Mode                               | PCI Clock Control                       | Gated Clock Control   |    | 40h     |
|                                     |                                             | Pin Status                              |                       |    | 44h     |
|                                     |                                             |                                         | *2 Power Control      |    | 48h     |
|                                     | Card Detect Reset                           |                                         | *2 Card Detect Mode   |    | 4Ch     |
|                                     |                                             |                                         |                       |    | 50h-7Fh |
| Power Management Capabilities (PMC) |                                             | Next Item Ptr                           | Capability ID         |    | 80h     |
| Data                                | PMCSR PCI to PCI Bridge Support (PMCSR_BSE) | Power Management Control/Status (PMCSR) |                       |    | 84h     |
|                                     |                                             |                                         | *2 PME Trigger Enable |    | 88h     |
|                                     |                                             |                                         |                       |    | 8Ch-9Fh |
| *2 CIS                              |                                             |                                         |                       |    | A0h-EFh |
|                                     |                                             |                                         |                       |    | F0h-F7h |
|                                     |                                             |                                         | TEST                  |    | F8h     |
| Single Function                     |                                             | *2 PM Write Protect                     | Write Protect         |    | FCh     |

\*1: Regarding Subsystem Vendor ID and Subsystem Device ID, the default values of these register are The TOSHIBA's ID. In the case of using TC6371AF, please set these register to your ID. Please set your ID by BIOS as followings.

- (1) Set 01h to Write Protect Register(Config.FCh).
- (2) Set your ID to Subsystem Vendor ID and Subsystem Device ID Register.
- (3) Set 00h to Write Protect Register(Config.FCh).

\*2: PME context register

## 4.2.2 SD Control Register

| Offset          | 15-08 bit | 07-00 bit     | Offset          | 15-08 bit | 07-00 bit    |
|-----------------|-----------|---------------|-----------------|-----------|--------------|
| 02h             |           | SD_PORT       | 00h             |           | SD_CMD       |
| 06h             |           | SD_ARG1       | 04h             |           | SD_ARG0      |
| 0Ah             |           | SD_LENGTH     | 08h             |           | SD_STOP      |
| 0Eh             |           | SD_RSP1       | 0Ch             |           | SD_RSP0      |
| 12h             |           | SD_RSP3       | 10h             |           | SD_RSP2      |
| 16h             |           | SD_RSP5       | 14h             |           | SD_RSP4      |
| 1Ah             |           | SD_RSP7       | 18h             |           | SD_RSP6      |
| 1Eh             |           | SD_INFO2      | 1Ch             |           | SD_INFO      |
| 22h             |           | SD_INFO2_MASK | 20h             |           | SD_INFO_MASK |
| 26h             |           | SD_WIDTH      | 24h             |           | SD_CLK       |
| 2Ah             |           | ---           | 28h             |           | SD_OPTION    |
| 2Eh             |           | ---           | 2Ch             |           | ---          |
| 32h             |           | SD_BUF1       | 30h             |           | SD_BUF0      |
| 36h             |           | ---           | 34h             |           | ---          |
| 3Ah             |           | ---           | 38h             |           | ---          |
| 3Eh             |           | ---           | 3Ch             |           | ---          |
| 42h             |           | ---           | 40h             |           | ---          |
| 46h             |           | ---           | 44h             |           | ---          |
| 4Ah             |           | ---           | 48h             |           | ---          |
| 4Eh             |           | ---           | 4Ch             |           | ---          |
| 52h             |           | ---           | 50h             |           | ---          |
| 56h             |           | ---           | 54h             |           | ---          |
| 5Ah             |           | ---           | 58h             |           | ---          |
| 5Eh             |           | ---           | 5Ch             |           | ---          |
| 62h<br> <br>7Eh |           | ---           | 60h<br> <br>7Ch |           | ---          |
| 82h             |           | ---           | 80h             |           | ---          |
| 86h             |           | ---           | 84h             |           | ---          |
| 8Ah             |           | ---           | 88h             |           | ---          |
| 8Eh             |           | ---           | 8Ch             |           | ---          |
| 92h             |           | ---           | 90h             |           | ---          |
| 96h             |           | ---           | 94h             |           | ---          |
| 9Ah             |           | ---           | 98h             |           | ---          |
| 9Eh             |           | ---           | 9Ch             |           | ---          |
| A2h             |           | ---           | A0h             |           | ---          |
| A6h             |           | ---           | A4h             |           | ---          |
| AAh             |           | ---           | A8h             |           | ---          |
| AEh             |           | ---           | ACh             |           | ---          |
| B2h             |           | ---           | B0h             |           | ---          |
| B6h             |           | ---           | B4h             |           | ---          |
| BAh             |           | ---           | B8h             |           | ---          |
| BEh             |           | ---           | BCh             |           | ---          |
| C2h<br> <br>DEh |           | ---           | C0h<br> <br>DCh |           | ---          |
| E2h             |           | CORE_REV      | E0h             |           | SOFT_RST     |
| E6h             |           | BUF_ADR       | E4h             |           | ---          |
| EAh             |           | ---           | <b>E8h</b>      |           | Resp_Header  |
| EEh             |           | ---           | ECh             |           | ---          |
| F2h             |           | ---           | F0h             |           | ---          |
| F6h             |           | ---           | F4h             |           | ---          |
| FAh             |           | ---           | F8h             |           | ---          |
| FEh             |           | Revision      | FCh             |           | ---          |

## 4.2.3 SmartMedia™ Host Controller Configuration Register

| 31                                           | 23                                             | 15                                         | 07                                 | 00                | Port    |
|----------------------------------------------|------------------------------------------------|--------------------------------------------|------------------------------------|-------------------|---------|
| Device ID (0804h)                            |                                                | Vendor ID (1179h)                          |                                    |                   | 00h     |
| Status (0490h)                               |                                                | Command (0000h)                            |                                    |                   | 04h     |
| Class Code (088000h)                         |                                                |                                            |                                    | Revision ID (02h) | 08h     |
|                                              | Header Type                                    |                                            |                                    |                   | 0Ch     |
| SmartMedia™ Controller Register Base Address |                                                |                                            |                                    |                   | 10h     |
|                                              |                                                |                                            |                                    |                   | 14h-27h |
| CIS Pointer                                  |                                                |                                            |                                    |                   | 28h     |
| Subsystem Device ID(0001h)                   |                                                | Subsystem Vendor ID(1179h)                 |                                    |                   | 2Ch     |
|                                              |                                                |                                            |                                    |                   | 30h     |
|                                              |                                                |                                            | Capability Pointer                 |                   | 34h     |
|                                              |                                                |                                            |                                    |                   | 38h     |
|                                              |                                                | Interrupt Pin                              | Interrupt Line                     |                   | 3Ch     |
|                                              |                                                |                                            |                                    |                   | 40h-47h |
|                                              | *2 Event Control                               | *2 PME Enable                              | *2 INT Enable                      |                   | 48h     |
|                                              |                                                |                                            | *2 CLKRUN Control                  |                   | 4Ch     |
|                                              |                                                |                                            |                                    |                   | 50h-57h |
| *2 Debug                                     |                                                |                                            |                                    |                   | 58h     |
|                                              |                                                |                                            |                                    |                   | 5Ch-5Fh |
| *2 SmartMedia™ Detect Control                | *2 SmartMedia™ Power Supply Control            |                                            | *2 SmartMedia™ Transaction Control |                   | 60h     |
|                                              |                                                |                                            |                                    |                   | 64h-7Fh |
| *2 Power Management Capabilities (PMC)       |                                                | *2 Next Item Ptr                           | *2 Capability ID                   |                   | 80h     |
| *2 Data                                      | *2 PMCSR PCI to PCI Bridge Support (PMCSR_BSE) | *2 Power Management Control/Status (PMCSR) |                                    |                   | 84h     |
|                                              |                                                |                                            |                                    |                   | 88h-9Fh |
| *2 CIS                                       |                                                |                                            |                                    |                   | A0h-EFh |
| *2 ROM Control                               | *2 ROM Index Port                              | *2 ROM Data Port                           |                                    |                   | F0h     |
|                                              |                                                |                                            |                                    |                   | F4h-FBh |
| *2 Monitor Select                            |                                                |                                            | *2 Configuration Control           |                   | FCh     |

\*1:Regarding Subsystem Vendor ID and Subsystem Device ID, the default values of these register are The TOSHIBA's ID. In the case of using TC6371AF, please set these register to your ID. Please set your ID by BIOS as followings.

- (1) Set 01h to Configuration Control Register(Config.FCh).
- (2) Set your ID to Subsystem Vendor ID and Subsystem Device ID Register.
- (3) Set 00h to Configuration Control Register(Config.FCh).

\*2: PME context register

#### 4.2.4 SmartMedia™ Control Register

| Config-60h<br>bit4=1 | Config-60h<br>bit4=0 | Register name              | R/W    |
|----------------------|----------------------|----------------------------|--------|
| Offset1              | Offset2              |                            |        |
| 00h                  | 03h-00h              | Data Register              | RW     |
| 01h                  | -                    | Reserved                   | -      |
| 02h(Write)           | 04h(Read/Write)      | *Mode Register             | W(R/W) |
| 02h(Read)            | 05h                  | *Status Register           | R      |
| 04h                  | 06h                  | *Interrupt Status Register | R      |
| 06h                  | 07h                  | *Interrupt Mask Register   | RW     |
| 03h, 05h, 07h        | -                    | Reserved                   | -      |

\* PME context register

The offset of this register set varies according to the status of the bit that controls the SmartMedia™ control register's High-Speed mode (config 60h bit 4). (Setting bit 4 = 0 enables 32/16-bit access to the data register.)

## 4.3 Clock / Reset

### 4.3.1 Clocks

The TC6371AF has two pins for input clocks: PCICLK and CLK32.

- (1) PCICLK: PCI clock input (33 MHz max)  
PCI interface and internal operation reference clock.
- (2) CLK32: 32-kHz clock input  
Used as detecting insertion and removal of SD card and SmartMedia and an interrupt detection clock and for event detection in D3 state. The interrupt signal, implied insertion or detachment, shall be generated synchronous to this clock signal. Note that if CLK32 is stopped, the interrupt detector does not operate while TC6371AF is suspended or in D1-3 state set according to the PCI bus power management interface specifications.

### 4.3.2 Reset

The TC6371AF uses the following two reset signals.

- (1) #PCIRST: PCI reset signal. Asserted at power on and at a transition to D3cold. When the input destination of this signal is set to D3 state, the contents of the context register are saved and not cleared even when #PCIRST is asserted.
- (2) #PWRST: Power-on reset signal. Asserted at power on. Asserting #PWRST clears all the TC6371AF's internal registers.

## **4.4 Detection of Insertion/Removal of SD Card/ SmartMedia™**

### **4.4.1 Detection of Insertion/Removal of SD Card**

The TC6371AF detects insertion and removal of the SD card using #SDCD and SD3. When #SDCD is Low or SD3 is High, the SD card is inserted. When #SDCD is High or SD3 is Low, the SD card is withdrawn.

The following is an example of how to detect insertion of the SD card.

1. The TC6371AF detects that #SDCD is Low, then turns power on to the SD card socket.
2. The TC6371AF detects that the SD3 pin is High.

The following is an example of how to detect removal of the SD card.

1. The TC6371AF detects that #SDCD is High, or SD3 is Low.
2. The TC6371AF turns power off.

\* Removing the SD card while the card is being accessed may damage the card.

The SD card insertion/removal status can be checked by bit 9, 8, 4, and 3 of 1Ch SD port register.

### **4.4.2 Detection of Insertion/Removal of SmartMedia™**

The TC6371AF can detect insertion and removal of the SmartMedia™ using #SMCD and #SMEJSW. When #SMCD or #SMEJSW is Low, the SmartMedia™ is inserted. When #SMCD or #SMEJSW is High, the SmartMedia™ is withdrawn. When the bit 7 of the SmartMedia™ host controller configuration register 63h set to "1" and when #SMEJSW is High, this indicates that the SmartMedia™ is inserted. When the bit 6 of SmartMedia™ host controller configuration register 63h set to "1", detection of SmartMedia™ has been masked using #SMEJSW.

The following is an example of how to detect insertion of the SmartMedia™.

1. The TC6371AF detects that #SMCD is Low, then #SMEJSW is Low.
2. The TC6371AF then turns power on to the SmartMedia™ socket.

The following is an example of how to detect removal of the SmartMedia™.

1. The TC6371AF detects that #SMEJSW is High, then #SMCD is High.
2. The TC6371AF then turns power off.

\* Removing the SmartMedia™ card when the SmartMedia™ is being accessed may damage the SmartMedia™.

The SmartMedia™ insertion status can be checked using status bits 3 and 2 and interrupt status bit 3 of the SmartMedia™ control register.

## 4.5 Interrupts

When the TC6371AF detects the following interrupt sources, the TC6371AF asserts interrupt signals (#INTA, #INTB, #PME). The power management register has to be set in order to get #PME output.

### 4.5.1 Interrupt Sources by SD Card

Interrupt sources by the SD card are as listed below:

#### Normal interrupts

- SD card insertion interrupt by #SDCD \*
- SD card removal interrupt by #SDCD \*
- SD card insertion interrupt by SDCD3 \*
- SD card removal interrupt by SDCD3 \*
- Interrupt by write enable buffer signal
- Interrupt by read enable buffer signal
- Interrupt by R/W end signal
- Interrupt by response end signal

#### Error interrupts

- Timeout error (command) interrupt
- Buffer underflow interrupt
- Buffer overflow interrupt
- Timeout error (data) interrupt
- End bit error interrupt
- CRC error interrupt
- CMD index error interrupt

### 4.5.2 Interrupt Sources by SmartMedia™

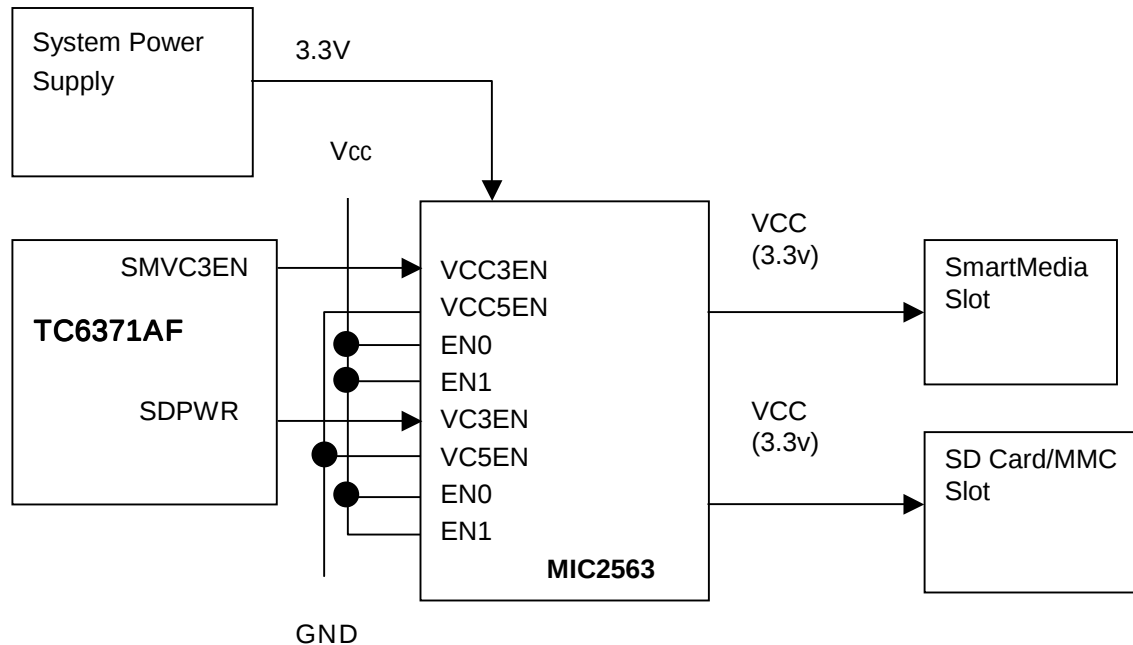
Interrupt sources by the SmartMedia™ are as listed below:

- SmartMedia™ insertion interrupt
- SmartMedia™ removal interrupt
- Interrupt by #SMEJSW signal
- Interrupt when #SMRB signal changes from Low to High

\* Interrupt sources which can be output to #PME. Other interrupt sources can only be output to #INTA or #INTB.

## 4.6 Card Slot Power Supply Control

The TC6371AF is designed so that it can be connected to MIC2563 (power supply control LSI). An example of application circuit is shown below.



### 4.6.1 SD Card Slot Power Supply Control

Setting the power control register (config offset: 48h) enables to control the power supply of SD card.

#### Parallel power supply control signal

| Signal name | Function                       | Pin |
|-------------|--------------------------------|-----|
| SDPWR       | Controls 3.3-V VCC for SD card | 69  |

### 4.6.2 SmartMedia™ Slot Power Supply Control

There are two modes for controlling power supply to the SmartMedia™ slot: Manual Power Supply Control mode and Automatic Power Supply Control mode. Those modes are switched using the bit 7 of the SmartMedia™ host controller configuration register at 62h. In Manual Power Supply Control mode, bits 3 and 2 of the SmartMedia™ control register (offset: 02h) are used. In Automatic Power Supply Control mode, when the SmartMedia™ is inserted, power is automatically turned on. When the SmartMedia™ is removed, power is turned off.

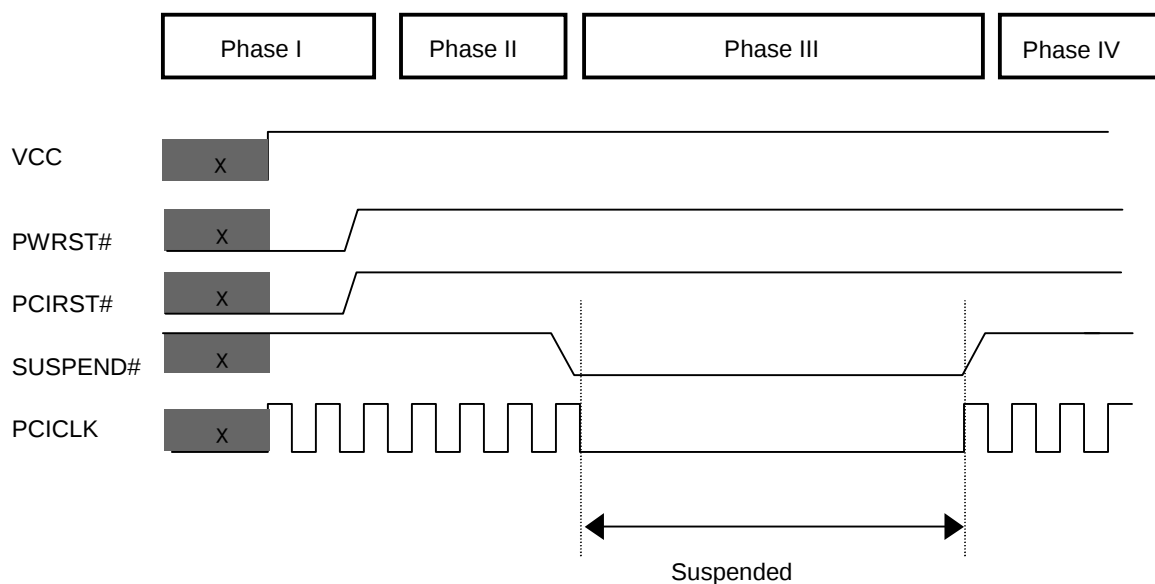
As of January, 2002, the SmartMedia™ driver uses a manual power supply control.

#### Parallel power supply control signal

| Signal name | Function                           | Pin |
|-------------|------------------------------------|-----|
| SMVC3EN     | Controls 3.3-V VCC for SmartMedia™ | 72  |

## 4.7 Suspend State

When #SUSPEND is Low, TC6371AF prevents throughput of data input from the SD card and SmartMedia™. Control signals, output from TC6371AF, are set at non-active level. Among PC system is Suspend state, it is recommended that VDD of TC6371AF is power off.



- Phase I: Immediately after power on, #PCIRST and #PWRST are L and #SUSPEND is H. This state clears all circuits.
- Phase II: Normal state with #PCIRST de-asserted (H).
- Phase III: Asserting #SUSPEND sets suspend state. In this state, TC6371AF prevents throughput of signals input from the SD card and SmartMedia™. (\*) In this state, TC6371AF cannot accept PCI transactions. Stopping the PCICLK in suspend state reduces power consumption.
- Phase IV: De-asserting #SUSPEND restores TC6371AF to its normal operating state.

\* When #SUSPEND is Low, TC6371AF prevents current flow from VCC to GND even if an intermediate potential is applied and TC6371AF masks out the input buffer signals as well.

## 4.8 Power Management

The TC6371AF supports a power management function conforming to PCI bus power management interface specification revision 1.1 (PCI-PM) for both the SD host controller and the SmartMedia™ host controller. As of January, 2002, the SD/MMC/ SmartMedia™ driver does not support a function which enables #PME and then performs output.

### 4.8.1 PME Register Structure

To support the #PME, the TC6371AF registers conform to PCI-PM specifications.

|                                        |                                                   |                                            |                   |     |
|----------------------------------------|---------------------------------------------------|--------------------------------------------|-------------------|-----|
| PME Registers                          |                                                   |                                            | Config.<br>Offset |     |
| Power Management Capabilities<br>(PMC) |                                                   | Next Item Ptr                              | Capability ID     | 80h |
| Data                                   | PMCSR PCI to PCI<br>Bridge Support<br>(PMCSR_BSE) | Power Management Control/Status<br>(PMCSR) |                   | 84h |

### 4.8.2 PME State

The PCI power management specifications are defined by five states (D0uninitialized D0active, D1, D2, D3hot, and D3cold) according to the power dissipation level.

The TC6371AF can support all five states.

### 4.8.3 PME Context Register

In D3hot and D3cold states, TC6371AF supports PME. This allows the TC6371AF to detect wakeup events and assert #PME even when #PCIRST is asserted and auxiliary power only (D3cold) is supplied. The required registers must therefore be saved. The following are the registers to be saved.

#### 1) SD Host Controller

##### Configuration register

- |                 |                                   |
|-----------------|-----------------------------------|
| • Offset 80-87h | Power management-related register |
| • Offset 48h    | Power Control                     |
| • Offset 4Ch    | CardDetect Mode                   |
| • Offset 88h    | PME Trigger Enable                |
| • Offset A0-Efh | CIS                               |
| • Offset FDh    | PM Write Protect                  |

##### SD IO register

- |                |                       |
|----------------|-----------------------|
| • Offset 20h   | SD INFO MASK register |
| bit 9, 8, 4, 3 |                       |

#### 2) Smart Media™ Host Controller

##### Configuration register

- |                 |                                   |
|-----------------|-----------------------------------|
| • Offset 80-87h | Power management-related register |
| • Offset 48h    | Interrupt Enable                  |
| • Offset 49h    | PME Enable                        |
| • Offset 4Ah    | Event Control                     |
| • Offset 4Ch    | CLKRUN Control                    |
| • Offset 5Bh    | Debug                             |
| • Offset 60h    | SmartMedia™ Transaction Control   |
| • Offset 62h    | SmartMedia™ Power Supply Control  |
| • Offset 63h    | SmartMedia™ Detect Control        |
| • Offset A0-EFh | CIS                               |
| • Offset F0-F1h | ROM Data Port                     |
| • Offset F2h    | ROM Index Port                    |
| • Offset F3h    | ROM Control                       |
| • Offset FCh    | Configuration Control             |
| • Offset FFh    | Monitor Select Protect            |

##### SmartMedia™ Control register

- |                         |                           |
|-------------------------|---------------------------|
| • Offset 00-03h(00h)    | Data register             |
| • Offset 04h(02h Write) | Mode register             |
| • Offset 05h(02h Read)  | Status register           |
| • Offset 06h(04h)       | Interrupt Status register |
| • Offset 07h(06h)       | Interrupt Mask register   |

#### 4.8.4 #PME Generation

#PME is controlled (enabled/disabled) by the bit 8 (PME\_EN) of the power management control/status register (config offset: 84h). The status can be checked using the bit 15 of the register. When the TC6371AF detects card insertion/removal events or other interrupt events, the TC6371AF asserts #PME. The host controller controls registers to perform masking events and controlling flags.

| Card type                   | Interrupt event        | Pin name        | Details                                         |
|-----------------------------|------------------------|-----------------|-------------------------------------------------|
| SD host controller          | Card insertion/removal | #SDCD、SDCD3(CD) | Indicates insertion into/removal from card slot |
| SmartMedia™ host controller | Card insertion/removal | #SMCD、#SMEJSW   | Indicates insertion into/removal from card slot |
|                             | BSY release            | #SMRB           | Triggered by SmartMedia™ BSY release            |

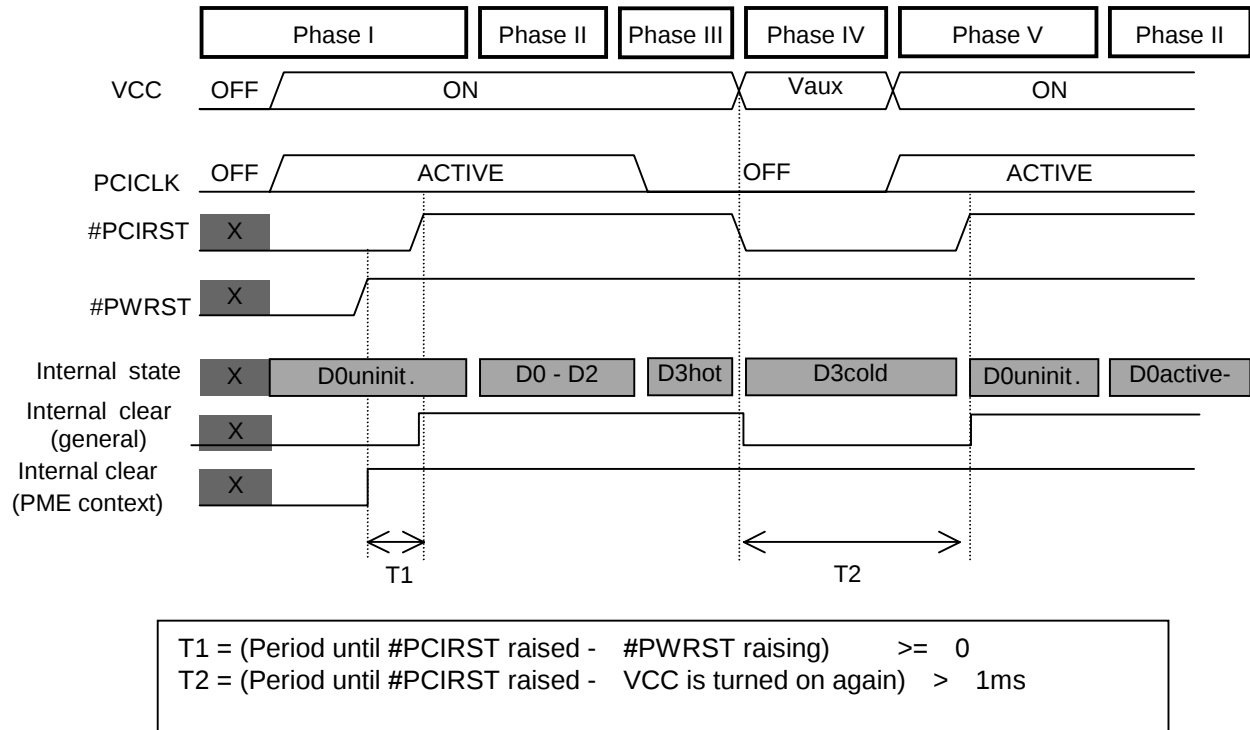
Note: The TC6371AF uses a 32-kHz clock (CLK32) for the #PME control circuit.  
In D3hot/D3cold state or in D1/D2 state where the CLKRUN protocol operates, PCICLK is stopped. Therefore, when CLK32 is not input, the TC6371AF's #PME control circuit does not operate and #PME cannot be supported.

#### 4.8.5 #PME Pin

The #PME pin outputs power management interrupts according to PCI bus power management interface specifications. Because the pin is an open drain output determined by PCI bus power management interface specifications, it must be pulled up outside the TC6371AF. To prevent leak current from the external pull-up even when the power supply to this pin is off, the pin is open-drain output with failsafe measures.

#### 4.8.6 #PWRST

The TC6371AF supports a #PME wakeup from D3cold state (in conformance to the PCI 2.1 power-on reset sequence). The #PWRST signal is used to reset the PME context at power on.



- Phase I: #PWRST and #PCIRST are L when the VCC is turned on from power off. This state clears all circuits, including the PME context.
- Phase II: Normal operating mode. #PWRST and #PCIRST are both H.
- Phase III: Setting PMCSR (config 84h) bits 1 and 0 to 11b sets the internal circuitry to D3hot. The PCICLK is set to L except at a configuration access of PMCSR. Setting bits 1 and 0 of PMCSR to 00b shifts to D0uninit state. Asserting #PCIRST at L shifts to Phase IV D3cold.
- Phase IV: Asserting #PCIRST at L sets the internal circuitry to D3cold. During this period, the power supply to VCC can be switched to Vaux. At that time, VCCP can be turned off, but because #PCIRST is L and #PWRST is H, the PME context is saved.
- Phase V: VCCP is turned back on and PCICLK goes active. While #PCIRST is L, an internal (general) clear resets all circuits except the PME context. Next, the TC6371AF returns to normal operating mode and the context can be written.

| #PWRST | #PCIRST | PME context |
|--------|---------|-------------|
| L      | X       | Cleared     |
| H      | L       | Saved       |
| H      | H       | Normal      |

#### Notes:

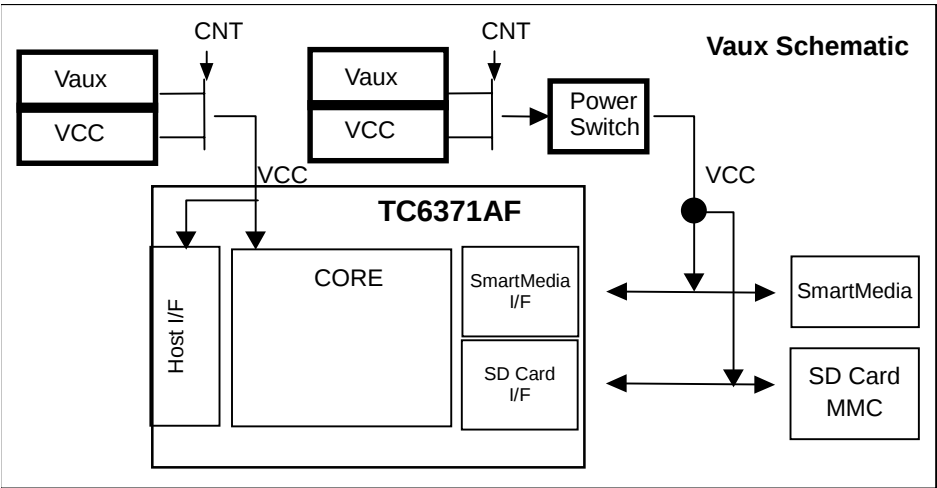
- If D3cold is not supported, set the #PCIRST input signal level the same as that of the #PWRST input signal.
- If D3cold is supported, it is desirable to switch Vaux after asserting #PCIRST. When restoring from D3cold state, make sure that the PCICLK waveform is stable.

4.8.7 Vaux in D3cold State

Because the TC6371AF supports a D3cold state, it requires an auxiliary power supply (Vaux). The four systems that need the auxiliary power supply are:

- TC6371AF internal PME context (includes interrupt detection): VCC
- Card slot power supply (power-SW) related control: VCC
- Interface with host (system interface): VCC
- SmartMedia™ slot/SD card slot interface: VCC

Toshiba recommends asserting #PCIRST to be “Low” before moving to Vaux operation.



Pins that are active when operating on auxiliary power supply.

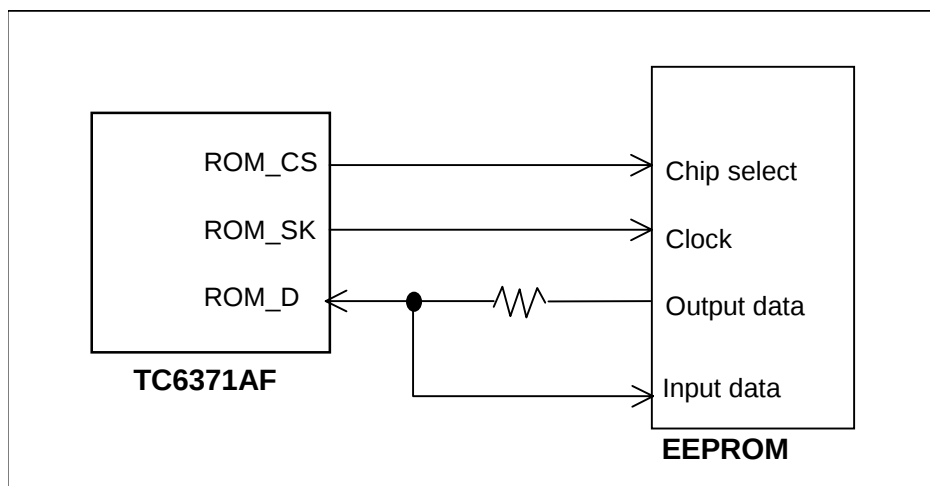
| Host I/F                                                | SD I/F (VCC) | SmartMedia™ (VCC) |
|---------------------------------------------------------|--------------|-------------------|
| #PME<br>CLK32<br>#PWRST<br>#SUSPEND<br>SDPWR<br>SMVC3EN | #SDCD        | #SMCD<br>#SMEJSW  |

## 4.9 Serial ROM Interface

The TC6371AF supports a serial ROM interface. The ROM interface is used to load the configuration register initial values (mainly subsystem ID and subsystem vendor ID initial values) and CIS information when using the CardBus card.

When using the serial ROM interface, connect the interface as below and set the external pins TST1[3-0] to D010.

Toshiba verified operation of the serial ROM interface using one "NM93C66"(Fairchild) with a 10-k $\Omega$  resistor connected shown as the figure below.



## 4.10 Pulled-Up/Pulled-Down Resistors

The TC6371AF needs pulled-up/pulled-down resistors attached to each interface. The following resistance values are provided as a guide.

### 4.10.1 SD Card Interface

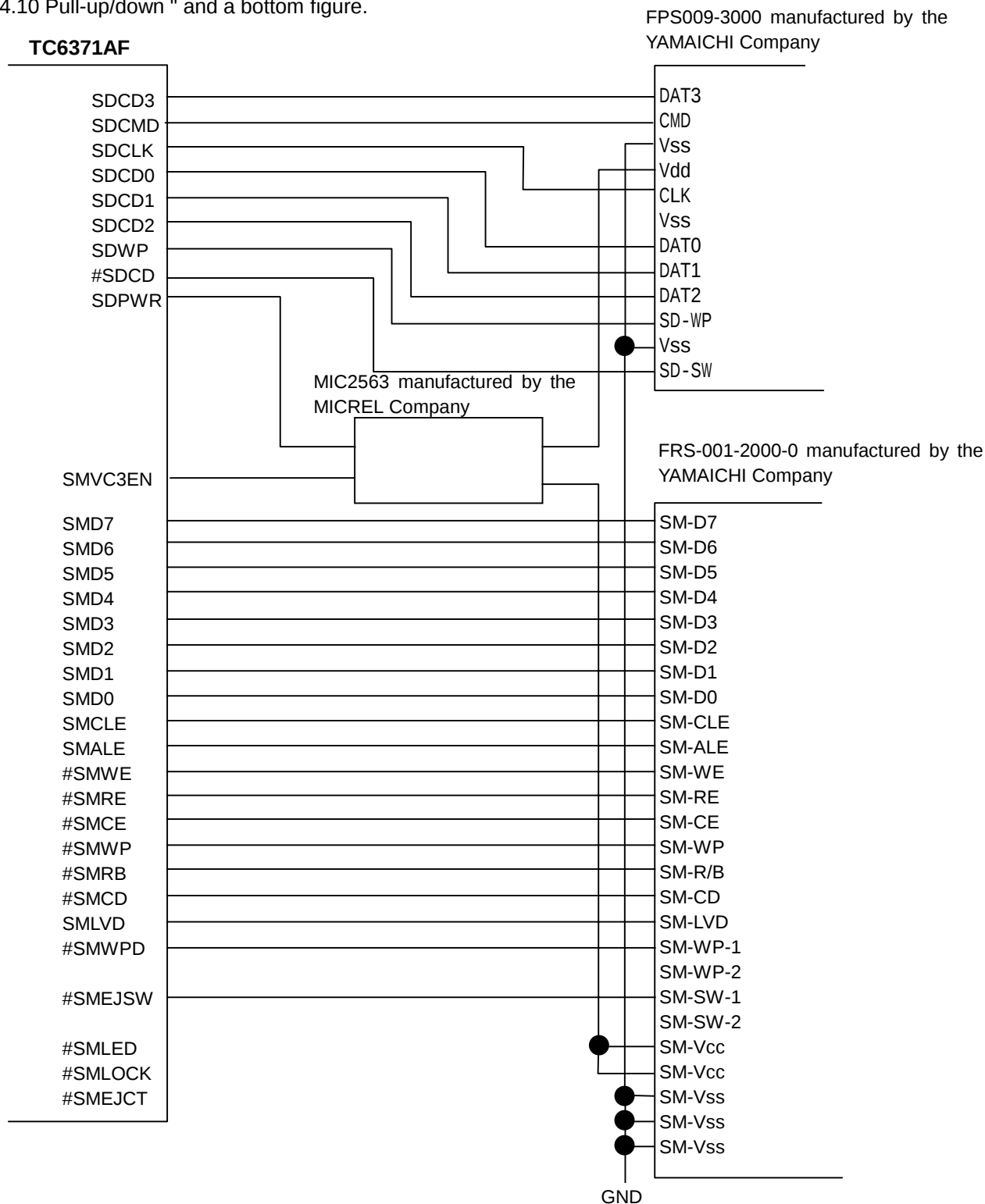
| NAME  | Pin | IO | Pull-up/<br>Pull-down | Pull-up power<br>supply | Resistance                              | FUNCTION                                                                                |
|-------|-----|----|-----------------------|-------------------------|-----------------------------------------|-----------------------------------------------------------------------------------------|
| SDCD3 | 85  | IO | Pull-up               | SDVCC                   | 47K $\Omega$                            | SD card data bus                                                                        |
| SDCD2 | 83  |    | Pull-up               | SDVCC                   | 100K $\Omega$                           |                                                                                         |
| SDCD1 | 102 |    | Pull-up               | SDVCC                   | 100K $\Omega$                           |                                                                                         |
| SDCD0 | 101 |    | Pull-up               | SDVCC                   | 100K $\Omega$                           |                                                                                         |
| SDCMD | 89  | IO | Pull-up               | SDVCC                   | *1 : 33K $\Omega$<br>*2 : 100K $\Omega$ | SD card / command<br>*1: MultiMedia Card supported<br>*2: MultiMedia Card not supported |
| SDCLK | 98  | O  | —                     | —                       | —                                       | SD card clock                                                                           |
| #SDCD | 104 | I  | Pull-up               | VCC                     | 10K $\Omega$                            | SD card detection                                                                       |
| SDWP  | 105 | I  | Pull-up               | VCC                     | 10K $\Omega$                            | SD card write-protection                                                                |

### 4.10.2 SmartMedia™ Interface

| NAME    | Pin | IO         | Pull-up/<br>Pull-down | Pull-up power<br>supply | Resistance    | FUNCTION                   |
|---------|-----|------------|-----------------------|-------------------------|---------------|----------------------------|
| SMD7    | 91  | IO         | Pull-down             | —                       | 100K $\Omega$ | Data                       |
| SMD6    | 94  |            |                       |                         |               |                            |
| SMD5    | 96  |            |                       |                         |               |                            |
| SMD4    | 99  |            |                       |                         |               |                            |
| SMD3    | 95  |            |                       |                         |               |                            |
| SMD2    | 93  |            |                       |                         |               |                            |
| SMD1    | 90  |            |                       |                         |               |                            |
| SMD0    | 86  |            |                       |                         |               |                            |
| SMCLE   | 75  | O (3state) | Pull-down             | —                       | 100K $\Omega$ | Enables the command latch. |
| SMALE   | 78  | O (3state) | Pull-down             | —                       | 100K $\Omega$ | Enables the address latch. |
| #SMCE   | 77  | O (3state) | Pull-up               | SMVCC                   | 100K $\Omega$ | Enables the chip.          |
| #SMWE   | 80  | O (3state) | Pull-up               | SMVCC                   | 100K $\Omega$ | Enables a write.           |
| #SMRE   | 79  | O (3state) | Pull-up               | SMVCC                   | 100K $\Omega$ | Enables a read.            |
| #SMWP   | 84  | O (3state) | Pull-down             | —                       | 100K $\Omega$ | Write-protection           |
| #SMRB   | 82  | I          | Pull-up               | SMVCC                   | 10K $\Omega$  | Busy                       |
| #SMCD   | 100 | I          | Pull-up               | VCC                     | 10K $\Omega$  | Detects card.              |
| SMLVD   | 88  | I          | Pull-down             | —                       | 100K $\Omega$ | Detects low voltage.       |
| #SMWPD  | 73  | I          | Pull-up               | VCC                     | 10K $\Omega$  | Write-protection seal      |
| #SMEJSW | 74  | I          | Pull-up               | VCC                     | 10K $\Omega$  | Eject request              |
| #SMLED  | 107 | O (OD)     | Pull-up               | VCC                     | 100K $\Omega$ | Turns on the LED.          |
| #SMLOCK | 109 | O (OD)     | Pull-up               | VCC                     | 100K $\Omega$ | Lock mode                  |
| #SMEJCT | 106 | O (OD)     | Pull-up               | VCC                     | 100K $\Omega$ | Eject response             |

#### 4.11 Connection example of SD Card/SmartMedia™ socket

It is shown that total 32 signal connections example of TC6371AF which have 8 signals of SD card interface, 1 signal of a power supply control for SD card, 22 signals of SmartMedia™ interface and 1 signal of a power supply control for SmartMedia™. As for our company, a movement confirmation of the SD card /SmartMedia™ was done by using FRS-001-2000-0 and FPS009-3000 of the YAMAICHI Company. An outside pull-up/down resistance that is mentioned on an item of the "4.10 Pull-up/down resistance" is not shown in a bottom figure. When you design a circuit, please refer to recommended resistance by an item of the "4.10 Pull-up/down " and a bottom figure.



## 4.12 Processing Unused Interface External Pins

TC6371AF accommodates one port of SD Card Interface and one port of SmartMedia™ Interface. See descriptions for processing pins in respective sections of interface when dealing with unused External Pins for interfaces.

### 4.12.1 Processing Pins (SmartMedia™ Interface unsupported)

Process Pins according to the following table when SmartMedia™ Interface is unused (when each signals are not connected to other parts) :

| NAME    | Pin | I/O        | Process                      |
|---------|-----|------------|------------------------------|
| SMD7    | 91  | IO         | Pull-up resistance for 100KΩ |
| SMD6    | 94  | IO         | Pull-up resistance for 100KΩ |
| SMD5    | 96  | IO         | Pull-up resistance for 100KΩ |
| SMD4    | 99  | IO         | Pull-up resistance for 100KΩ |
| SMD3    | 95  | IO         | Pull-up resistance for 100KΩ |
| SMD2    | 93  | IO         | Pull-up resistance for 100KΩ |
| SMD1    | 90  | IO         | Pull-up resistance for 100KΩ |
| SMD0    | 86  | IO         | Pull-up resistance for 100KΩ |
| SMCLE   | 75  | O (3state) | OPEN                         |
| SMALE   | 78  | O (3state) | OPEN                         |
| #SMCE   | 77  | O (3state) | OPEN                         |
| #SMWE   | 80  | O (3state) | OPEN                         |
| #SMRE   | 79  | O (3state) | OPEN                         |
| #SMWP   | 84  | O (3state) | OPEN                         |
| #SMRB   | 82  | I          | High                         |
| SMLVD   | 88  | I          | Low                          |
| #SMCD   | 100 | I          | High                         |
| #SMWPD  | 73  | I          | High                         |
| #SMEJSW | 74  | I          | High                         |
| #SMLED  | 107 | O (OD)     | OPEN                         |
| #SMLOCK | 109 | O (OD)     | OPEN                         |
| #SMEJCT | 106 | O (OD)     | OPEN                         |
| SMVC3EN | 72  | O          | OPEN                         |

And,

| NAME   | Pin | I/O | Process                |
|--------|-----|-----|------------------------|
| FCMODE | 58  | I   | Low                    |
| IDSEL0 | 13  | I   | Connect to any AD line |
| IDSEL1 | 120 | I   | Low                    |

#### 4.12.2 Processing Pins (SD Interface unsupported)

Process Pins according to the following table when SD Interface is unused (when each signals are not connected to other parts):

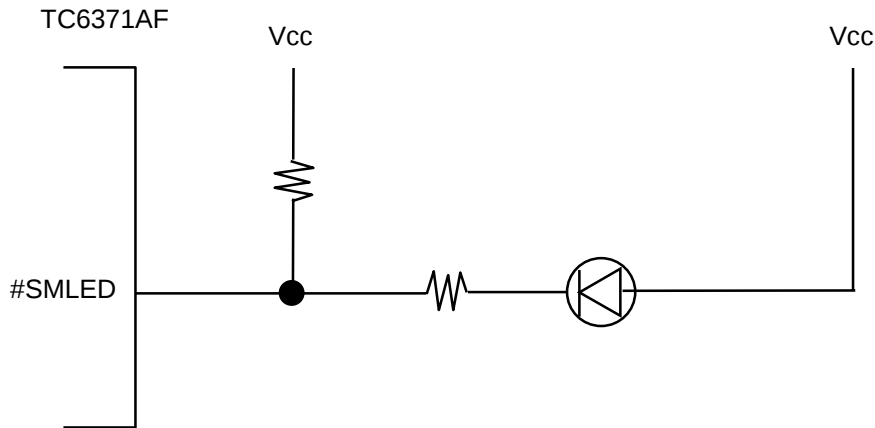
| NAME  | Pin | I/O | Process                      |
|-------|-----|-----|------------------------------|
| SDCD3 | 85  | IO  | Pull-up resistance for 100KΩ |
| SDCD2 | 83  | IO  | Pull-up resistance for 100KΩ |
| SDCD1 | 102 | IO  | Pull-up resistance for 100KΩ |
| SDCD0 | 101 | IO  | Pull-up resistance for 100KΩ |
| SDCMD | 89  | IO  | Pull-up resistance for 100KΩ |
| SDCLK | 98  | O   | Low                          |
| #SDCD | 104 | I   | High                         |
| SDWP  | 105 | I   | Low                          |
| SDPWR | 69  | O   | OPEN                         |

And,

| NAME   | Pin | I/O | Process                |
|--------|-----|-----|------------------------|
| FCMODE | 58  | I   | Low                    |
| IDSEL0 | 13  | I   | Low                    |
| IDSEL1 | 120 | I   | Connect to any AD line |

#### 4.13 #SMLED signal

TC6371AF has the #SMLED signal for SmartMedia interface. It is recommended that this signal is used for access LED, for example reading and writing. This signal is controlled by setting Mode Register(Offset:04h) of SmartMedia control register.



When Mode Register is written 04h, #SMLED becomes low and LED turns on. In reverse, in the case of being written 00h, #SMLED becomes high and LED turns off.

#### 4.14 GPIO interface specification

TC6380AF holds 8 pins(GPIO[7:0] signals) as general port. As GPIO[7:4] signals are input ones, please use them as fixed values with referring to page 14. It shows a usage method of GPIO[3:0] signals.

GPIO[3:0] signals can be output by setting 1b to D5 of Monitor Select Register(Config Offset:FFh) of SmartMedia host controller register. GPIO3 signal can be controlled by D3 of Monitor Select Register, GPIO2 signal can be controlled by D2 of Monitor Select Register, GPIO1 signal can be controlled by D3 of Monitor Select Register and GPIO0 signal can be controlled by D0 of Monitor Select Register.

As of January. 2002, the SD/MMC/SmartMedia driver does not perform any functions by controlling GPIO signals.

## 5 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings

| Symbol | Parameter                 | Min  | Max     | Unit | Condition | Note |
|--------|---------------------------|------|---------|------|-----------|------|
| Vcc    | Supply Voltage Range      | -0.3 | 5.0     | V    | GND=0V    | 1    |
| Vin3   | Input Voltage (3.3V)      | -0.3 | Vcc+0.3 | V    | GND=0V    |      |
| Vout   | Output Voltage            | -0.3 | Vcc+0.3 | V    | GND=0V    |      |
| Tstg   | Storage Temperature Range | -40  | 125     | °C   |           |      |

Note 1: VCC power supply

(Caution)

The absolute maximum ratings indicate a level at which permanent damage to the device may occur if those ratings are exceeded and are not intended to provide a guarantee that damage will not occur by staying within the level of the ratings.

### 5.2 DC Characteristics

#### 5.2.1 Power Supply Voltage: Recommended Conditions

| Power Pin | Parameter                      | Min | Typ | Max | Unit | Note |
|-----------|--------------------------------|-----|-----|-----|------|------|
| Vcc       | Supply Voltage for Core Logic  | 3.0 | 3.3 | 3.6 | V    |      |
| Topr      | Ambient Temperature under bias | 0   | 25  | 70  | °C   |      |

## 5.2.2 PCI Interface DC Characteristics

PCI interface DC characteristics at 3.3 V operation.

| Symbol | Parameter                | Min    | Max     | Unit | Test Condition | Note |
|--------|--------------------------|--------|---------|------|----------------|------|
| Vih    | Input High Voltage       | 0.5Vcc | Vcc+0.5 | V    |                | 1-1  |
| Vil    | Input Low Voltage        | -0.5   | 0.3Vcc  | V    |                | 1-1  |
| Vih    | Input High Voltage       | 0.7Vcc | Vcc+0.5 | V    |                | 1-2  |
| Vil    | Input Low Voltage        | -0.5   | 0.2Vcc  | V    |                | 1-2  |
| Voh    | Output High Voltage      | 0.9Vcc | —       | V    | Iout=-500μA    | 1-3  |
| Vol    | Output Low Voltage       | —      | 0.1Vcc  | V    | Iout=1500μA    | 1-4  |
| Ioh    | Switching Current High 1 | -12Vcc | —       | mA   | Vout=0.3Vcc    | 1-3  |
|        | Switching Current High 2 | —      | -32Vcc  | mA   | Vout=0.7Vcc    | 1-3  |
| Iol    | Switching Current Low 1  | 16Vcc  | —       | mA   | Vout=0.6Vcc    | 1-4  |
|        | Switching Current Low 2  | —      | 38Vcc   | mA   | Vout=0.18Vcc   | 1-4  |
| Iil    | Input Leakage Current    | -10    | 10      | μA   | 0<Vin<Vcc      | 1-1  |
|        |                          |        |         |      |                | 1-2  |
| Slewr  | Output Rise Slew Rate    | 1      | 4       | V/ns |                | 1-3  |
| Slewf  | Output Fall Slew Rate    | 1      | 4       | V/ns |                | 1-3  |

Note 1-1: Applied for AD[31:0], CBE#[3:0], #FRAME, #IRDY, #CLKRUN, IDSEL0, IDSEL1 pins

Note1-2: Applied for #PCIRST PCICLK pins

Note1-3: Applied for AD[31:0], CBE#[3:0], PAR, #TRDY, #STOP, #DEVSEL, #CLKRUN pins

Note1-4: Applied for AD[31:0], CBE#[3:0], PAR, #TRDY, #STOP, #DEVSEL, #CLKRUN, #INTA, #INTB, #PME pins

### 5.2.3 SmartMedia™ Interface DC Characteristics

SmartMedia™ interface DC characteristics at 3.3 V operation (VCC =3.0-3.6V, Ta=0-70°C)

| Symbol           | Parameter             | Min | Max | Unit | Condition                                            | Note |
|------------------|-----------------------|-----|-----|------|------------------------------------------------------|------|
| Vih              | Input High Voltage    | 2.2 | —   | V    |                                                      | 2-1  |
| Vil              | Input Low Voltage     | —   | 0.6 | V    |                                                      | 2-1  |
| Voh              | Output High Voltage   | 2.4 | —   | V    | I <sub>out</sub> =-1mA<br>3.0V<V <sub>cc</sub> <3.6V | 2-2  |
| Vol1             | Output Low Voltage    | —   | 0.4 | V    | I <sub>out</sub> =1mA<br>3.0V<V <sub>cc</sub> <3.6V  | 2-2  |
| Vol2             | Output Low Voltage    | —   | 0.4 | V    | I <sub>out</sub> =8mA<br>3.0V<V <sub>cc</sub> <3.6V  | 2-3  |
| I <sub>ilk</sub> | Input Leakage Current | -10 | 10  | μA   | V <sub>in</sub> =0-V <sub>cc</sub>                   | 2-1  |

Note2-1: Applied for SMD[7:0], #SMRB, #SMCD, SMLVD, #SMWPD, #SMEJSW pins

Note2-2: Applied for SMD[7:0], SMCLE, SMALE, #SMCE, #SMWE, #SMRE, #SMWP pins

Note2-3: Applied for #SMLOCK, #SMEJCT, #SMLED pins

### 5.2.4 SmartMedia™ Power Supply Control DC Characteristics

SmartMedia™ power supply control DC characteristics at 3.3 V operation (Vcc =3.0-3.6V, Ta=0-70 °C)

| Symbol | Parameter           | Min | Max | Unit | Condition                                              | Note |
|--------|---------------------|-----|-----|------|--------------------------------------------------------|------|
| Voh    | Output High Voltage | 2.4 | —   | V    | I <sub>out</sub> =-100μA<br>3.0V<V <sub>cc</sub> <3.6V | 2-4  |
| Vol    | Output Low Voltage  | —   | 0.6 | V    | I <sub>out</sub> =100μA<br>3.0V<V <sub>cc</sub> <3.6V  | 2-4  |

Note2-4: Applied for SMVC3EN pin

### 5.2.5 SD Card Interface Pin DC Characteristics

SD card interface DC characteristics at 3.3 V operation ( $V_{CC} = 3.0\text{--}3.6\text{V}$ ,  $T_a = 0\text{--}70^\circ\text{C}$ )

| Symbol | Parameter                             | Min          | Max           | Unit             | Condition                                                       | Note       |
|--------|---------------------------------------|--------------|---------------|------------------|-----------------------------------------------------------------|------------|
| Vih    | Input High Voltage                    | $0.7V_{CC}$  | $V_{CC}+0.3$  | V                |                                                                 | 3-1        |
| Vil    | Input Low Voltage                     | $V_{SS}-0.3$ | $0.175V_{CC}$ | V                |                                                                 | 3-1        |
| Vih    | Input High Voltage                    | $0.8V_{CC}$  | —             | V                |                                                                 | 3-2        |
| Vil    | Input Low Voltage                     | —            | $0.2V_{CC}$   | V                |                                                                 | 3-2        |
| Voh    | Output High Voltage                   | $0.75V_{CC}$ | —             | V                | $I_{out} = -1\text{mA}$<br>$3.0\text{V} < V_{CC} < 3.6\text{V}$ | 3-3        |
| Vol    | Output Low Voltage                    | —            | $0.125V_{CC}$ | V                | $I_{out} = 1\text{mA}$<br>$3.0\text{V} < V_{CC} < 3.6\text{V}$  | 3-3        |
| Iiik   | Input Leakage Current                 | -10          | 10            | $\mu\text{A}$    | $0 < V_{in} < V_{CC}$                                           | 3-1<br>3-2 |
| Rdat3  | Pull-up resistance inside card (pin1) | 10           | 90            | $\text{K}\Omega$ |                                                                 |            |

Note3-1: Applied for SD $\overline{\text{CD}}$ [3:0], SDCMD, SDWP pins

Note3-2: Applied for #SD $\overline{\text{CD}}$  pins

Note3-3: Applied for SD $\overline{\text{CD}}$ [3:0], SDCMD, SDCLK pins

### 5.2.6 SD Card Power Supply Control DC Characteristics

SD card power supply control DC characteristics at 3.3 V operation ( $V_{CC} = 3.0\text{--}3.6\text{V}$ ,  $T_a = 0\text{--}70^\circ\text{C}$ )

| Symbol | Parameter           | Min | Max | Unit | Condition                                                           | Note |
|--------|---------------------|-----|-----|------|---------------------------------------------------------------------|------|
| Voh    | Output High Voltage | 2.4 | —   | V    | $I_{out} = -100\mu\text{A}$<br>$3.0\text{V} < V_{CC} < 3.6\text{V}$ | 3-3  |
| Vol    | Output Low Voltage  | —   | 0.6 | V    | $I_{out} = 100\mu\text{A}$<br>$3.0\text{V} < V_{CC} < 3.6\text{V}$  | 3-3  |

Note3-3: Applied for SDPWR pin

## 5.2.7 System Interface Pin (5 V-Tolerant) DC Characteristics

System interface pin DC characteristics (VCC =3.0-3.6V, Ta=0-70°C)

| Symbol | Parameter             | Min     | Max    | Unit | Test Condition | Note |
|--------|-----------------------|---------|--------|------|----------------|------|
| Vih    | Input High Voltage    | Vcc-0.6 | —      | V    |                | 4-1  |
| Vil    | Input Low Voltage     | —       | 0.6    | V    |                | 4-1  |
| Iilk   | Input Leakage Current | -10     | 10     | μA   | 0<Vin<Vcc      | 4-1  |
| Vih    | Input High Voltage    | 0.8Vcc  | —      | V    |                | 4-2  |
| Vil    | Input Low Voltage     | —       | 0.6    | V    |                | 4-2  |
| Iilk   | Input Leakage Current | -10     | 10     | μA   | 0<Vin<Vcc      | 4-2  |
| Vih    | Input High Voltage    | 0.8Vcc  | —      | V    |                | 4-3  |
| Vil    | Input Low Voltage     | —       | 0.2Vcc | V    |                | 4-3  |
| Iilk   | Input Leakage Current | -10     | 10     | μA   | Vin=           | 4-3  |
| Vih    | Input High Voltage    | 0.8Vcc  | —      | V    |                | 4-4  |
| Vil    | Input Low Voltage     | —       | 0.2Vcc | V    |                | 4-4  |
| Iilk   | Input Leakage Current | -10     | 10     | μA   | 0<Vin<Vcc      | 4-4  |

Note4-1: Applied for CLK32 pin

Note4-2: Applied for #PWRST pin

Note4-3: Applied for #SUSPEND pin

Note4-4: Applied for FCMODE pin

### 5.2.8 GPIO Interface Pin DC Characteristics

GPIO interface pin DC characteristics ( $V_{CC} = 3.0\text{--}3.6\text{V}$ ,  $T_a = 0\text{--}70^\circ\text{C}$ )

| Symbol           | Parameter             | Min                | Max                | Unit | Condition                          | Note |
|------------------|-----------------------|--------------------|--------------------|------|------------------------------------|------|
| V <sub>Ih</sub>  | Input High Voltage    | 0.8V <sub>CC</sub> | —                  | V    |                                    | 5-1  |
| V <sub>Il</sub>  | Input Low Voltage     | —                  | 0.2V <sub>CC</sub> | V    |                                    | 5-1  |
| I <sub>Oh</sub>  | Output High Current   | —                  | -4                 | mA   | V <sub>Oh</sub> =2.4V              | 5-2  |
| I <sub>Ol</sub>  | Output Low Current    | 4                  | —                  | mA   | V <sub>Ol</sub> =0.4V              | 5-2  |
| I <sub>Ilk</sub> | Input Leakage Current | -10                | 10                 | μA   | 0<V <sub>in</sub> <V <sub>CC</sub> | 5-1  |

Note5-1: Applied for GPIO[7:0] pins

Note5-2: Applied for GPIO[3:0] pins

### 5.2.9 TEST Pin DC Characteristics

TEST pin DC characteristics ( $V_{CC} = 3.0\text{--}3.6\text{V}$ ,  $T_a = 0\text{--}70^\circ\text{C}$ )

| Symbol           | Parameter             | Min                | Max                | Unit | Condition                          | Note |
|------------------|-----------------------|--------------------|--------------------|------|------------------------------------|------|
| V <sub>Ih</sub>  | Input High Voltage    | 0.8V <sub>CC</sub> | —                  | V    |                                    | 6-1  |
| V <sub>Il</sub>  | Input Low Voltage     | —                  | 0.2V <sub>CC</sub> | V    |                                    | 6-1  |
| I <sub>Ilk</sub> | Input Leakage Current | -10                | 10                 | μA   | 0<V <sub>in</sub> <V <sub>CC</sub> | 6-1  |

Note6-1: Applied for TSTI[3:0] pins

## 5.2.10 Current Dissipation Characteristics

### Power Supply Current

| Symbol        | Parameter                                                        | Min | Typ | Max | Unit | Condition                                            |
|---------------|------------------------------------------------------------------|-----|-----|-----|------|------------------------------------------------------|
| Iccstd        | Power Supply Current,<br>Standby                                 |     |     | 100 | μA   | PCICLK=0,<br>CLK32=32KHz<br>VCC=3.6V<br>#SUSPEND=low |
| IccSM         | Power Supply Current,<br>Operating SmartMedia™                   |     |     | 56  | mA   | PCICLK=33MHz,<br>CLK32=32KHz<br>VCC=3.6V             |
| IccSD/<br>MMC | Power Supply Current,<br>Operating SD Card or MultiMedia<br>Card |     |     | 75  | mA   | PCICLK=33MHz,<br>CLK32=32KHz<br>VCC=3.6V             |

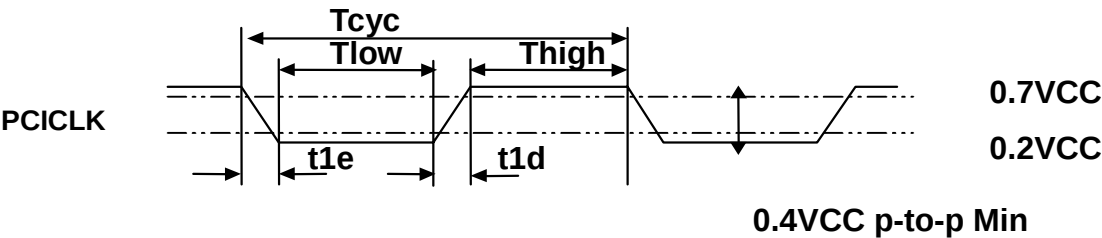
5.3 AC Characteristics

5.3.1 PCI Interface Signal AC Characteristics

PCI clock AC characteristics (VCC=3.0-3.6V, Ta=0-70°C)

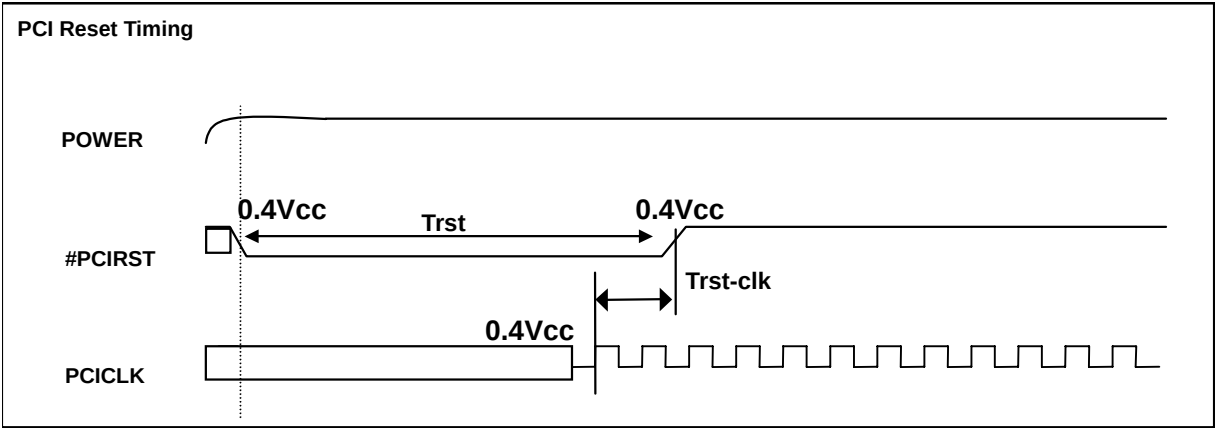
| Symbol | Parameter                      | Min | Max | Unit | Notes |
|--------|--------------------------------|-----|-----|------|-------|
|        | PCICLK                         |     |     |      |       |
| Tcyc   | CLK cycle time                 | 30  | ∞   | ns   |       |
| Thigh  | CLK High time                  | 11  | —   | ns   |       |
| Tlow   | CLK Low time                   | 11  | —   | ns   |       |
| t1d    | Slew Rate, PCICLK Rising Edge  | 1   | 4   | V/ns |       |
| t1e    | Slew Rate, PCICLK Falling Edge | 1   | 4   | V/ns |       |

PCICLK Timing



PCI Reset AC Characteristics (VCC=3.0-3.6V, Ta=0-70°C)

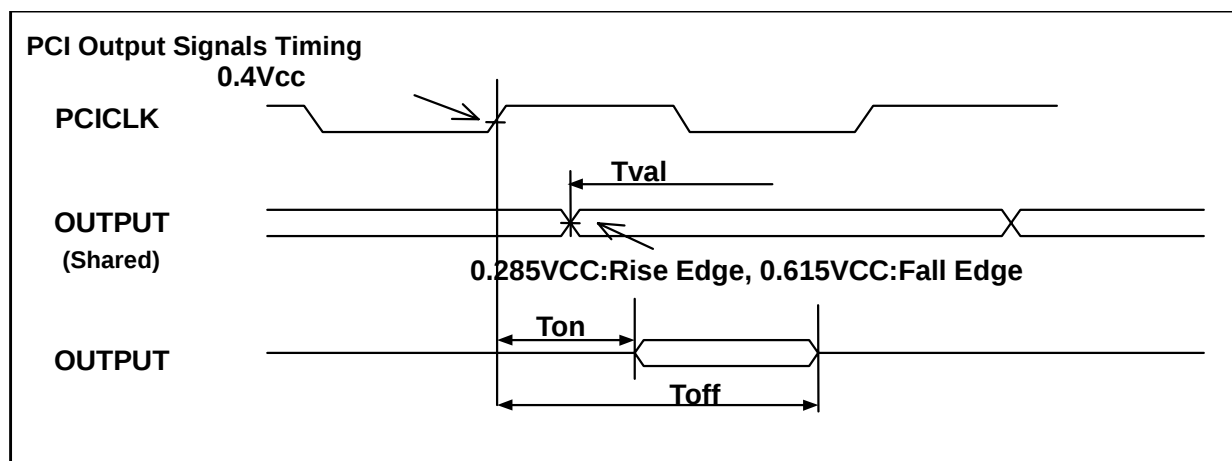
| Symbol   | Parameter                            | Min | Max | Unit | Notes |
|----------|--------------------------------------|-----|-----|------|-------|
|          | #PCIRST                              |     |     |      |       |
| Trst     | Reset active time after power stable | 1   |     | ms   |       |
| Trst-clk | Reset active time after CLK stable   | 100 |     | μs   |       |



PCI Reset Timing

## PCI Interface Output AC Characteristics (VCC=3.0-3.6V, Ta=0-70°C)

| Symbol | Parameter                                                | Min | Max | Unit | Notes   |
|--------|----------------------------------------------------------|-----|-----|------|---------|
|        | AD[31:0], #CBE[3:0], PAR, #DEVSEL, #TRDY, #STOP, #CLKRUN |     |     |      |         |
| Tval   | CLK to signal valid delay-bused signals                  | 2   | 11  | ns   | CL=10pF |
| Ton    | Float to active delay                                    | 2   | —   | ns   |         |
| Toff   | Active to float delay                                    | —   | 28  | ns   |         |

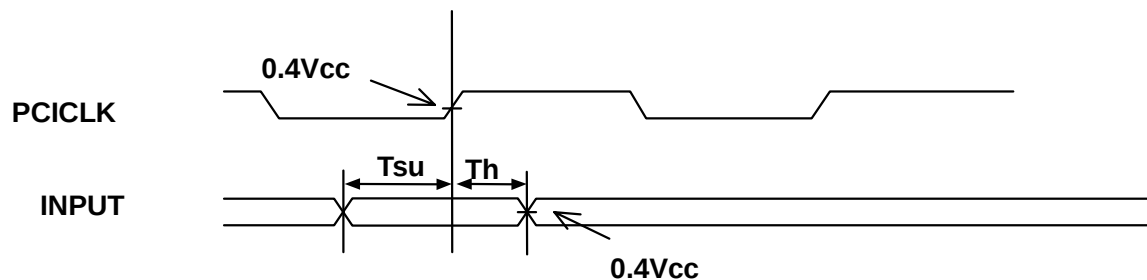


PCI Output Signal Timing

## PCI Interface Input Signal AC Characteristics (VCC=3.0-3.6V, Ta=0-70°C)

| Symbol | Parameter                                                   | Min | Max | Unit | Notes |
|--------|-------------------------------------------------------------|-----|-----|------|-------|
|        | AD[31:0], #CBE[3:0], #FRAME, #IRDY, #CLKRUN, IDSEL0, IDSEL1 |     |     |      |       |
| Tsu    | Input setup time to CLK-based signals                       | 7   | —   | ns   |       |
| Th     | Input hold time from CLK                                    | 0   | —   | ns   |       |

## PCI Input Signals Timing



PCI Input Signals Timing

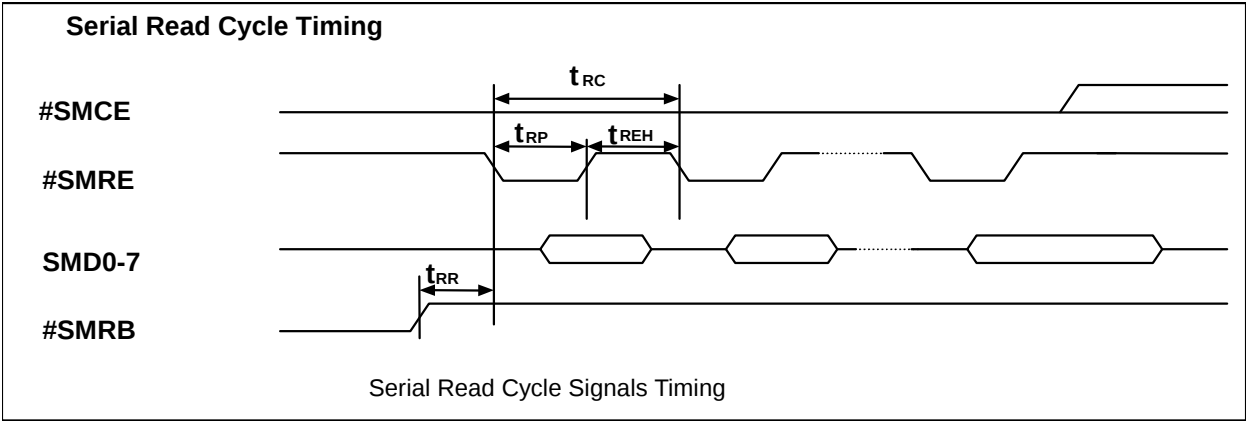
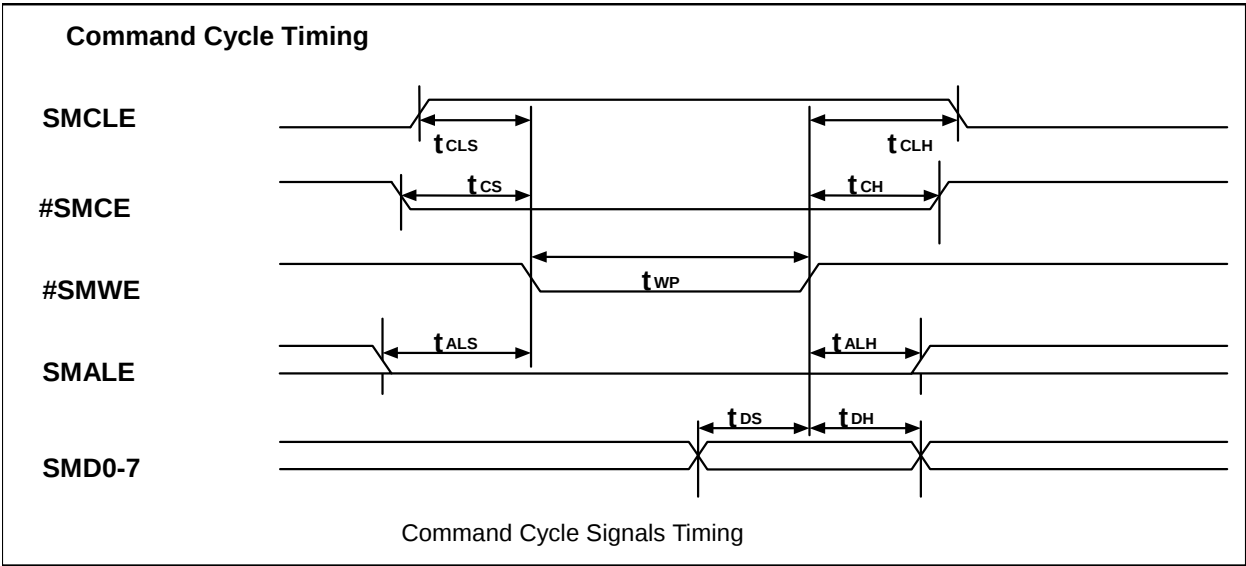
## 5.3.2 SmartMedia™ Interface Signal AC Characteristics

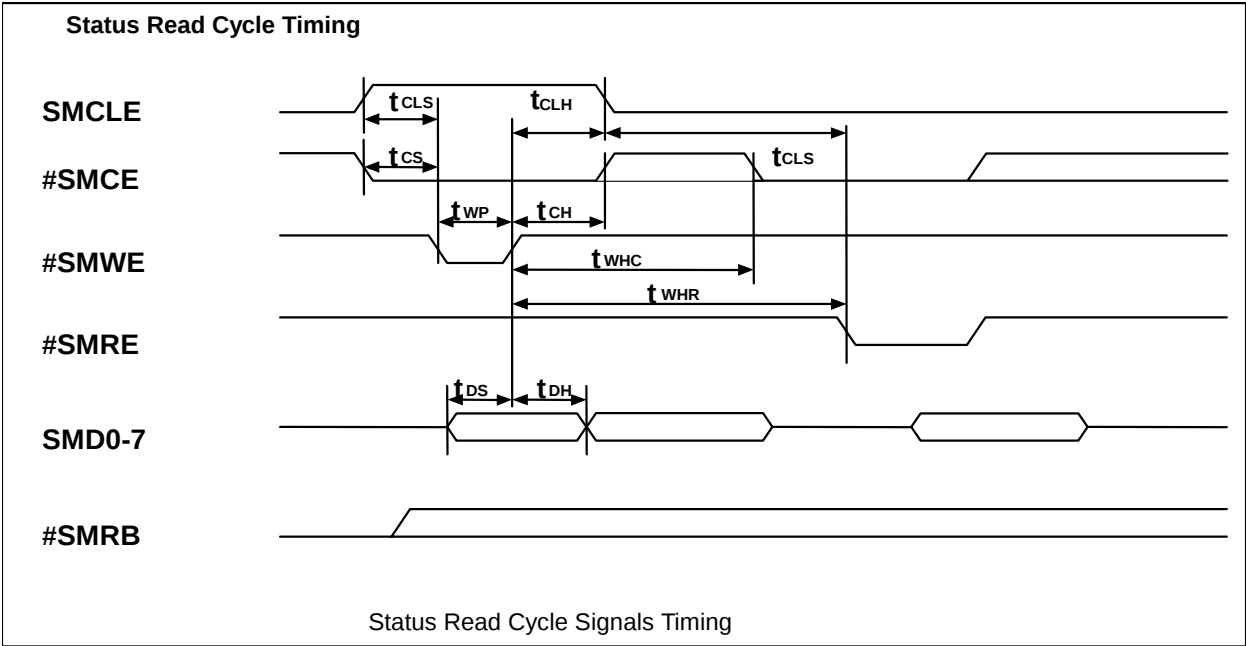
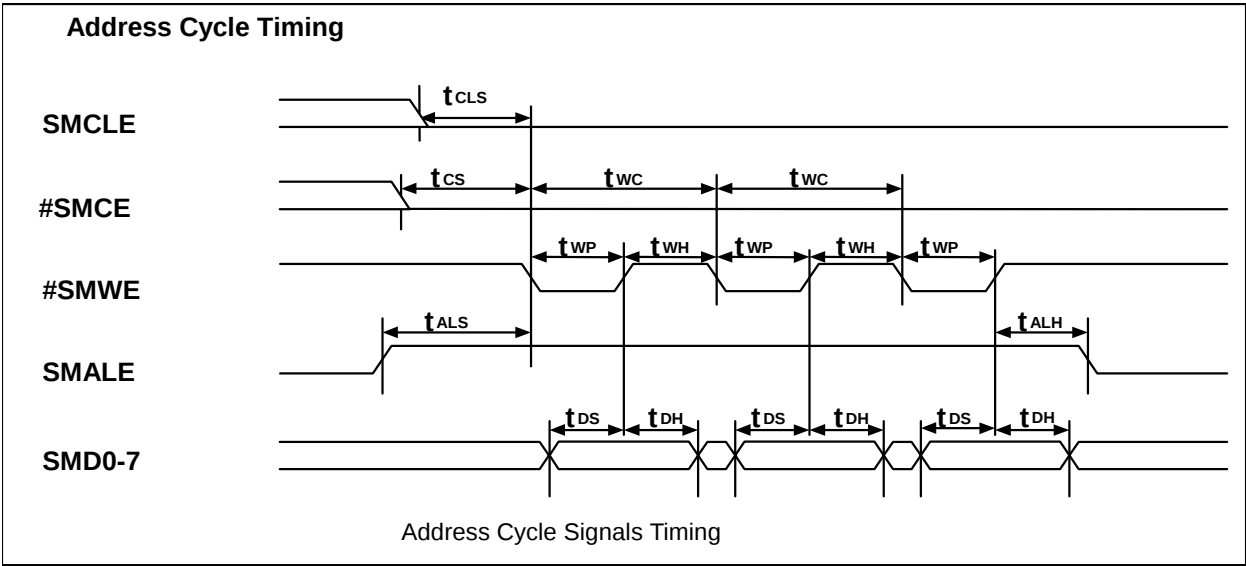
(VCC=3.0-3.6V, Ta=0-70°C)

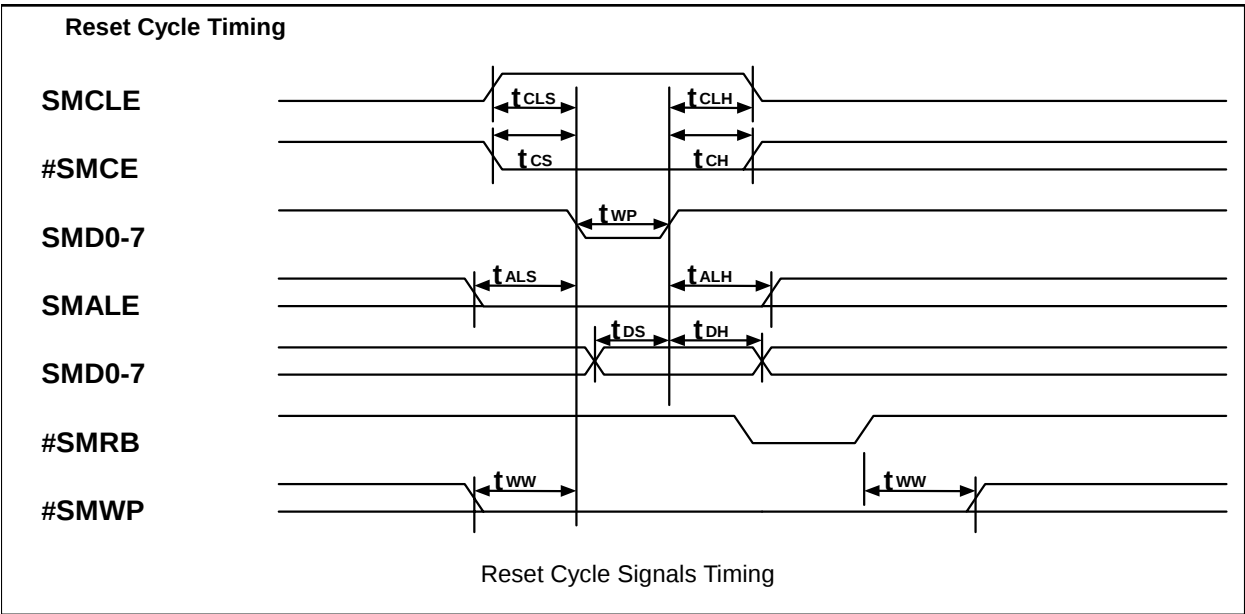
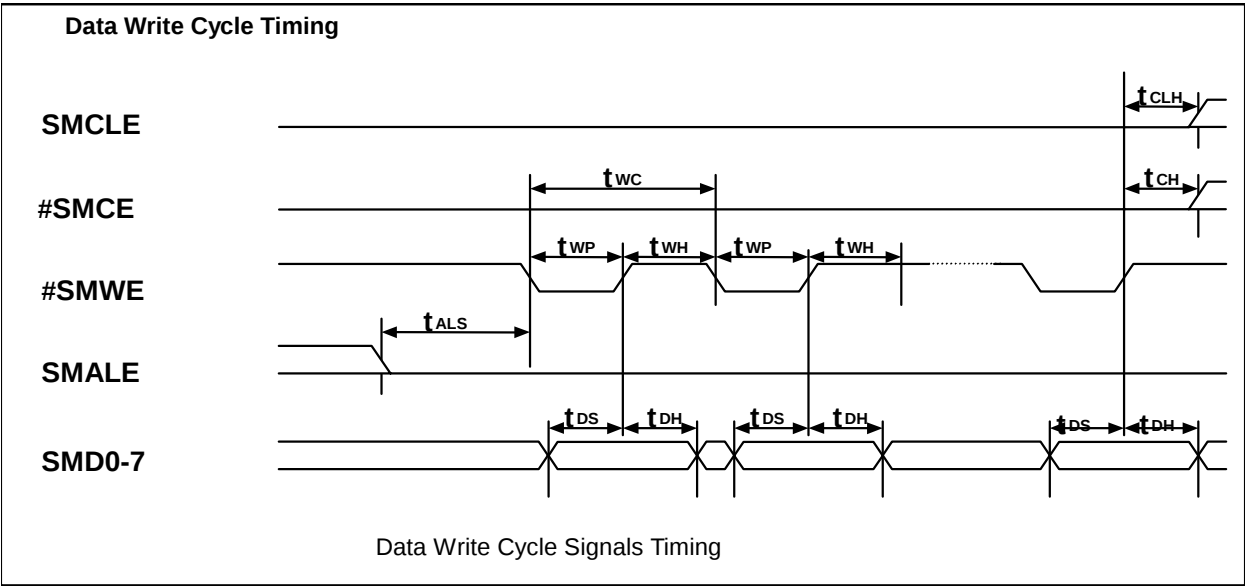
| Symbol           | Parameter                                              | Min     | Max     | Unit |
|------------------|--------------------------------------------------------|---------|---------|------|
| t <sub>CLS</sub> | SMCLE Setup Time                                       | 20      | —       | ns   |
| t <sub>CLH</sub> | SMCLE Hold Time                                        | 40      | —       | ns   |
| t <sub>CS</sub>  | #SMCE Setup Time                                       | 20      | —       | ns   |
| t <sub>CH</sub>  | #SMCE Hold Time                                        | 40      | —       | ns   |
| t <sub>WP</sub>  | #SMWE Pulse Width                                      | 2PCICLK | 6PCICLK | ns   |
| t <sub>ALS</sub> | SMALE Setup Time                                       | 20      | —       | ns   |
| t <sub>ALH</sub> | SMALE Hold Time                                        | 40      | —       | ns   |
| t <sub>DS</sub>  | Data Setup Time                                        | 30      | —       | ns   |
| t <sub>DH</sub>  | Data Hold Time                                         | 20      | —       | ns   |
| t <sub>WH</sub>  | #SMWE High Hold Time                                   | 3PCICLK | —       | ns   |
| t <sub>WW</sub>  | #SMWP High to #SMWE Low                                | 100     | —       | ns   |
| t <sub>RR</sub>  | Ready to #SMRE Low                                     | 20      | —       | ns   |
| t <sub>RP</sub>  | Read Pulse Width                                       | 3PCICLK | 6PCICLK | ns   |
| t <sub>RC</sub>  | Read Cycle Time                                        | 80      | —       | ns   |
| t <sub>CEH</sub> | #SMCE High Hold Time(at the Last Serial Read)          | 250     | —       | ns   |
| t <sub>REH</sub> | #SMRE High Hold Time                                   | 2PCICLK | —       | ns   |
| t <sub>IR</sub>  | Output Hi-Z to #SMRE Low                               | 0       | —       | ns   |
| t <sub>WHC</sub> | #SMWE High to #SMCE Low                                | 50      | —       | ns   |
| t <sub>WHR</sub> | #SMWE High to #SMRE Low                                | 60      | —       | ns   |
| t <sub>AR1</sub> | SMALE Low to #SMRE Low(Address Register Read, ID Read) | 200     | —       | ns   |
| t <sub>CR</sub>  | #SMCE Low to #SMRE Low(Data Register Read ,ID Read)    | 200     | —       | ns   |

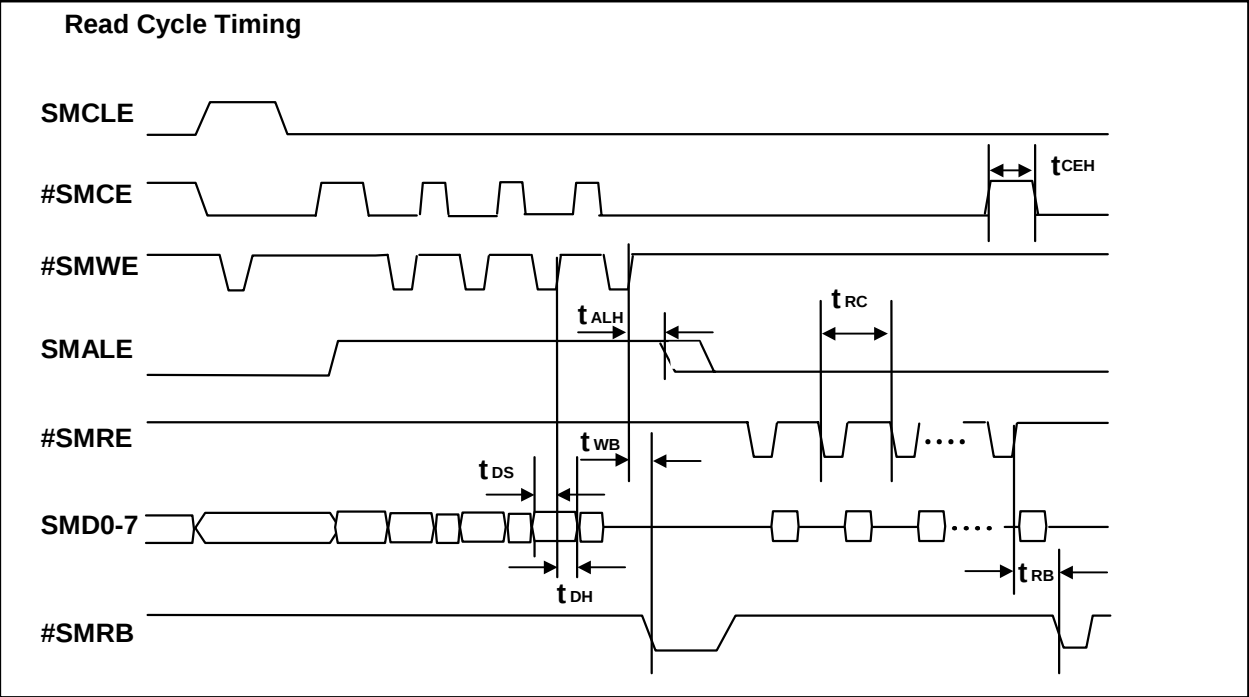
## AC Test Conditions

| Parameter                    | 3.3V Model             |
|------------------------------|------------------------|
| Input Pulse Level            | 0.4V~2.4V              |
| Input comparison Level       | 1.5V / 1.5V            |
| Output Data comparison Level | 1.5V / 1.5V            |
| Output Load                  | 1TTL Gate and Cl=100pF |

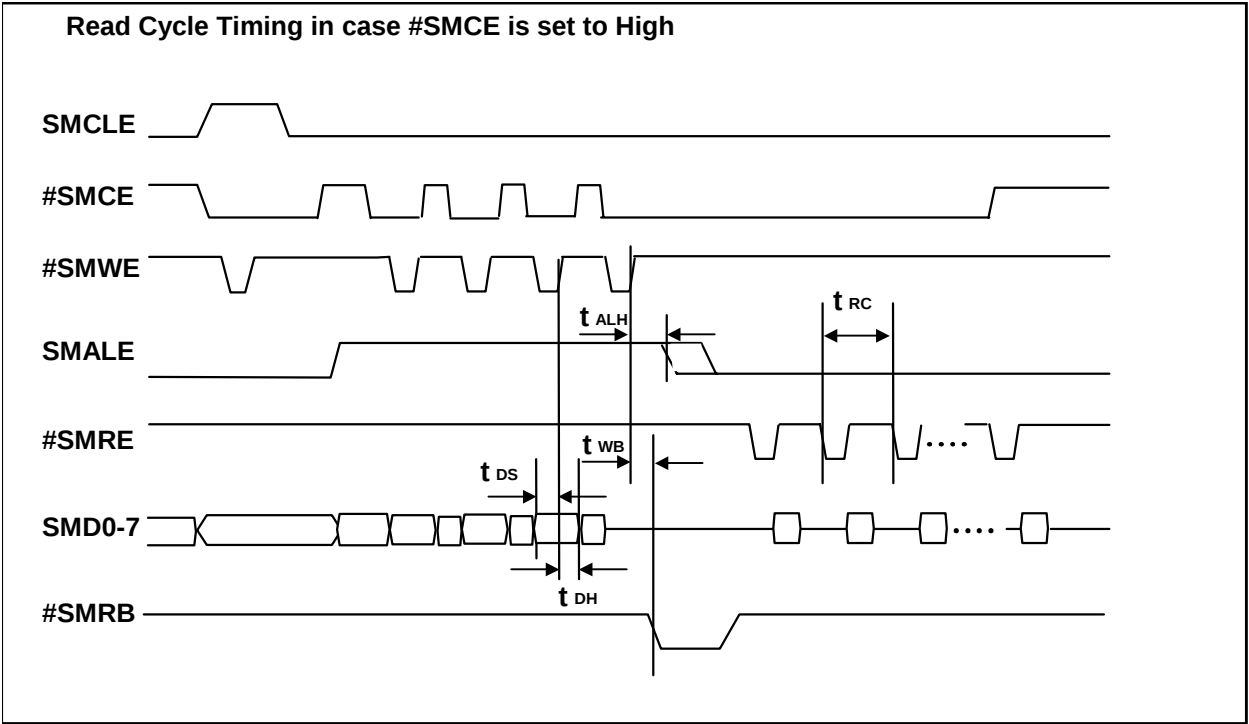




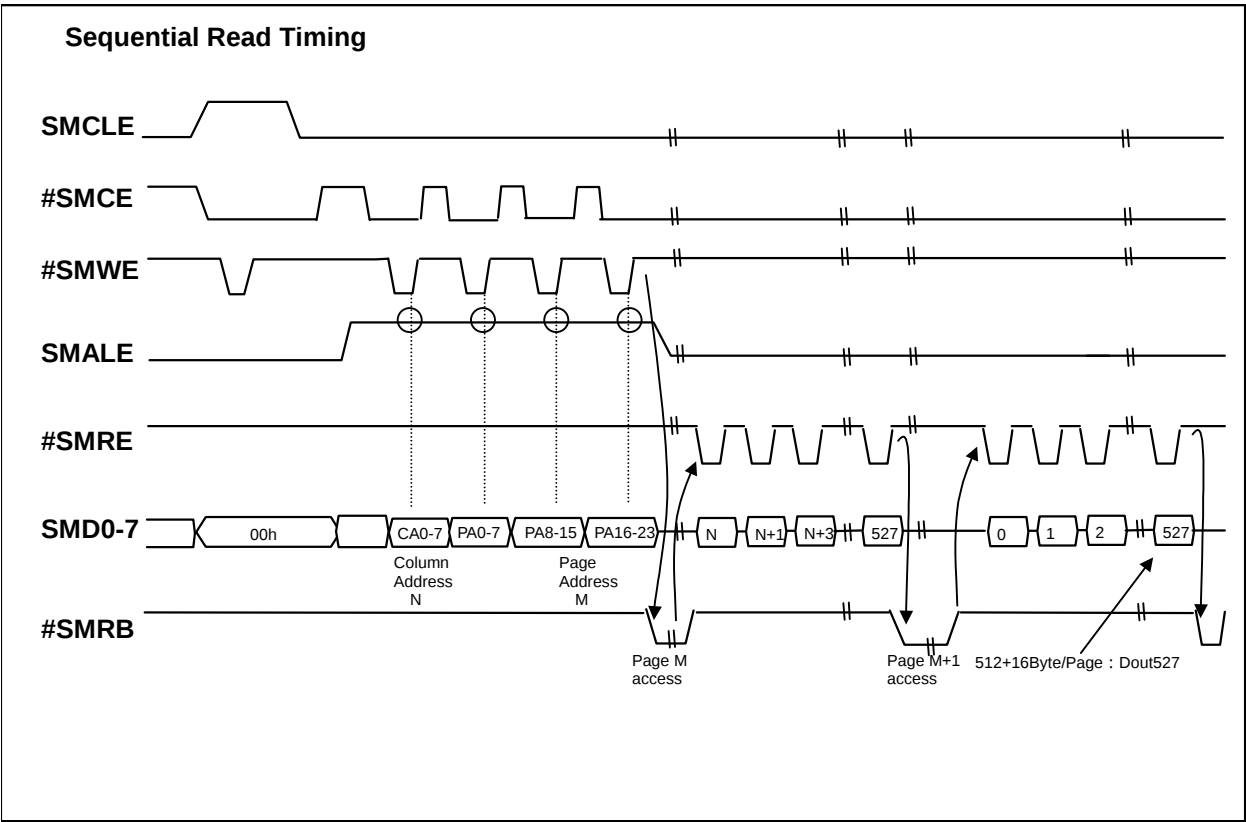
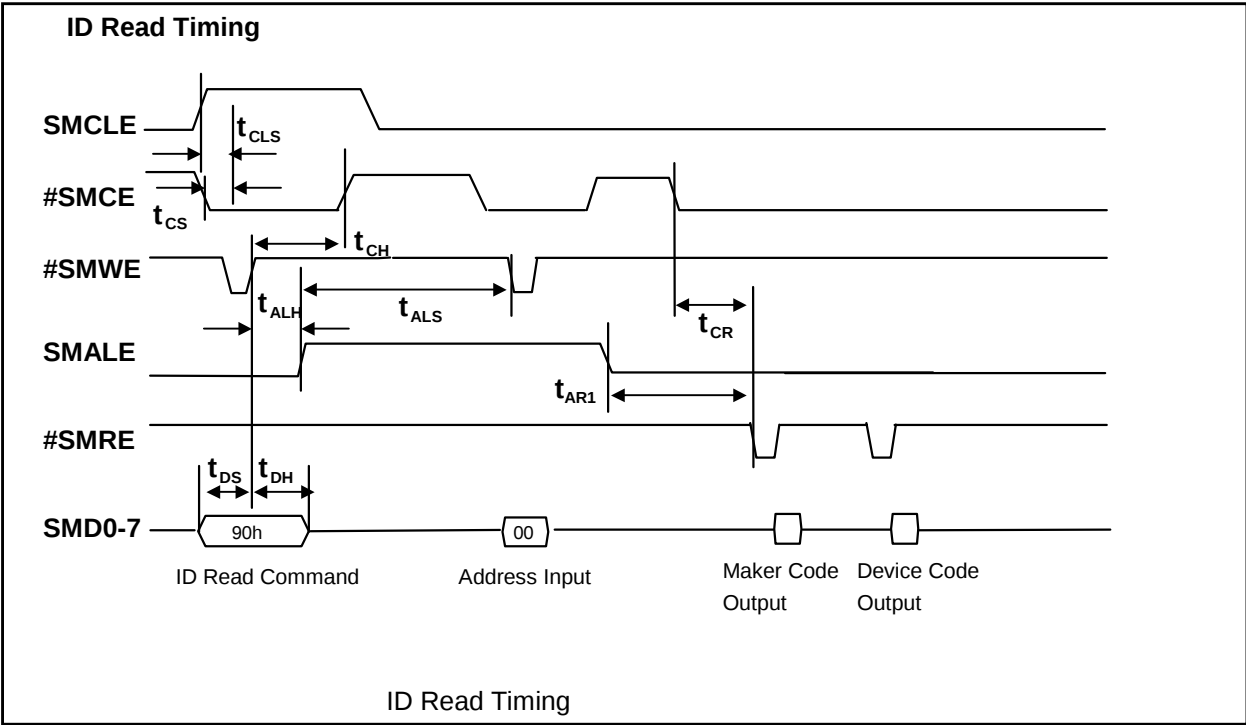


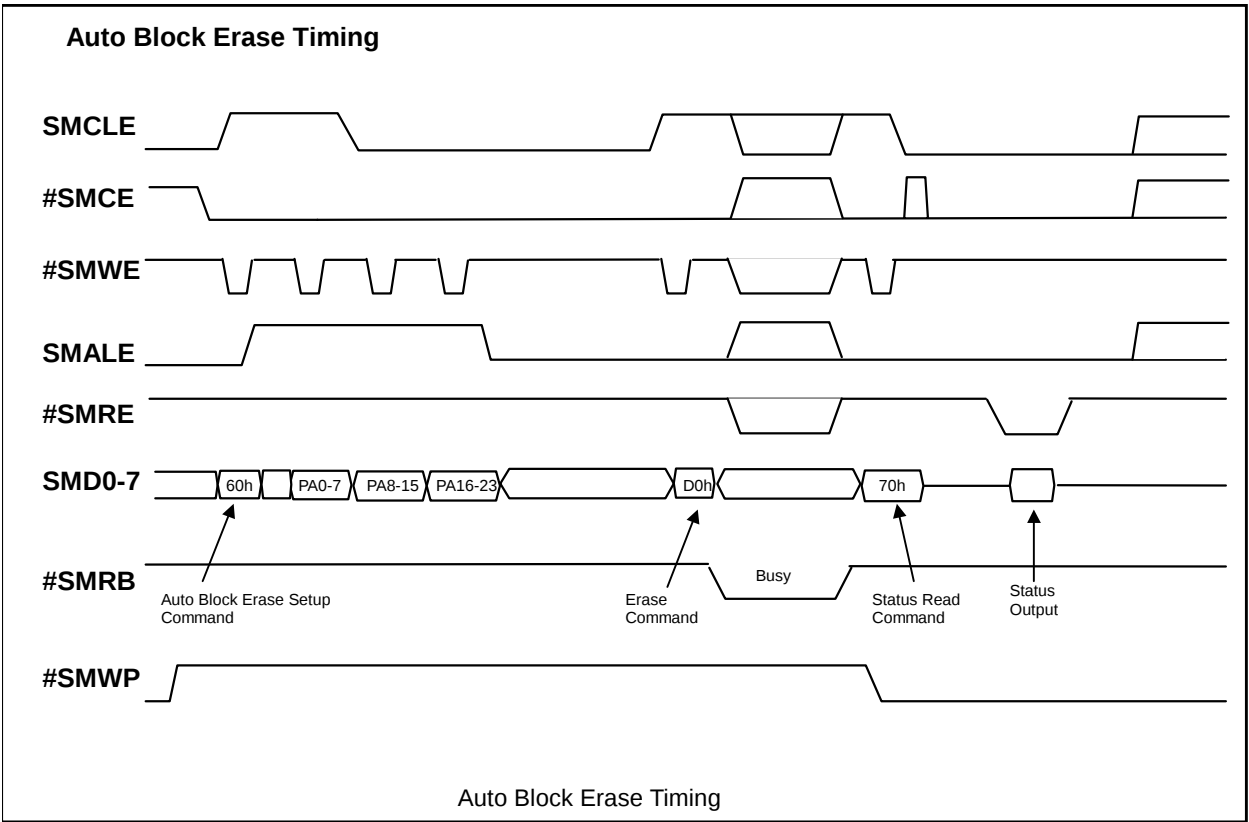
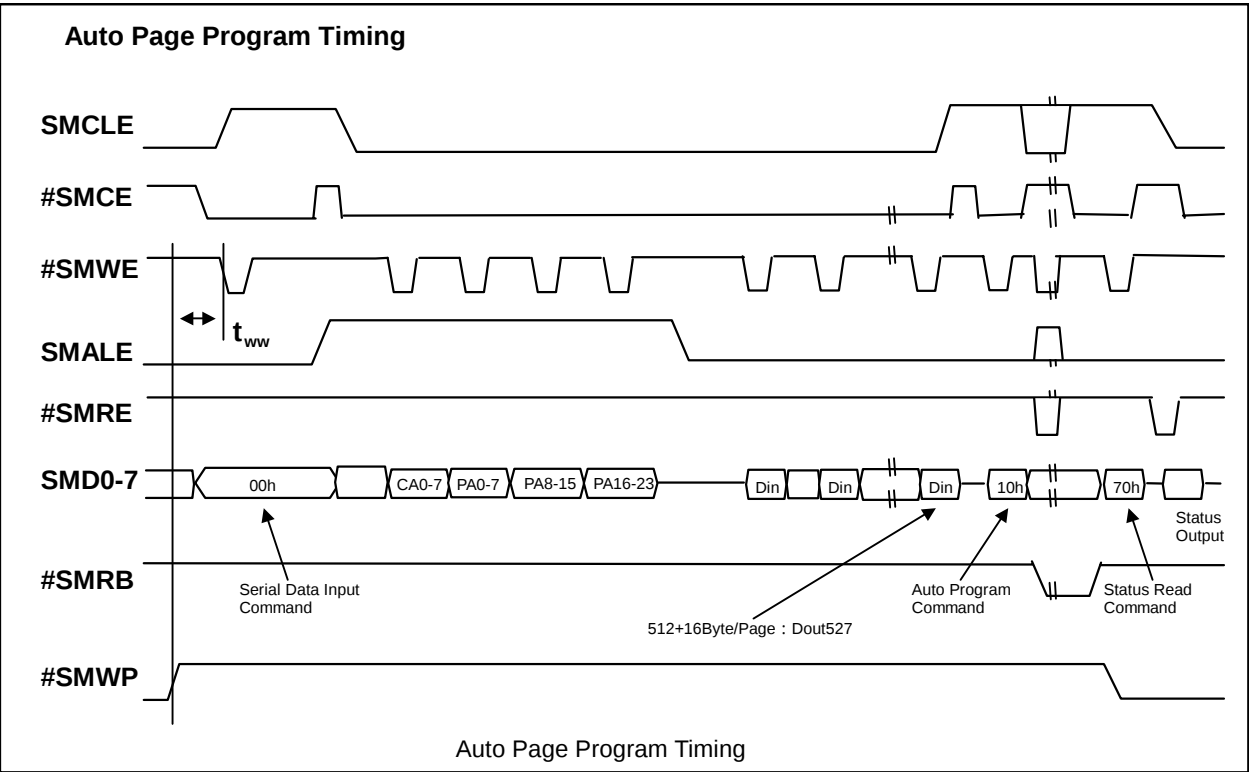


Read Cycle Timing



Read Cycle Timing in case #SMCE is set to High

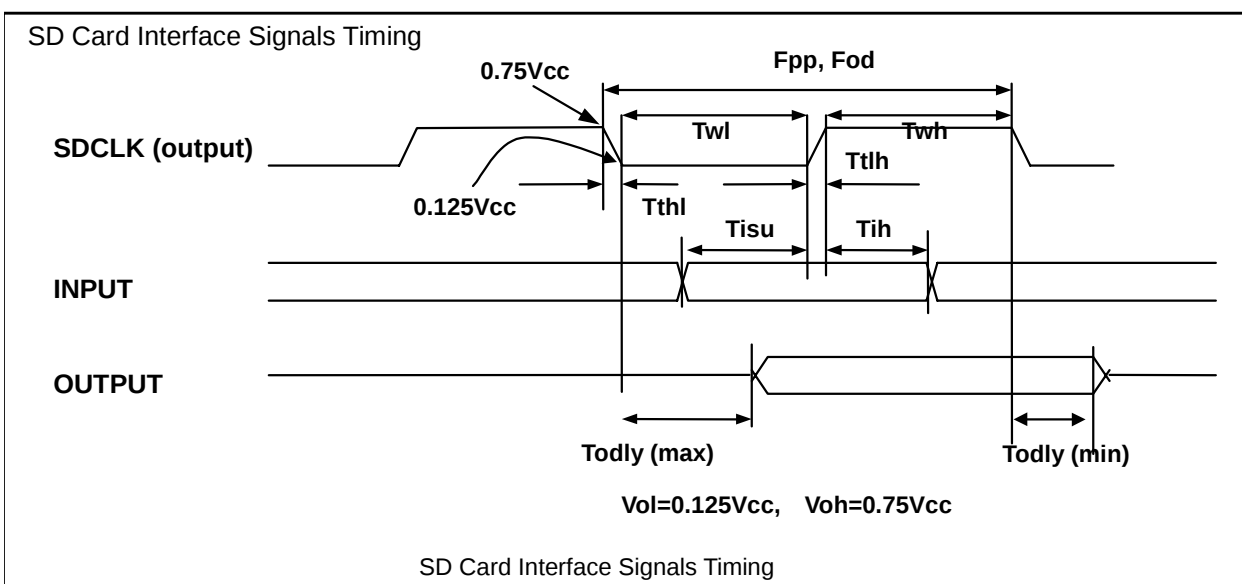




## 5.3.3 SD Card Interface Signal AC Characteristics

(VCC=3.0-3.6V, Ta=0-70°C)

| Symbol | Parameter                           | Min | Max | Unit | Notes   |
|--------|-------------------------------------|-----|-----|------|---------|
|        | SDCD[3:0], SDCMD, SDCLK             |     |     |      |         |
| Fpp    | Clock frequency Data Transfer Mode  | 0   | 16  | MHz  | Cl=25pF |
| Fod    | Clock frequency Identification Mode | 0   | 256 | KHz  | Cl=25pF |
| Twl    | Clock Low time                      | 30  | —   | ns   | Cl=25pF |
| Twh    | Clock High time                     | 30  | —   | ns   | Cl=25pF |
| Ttlh   | Clock fall time                     | —   | 10  | ns   | Cl=25pF |
| Tthl   | Clock rise time                     | —   | 10  | ns   | Cl=25pF |
| Tisu   | Input set-up time                   | 10  | —   | ns   | Cl=25pF |
| Tih    | Input hold time                     | 10  | —   | ns   | Cl=25pF |
| Todly  | Output delay time                   | —   | 25  | ns   | Cl=25pF |

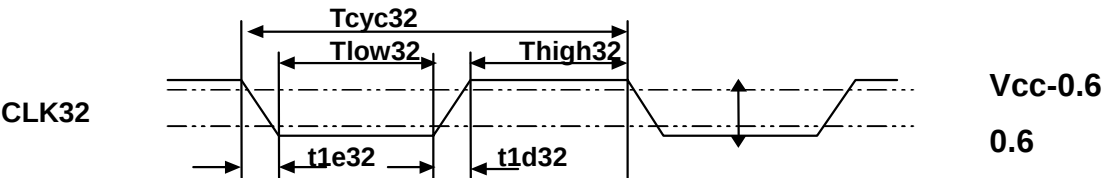


5.3.4 System Interface Signal AC Characteristics

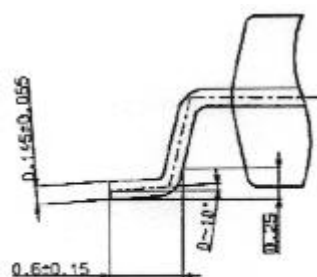
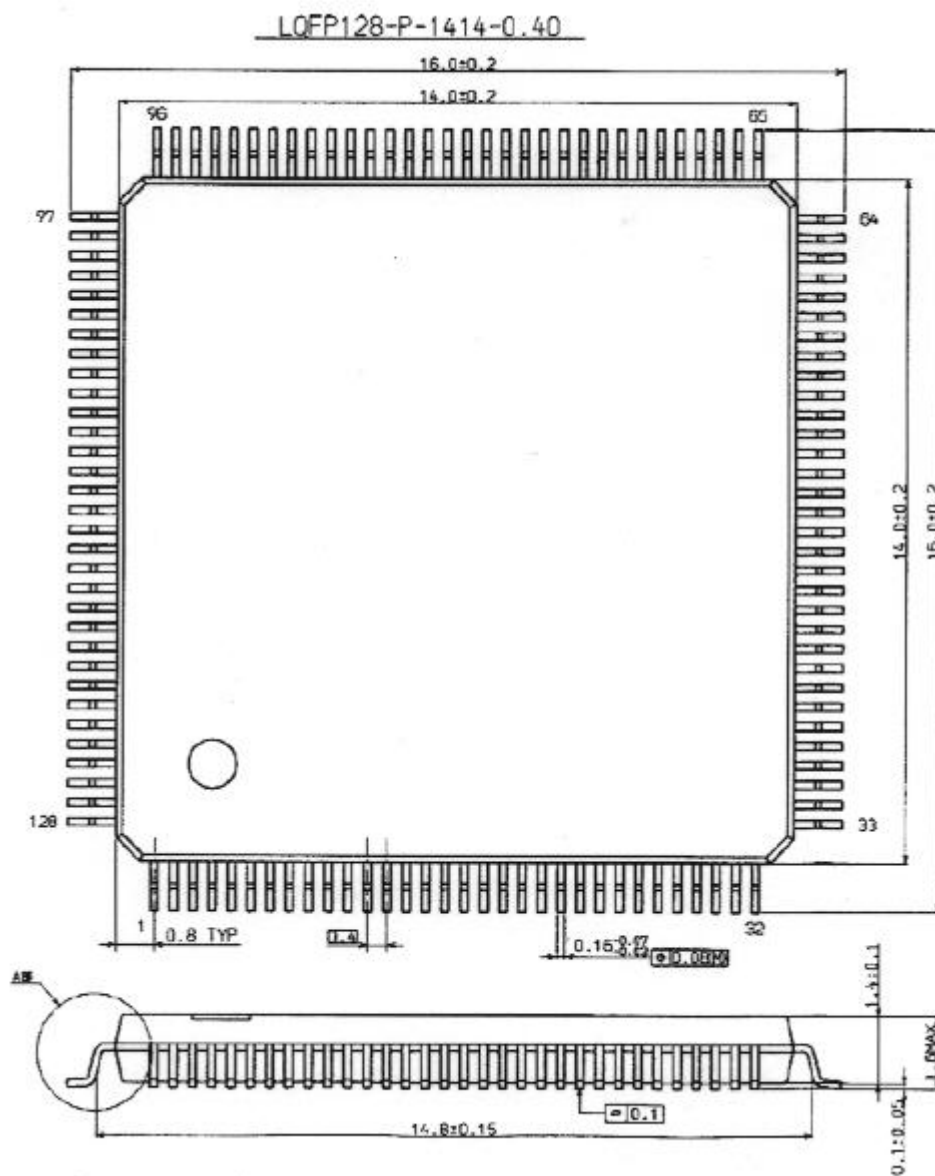
CLK32 AC Characteristics (VCC=3.0-3.6V, Ta=0-70°C)

| Symbol  | Parameter                     | Min | Max | Unit | Notes |
|---------|-------------------------------|-----|-----|------|-------|
|         | CLK32                         |     |     |      |       |
| Tcyc32  | CLK cycle time                | 31  | ∞   | μs   |       |
| Thigh32 | CLK High time                 | 11  | —   | μs   |       |
| Tlow32  | CLK Low time                  | 11  | —   | μs   |       |
| t1d32   | Slew Rate, CLK32 Rising Edge  | 10  | —   | ns   |       |
| t1e32   | Slew Rate, CLK32 Falling Edge | 10  | —   | ns   |       |

CLK32 Timing



## 6 Package outline



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