



VCISO BASED CLOCK PLL WITH AUTO SWITCH

The M2041 is a VCISO (Voltage Controlled SAW Oscillator) based clock generator PLL. It is designed for clock protection, frequency translation and jitter attenuation in optical networking systems supporting 2.5-10Gb data rates. It features dual differential inputs with two modes of input selection: manual and automatic upon clock failure. The clock multiplication ratios and output divider ratio are pin selectable. External loop components allow the tailoring of PLL loop response.

- Integrated SAW (surface acoustic wave) delay line; output frequencies of 125 to 700 MHz; outputs VCISO frequency or 1/4; pin-configurable dividers
- Loss of Lock (LOL) indicator output
- Narrow Bandwidth control input (NBW pin); Initialization (INIT) input overrides NBW at power-up
- Dual reference clock inputs support LVDS, LVPECL, LVC MOS, LV TTL
- AutoSwitch (AUTO pin) - automatic (non-revertive) reference clock reselection upon clock failure; Hitless Switching (HS) options with or without Phase Build-out (PBO) enable SONET (GR-253) /SDH (G.813) MTIE and TDEV compliance
- Acknowledge pin (REF_ACK pin) indicates the actively selected reference input
- Dual differential LVPECL outputs
- Low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz or 50kHz to 80MHz)
- Single 3.3V power supply
- Small 9 x 9 mm SMT (surface mount) package

M2041
(Top View)

Pin 1: GND
Pin 2: GND
Pin 3: GND
Pin 4: OP_IN
Pin 5: OP_OUT
Pin 6: nVC
Pin 7: VC
Pin 8: OP_OUT
Pin 9: nOP_IN
Pin 10: VCC
Pin 11: VCC
Pin 12: FOUT1
Pin 13: nFOUT1
Pin 14: GND
Pin 15: FOUT0
Pin 16: nFOUT0
Pin 17: INIT
Pin 18: P_SEL
Pin 19: 19
Pin 20: nDIF_REF1
Pin 21: DIF_REF1
Pin 22: REF_SEL
Pin 23: nDIF_REF0
Pin 24: DIF_REF0
Pin 25: AUTO
Pin 26: GND
Pin 27: 27
Pin 28: FIN_SEL0
Pin 29: MR_SEL
Pin 30: REF_ACK
Pin 31: LOL
Pin 32: NBW
Pin 33: VCC
Pin 34: DNC
Pin 35: DNC
Pin 36: DNC

Input Reference Clock (MHz)	PLL Ratio (Pin Selectable)	Output Clock (MHz) (Pin Selectable)
19.44	32	622.08
77.76	8	or
155.52	4	155.52
622.08	1	

* Specify VCSO center frequency at time of order.

