

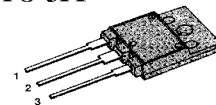
FEATURES

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25 μ A (Max.) @ $V_{DS} = 900V$
- Low $R_{DS(ON)}$: 1.247 Ω (Typ.)

$$BV_{DSS} = 900 V$$

$$R_{DS(on)} = 1.6 \Omega$$

$$I_D = 5.5 A$$

TO-3PF

1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	900	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	5.5	A
	Continuous Drain Current ($T_C=100^\circ C$)	3.5	
I_{DM}	Drain Current-Pulsed ①	32	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	801	mJ
I_{AR}	Avalanche Current ①	5.5	A
E_{AR}	Repetitive Avalanche Energy ①	9.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.5	V/ns
P_D	Total Power Dissipation ($T_C=25^\circ C$)	95	W
	Linear Derating Factor	0.76	W/ $^\circ C$
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8 " from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.32	$^\circ C / W$
$R_{\theta JA}$	Junction-to-Ambient	--	40	

Electrical Characteristics (T_C=25 °C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV _{DSS}	Drain-Source Breakdown Voltage	900	--	--	V	V _{GS} =0V, I _D =250μA
ΔBV/ΔT _J	Breakdown Voltage Temp. Coeff.	--	1.06	--	V/ °C	I _D =250μA See Fig 7
V _{GS(th)}	Gate Threshold Voltage	2.0	--	3.5	V	V _{DS} =5V, I _D =250μA
I _{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V _{GS} =30V
	Gate-Source Leakage , Reverse	--	--	-100	nA	V _{GS} =-30V
I _{DSS}	Drain-to-Source Leakage Current	--	--	25	μA	V _{DS} =900V
		--	--	250	μA	V _{DS} =720V, T _C =125 °C
R _{DS(on)}	Static Drain-Source On-State Resistance	--	--	1.6	Ω	V _{GS} =10V, I _D =2.75A ④*
g _{fs}	Forward Transconductance	--	5.0	--	Ω	V _{DS} =50V, I _D =2.75A ④
C _{iss}	Input Capacitance	--	2070	2690	pF	V _{GS} =0V, V _{DS} =25V, f = 1MHz See Fig 5
C _{oss}	Output Capacitance	--	185	215		
C _{rss}	Reverse Transfer Capacitance	--	78	90		
t _{d(on)}	Turn-On Delay Time	--	25	60	ns	V _{DD} =450V, I _D =8A, R _G =10Ω See Fig 13 ④ ⑤
t _r	Rise Time	--	38	85		
t _{d(off)}	Turn-Off Delay Time	--	122	255		
t _f	Fall Time	--	41	90		
Q _g	Total Gate Charge	--	94	123	nC	V _{DS} =720V, V _{GS} =10V, I _D =8A See Fig 6 & Fig 12 ④ ⑤
Q _{gs}	Gate-Source Charge	--	14.9	--		
Q _{gd}	Gate-Drain("Miller") Charge	--	43.5	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I _S	Continuous Source Current	--	--	5.5	A	Integral reverse pn-diode in the MOSFET
I _{SM}	Pulsed-Source Current ①	--	--	32		
V _{SD}	Diode Forward Voltage ④	--	--	1.4	V	T _J =25 °C , I _S =5.5A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	620	--	ns	T _J =25 °C , I _F =8A di _F /dt=100A/μs ④
Q _{rr}	Reverse Recovery Charge	--	9.3	--	μC	

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=50mH, I_{AS}=5.5A, V_{DD}=50V, R_G=27Ω, Starting T_J=25 °C
- ③ I_{SD} < 8A, di/dt < 170A/ μs, V_{DD} < BV_{DSS}, Starting T_J=25 °C
- ④ Pulse Test : Pulse Width = 250 μs, Duty Cycle < 2%
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

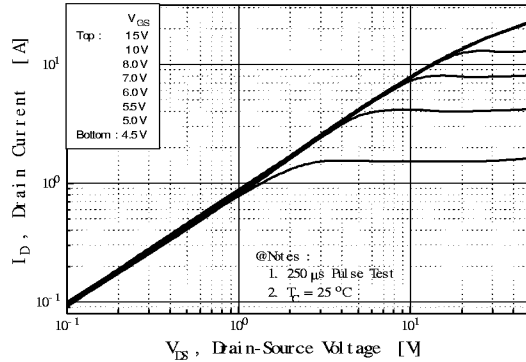


Fig 2. Transfer Characteristics

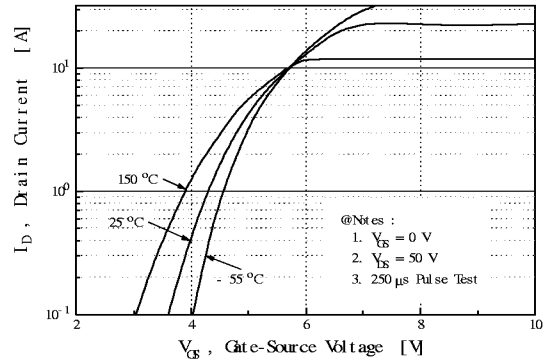


Fig 3. On-Resistance vs. Drain Current

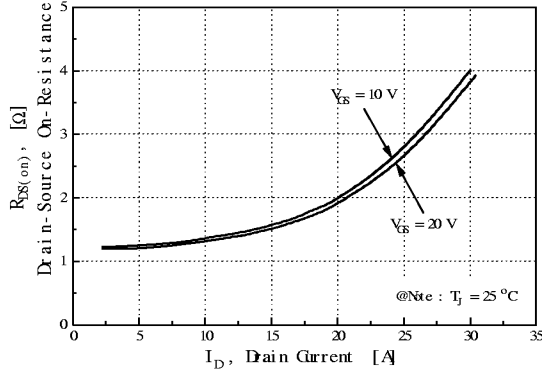


Fig 4. Source-Drain Diode Forward Voltage

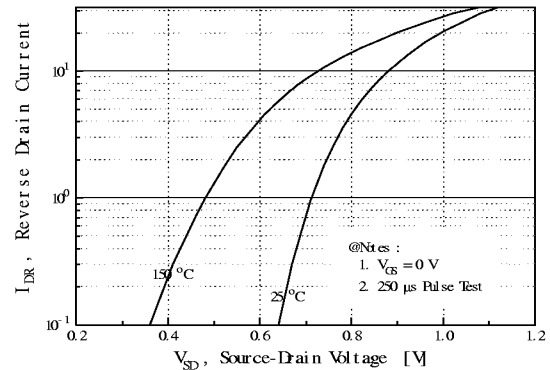


Fig 5. Capacitance vs. Drain-Source Voltage

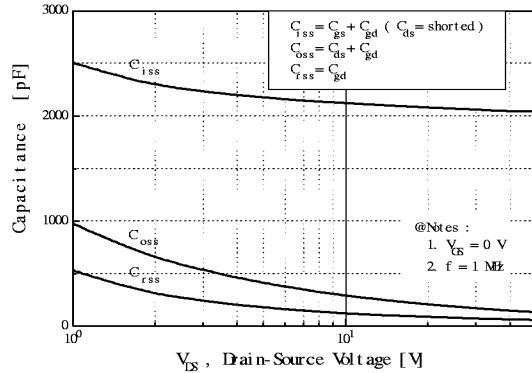
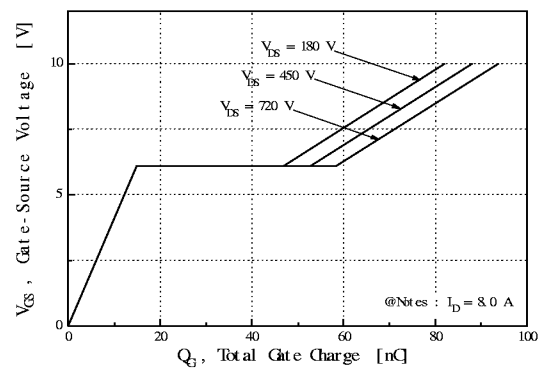
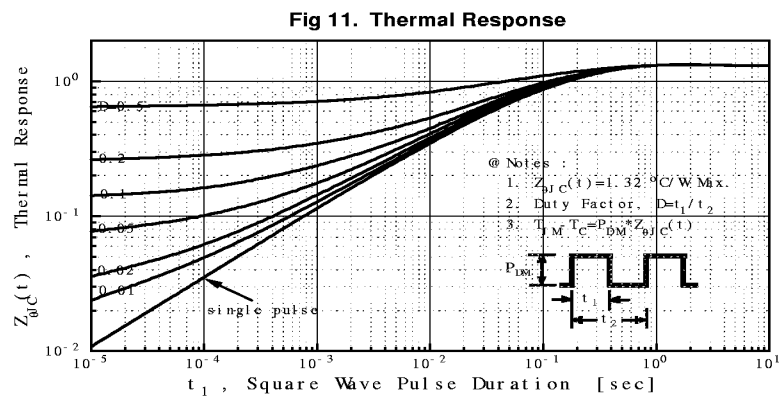
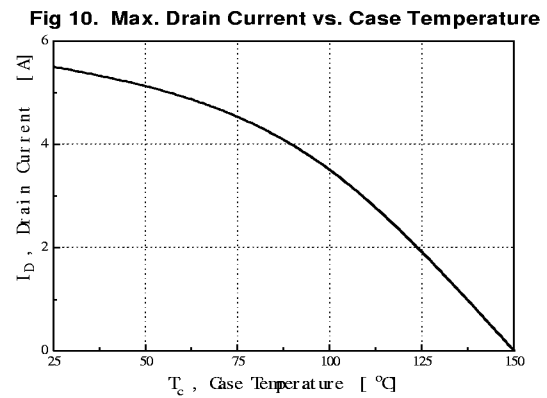
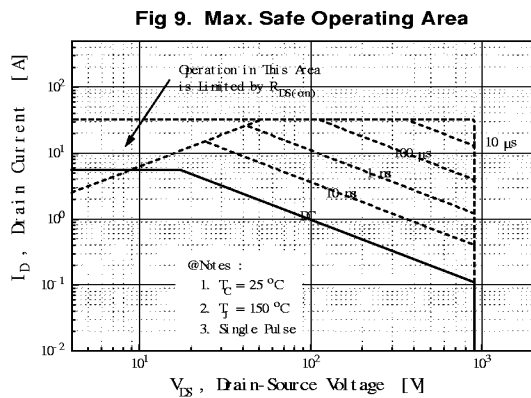
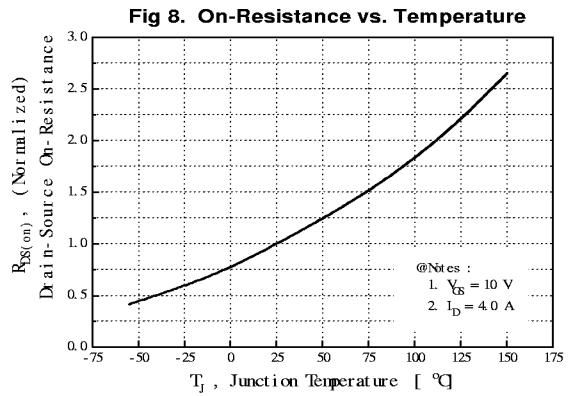
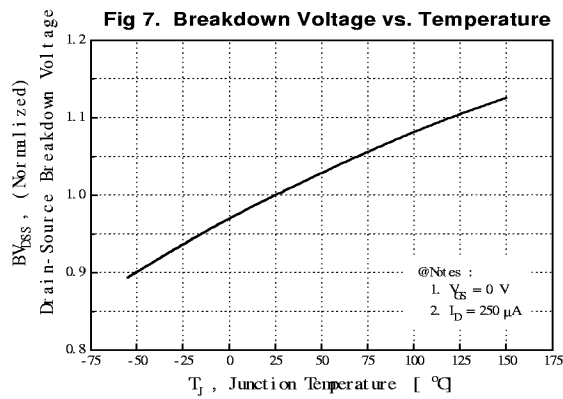


Fig 6. Gate Charge vs. Gate-Source Voltage



SSF8N90A

N-CHANNEL POWER MOSFET



FAIRCHILD
SEMICONDUCTOR™

Fig 12. Gate Charge Test Circuit & Waveform

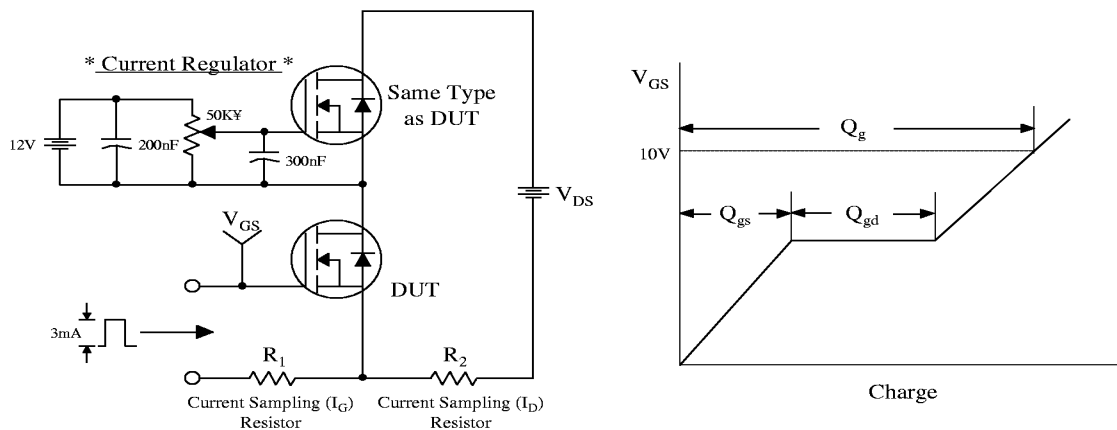


Fig 13. Resistive Switching Test Circuit & Waveforms

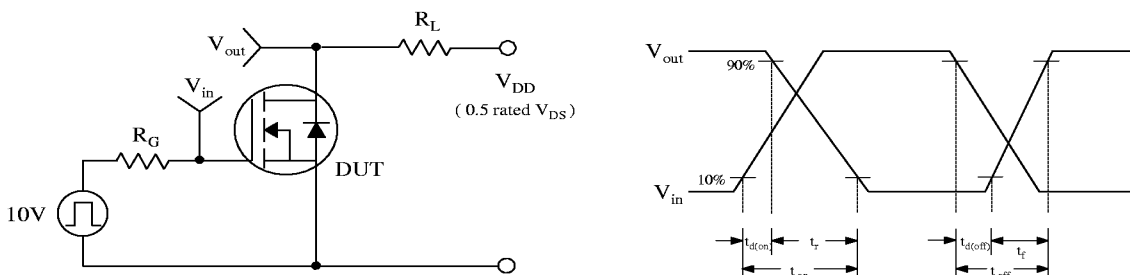
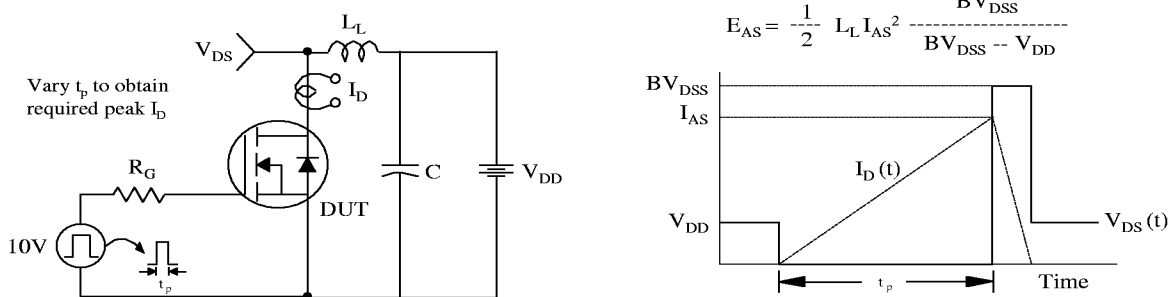


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



The diagram shows a half-bridge inverter circuit. The top MOSFET is the **DUT** (Device Under Test). Its gate is connected to the positive rail, and its source is connected to the negative rail. The drain is connected to the positive rail through a switch labeled **+**. The drain is also connected to the negative rail through a switch labeled **--**. The voltage across the DUT is V_{DS} . The current through the DUT is I_s . The bottom MOSFET is the **Driver**. Its gate is connected to the positive rail through a resistor R_G and to the negative rail through a switch labeled **+**. The drain is connected to the positive rail through a switch labeled **--**. The voltage across the Driver is V_{GS} . The current through the Driver is I_s . The output of the inverter is connected to the positive rail through an inductor L and to the negative rail through a switch labeled **+**. The voltage across the inductor is V_{DD} . The circuit is controlled by a **Duty Factor D**.

- dv/dt controlled by R_G
- I_s controlled by Duty Factor D

