i960® VH Embedded-PCI Processor

Preliminary Datasheet

Product Features

- High Performance 80960JT Core
  - Sustained One Instruction/Clock Execution
  - 16 Kbyte Two-Way Set-Associative Instruction Cache
  - 4 Kbyte Direct-Mapped Data Cache
  - Sixteen 32-Bit Global Registers
  - Sixteen 32-Bit Local Registers
  - Programmable Bus Widths: 8-, 16-, 32-Bit
  - 1 Kbyte Internal Data RAM
  - Local Register Cache (Eight Available Stack Frames)
  - Two 32-Bit On-Chip Timer Units
  - Core Clock Rate: 1x, 2x or 3x Local Bus Clock
- PCI Interface
  - Complies with PCI Local Bus Specification 2.2
  - Runs at Local Bus Clock Rate
  - 5 Volts PCI Signaling Environment
- Address Translation Unit
  - Connects Local Bus to PCI Bus
  - Inbound/Outbound Address Translation Support
  - Direct Outbound Addressing Support
- Messaging Unit
  - Four Message Registers
  - Two Doorbell Registers
- Memory Controller
  - 256 Mbytes of 32- or 36-Bit DRAM
  - Interleaved or Non-Interleaved DRAM
  - Fast Page-Mode DRAM Support
  - Extended Data Out DRAM Support
  - Two Independent Banks for SRAM / ROM / Flash (16 Mbytes/Bank; 8- or 32-Bit)
- DMA Controller
  - Two Independent Channels
  - PCI Memory Controller Interface
  - 32-Bit Local Bus Addressing
  - 64-Bit PCI Bus Addressing
  - Independent Interface to PCI Bus
  - 132 Mbyte/sec Burst Transfers to PCI and Local Buses
  - Direct Addressing to and from PCI Buses
  - Unaligned Transfers Supported in Hardware
  - Channels Dedicated to PCI Bus
- I^2C Bus Interface Unit
  - Serial Bus
  - Master/Slave Capabilities
  - System Management Functions
- 3.3 V Supply
  - 5 V Tolerant Inputs
  - TTL Compatible Outputs
- Plastic BGA* Package
  - 324 Ball-Grid Array (PBGA)

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1.0 About This Document

This is the Preliminary data sheet for the low-power (3.3 V) version of Intel's i960® VH processor ("80960VH") family.

This data sheet contains a functional overview, mechanical data (package signal locations and simulated thermal characteristics), targeted electrical specifications (simulated), and bus functional waveforms. Detailed functional descriptions other than parametric performance is published in the *i960® VH Processor Developer's Manual*.

1.1 Solutions960® Program

Intel's *Solutions960®* program features a wide variety of development tools which support the i960 processor family. Many of these tools are developed by partner companies; some are developed by Intel, such as profile-driven optimizing compilers. For more information on these products, contact your local Intel representative.

1.2 Terminology

In this document, the following terms are used:

- local bus refers to the 80960VH's internal local bus, not the PCI local bus.
- *primary PCI bus* is the 80960VH's internal PCI bus which conforms to PCI SIG specifications.
- 80960 core refers to the 80960JT processor which is integrated into the 80960VH.

1.3 Additional Information Sources

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

Call 1-800-879-4683 or visit Intel's website at http://www.intel.com.

Table 1. Related Documentation

Document Title	Order / Contact
i960® VH Processor Developer's Manual	Intel Order # 273173
i960® Jx Microprocessor User's Guide	Intel Order # 272483
PCI Local Bus Specification, revision 2.2	PCI Special Interest Group 1-800-433-5177
I^2C Peripherals for Microcontrollers	Philips Semiconductor

2.0 Functional Overview

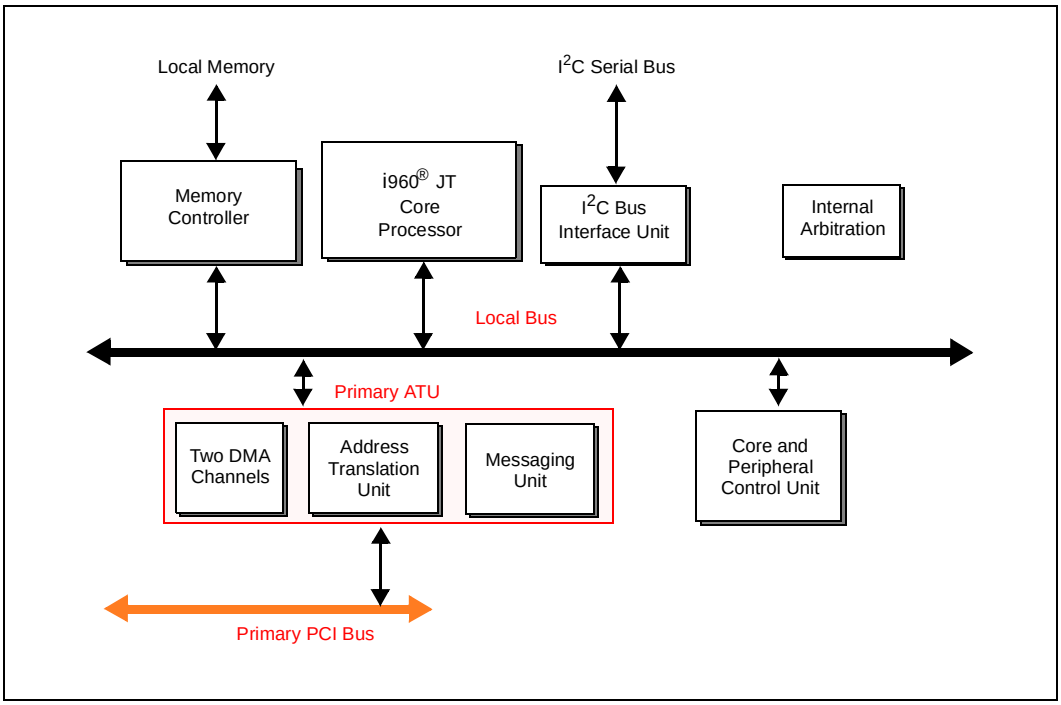
As indicated in Figure 1, the 80960VH combines many features with the 80960JT to create a highly integrated processor. Subsections following the figure briefly describe the main features; for detailed functional descriptions, refer to the *i960® VH Processor Developer's Manual*.

The PCI bus is an industry standard, high performance, low latency system bus that operates up to 132 Mbyte/sec. The 80960VH is fully compliant with the *PCI Local Bus Specification*, revision 2.2. Function 0 is the address translation unit.

The 80960VH, object code compatible with the i960 core processor, is capable of sustained execution at the rate of one instruction per clock.

The local bus, a 32-bit multiplexed burst bus, is a high-speed interface to system memory and I/O. A full complement of control signals simplifies the connection of the 80960VH to external components. Physical and logical memory attributes are programmed via memory-mapped control registers (MMRs), an extension not found on the i960 Kx, Sx or Cx processors. Physical and logical configuration registers enable the processor to operate with all combinations of bus width and data object alignment.

Figure 1. Product Name Functional Block Diagram



2.1 Key Functional Units

2.1.1 DMA Controller

The DMA Controller supports low-latency, high-throughput data transfers between PCI bus agents and 80960 local memory. Two separate DMA channels accommodate data transfers for the primary PCI bus. The DMA Controller supports chaining and unaligned data transfers. It is programmable only through the i960 core processor.

2.1.2 Address Translation Unit

The Address Translation Unit (ATU) allows PCI transactions direct access to the 80960VH local memory. The 80960VH has direct access to the PCI bus. The ATU supports transactions between PCI address space and 80960VH address space.

Address translation is controlled through programmable registers accessible from the PCI interface and the 80960 core. Dual access to registers allows flexibility in mapping the two address spaces.

2.1.3 Messaging Unit

The Messaging Unit (MU) provides data transfer between the PCI system and the 80960VH. It uses interrupts to notify each system when new data arrives. The MU has two messaging mechanisms. Each allows a host processor or external PCI device and the 80960VH to communicate through message passing and interrupt generation. The two mechanisms are Message Registers and Doorbell Registers.

2.1.4 Memory Controller

The Memory Controller allows direct control of external memory systems, including DRAM, SRAM, ROM and Flash Memory. It provides a direct connect interface to memory that typically does not require external logic. It features programmable chip selects, a wait state generator and byte parity. External memory can be configured as PCI addressable memory.

2.1.5 Core and Peripheral Unit

The Core and Peripheral Unit allows software to control the 80960VH through the primary PCI bus. For example, the 80960 processor core and the 80960VH local bus can be reset via the PCI bus.

2.1.6 I^2C Bus Interface Unit

The I^2C (Inter-Integrated Circuit) Bus Interface Unit allows the 80960 core to serve as a master and slave device residing on the I^2C bus. The I^2C bus is a serial bus developed by Philips Semiconductor consisting of a two pin interface. The bus allows the 80960VH to interface to other I^2C peripherals and microcontrollers for system management functions. It requires a minimum of hardware for an economical system to relay status and reliability information on the I/O subsystem to an external device. For more information, see *I^2C Peripherals for Microcontrollers* (Philips Semiconductor).

2.2 i960® Core Features (80960JT)

The processing power of the 80960VH comes from the 80960JT processor core. The 80960JT is a new, scalar implementation of the 80960 Core Architecture. Figure • shows a block diagram of the 80960JT Core processor.

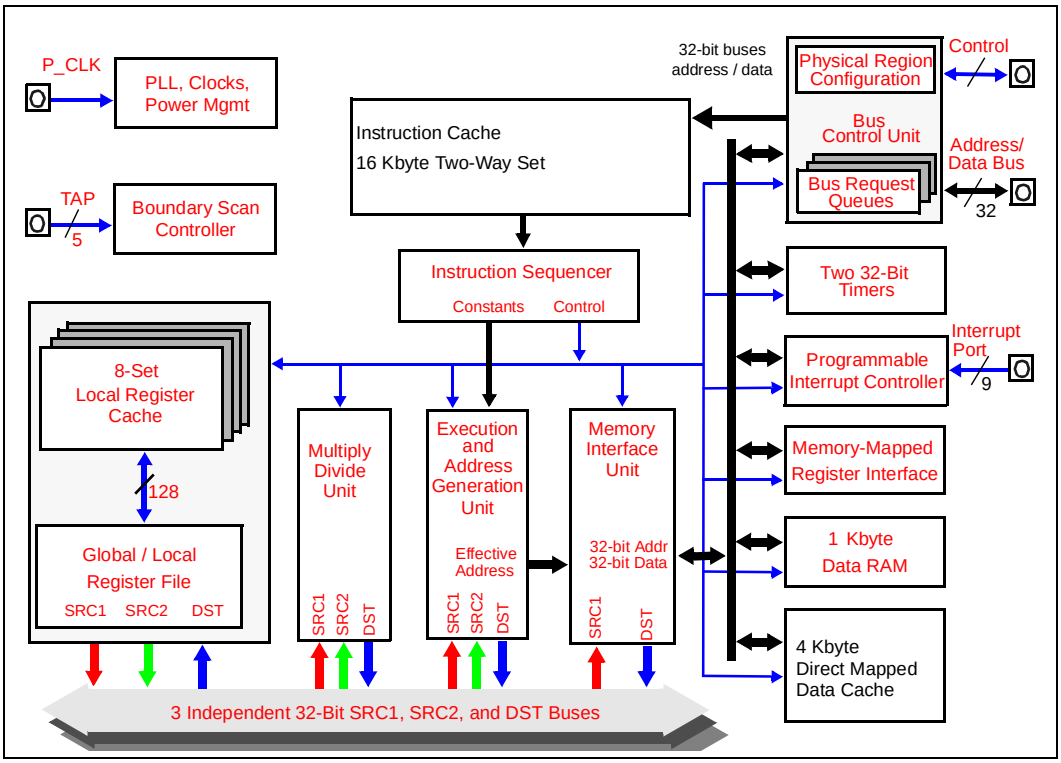
Factors that contribute to the 80960 family core's performance include:

- Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- Efficient instruction pipeline minimizes pipeline break latency
- Register and resource scoreboarding allow overlapped instruction execution
- 128-bit register bus speeds local register caching
- 16 Kbyte two-way set-associative, integrated instruction cache
- 4 Kbyte direct-mapped, integrated data cache
- 1 Kbyte integrated data RAM delivers zero wait state program data

The 80960 core operates out of its own 32-bit address space, which is independent of the PCI address space. The local bus memory can be:

- Made visible to the PCI address space
- Kept private to the 80960 core
- Allocated as a combination of the two

Figure 2. 80960JT Core Block Diagram



2.2.1 Burst Bus

A 32-bit high-performance bus controller interfaces the 80960VH to external memory and peripherals. The Bus Control Unit fetches instructions and transfers data on the local bus at the rate of up to four 32-bit words per six clock cycles. The external address/data bus is multiplexed.

Users may configure the 80960VH's bus controller to match an application's fundamental memory organization. Physical bus width is programmable for up to eight regions. Data caching is programmed through a group of logical memory templates and a defaults register. The Bus Control Unit's features include:

- Multiplexed external bus minimizes pin count
- 32-, 16- and 8-bit bus widths simplify I/O interfaces
- External ready control for address-to-data, data-to-data and data-to-next-address wait state types
- Little endian byte ordering
- Unaligned bus accesses performed transparently
- Three-deep load/store queue decouples the bus from the 80960 core

Upon reset, the 80960VH conducts an internal self test. Before executing its first instruction, it performs an external bus confidence test by performing a checksum on the first words of the Initialization Boot Record.

2.2.2 Timer Unit

The timer unit (TU) contains two independent 32-bit timers that are capable of counting at several clock rates and generating interrupts. Each is programmed by use of the Timer Unit registers. These memory-mapped registers are addressable on 32-bit boundaries. The timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the 80960VH's interrupt controller. The TU can generate a fault when unauthorized writes from user mode are detected.

2.2.3 Priority Interrupt Controller

Low interrupt latency is critical to many embedded applications. As part of its highly flexible interrupt mechanism, the 80960VH exploits several techniques to minimize latency:

- Interrupt vectors and interrupt handler routines can be reserved on-chip
- Register frames for high-priority interrupt handlers can be cached on-chip
- The interrupt stack can be placed in cacheable memory space

2.2.4 Faults and Debugging

The 80960VH employs a comprehensive fault model. The processor responds to faults by making implicit calls to a fault handling routine. Specific information collected for each fault allows the fault handler to diagnose exceptions and recover appropriately.

The processor also has built-in debug capabilities. Via software, the 80960VH may be configured to detect as many as seven different trace event types. Alternatively, **mark** and **fmark** instructions can generate trace events explicitly in the instruction stream. Hardware breakpoint registers are also available to trap on execution and data addresses.

2.2.5 On-Chip Cache and Data RAM

External memory subsystems often impose substantial wait state penalties. The 80960VH integrates considerable storage resources on-chip to decouple CPU execution from the external bus by including a 16 Kbyte instruction cache, a 4 Kbyte data cache and 1 Kbyte data RAM.

2.2.6 Local Register Cache

The 80960VH rapidly allocates and deallocates local register sets during context switches. The processor needs to flush a register set to the stack only when it saves more than seven sets to its local register cache.

2.2.7 Test Features

The 80960VH incorporates numerous features that enhance the user's ability to test both the processor and the system to which it is attached. These features include ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG).

The 80960VH provides testability features compatible with IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std. 1149.1).

One of the boundary scan instructions, HIGHZ, forces the processor to float all its output pins (ONCE mode). ONCE mode can also be initiated at reset without using the boundary scan mechanism.

ONCE mode is useful for board-level testing. This feature allows a mounted 80960VH to electrically "remove" itself from a circuit board. This mode allows system-level testing where a remote tester can exercise the processor system.

The test logic does not interfere with component or system behavior and ensures that components function correctly, and also the connections between various components are correct.

The JTAG Boundary Scan feature is an alternative to conventional "bed-of-nails" testing. It can examine connections that might otherwise be inaccessible to a test system.

2.2.8 Memory-Mapped Control Registers

The 80960VH is compliant with 80960 family architecture and has the added advantage of memory-mapped, internal control registers not found on the 80960Kx, Sx or Cx processors. This feature provides software an interface to easily read and modify internal control registers.

Each memory-mapped, 32-bit register is accessed via regular memory-format instructions. The processor ensures that these accesses do not generate external bus cycles.

2.2.9 Instructions, Data Types and Memory Addressing Modes

As with all 80960 family processors, the 80960VH instruction set supports several different data types and formats:

- Bit
- Bit fields
- Integer (8-, 16-, 32-, 64-bit)
- Ordinal (8-, 16-, 32-, 64-bit unsigned integers)
- Triple word (96 bits)
- Quad word (128 bits)

The 80960VH provides a full set of addressing modes for C and assembly:

- Two Absolute modes
- Five Register Indirect modes
- Index with displacement mode
- IP with displacement mode

Table 2 shows the available instructions.

Table 2. 80960VH Instruction Set

Data Movement	Arithmetic	Logical	Bit, Bit Field and Byte
Load Store Move Conditional Select Load Address	Add Subtract Multiply Divide Remainder Modulo Shift Extended Shift Extended Multiply Extended Divide Add with Carry Subtract with Carry Conditional Add Conditional Subtract Rotate	And Not And And Not Or Exclusive Or Not Or Or Not Nor Exclusive Nor Not Nand	Set Bit Clear Bit Not Bit Alter Bit Scan For Bit Span Over Bit Extract Modify Scan Byte for Equal Byte Swap
Comparison	**Branch**	**Call/Return**	**Fault**
Compare Conditional Compare Compare and Increment Compare and Decrement Test Condition Code Check Bit	Unconditional Branch Conditional Branch Compare and Branch	Call Call Extended Call System Return Branch and Link	Conditional Fault Synchronize Faults
Debug	**Processor Management**	**Atomic**	
Modify Trace Controls Mark Force Mark	Flush Local Registers Modify Arithmetic Controls Modify Process Controls Halt System Control Cache Control Interrupt Control	Atomic Add Atomic Modify	

3.0 Package Information

3.1 Package Introduction

The 80960VH is offered in a Plastic Ball Grid Array (PBGA) package. This is a perimeter array package with five rows of ball connections in the outer area of the package. See Figure , (pg. 26).

Section 3.1.1, Functional Signal Definitions describes signal function. Section 3.1.2, 324-Lead PBGA Package defines the signal and ball locations.

3.1.1 Functional Signal Definitions

Table 3 presents the legend for interpreting the Type Field in the following tables. Table 4 defines signals associated with the bus interface. Table 5 defines signals associated with basic control and test functions. Table 6 defines signals associated with the Interrupt Unit. Table 7 defines PCI signals. Table 8 defines Memory Controller signals. Table 9 defines DMA, and I^2C signals. Table 10 defines clock signals.

Table 3. Signal Type Definition

Symbol	Description
I	Input signal only.
O	Output signal only.
I/O	Signal can be either an input or output.
OD	Open Drain signal.
–	Signal must be connected as described.
S (...)	Synchronous. Inputs must meet setup and hold times relative to P_CLK. S(E) Edge sensitive input S(L) Level sensitive input
A (...)	Asynchronous. Inputs may be asynchronous relative to P_CLK. A(E) Edge sensitive input A(L) Level sensitive input
R (...)	While the P_RST# signal is asserted, the signal: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Q) is a valid output R(Z) Floats R(H) is pulled up to V_{CC} R(X) is driven to an unknown state

Table 3. Signal Type Definition

Symbol	Description
H (...)	While the is in the hold state, the signal: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Q) Maintains previous state or continues to be a valid output H(Z) Floats
P (...)	While the 80960VH is halted, the signal: P(1) is driven to V_{CC} P(0) is driven to V_{SS} P(Q) Maintains previous state or continues to be a valid output
K (...)	While the PCI Bus is in park mode, the pin: K(Z) Floats K(Q) Maintains previous state or continues to be a valid output

Table 4. Signal Descriptions (Sheet 1 of 4)

NAME	TYPE	DESCRIPTION
AD31:0	**I/O** S(L) R(Z) H(Z) P(Q)	**ADDRESS / DATA BUS** carries 32-bit physical addresses and 8-, 16- or 32-bit data to and from memory. During an address (T_a) cycle, bits 2-31 contain a physical word address (bits 0-1 indicate SIZE; see below). During a data (T_d) cycle, read or write data is present on one or more contiguous bytes, comprising AD31:24, AD23:16, AD15:8 and AD7:0. During write operations, unused signals are driven to determinate values. **SIZE**, which comprises bits 0-1 of the AD lines during a T_a cycle, specifies the number of data transfers during the bus transaction on the local bus. When the DMA or ATUs initiate data transfers, transfer size shown below is **not** valid. **AD1** **AD0** **Bus Transfers** 0 0 1 Transfer 0 1 2 Transfers 1 0 3 Transfers 1 1 4 Transfers When the 80960VH enters Halt mode and the previous bus operation was: • write — AD31:2 are driven with the last data value on the AD bus. • read — AD31:2 are driven with the last address value on the AD bus. Typically, AD1:0 reflect the SIZE information of the last bus transaction (either instruction fetch or load/store) that was executed before entering Halt mode.
ADS#	**O** R(1) H(Z) P(1)	**ADDRESS STROBE** indicates a valid address and the start of a new bus access. The processor asserts ADS# for the entire T_a cycle. External bus control logic typically samples ADS# at the end of the cycle.
ALE	**O** R(0) H(Z) P(0)	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. ALE is asserted during a T_a cycle and deasserted before the beginning of the T_d state. It is active HIGH and floats to a high impedance state during a hold cycle (T_h).
BLAST#	**O** **R(H)** H(Z) P(1)	**BURST LAST** indicates the last transfer in a bus access. BLAST# is asserted in the last data transfer of burst and non-burst accesses. BLAST# remains active while wait states are detected via the LRDYRCV# or RDYRCV# signal on the memory controller. BLAST# becomes inactive after the final data transfer in a bus cycle. BLAST# has a weak internal pullup which is active during reset to ensure normal operation when the signal is not connected. 0 = Last Data Transfer 1 = Not the Last Data Transfer

Table 4. Signal Descriptions (Sheet 2 of 4)

NAME	TYPE	DESCRIPTION
BE3:0#	**O** R(1) H(Z) P(1)	**BYTE ENABLES** select which of up to four data bytes on the bus participate in the current bus access. Byte enable encoding depends on the bus width of the memory region accessed: *32-bit bus:* BE3# enables data on AD31:24 BE2# enables data on AD23:16 BE1# enables data on AD15:8 BE0# enables data on AD7:0 *16-bit bus:* BE3# becomes Byte High Enable (enables data on AD15:8) BE2# is not used (state is high) BE1# becomes Address Bit 1 (A1) (increments with the assertion of LRDY# or RDYRCV#) BE0# becomes Byte Low Enable (enables data on AD7:0) *8-bit bus:* BE3# is not used (state is high) BE2# is not used (state is high) BE1# becomes Address Bit 1 (A1) (increments with the assertion of LRDY# or RDYRCV#) BE0# becomes Address Bit 0 (A0) (increments with the assertion of LRDY# or RDYRCV#) The processor asserts byte enables, byte high enable and byte low enable during T_a. Since unaligned bus requests are split into separate bus transactions, these signals do not toggle during a burst (32-bit bus only) from the i960 core processor; they do toggle for DMA and ATU cycles. They remain active through the last T_d cycle.
DEN#	**O** **R(H)** H(Z) P(1)	**DATA ENABLE** indicates data transfer cycles during a bus access. DEN# is asserted at the start of the first data cycle in a bus access and deasserted at the end of the last data cycle. DEN# is used with DT/R# to provide control for data transceivers connected to the data bus. DEN# has a weak internal pullup which is active during reset to ensure normal operation when the signal is not connected. 0 = Data Cycle 1 = Not a Data Cycle
D/C#/ RST_MODE#	**I/O** R(H) H(Z) P(Q)	**DATA/CODE/RESET_MODE** indicates that a bus access is a data access or an instruction access. D/C# has the same timing as W/R#. 0 = Instruction Access 1 = Data Access The RST_MODE# signal is sampled at primary PCI bus reset to determine whether the 80960 core is to be held in reset. When RST_MODE# is high, the 80960VH begins initialization immediately following the deassertion of P_RST#. When RST_MODE# is low, the 80960 core remains in reset until the 80960 core reset bit is cleared in the Reset/Retry control register. This signal has a weak internal pullup that is active during reset to ensure normal operation when the signal is left unconnected. 0 = RST_MODE enabled 1 = RST_MODE not enabled While the 80960 core is in reset, all peripherals may be accessed from the primary PCI bus depending on the status of the WIDTH/HLTD1/RETRY/ signal.
DT/R#	**O** R(0) H(Z) P(Q)	**DATA TRANSMIT/RECEIVE** indicates the direction of data transfer to and from the address/data bus. It is low during T_a and T_w/T_d cycles for a read; it is high during T_a and T_w/T_d cycles for a write. DT/R# never changes state when DEN# is asserted. 0 = Receive 1 = Transmit

Table 4. Signal Descriptions (Sheet 3 of 4)

NAME	TYPE	DESCRIPTION
LOCK#/ONCE#	**I/O** S(L) R(H) H(Z) P(Q)	**BUS LOCK** indicates that an atomic read-modify-write operation is in progress. The LOCK# output is asserted in the first clock of an atomic operation and deasserted in the last data transfer of the sequence. The processor does not grant HOLDA while asserting LOCK#. This prevents external agents from accessing memory involved in semaphore operations. 0 = Atomic Read-Modify-Write in Progress 1 = No Atomic Read-Modify-Write in Progress **ONCE MODE:** The processor samples the ONCE input during reset. When ONCE# is asserted LOW at the end of reset, the processor enters ONCE mode, stops all clocks and floats all output signals. This signal has a weak internal pullup which is active during reset to ensure normal operation when the signal is not connected. 0 = ONCE Mode Enabled 1 = ONCE Mode Not Enabled
LRDYRCV#/ STEST	**I/O** R(H) H(Q) P(Q)	**LOCAL READY/RECOVER**, generated by the 80960VH's memory controller unit, is an output version of the READY/RECOVER (RDYRCV#) signal. Refer to the RDYRCV# signal description. **SELF TEST** enables or disables the processor's internal self-test feature at initialization. STEST is examined at the end of P_RST#. When STEST is asserted, the processor performs its internal self-test and the external bus confidence test. When STEST is deasserted, the processor performs only the external bus confidence test. This signal has a weak internal pullup which is active during reset to ensure normal operation. 0 = Self Test Disabled 1 = Self Test Enabled
HOLD	**I** S(L)	**HOLD** is a request from an external bus master to acquire the bus. When the processor receives HOLD and grants bus control to another master, it asserts HOLDA, floats the address/data and control lines and enters the T_h state. When HOLD is deasserted, the processor deasserts HOLDA and enters either the T_i or T_a state, resuming control of the address/data and control lines. See Figure , (pg. 61). 0 = No Hold Request 1 = Hold Requested
HOLDA	**O** R(0) H(1) P(Q)	**HOLD ACKNOWLEDGE** indicates to an external bus master that the processor has relinquished bus control. The processor can grant HOLD requests and enter the T_h state and while halted as well as during regular operation. See Figure , (pg. 61). 0 = No Hold Acknowledged 1 = Hold Acknowledged
RDYRCV#	**I** S(L)	**READY/RECOVER** is only used in systems that use an external memory controller (and do not use the 80960VH's memory controller unit). This signal indicates that data on AD lines can be sampled or removed. When RDYRCV# is not asserted during a T_d cycle, the T_d cycle extends to the next cycle by inserting a wait state (T_w). 0 = Sample Data 1 = Do Not Sample Data RDYRCV# has an alternate function during the recovery (T_r) state. The processor continues to insert recovery states until it samples the signal HIGH. This gives slow external devices more time to float their buffers before the processor drives addresses. 0 = Insert Wait States 1 = Recovery Complete When using the internal memory controller, connect this signal to V_{CC} through a 2.7 KΩ resistor.

Table 4. Signal Descriptions (Sheet 4 of 4)

NAME	TYPE	DESCRIPTION
W/R#	**O** R(0) H(Z) P(Q)	**WRITE/READ** specifies during a T_a cycle whether the operation is a write or read. It is latched on-chip and remains valid during T_d cycles. 0 = Read 1 = Write
WIDTH/ HLTD0	**I/O** R(H) H(Z) P(Q)	**WIDTH** denotes the physical memory attributes for a bus transaction in conjunction with WIDTH/HLTD1/RETRY: WIDTH/HLTD1/RETRY WIDTH/HLTD0 0 0 8 Bits Wide 0 1 16 Bits Wide 1 0 32 Bits Wide 1 1 Undefined WIDTH/HLTD0 For proper operation, do not connect this signal to ground. This signal has a weak internal pullup which is active during reset to ensure normal operation. **HLTD0** signal name has no function in the 80960VH; the signal name is included for 80960JT naming convention compatibility.
WIDTH/ HLTD1/ RETRY	**I/O** R(H) H(Z) P(Q)	**WIDTH** denotes the physical memory attributes for a bus transaction in conjunction with the WIDTH/HLTD0 signal. Refer to description above. **RETRY** is sampled at primary PCI bus reset to determine when the primary PCI interface is disabled. When high, the Primary PCI interface disables PCI configuration cycles by signaling a RETRY until the Reset/Retry Control Register's Configuration Cycle Disable bit is cleared. When low, the primary PCI interface allows configuration cycles to occur. WIDTH/HLTD1/RETRY has a weak internal pullup which is active during reset to ensure normal operation when the signal is not connected. When the RST_MODE# pin is asserted, RETRY is internally forced low [inactive] regardless of its external state. **HLTD1** signal name has no function in the 80960VH; the signal name is included for 80960JT naming convention compatibility.

Table 5. Power Requirement, Processor Control and Test Signal Descriptions (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
FAIL#	**O** R(0) H(Q)	**FAIL** indicates a failure of the processor's built-in self-test performed during initialization. FAIL# is asserted immediately upon reset and toggles during self-test to indicate the status of individual tests: • When self-test passes, the processor deasserts FAIL# and commences operation from user code. • When self-test fails, the processor asserts FAIL# and then stops executing. 0 = Self Test Failed 1 = Self Test Passed
L_RST#	**O**	**LOCAL BUS RESET** notifies external devices that the local bus has reset.
TCK	**I**	**TEST CLOCK** is a CPU input that provides the clocking function for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the processor on the rising edge; data is clocked out of the processor on the falling edge.
TDI	**I** S(L)	**TEST DATA INPUT** is the serial input signal for JTAG. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pullup to ensure normal operation.

Table 5. Power Requirement, Processor Control and Test Signal Descriptions (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
TDO	**O** R(Q) H(Q) P(Q)	**TEST DATA OUTPUT** is the serial output signal for JTAG. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, TDO floats.
TMS	**I** S(L)	**TEST MODE SELECT** is sampled at the rising edge of TCK to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing. This signal has a weak internal pullup to ensure normal operation.
TRST#	**I** A(L)	**TEST RESET** asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan testing (JTAG). When using the Boundary Scan feature, connect a pulldown resistor (1.5 KΩ) between this signal and V_{SS}. When TAP is not used, this signal must be connected to V_{SS}; however, no resistor is required. The signal has a weak internal pullup which must be overcome during reset to ensure normal operation. **NOTE:** The system must ensure that TRST# is asserted after power-up to put the TAP controller in a known state. Failure to do so may cause improper processor operation.
LCDINIT#	**I**	**LCD INITIALIZATION** is a static signal used to initialize the internal logic of the LCD960 debugger. This signal has an internal pullup for normal operation.
V_{CC}	–	**POWER**. Connect to a 3.3 Volt power board plane.
V_{CC5}REF	–	**5 VOLT REFERENCE VOLTAGE.** Input is the reference voltage for the 5 V-tolerant I/O buffers. Connect this signal to +5 V for use with signals which exceed 3.3 V. When all inputs are from 3.3 V components, connect this signal to 3.3 V.
V_{SS}	–	**GROUND.** Connect to a V_{SS} board plane.
N.C.	–	**NO CONNECT**. Do not make electrical connections to these balls.
VCCPLL2:1	**I**	**PLL POWER**. For external connection to a 3.3 V V_{CC} board plane. Power to PLLs requires external filtering. See Section 4.2, VCCPLL Pin Requirements.

Table 6. Interrupt Unit Signal Descriptions

NAME	TYPE	DESCRIPTION
NMI#	I A(L)	**NON-MASKABLE INTERRUPT** causes a non-maskable interrupt event to occur. NMI# is the highest priority interrupt source and is level-detect. When NMI# is unused, it is recommended that you connect it to V_{CC}.
XINT3:0#	I A(L)	**EXTERNAL INTERRUPT**. External devices use this signal to request an interrupt service. These signals operate in dedicated mode, where each signal is assigned a dedicated interrupt level. The XINT3:0# signals can be directed as follows: **External Int. — Primary PCI — 80960 Core Processor** XINT0# ⇒ P_INTA# or XINT0# XINT1# ⇒ P_INTB# or XINT1# XINT2# ⇒ P_INTC# or XINT2# XINT3# ⇒ P_INTD# or XINT3#
XINT7:4#	I A(L)	**EXTERNAL INTERRUPT**. External devices use this signal to request an interrupt service. These signals operate in dedicated mode, where each signal is assigned a dedicated interrupt level.

NOTE:
1. PCI signal functions are summarized in this data sheet. Refer to the *PCI Local Bus Specification*, revision 2.2 for a more complete definition.

Table 7. PCI Signal Descriptions (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION[1]
P_AD31:0	I/O K(Q) R(Z)	**PRIMARY PCI ADDRESS/DATA** is the primary multiplexed PCI address and data bus.
P_C/BE3:0#	I/O K(Q) R(Z)	**PRIMARY PCI BUS COMMAND** and **BYTE ENABLE** signals are multiplexed on the same PCI signals. During an address phase, P_C/BE3:0# define the bus command. During a data phase, P_C/BE3:0# are used as byte enables.
P_DEVSEL#	I/O R(Z)	**PRIMARY PCI BUS DEVICE SELECT** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
P_FRAME#	I/O R(Z)	**PRIMARY PCI BUS CYCLE FRAME** is asserted to indicate the beginning and duration of an access on the Primary PCI bus.
P_GNT#	I R(Z)	**PRIMARY PCI BUS GRANT** indicates to the agent that access to the bus has been granted. This is a point-to-point signal.
P_IDSEL	I S(L)	**PRIMARY PCI BUS INITIALIZATION DEVICE SELECT** selects the 80960VH during a Configuration Read or Write command on the primary PCI bus.
P_INT[A:D]#	O OD R(Z)	**PRIMARY PCI BUS INTERRUPT** requests an interrupt. The assertion and deassertion of P_INTx# is asynchronous to **P_CLK**. A device asserts its P_INTx# line when requesting attention from its device driver. Once the P_INTx# signal is asserted, it remains asserted until the device driver clears the pending request. P_INTx# Interrupts are level sensitive.
P_IRDY#	I/O R(Z)	**PRIMARY PCI BUS INITIATOR READY** indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.

NOTE:
1. PCI signal functions are summarized in this data sheet; refer to the *PCI Local Bus Specification*, revision 2.2 for a more complete definition.

Table 7. PCI Signal Descriptions (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION[1]
P_LOCK#	**I** S(L)	**PRIMARY PCI BUS LOCK** indicates an atomic operation that may require multiple transactions to complete.
P_PAR	**I/O** K(Q) R(Z)	**PRIMARY PCI BUS PARITY**. This signal ensures even parity across P_AD31:0 and P_C/BE3:0. All PCI devices must provide a parity signal.
P_PERR#	**I/O** R(Z)	**PRIMARY PCI BUS PARITY ERROR** is used for reporting data parity errors during all PCI transactions except a special cycle.
P_REQ#	**O** K(Q) R(Z)	**PRIMARY PCI BUS REQUEST** indicates to the arbiter that this agent desires use of the bus. This is a point to point signal.
P_RST#	**I** A(L)	**PRIMARY RESET** brings 80960VH to a consistent state. When P_RST# is asserted: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • open drain signals such as P_SERR# are floated. • S_RST# asserts. P_RST# may be asynchronous to P_CLK when asserted or deasserted. Although asynchronous, deassertion must be guaranteed to be a clean, bounce-free edge.
P_SERR#	**I/O** OD R(Z)	**PRIMARY PCI BUS SYSTEM ERROR** reports address and data parity errors on the special cycle command, or any other system error where the result would be catastrophic.
P_STOP#	**I/O** R(Z)	**PRIMARY PCI BUS STOP** indicates that the current target is requesting the master to stop the current transaction on the primary PCI bus.
P_TRDY#	**I/O** R(Z)	**PRIMARY PCI BUS TARGET READY** indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.

NOTE:

1. PCI signal functions are summarized in this data sheet; refer to the *PCI Local Bus Specification*, revision 2.2 for a more complete definition.

Table 8. Memory Controller Signal Descriptions (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
CAS7:0#	**O** R(1) H(Q) P(Q)	**COLUMN ADDRESS STROBE** signals are used for DRAM accesses and are asserted when the MA11:0 signals contain a valid column address. CAS7:0# signals are asserted during refresh. *Non-Interleaved Operation:* CAS0#,CAS4# = BE0# lane access CAS1#,CAS5# = BE1# lane access CAS2#,CAS6# = BE2# lane access CAS3#,CAS7# = BE3# lane access *Interleaved Operation:* CAS0# = BE0# Even leaf lane access CAS1# = BE1# Even leaf lane access CAS2# = BE2# Even leaf lane access CAS3# = BE3# Even leaf lane access CAS4# = BE0# Odd leaf lane access CAS5# = BE1# Odd leaf lane access CAS6# = BE2# Odd leaf lane access CAS7# = BE3# Odd leaf lane access
CE1:0#	**O** R(1) H(Q) P(Q)	**CHIP ENABLE** signals indicate an access to one of the two SRAM/ FLASH/ ROM memory banks. CE0# and CE1# are never asserted at the same time. These signals are valid during the entire memory operation. CE0# is asserted for accesses to memory bank 0. CE1# is asserted for accesses to memory bank 1.
DALE1:0	**O** R(0) H(Q) P(Q)	**DRAM ADDRESS LATCH ENABLE** signals support external address demultiplexing of the MA11:0 address lines for interleaved DRAM systems. Use these to directly interface to ‘373’ type latches. These signals are only valid for accesses to interleaved memory systems. DALE0 is asserted during a valid even leaf address. DALE1 is asserted during a valid odd leaf address.
DP3:0	**I/O** R(X) H(Q) P(Q)	**DATA PARITY** carries the parity information for DRAM accesses. Each parity bit corresponds to a group of 8 data bus signals as follows: DP0 — AD7:0 DP2 — AD23:16 DP1 — AD15:8 DP3 — AD31:24 The memory controller generates parity information for local bus writes during data cycles. During read data cycles, the memory controller checks parity and provides notification of parity errors on the clock following the data cycle. Parity checking and polarity are user-programmable. Parity generation and checking are valid only for data lines that have their associated enable bits asserted.
DWE1:0#	**O** R(1) H(Q) P(Q)	**DRAM WRITE ENABLE** signals distinguish between read and write accesses to DRAM. DWE1:0# lines are asserted for writes and deasserted for reads. CAS7:0# determine valid bytes lanes during the access. These two outputs are functionally equivalent for all DRAM accesses; these provide increased drive capability for heavily loaded systems.
LEAF1:0#	**O** R(1) H(Q) P(Q)	**LEAF ENABLE** signals control the data output enables of the memory system during an interleaved DRAM read access. Use these to directly interface to either DRAM or transceiver output enable signals. LEAF0# is asserted during an even leaf access. LEAF1# is asserted during an odd leaf access.

Table 8. Memory Controller Signal Descriptions (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
MA11:0	**O** R(X) H(Q) P(Q)	**MULTIPLEXED ADDRESS** signals are multi-purpose depending on the device that is selected. For memory banks 0 and 1, these signals output address bits A13:2. These address bits are incremented for each data transfer of a burst access. For DRAM bank, these signals output the row/column multiplexed address bits 11:0. The relationship between the AD31:0 lines and the MA11:0 lines depends on the bank size, type and arrangement of the DRAM that is accessed.
MWE3:0#	**O** R(1) H(Q) P(Q)	**MEMORY WRITE ENABLE** signals for write accesses to SRAM/FLASH devices. The MWE's rising edge strobes valid data into these devices. MWE0# is asserted for writes to the BE0# lane MWE1# is asserted for writes to the BE1# lane MWE2# is asserted for writes to the BE2# lane MWE3# is asserted for writes to the BE3# lane
RAS3:0#	**O** R(1) H(Q) P(Q)	**ROW ADDRESS STROBE** signals are used for DRAM accesses and are asserted when the MA11:0 signals contain a valid row address. RAS3:0# always deasserts after the last data transfer in a DRAM access. *Non-Interleaved Operation:* RAS0# = Bank0 access RAS1# = Bank1 access RAS2# = Bank2 access RAS3# = Bank3 access *Interleaved Operation:* RAS0,2# = Even leaf RAS1,3# = Odd leaf

Table 9. DMA, I^2C Units Signal Descriptions

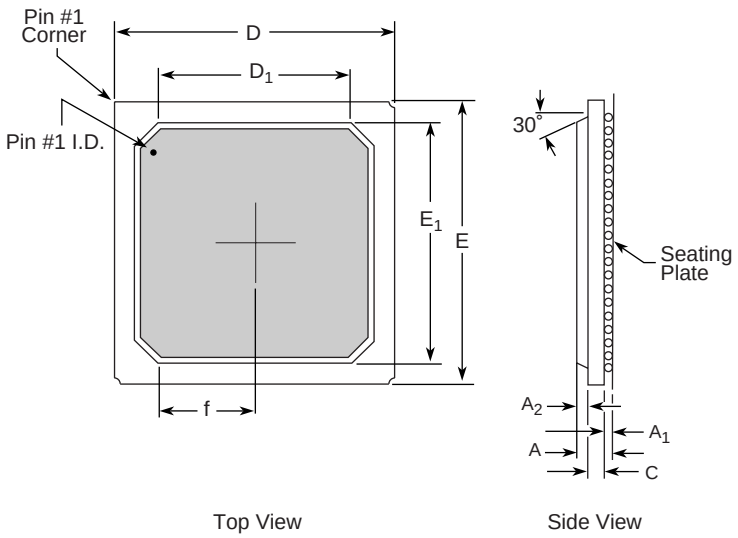
NAME	TYPE	DESCRIPTION
DACK#	**O** R(H) H(Q) P(Q)	**DMA DEMAND MODE ACKNOWLEDGE** The DMA Controller asserts this signal to indicate (1) it can receive new data from an external device or (2) it has data to send to an external device. This signal has a weak internal pullup which is active during reset to ensure normal operation.
DREQ#	**I** S(L)	**DMA DEMAND MODE REQUEST** External devices use this signal to indicate (1) new data is ready for transfer to the DMA controller or (2) buffers are available to receive data from the DMA controller.
SCL	**I/O OD** R(Z) H(Q) P(Q)	**I^2C CLOCK** provides synchronous I^2C bus operation.
SDA	**I/O OD** R(Z) H(Q) P(Q)	**I^2C DATA** used for data transfer and arbitration on the I^2C bus.
WAIT#	**O** R(1) H(Q) P(Q)	**WAIT** is an output that allows the DMA controller to insert wait states during DMA accesses to an external memory system.

Table 10. Clock Related Signals

NAME	TYPE	DESCRIPTION
P_CLK	I	**SYNCHRONOUS PCI BUS CLOCK** Provides the timing for all primary PCI transactions and is the clock source for all internal units. All input/output timings are relative to **P_CLK**.
CLKMODE1:0#	I	**CLOCK MODE** are used to select the mode of operation in terms of the 80960 local bus / PCI bus vs. the internal 80960 processor core. These signals are internally pulled high. This causes the 80960 processor core to run in DX mode after reset. In this mode, the 80960 processor core speed can be altered by using the Core Select Register (CSR). 00 - DX4 Mode 01 - DX2 Mode 10 - DX Mode 11 - Select Speed via PCI Bus

3.1.2 324-Lead PBGA Package

Figure 3. 324-Plastic Ball Grid Array Top and Side View



Note: All Dimensions are in Millimeters

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Figure 4. 324-Plastic Ball Grid Array (Top View)

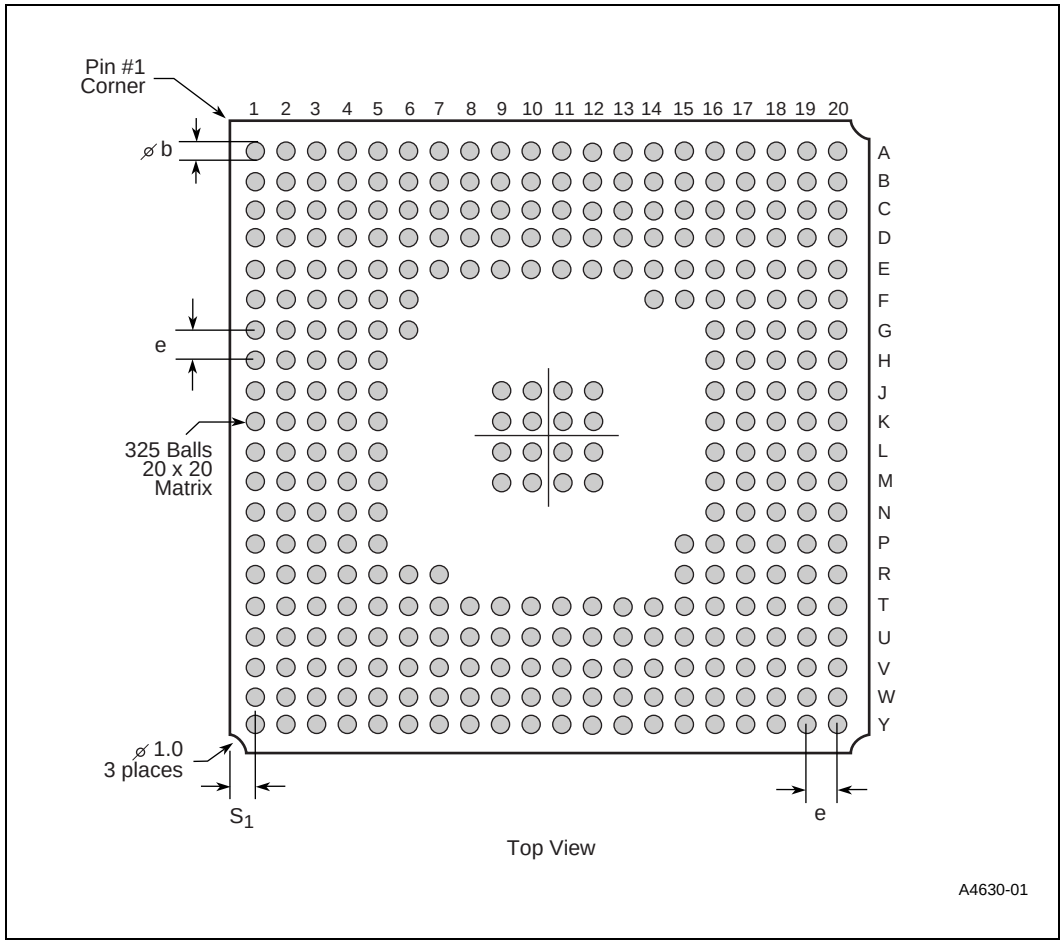


Table 11. PBGA 324 Package Dimensions

PBGA Package Dimensions		
	Min	**Max**
N (# of balls)	324	
A	2.14	2.52
A_1	0.50	0.70
A_2	1.12	1.22
D/E	26.80	27.20
D_1/E_1	23.75	24.25
S_1	1.44 Ref	
b	0.60	0.90
C	0.52	0.60
e	1.27	

Table 12. 324-Plastic Ball Grid Array Ballout — In Ball Order (Sheet 1 of 3)

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A1	V_{SS}	B12	P_LOCK#	D3	CLKMODE1#	E14	NC
A2	WAIT#	B13	V_{CC}	D4	V_{SS}	E15	NC
A3	P_AD3	B14	P_C/BE2#	D5	P_AD2	E16	NC
A4	V_{CC}	B15	V_{SS}	D6	V_{CC}	E17	NC
A5	P_C/BE0#	B16	P_AD21	D7	P_AD7	E18	NC
A6	V_{SS}	B17	V_{CC}	D8	V_{SS}	E19	NC
A7	P_AD10	B18	P_AD24	D9	NC	E20	P_AD31
A8	V_{CC}	B19	V_{SS}	D10	V_{CC}	F1	MA6
A9	P_AD13	B20	P_AD28	D11	V_{CC}	F2	V_{SS}
A10	P_AD14	C1	DP3	D12	V_{CC}	F3	MA11
A11	P_PAR	C2	CLKMODE0#	D13	V_{SS}	F4	V_{CC}
A12	P_PERR#	C3	DACK#	D14	P_AD18	F5	NC
A13	V_{CC}	C4	P_AD1	D15	V_{CC}	F6	V_{CC}
A14	P_TRDY#	C5	P_AD4	D16	P_AD26	F14	V_{CC}
A15	V_{SS}	C6	P_AD6	D17	V_{SS}	F15	V_{CC}
A16	P_AD17	C7	P_AD8	D18	P_AD30	F16	NC
A17	P_AD22	C8	P_AD11	D19	V_{CC}	F17	V_{CC}
A18	P_IDSEL	C9	NC	D20	NC	F18	P_REQ#
A19	P_C/BE3#	C10	P_AD15	E1	MA9	F19	V_{SS}
A20	V_{SS}	C11	P_SERR#	E2	DP0	F20	P_GNT#
B1	DREQ#	C12	**P_DEVSEL#**	E3	DP2	G1	NC
B2	V_{SS}	C13	P_IRDY#	E4	V_{CC}	G2	MA5
B3	P_AD0	C14	P_AD16	E5	NC	G3	MA7
B4	V_{CC}	C15	P_AD20	E6	NC	G4	MA10
B5	P_AD5	C16	P_AD23	E7	NC	G5	NC
B6	V_{SS}	C17	P_AD25	E8	NC	G6	V_{CC}
B7	P_AD9	C18	P_AD27	E9	NC	G16	NC
B8	V_{CC}	C19	P_AD29	E10	P_C/BE1#	G17	P_RST#
B9	P_AD12	C20	V_{CC}	E11	P_STOP#	G18	P_INTD#
B10	V_{SS}	D1	DP1	E12	P_FRAME#	G19	V_{CC}

Table 12. 324-Plastic Ball Grid Array Ballout — In Ball Order (Sheet 2 of 3)

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
B11	V_{SS}	D2	V_{CC}	E13	P_AD19	G20	VCCPLL2
H1	V_{CC}	K11	V_{SS}	M17	BE3#	R7	V_{CC}
H2	V_{CC}	K12	V_{SS}	M18	BE2#	R15	V_{CC}
H3	MA4	K16	BE0#	M19	BE1#	R16	NC
H4	V_{SS}	K17	V_{CC}	M20	V_{CC}	R17	V_{CC}
H5	MA8	K18	DT/R#	N1	V_{CC}	R18	AD23
H16	P_INTC#	K19	V_{SS}	N2	V_{CC}	R19	V_{SS}
H17	V_{SS}	K20	W/R#	N3	MWE0#	R20	V_{SS}
H18	P_INTB#	L1	LEAF0#	N4	V_{SS}	T1	CAS4#
H19	V_{CC}	L2	V_{SS}	N5	CAS5#	T2	CAS1#
H20	V_{CC}	L3	CE1#	N16	NC	T3	RAS3#
J1	MA0	L4	V_{CC}	N17	V_{SS}	T4	RAS0#
J2	MA1	L5	CE0#	N18	AD30	T5	NC
J3	MA2	L9	V_{SS}	N19	V_{CC}	T6	NC
J4	MA3	L10	V_{SS}	N20	V_{CC}	T7	XINT0#
J5	V_{CC}	L11	V_{SS}	P1	CAS7#	T8	FAIL#
J9	V_{SS}	L12	V_{SS}	P2	V_{CC}	T9	D/C#/ RST_MODE#
J10	V_{SS}	L16	AD31	P3	CAS6#	T10	RDYRCV#
J11	V_{SS}	L17	V_{CC}	P4	CAS3#	T11	NC
J12	V_{SS}	L18	ALE	P5	NC	T12	V_{CC}
J16	ADS#	L19	V_{SS}	P15	V_{CC}	T13	AD6
J17	BLAST#	L20	DEN#	P16	NC	T14	TCK
J18	SDA	M1	DWE1#	P17	AD22	T15	TDI
J19	SCL	M2	DWE0#	P18	AD27	T16	NC
J20	P_INTA#	M3	MWE3#	P19	AD29	T17	AD17
K1	LEAF1#	M4	MWE2#	P20	VCC5REF	T18	AD20
K2	V_{SS}	M5	MWE1#	R1	V_{SS}	T19	AD24
K3	DALE0	M9	V_{SS}	R2	V_{SS}	T20	AD28
K4	V_{CC}	M10	V_{SS}	R3	CAS2#	U1	CAS0#
K5	DALE1	M11	V_{SS}	R4	V_{CC}	U2	V_{CC}
K9	V_{SS}	M12	V_{SS}	R5	NC	U3	RAS1#

Table 12. 324-Plastic Ball Grid Array Ballout — In Ball Order (Sheet 3 of 3)

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
K10	V_{SS}	M16	AD26	R6	V_{CC}	U4	V_{SS}
U5	V_{CC}	V13	AD5	Y1	V_{SS}		
U6	V_{CC}	V14	AD8	Y2	XINT5#		
U7	WIDTH/HLTD0	V15	TMS	Y3	XINT3#		
U8	V_{SS}	V16	AD12	Y4	XINT1#		
U9	V_{CC}	V17	AD13	Y5	V_{CC}		
U10	V_{CC}	V18	AD16	Y6	V_{SS}		
U11	V_{CC}	V19	AD19	Y7	LCDINIT#		
U12	V_{CC}	V20	AD21	Y8	HOLD		
U13	V_{SS}	W1	NC	Y9	LRDYRCV#/ STEST		
U14	AD9	W2	V_{SS}	Y10	VCCPLL1		
U15	V_{CC}	W3	V_{CC}	Y11	AD1		
U16	V_{CC}	W4	V_{CC}	Y12	AD4		
U17	V_{SS}	W5	LRST#	Y13	AD7		
U18	AD18	W6	V_{SS}	Y14	TRST#		
U19	V_{CC}	W7	V_{CC}	Y15	V_{SS}		
U20	AD25	W8	V_{CC}	Y16	AD10		
V1	RAS2#	W9	NMI#	Y17	NC		
V2	XINT7#	W10	V_{SS}	Y18	AD14		
V3	XINT6#	W11	V_{SS}	Y19	AD15		
V4	XINT4#	W12	AD3	Y20	V_{SS}		
V5	XINT2#	W13	V_{CC}				
V6	WIDTH/HLTD1/RETRY	W14	V_{CC}				
V7	NC	W15	V_{SS}				
V8	LOCK#/ONCE#	W16	NC				
V9	HOLDA	W17	AD11				
V10	TDO	W18	V_{CC}				
V11	AD0	W19	V_{SS}				
V12	AD2	W20	P_CLK				

NOTE:
1. Do not connect any external logic to balls marked NC (no connect balls).

Table 13. 324-Plastic Ball Grid Array Ballout — In Signal Order (Sheet 1 of 3)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
AD0	V11	AD31	L16	DWE0#	M2	NC	E6
AD1	Y11	ADS#	J16	DWE1#	M1	NC	E7
AD2	V12	ALE	L18	FAIL#	T8	NC	E8
AD3	W12	BE0#	K16	HOLD	Y8	NC	E9
AD4	Y12	BE1#	M19	HOLDA	V9	NC	E14
AD5	V13	BE2#	M18	LCDINIT#	Y7	NC	E15
AD6	T13	BE3#	M17	LEAF0#	L1	NC	E16
AD7	Y13	BLAST#	J17	LEAF1#	K1	NC	E17
AD8	V14	CAS0#	U1	LOCK#/ONCE#	V8	NC	E18
AD9	U14	CAS1#	T2	LRDYRCV#/STEST	Y9	NC	E19
AD10	Y16	CAS2#	R3	LRST#	W5	NC	F5
AD11	W17	CAS3#	P4	MA0	J1	NC	F16
AD12	V16	CAS4#	T1	MA1	J2	NC	G1
AD13	V17	CAS5#	N5	MA2	J3	NC	G5
AD14	Y18	CAS6#	P3	MA3	J4	NC	G16
AD15	Y19	CAS7#	P1	MA4	H3	NC	N16
AD16	V18	CE0#	L5	MA5	G2	NC	P5
AD17	T17	CE1#	L3	MA6	F1	NC	P16
AD18	U18	CLKMODE0#	C2	MA7	G3	NC	R5
AD19	V19	CLKMODE1#	D3	MA8	H5	NC	R16
AD20	T18	D/C#/RST_MODE#	T9	MA9	E1	NC	T5
AD21	V20	DACK#	C3	MA10	G4	NC	T6
AD22	P17	DALE0	K3	MA11	F3	NC	T11
AD23	R18	DALE1	K5	MWE0#	N3	NC	T16
AD24	T19	DEN#	L20	MWE1#	M5	NC	V7
AD25	U20	DP0	E2	MWE2#	M4	NC	W1
AD26	M16	DP1	D1	MWE3#	M3	NC	W16
AD27	P18	DP2	E3	NC	C9	NC	Y17
AD28	T20	DP3	C1	NC	D9	NMI#	W9
AD29	P19	DREQ#	B1	NC	D20	P_AD0	B3
AD30	N18	DT/R#	K18	NC	E5	P_AD1	C4

Table 13. 324-Plastic Ball Grid Array Ballout — In Signal Order (Sheet 2 of 3)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
P_AD2	D5	P_C/BE1#	E10	TMS	V15	V_{CC}	N20
P_AD3	A3	P_C/BE2#	B14	TRST#	Y14	V_{CC}	P15
P_AD4	C5	P_C/BE3#	A19	V_{CC}	A8	V_{CC}	R4
P_AD5	B5	P_CLK	W20	V_{CC}	A13	V_{CC}	R6
P_AD6	C6	**P_DEVSEL#**	C12	V_{CC}	B4	V_{CC}	R7
P_AD7	D7	P_FRAME#	E12	V_{CC}	B8	V_{CC}	R15
P_AD8	C7	P_GNT#	F20	V_{CC}	B13	V_{CC}	R17
P_AD9	B7	P_IDSEL	A18	V_{CC}	B17	V_{CC}	U2
P_AD10	A7	P_INTA#	J20	V_{CC}	D2	V_{CC}	U6
P_AD11	C8	P_INTB#	H18	V_{CC}	D6	V_{CC}	U10
P_AD12	B9	P_INTC#	H16	V_{CC}	D10	V_{CC}	U11
P_AD13	A9	P_INTD#	G18	V_{CC}	D11	V_{CC}	U15
P_AD14	A10	P_IRDY#	C13	V_{CC}	D15	V_{CC}	U19
P_AD15	C10	P_LOCK#	B12	V_{CC}	D19	V_{CC}	W4
P_AD16	C14	P_PAR	A11	V_{CC}	F4	V_{CC}	W8
P_AD17	A16	P_PERR#	A12	V_{CC}	F6	V_{CC}	W13
P_AD18	D14	P_REQ#	F18	V_{CC}	F14	V_{CC}	Y5
P_AD19	E13	P_RST#	G17	V_{CC}	F15	V_{CC}	A4
P_AD20	C15	P_SERR#	C11	V_{CC}	F17	V_{CC}	D12
P_AD21	B16	P_STOP#	E11	V_{CC}	G6	V_{CC}	G19
P_AD22	A17	P_TRDY#	A14	V_{CC}	H1	V_{CC}	J5
P_AD23	C16	RAS0#	T4	V_{CC}	H2	V_{CC}	M20
P_AD24	B18	RAS1#	U3	V_{CC}	H19	V_{CC}	P2
P_AD25	C17	RAS2#	V1	V_{CC}	H20	V_{CC}	U5
P_AD26	D16	RAS3#	T3	V_{CC}	K4	V_{CC}	U9
P_AD27	C18	RDYRCV#	T10	V_{CC}	K17	V_{CC}	U12
P_AD28	B20	SCL	J19	V_{CC}	L4	V_{CC}	U16
P_AD29	C19	SDA	J18	V_{CC}	L17	V_{CC}	W3
P_AD30	D18	TCK	T14	V_{CC}	N1	V_{CC}	W7
P_AD31	E20	TDI	T15	V_{CC}	N2	V_{CC}	W14
P_C/BE0#	A5	TDO	V10	V_{CC}	N19	V_{CC}	W18

Table 13. 324-Plastic Ball Grid Array Ballout — In Signal Order (Sheet 3 of 3)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
V_{CC}	C20	V_{SS}	K2	V_{SS}	W10		
V_{CC}	E4	V_{SS}	K9	V_{SS}	W11		
V_{CC}	T12	V_{SS}	K10	V_{SS}	W15		
VCC5REF	P20	V_{SS}	K11	V_{SS}	W19		
VCCPLL1	Y10	V_{SS}	K12	V_{SS}	Y1		
VCCPLL2	G20	V_{SS}	K19	V_{SS}	Y6		
V_{SS}	A1	V_{SS}	L2	V_{SS}	Y15		
V_{SS}	A6	V_{SS}	L9	V_{SS}	Y20		
V_{SS}	A15	V_{SS}	L10	W/R#	K20		
V_{SS}	A20	V_{SS}	L11	WAIT#	A2		
V_{SS}	B2	V_{SS}	L12	**WIDTH/HLTD0**	U7		
V_{SS}	B6	V_{SS}	L19	**WIDTH**/HLTD1/RETRY	V6		
V_{SS}	B10	V_{SS}	M9	XINT0#	T7		
V_{SS}	B11	V_{SS}	M10	XINT1#	Y4		
V_{SS}	B15	V_{SS}	M11	XINT2#	V5		
V_{SS}	B19	V_{SS}	M12	XINT3#	Y3		
V_{SS}	D4	V_{SS}	N4	XINT4#	V4		
V_{SS}	D8	V_{SS}	N17	XINT5#	Y2		
V_{SS}	D13	V_{SS}	R1	XINT6#	V3		
V_{SS}	D17	V_{SS}	R2	XINT7#	V2		
V_{SS}	F2	V_{SS}	R19				
V_{SS}	F19	V_{SS}	R20				
V_{SS}	H4	V_{SS}	U4				
V_{SS}	H17	V_{SS}	U8				
V_{SS}	J9	V_{SS}	U13				
V_{SS}	J10	V_{SS}	U17				
V_{SS}	J11	V_{SS}	W2				
V_{SS}	J12	V_{SS}	W6				

NOTE:
1. Do not connect any external logic to balls marked NC (no connect balls).

3.2 Package Thermal Specifications

The device is specified for operation when T_C (case temperature) is within the range of 0° C to 95° C. Case temperature may be measured in any environment to determine whether the processor is within specified operating range. Measure the case temperature at the center of the top surface, opposite the ballpad.

3.2.1 Thermal Specifications

This section defines the terms used for thermal analysis.

3.2.1.1 Ambient Temperature

Ambient temperature, T_A, is the temperature of the ambient air surrounding the package. In a system environment, ambient temperature is the temperature of the air upstream from the package.

3.2.1.2 Case Temperature

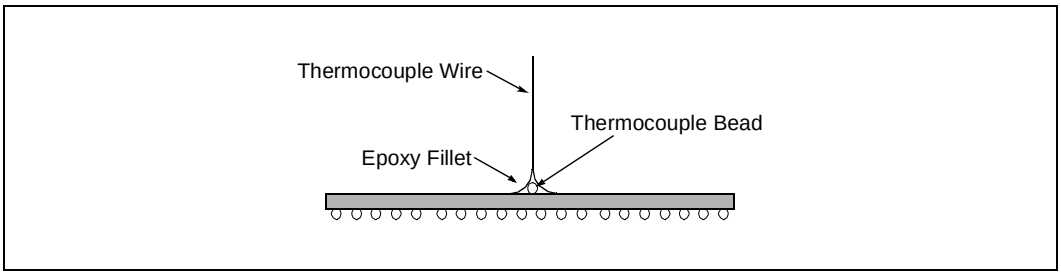
To ensure functionality and reliability, the device is specified for proper operation when the case temperature, T_C, is within the specified range in Table 16, Operating Conditions (pg. 36).

When measuring case temperature, attention to detail is required to ensure accuracy. If a thermocouple is used, then calibrate it before taking measurements. Errors may result when the measured surface temperature is affected by the surrounding ambient air temperature. Such errors may be due to a poor thermal contact between thermocouple junction and the surface, heat loss by radiation, or conduction through thermocouple leads.

To minimize measurement errors:

- Use a 35 gauge K-type thermocouple or equivalent.
- Attach the thermocouple bead or junction to the package top surface at a location corresponding to the center of the die (). The center of the die gives a more accurate measurement and less variation as the boundary condition changes.
- Attach the thermocouple bead or junction at a 90° angle by an adhesive bond (such as thermal epoxy or heat-tolerant tape) to the package top surface as shown in .

Figure 5. Thermocouple Attachment



3.2.1.3 Thermal Resistance

The thermal resistance value for the case-to-ambient, θ_{CA}, is used as a measure of the cooling solution's thermal performance.

3.2.2 Thermal Analysis

Table 14 lists the case-to-ambient thermal resistances of the 80960VH for different air flow rates without a heat sink.

To calculate T_A, the maximum ambient temperature to conform to a particular case temperature:

$T_A = T_C - P (\theta_{CA})$

Compute P by multiplying I_{CC} and V_{CC}. Values for θ_{JC} and θ_{CA} are given in Table 14.

Junction temperature (T_J) is commonly used in reliability calculations. T_J can be calculated from θ_{JC} (thermal resistance from junction to case) using the following equation:

$T_J = T_C + P (\theta_{JC})$

Similarly, when T_A is known, the corresponding case temperature (T_C) can be calculated as follows:

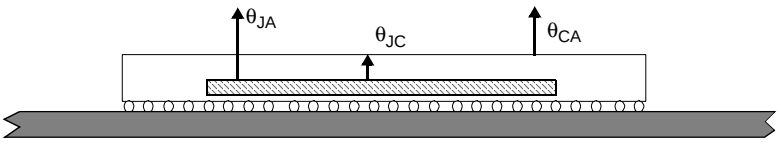
$T_C = T_A + P (\theta_{CA})$

The θ_{JA} (Junction-to-Ambient) for this package is currently estimated at 26.54° C/Watt with no airflow.

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

Table 14. 324-Lead PBGA Package Thermal Characteristics

Thermal Resistance — °C/Watt						
Parameter	Airflow — ft./min (m/sec)					
	0 (0)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
θ_{JC} (Junction-to-Case)	1.36	1.36	1.36	1.36	1.36	1.36
θ_{CA} (Case-to-Ambient) Without Heatsink	25.18	20.30	18.29	16.57	15.55	14.75



NOTE:

1. This table applies to a PBGA device soldered directly onto a board.

4.0 Electrical Specifications

Table 15. Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–55° C to + 125° C
Case Temperature Under Bias	0° C to + 95° C
Supply Voltage wrt. V_{SS}	–0.5 V to + 4.6 V
Supply Voltage wrt. V_{SS} on V_{CC5}	–0.5 V to + 6.5 V
Voltage on Any Ball wrt. V_{SS}	–0.5 V to V_{CC} + 0.5 V

NOTICE: This data sheet contains information on products in the design phases of development. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.

WARNING: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Table 16. Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.6	V	(1)
V_{CC5}	Input Protection Bias	3.0	5.25	V	(1)
F_{P_CLK}	Input Clock Frequency	16	33.33	MHz	
T_C	Case Temperature Under Bias i960® VH processor (324 PBGA)	0	95	°C	

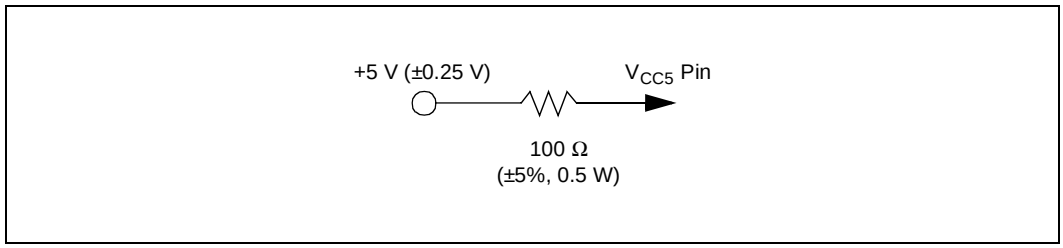
NOTE:
1. The 80960VH processor is produced on Intel’s advanced CMOS process. Proper bulk decoupling must be used to prevent device damage during power up and power down. Power supply behavior during these transitions, without proper bulk decoupling, can cause the power supply to exceed the maximum V_{CC} specification, causing device damage.

4.1 V_{CC5} Pin Requirements (V_{DIFF})

In mixed voltage systems that drive 80960VH inputs in excess of 3.3 V, the V_{CC5} pin must be connected to the system’s 5 V supply. To limit current flow into the V_{CC5} pin, there is a limit to the voltage differential between the V_{CC5} pin and the other V_{CC} pins. The voltage differential between the 80960VH V_{CC5} pin and its 3.3 V V_{CC} pins should never exceed 2.25 V. This limit applies to power-up, power-down, and steady-state operation. Table 17 outlines this requirement. Meeting this requirement ensures proper operation and guarantees that the current draw into the V_{CC5} pin does not exceed the I_{CC5} specification.

If the voltage difference requirements cannot be met due to system design limitations, then an alternate solution may be employed. As shown in Figure 6., a minimum of 100 Ω series resistor may be used to limit the current into the V_{CC5} pin. This resistor ensures that current drawn by the V_{CC5} pin does not exceed the maximum rating for this pin.

Figure 6. V_{CC5} Current-Limiting Resistor



This resistor is not necessary in systems that can guarantee the V_{DIFF} specification.

In 3.3 V-only systems and systems that drive 80960VH pins from 3.3 V logic, connect the V_{CC5} pin directly to the 3.3 V V_{CC} plane.

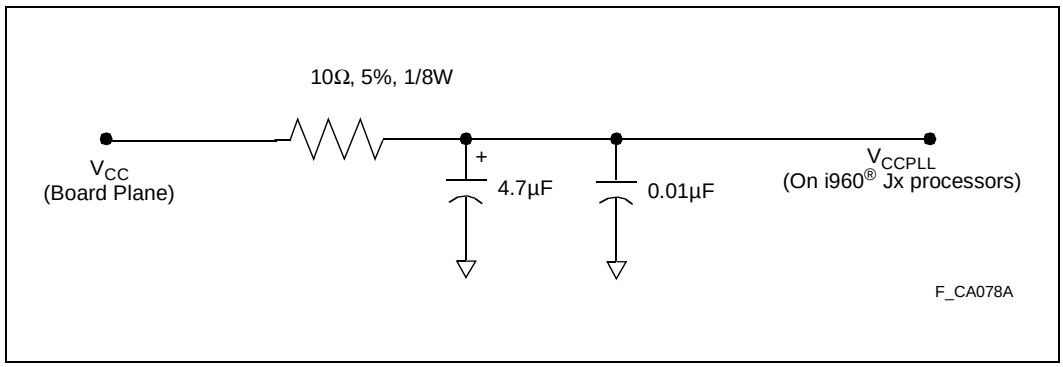
Table 17. V_{DIFF} Specification for Dual Power Supply Requirements (3.3 V, 5 V)

Symbol	Parameter	Min	Max	Units	Notes
V_{DIFF}	V_{CC5}-V_{CC} Difference		2.25	V	V_{CC5} input should not exceed V_{CC} by more than 2.25 V during power-up and power-down, or during steady-state operation.

4.2 V_{CCPLL} Pin Requirements

To reduce clock skew on the i960 Jx processor, the V_{CCPLL} pin for the Phase Lock Loop (PLL) circuit is isolated on the pinout. The lowpass filter, as shown in Figure 7., reduces noise-induced clock jitter and its effects on timing relationships in system designs. The 4.7 µF capacitor must be (low ESR solid tantalum), the 0.01 µF capacitor must be of the type X7R and the node connecting V_{CCPLL} must be as short as possible.

Figure 7. V_{CCPLL} Lowpass Filter



4.3 DC Specifications

Table 18. DC Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	-0.5	0.8	V	(1)
V_{IH1}	Input High Voltage for all signals except P_CLK	2.0	V_{CC} + 0.5	V	(1)
V_{OL1}	Output Low Voltage Processor signals		0.45	V	I_{OL} = 6 mA (3)
V_{OH1}	Output High Voltage Processor signals	2.4 V_{CC} - 0.5		V	I_{OH} = -2 mA (3) I_{OH} = -200 µA (3)
V_{OL2}	Output Low Voltage PCI signals		0.55	V	I_{OL} = 1.5 mA (1)
V_{OH2}	Output High Voltage PCI signals	2.4		V	I_{OH} = 0.5 mA (1)
V_{OL3}	Output Low Voltage Memory Controller Normal drive		0.45	V	I_{OL} = 6 mA (4)
V_{OH3}	Output High Voltage Memory Controller Normal drive	2.4		V	I_{OH} = -2 mA (4)
V_{OL4}	Output Low Voltage Memory Controller High Drive		0.45	V	I_{OL} = 7 mA
V_{OH4}	Output High Voltage Memory Controller High Drive	2.4		V	I_{OH} = -2 mA
C_{IN}	Input Capacitance - PBGA		10	pF	F_{P_CLK} = T_F Min (1, 2)
C_{OUT}	I/O or Output Capacitance - PBGA		10	pF	F_{P_CLK} = T_F Min (1, 2)
C_{CLK}	P_CLK Capacitance - PBGA	5	12	pF	F_{P_CLK} = T_F Min (1, 2)
C_{IDSEL}	IDSEL Ball Capacitance		8	pF	(1)
L_{PIN}	Ball Inductance		20	nH	(1)

NOTES:

1. As required by the *PCI Local Bus Specification*, revision 2.2.
2. Not tested.
3. Processor signals include AD31:0, ALE, ADS#, BE3:0#, WIDTH/HLTD0, WIDTH/HLTD1/RETRY, D/C#/RST_MODE#, W/R#, DT/R#, DEN#, BLAST#, LRDYRCV#, LOCK#/ONCE#, HOLD, FAIL#, TDO, DACK#, WAIT#, SDA, SCL.
4. Memory Controller signals include MA11:0, DP3:0, RAS3:0#, CAS7:0#, MWE3:0#, DWE1:0#, DALE1:0, CE1:0#, LEAF1:0#.
5. Memory Controller signals capable of high drive are MA11:0, CAS7:0#, RAS3:0#, DWE1:0#.

Table 19. I_{CC} Characteristics

Symbol	Parameter	Typ	Max	Units	Notes
I_{LI1}	Input Leakage Current for each signal except PCI Bus Signals, LOCK#/ONCE#, WIDTH/ HLTD0, WIDTH/HLTD1/RETRY, BLAST#, D/C#/RST_MODE#, DEN#, TMS, TRST#, TDI, DACK#/PLLEN, LCDINIT#, LRDYRCV#/STEST, CLKMODE1:0#		± 5	µA	V_{IN} = 0.8 V (V_{IL}) and 2.0 V (V_{IH})
I_{LI2}	Input Leakage Current for LOCK#/ONCE#, WIDTH/HLTD0, WIDTH/HLTD1/RETRY, BLAST#, D/C#/RST_MODE#, DEN#, TMS, TRST#, TDI, DACK#/PLLEN, LCDINIT#, LRDYRCV#/STEST, CLKMODE1:0#	-140	-250	µA	V_{IN} = 0.45 V (1)
I_{LI3}	Input Leakage Current for PCI Bus Signals (except PCLK)		± 5	µA	V_{IN} = 0.8 V (V_{IL}) and 2.0 V (V_{IH})
I_{LO}	Output Leakage Current		± 5	µA	$0.4 \le V_{OUT} \le V_{CC}$
I_{CC} Active (Power Supply)	Power Supply Current i960® VH processor				
	DX Mode		450	mA	(1,2)
	DX2 Mode		590	mA	(1,2)
	DX4 Mode		720	mA	(1,2)
I_{CC} Active (Thermal)	Thermal Current i960® VH processor				
	DX Mode	390		mA	(1,3)
	DX2 Mode	550		mA	(1,3)
	DX4 Mode	690		mA	(1,3)
I_{CC} Active (Power Modes)	Reset Mode i960® VH processor ONCE Mode i960® VH processor		470 40	mA	(4) (4)

NOTES:

1. Measured with device operating and outputs loaded to the test condition in Figure 8.
2. I_{CC} Active (Power Supply) value is provided for selecting your system's power supply. It is measured using one of the worst case instruction mixes with V_{CC} = 3.6 V and ambient temperature = 55 ° C. This parameter is characterized but not tested.
3. I_{CC} Active (Thermal) value is provided for your system's thermal management. Typical I_{CC} is measured with V_{CC} = 3.3 V and ambient temperature = 55 ° C. This parameter is characterized but not tested.
4. I_{CC} Active (Power modes) refers to the I_{CC} values that are tested when the device is in Reset mode or ONCE mode with V_{CC} = 3.6 V and ambient temperature = 55 ° C.

4.4 AC Specifications

Table 20. Input Clock Timings

Symbol	Parameter	Min	Max	Units	Notes
T_F	P_CLK Frequency	16	33.33	MHz	
T_C	P_CLK Period	30	62.5	ns	(1)
T_{CS}	P_CLK Period Stability		±250	ps	Adjacent Clocks (2,3)
T_{CH}	P_CLK High Time	12		ns	Measured at 1.5 V (2,3)
T_{CL}	P_CLK Low Time	12		ns	Measured at 1.5 V (2,3)
T_{CR}	P_CLK Rise Time		4	V/ns	0.4 V to 2.4 V (2,3)
T_{CF}	P_CLK Fall Time		4	V/ns	2.4 V to 0.4 V (2,3)

NOTES:

1. See Figure 9, (pg. 46).
2. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal clock, the jitter frequency spectrum should not have any power peaking between 500 KHz and 1/3 of the P_CLK frequency.
3. Not tested.

Table 21. Synchronous Output Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{OV1}	Output Valid Delay - All Local Bus Signals Except ALE Inactive and DT/R#	2	15.5	ns	(1,2,5)
T_{OV2}	Output Valid Delay, DT/R#	0.5 T_C +3	0.5 T_C +15	ns	(2,5)
T_{OV3}	Output Valid Delay - PCI Signals Except P_REQ#	2	11	ns	(2,5)
T_{OV4}	Output Valid Delay P_REQ#	2	12	ns	(2,5)
T_{OV5}	Output Valid Delay - DP3:0	3	19	ns	(2,5)
T_{OF}	Output Float Delay	3	13	ns	(3,4,5)

NOTES:

1. Inactive ALE refers to the falling edge of ALE. For inactive ALE timings, see Table 23, Relative Output Timings (pg. 42).
2. See Figure 10, (pg. 46).
3. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested, but is designed to be no longer than the valid delay.
4. See Figure 11, (pg. 47).
5. Outputs precharged to V_{CC5} maximum.

Table 22. Synchronous Input Timings

Sym	Parameter	Min	Max	Units	Notes
T_{IS1}	Input Setup to P_CLK — NMI#, XINT7:0#, DP3:0	6		ns	(1,2)
T_{IS1A}	Input Setup to P_CLK — for all accesses except Expansion ROM Accesses — AD31:0 only	6		ns	(1,2)
T_{IS1B}	Input Setup to P_CLK during Expansion ROM Accesses — AD31:0 only	8		ns	(1,2)
T_{IH1}	Input Hold from P_CLK — AD31:0, NMI#, XINT7:0#, DP3:0	2		ns	(1,2,4)
T_{IS2}	Input Setup to P_CLK — RDYRCV# and HOLD	10		ns	(2)
T_{IH2}	Input Hold from P_CLK — RDYRCV# and HOLD	2		ns	(2)
T_{IS3}	Input Setup to P_CLK — LOCK#/ONCE#, STEST	7		ns	(1,2,4)
T_{IH3}	Input Hold from P_CLK — LOCK#/ONCE#, STEST	3		ns	(1,2,4)
T_{IS4}	Input Setup to P_CLK — DREQ#	12		ns	(2)
T_{IH4}	Input Hold from P_CLK — DREQ#	7		ns	(2)
T_{IS5}	Input Setup to P_CLK — PCI Signals Except P_GNT#	7		ns	(2)
T_{IH5}	Input Hold from P_CLK — PCI Signals	0		ns	(2,4)
T_{IS6}	Input Setup to P_CLK — P_RST# - DX4 Mode	6		ns	(2,3)
T_{IS6}	Input Setup to P_CLK — P_RST# - DX2 and DX Mode	10		ns	(2,3)
T_{IH6}	Input Hold to P_CLK — P_RST#	2		ns	(2,3,4)
T_{IS7}	Input Setup to P_CLK — P_GNT#	10		ns	(2)
T_{IS8}	Input Setup to P_RST# — WIDTH/HLTD0, WIDTH/HLTD1/RETRY, D/C#/RST_MODE#	7		ns	(1,2,4)
T_{IH8}	Input Hold from P_RST# — WIDTH/HLTD0, WIDTH/HLTD1/RETRY, D/C#/RST_MODE#	3		ns	(1,2,4)

NOTES:

1. Setup and hold times must be met for proper processor operation. NMI#, and XINT7:0# may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge.
   For asynchronous operation, NMI#, and XINT7:0# must be asserted for a minimum of two P_CLK periods to guarantee recognition.
2. See Figure 12, (pg. 47).
3. P_RST# may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge.
4. Guaranteed by design. May not be 100% tested.

4.4.1 Relative Output Timings

Table 23. Relative Output Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{LXL}	ALE Width	$0.5T_C$-3		ns	(1,2,4)
T_{LXA}	Address Hold from ALE Inactive	$0.5T_C$-1		ns	Equal Loading (1,2,4)
T_{DXD}	DT/R# Valid to DEN# Active	$0.5T_C$-3		ns	Equal Loading (1,3,4)

NOTES:
1. Guaranteed by design. May not be 100% tested.
2. See Figure 13, (pg. 47).
3. See Figure 14, (pg. 48)
4. Outputs precharged to V_{CC5} maximum.

4.4.2 Memory Controller Relative Output Timings

Table 24. Fast Page Mode Non-interleaved DRAM Output Timings

Symbol	Description	Min	Max	Units	Notes
T_{OV6}	RAS3:0# Rising and Falling edge Output Valid Delay	1	9	ns	2
T_{OV7}	CAS7:0# Rising Edge Output Valid Delay	1	8	ns	2
T_{OV8}	CAS7:0# Falling Edge Output Valid Delay	0.5Tc+1	0.5Tc+8	ns	1,2
T_{OV9}	MA11:0 Output Valid Delay-Row Address	0.5Tc+1	0.5Tc+10	ns	1,2
T_{OV10}	MA11:0 Output Valid Delay-Column Address	1	10	ns	2
T_{OV11}	DWE1:0# Rising and Falling edge Output Valid Delay	1	11	ns	2

NOTES:
1. Signal generated on the rising edge of an internally generated 2XCLK which corresponds to the center of an P_CLK period. For testing purposes, the signal is specified relative to the rising edge of P_CLK with the 0.5Tc period offset.
2. Output switching between V_{CC3} maximum and V_{SS}.

Table 25. Fast Page Mode Interleaved DRAM Output Timings (Sheet 1 of 2)

Symbol	Description	Min	Max	Units	Notes
T_{OV12}	RAS3:0# Rising and Falling edge Output Valid Delay	1	9	ns	2
T_{OV13}	CAS7:0# Rising Edge Output Valid Delay	1	8	ns	2
T_{OV14}	CAS7:0# Falling Edge Output Valid Delay	0.5Tc+1	0.5Tc+8	ns	1,2
T_{OV15}	MA11:0 Output Valid Delay-Row Address	0.5Tc+1	0.5Tc+10	ns	1,2
T_{OV16}	MA11:0 Output Valid Delay-Column Address	1	10	ns	2
T_{OV17}	DWE1:0# Rising and Falling Edge Output Valid Delay	1	11	ns	2

NOTES:
1. Signal generated on the rising edge of an internally generated 2XCLK which corresponds to the center of an P_CLK period. For testing purposes, the signal is specified relative to the rising edge of P_CLK with the 0.5Tc period offset.
2. Output switching between V_{CC3} maximum and V_{SS}.

Table 25. Fast Page Mode Interleaved DRAM Output Timings (Sheet 2 of 2)

Symbol	Description	Min	Max	Units	Notes
T_{OV18}	DALE1:0 Initial Falling Edge Output Valid Delay	1	10	ns	2
T_{OV19}	DALE1:0 Burst Falling Edge Output Valid Delay	0.5Tc+1	0.5Tc+10	ns	1,2
T_{OV20}	DALE1:0 Rising Edge Output Valid Delay	1	10	ns	2
T_{OV21}	LEAF1:0# Rising and Falling Edge Output Valid Delay	1	10	ns	2

NOTES:

1. Signal generated on the rising edge of an internally generated 2XCLK which corresponds to the center of an P_CLK period. For testing purposes, the signal is specified relative to the rising edge of P_CLK with the 0.5Tc period offset.
2. Output switching between V_{CC3} maximum and V_{SS}.

Table 26. EDO DRAM Output Timings

Symbol	Description	Min	Max	Units	Notes
T_{OV22}	RAS3:0# Rising and Falling Edge Output Valid Delay	1	9	ns	2
T_{OV23}	CAS7:0# Rising Edge Output Valid Delay - Read Cycles	0.5Tc+1	0.5Tc+8	ns	1,2
T_{OV24}	CAS7:0# Falling Edge Output Valid Delay - Read Cycles	1	8	ns	2
T_{OV25}	CAS7:0# Rising Edge Output Valid Delay - Write Cycles	1	8	ns	2
T_{OV26}	CAS7:0# Falling Edge Output Valid Delay - Write Cycles	0.5Tc+1	0.5Tc+8	ns	1,2
T_{OV27}	MA11:0 Output Valid Delay - Row Address	0.5Tc+1	0.5Tc+10	ns	1,2
T_{OV28}	MA11:0 Output Valid Delay - Column Address Read Cycles	0.5Tc+1	0.5Tc+10	ns	1,2
T_{OV29}	MA11:0 Output Valid Delay - Column Address Write Cycles	1	10	ns	2
T_{OV30}	DWE1:0# Rising and Falling Edge Output Valid Delay	1	11	ns	2

NOTES:

1. Signal generated on the rising edge of an internally generated 2XCLK which corresponds to the center of an P_CLK period. For testing purposes, the signal is specified relative to the rising edge of P_CLK with the 0.5Tc period offset.
2. Output switching between V_{CC3} maximum and V_{SS}.

Table 27. SRAM/ROM Output Timings (Sheet 1 of 2)

Symbol	Description	Min	Max	Units	Notes
T_{OV40}	CE1:0# Rising and Falling Edge Output Valid Delay	1	8	ns	2
T_{OV41}	MWE3:0# Rising Edge Output Valid Delay	1	9	ns	2
T_{OV42}	MWE3:0# Falling Edge Output Valid Delay	0.5Tc+1	0.5Tc +9	ns	1,2

Table 27. SRAM/ROM Output Timings (Sheet 2 of 2)

Symbol	Description	Min	Max	Units	Notes
T_{OV43}	MA11:0 Output Valid Delay - Initial Address	0.5Tc+1	0.5Tc +10	ns	2
T_{OV44}	MA11:0 Output Valid Delay - Burst Address	1	10	ns	2

NOTES:

1. Signal generated on the rising edge of an internally generated 2XCLK which corresponds to the center of an P_CLK period. For testing purposes, the signal is specified relative to the rising edge of P_CLK with the 0.5Tc period offset.
2. Output switching between V_{CC3} maximum and V_{SS}.

4.4.3 Boundary Scan Test Signal Timings

Table 28. Boundary Scan Test Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{BSF}	TCK Frequency	0	$0.5T_F$	MHz	
T_{BSCH}	TCK High Time	15		ns	Measured at 1.5 V (1)
T_{BSCL}	TCK Low Time	15		ns	Measured at 1.5 V (1)
T_{BSCR}	TCK Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{BSCF}	TCK Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to TCK — TDI, TMS	4		ns	
T_{BSIH1}	Input Hold from TCK — TDI, TMS	6		ns	(1)
T_{BSOV1}	TDO Valid Delay	3	30	ns	Relative to falling edge of TCK (1,2)
T_{BSOF1}	TDO Float Delay	3	30	ns	Relative to falling edge of TCK (1,2)
T_{BSOV2}	All Outputs (Non-Test) Valid Delay	3	30	ns	Relative to falling edge of TCK (1,2)
T_{BSOF2}	All Outputs (Non-Test) Float Delay	3	30	ns	Relative to falling edge of TCK (1,2)
T_{BSIS2}	Input Setup to TCK — All Inputs (Non-Test)	4		ns	(1)
T_{BSIH2}	Input Hold from TCK — All Inputs (Non-Test)	6		ns	(1)

NOTES:

1. Guaranteed by design. Not tested.
2. Outputs precharged to V_{CC5} maximum.

4.4.4 I²C Interface Signal Timings

Table 29. I²C Interface Signal Timings

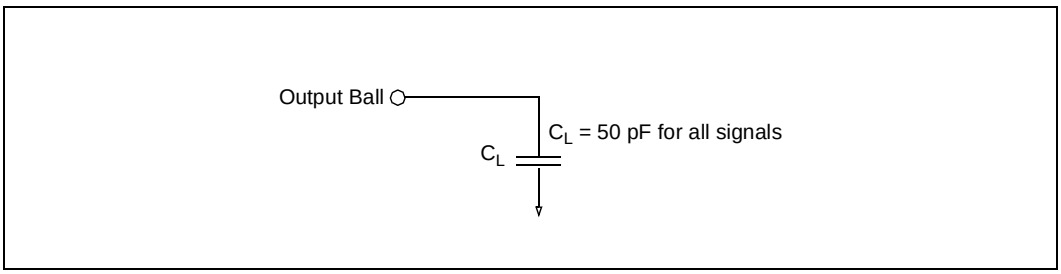
Symbol	Parameter	Std. Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCL}	SCL Clock Frequency	0	100	0	400	KHz	
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7		1.3		µs	(1)
T_{HDSTA}	Hold Time (repeated) START Condition	4		0.6		µs	(1,3)
T_{LOW}	SCL Clock Low Time	4.7		1.3		µs	(1,2)
T_{HIGH}	SCL Clock High Time	4		0.6		µs	(1,2)
T_{SUSTA}	Setup Time for a Repeated START Condition	4.7		0.6		µs	(1)
T_{HDDAT}	Data Hold Time	0		0	0.9	µs	(1)
T_{SUDAT}	Data Setup Time	250		100		ns	(1)
T_R	SCL and SDA Rise Time		1000	$20+0.1C_b$	300	ns	(1,4)
T_F	SCL and SDA Fall Time		300	$20+0.1C_b$	300	ns	(1,4)
T_{SUSTO}	Setup Time for STOP Condition	4		0.6		µs	(1)

NOTES:
1. See Figure 15, (pg. 48).
2. Not tested.
3. After this period, the first clock pulse is generated.
4. C_b = the total capacitance of one bus line, in pF.

4.5 AC Test Conditions

The AC Specifications in Section 4.4, AC Specifications (pg. 40) are tested with the 50 pF load indicated in .

Figure 8. AC Test Load



4.6 AC Timing Waveforms

Figure 9. P_CLK, TCLK Waveform

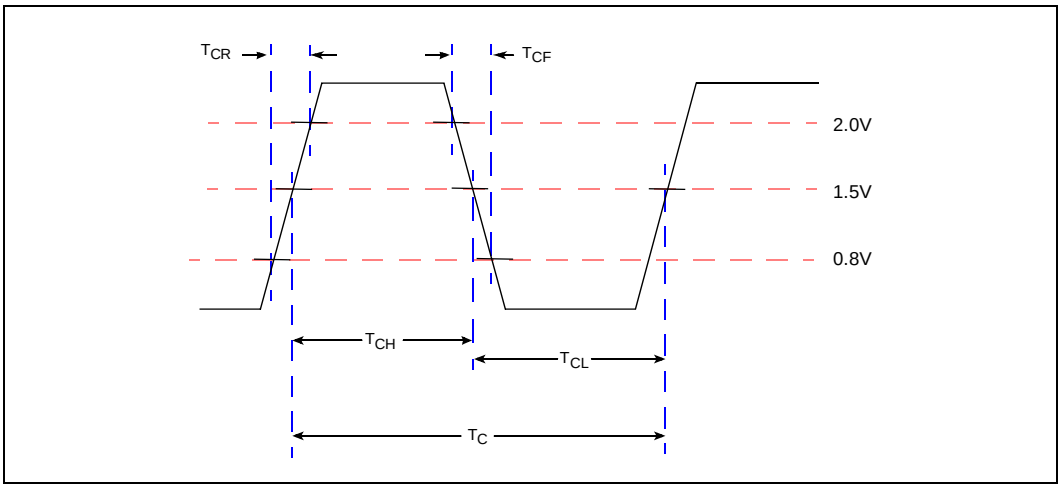


Figure 10. T_{OV} Output Delay Waveform

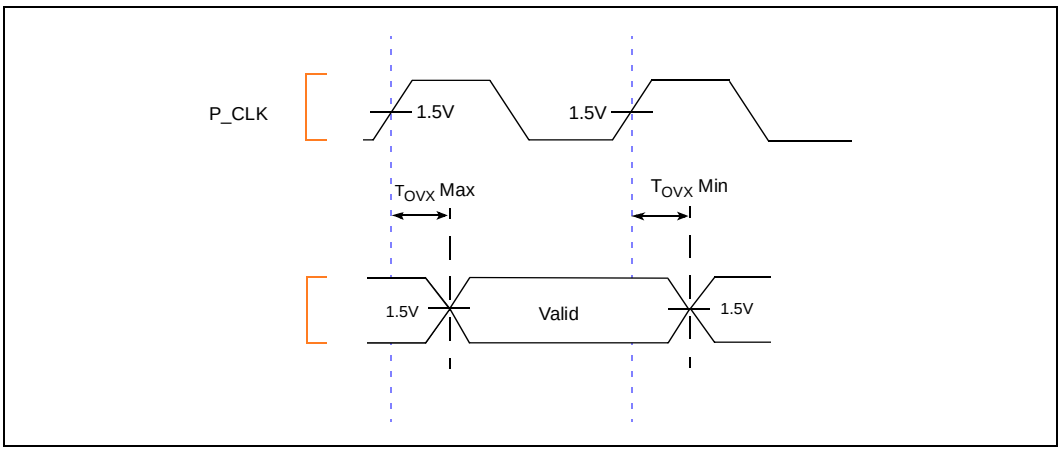


Figure 11. T_{OF} Output Float Waveform

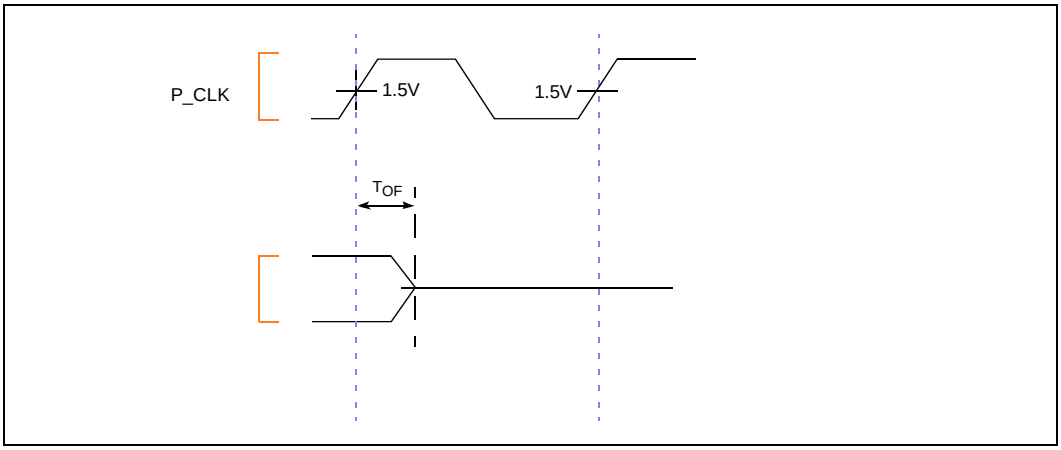


Figure 12. T_{IS} and T_{IH} Input Setup and Hold Waveform

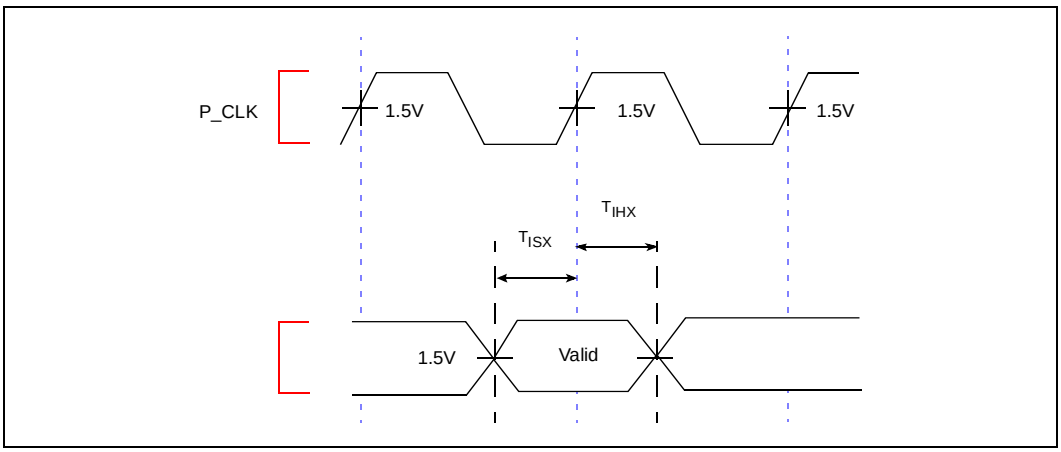


Figure 13. T_{LXL} and T_{LXA} Relative Timings Waveform

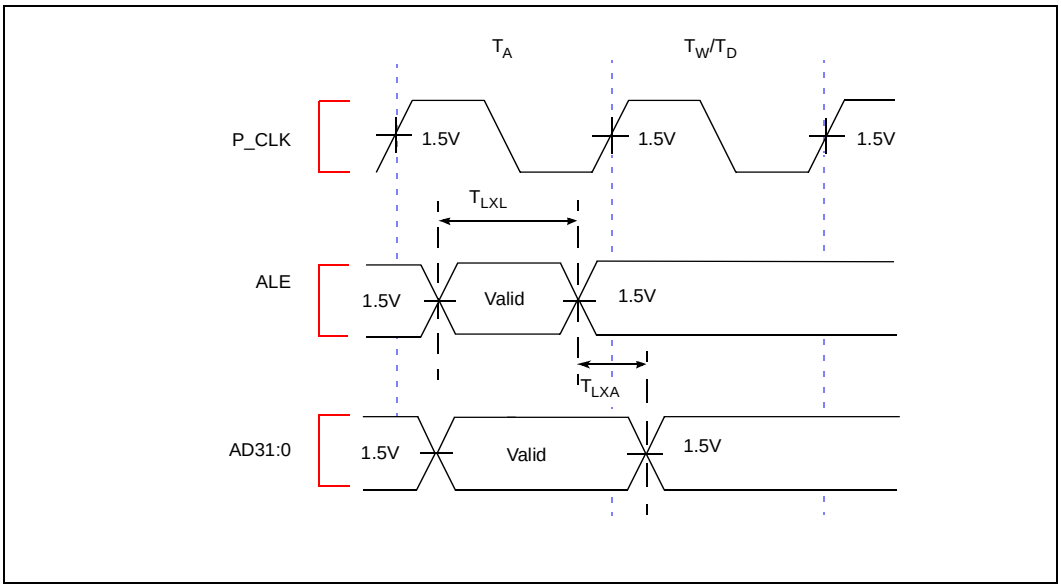


Figure 14. DT/R# and DEN# Timings Waveform

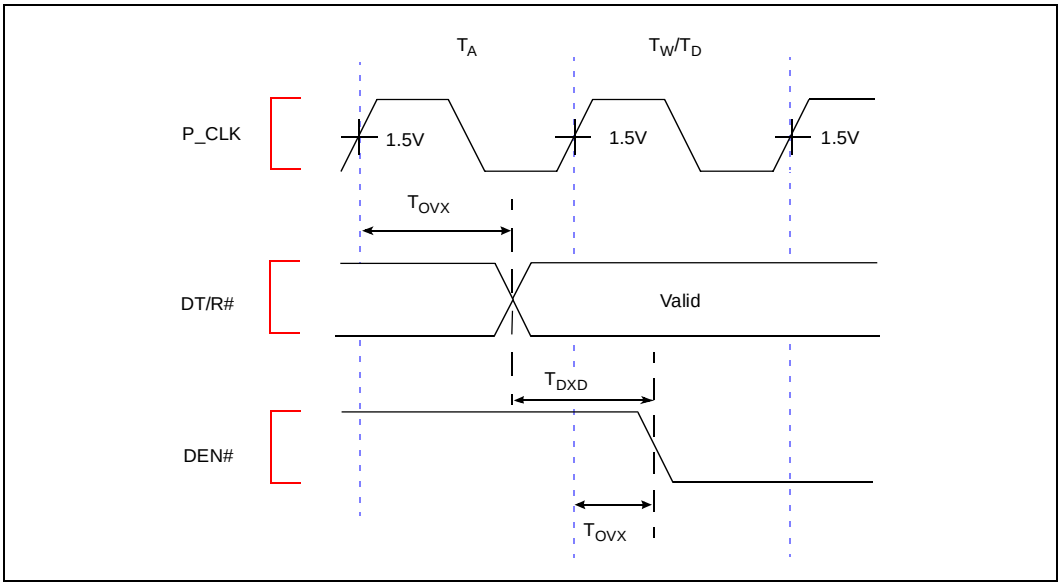
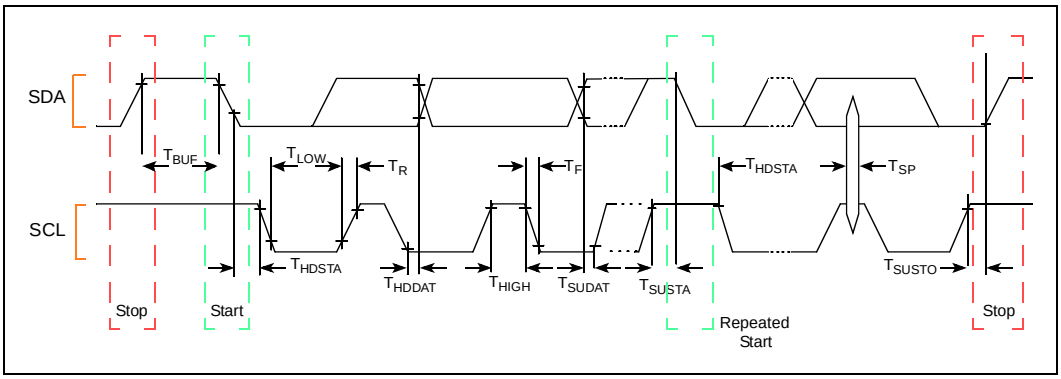


Figure 15. I^2C Interface Signal Timings



4.7 Memory Controller Output Timing Waveforms

Figure 16. Fast Page-Mode Read Access, Non-Interleaved, 2,1,1,1 Wait State, 32-Bit 80960 Local Bus

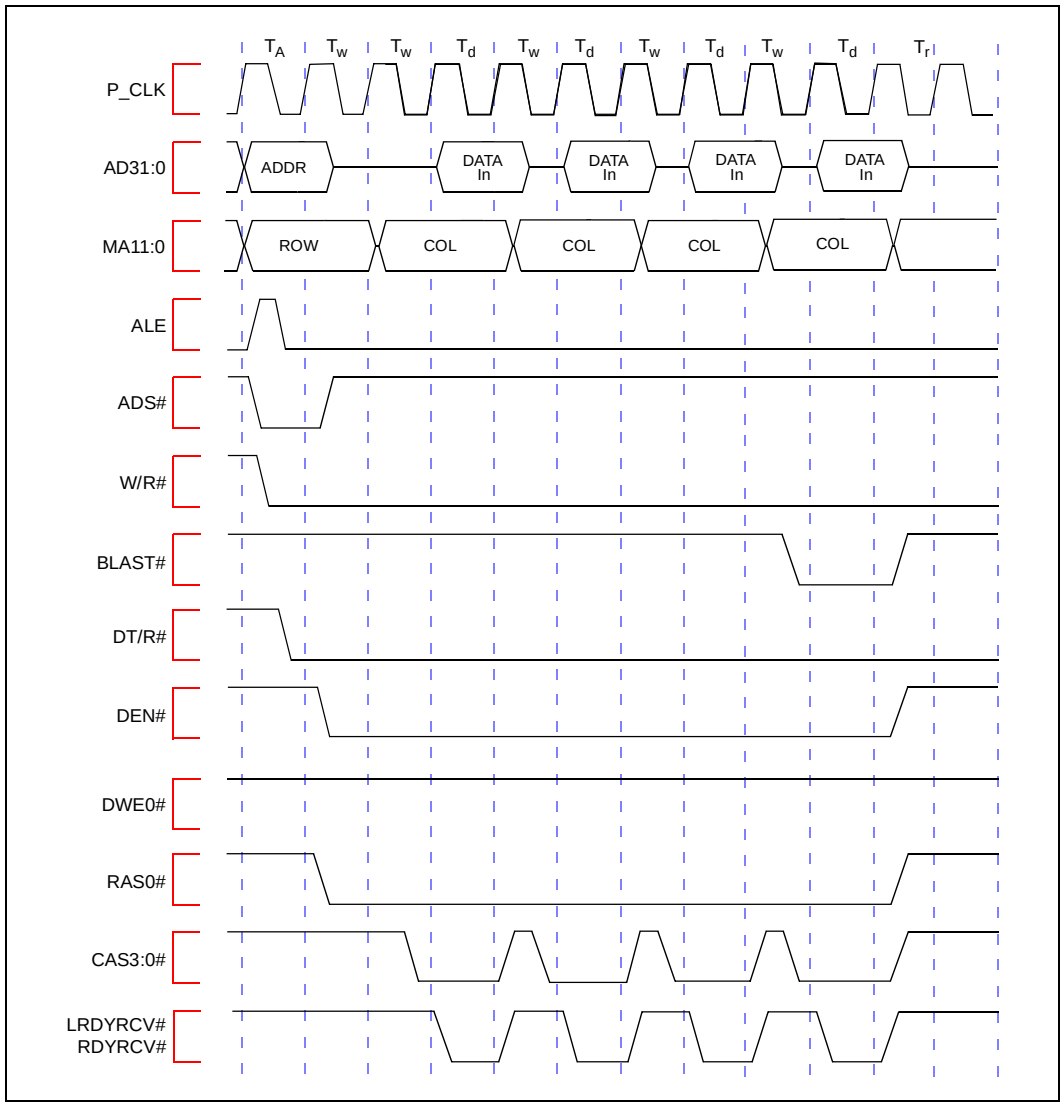


Figure 17. Fast Page-Mode Write Access, Non-Interleaved, 2,1,1,1 Wait States, 32-Bit 80960 Local Bus

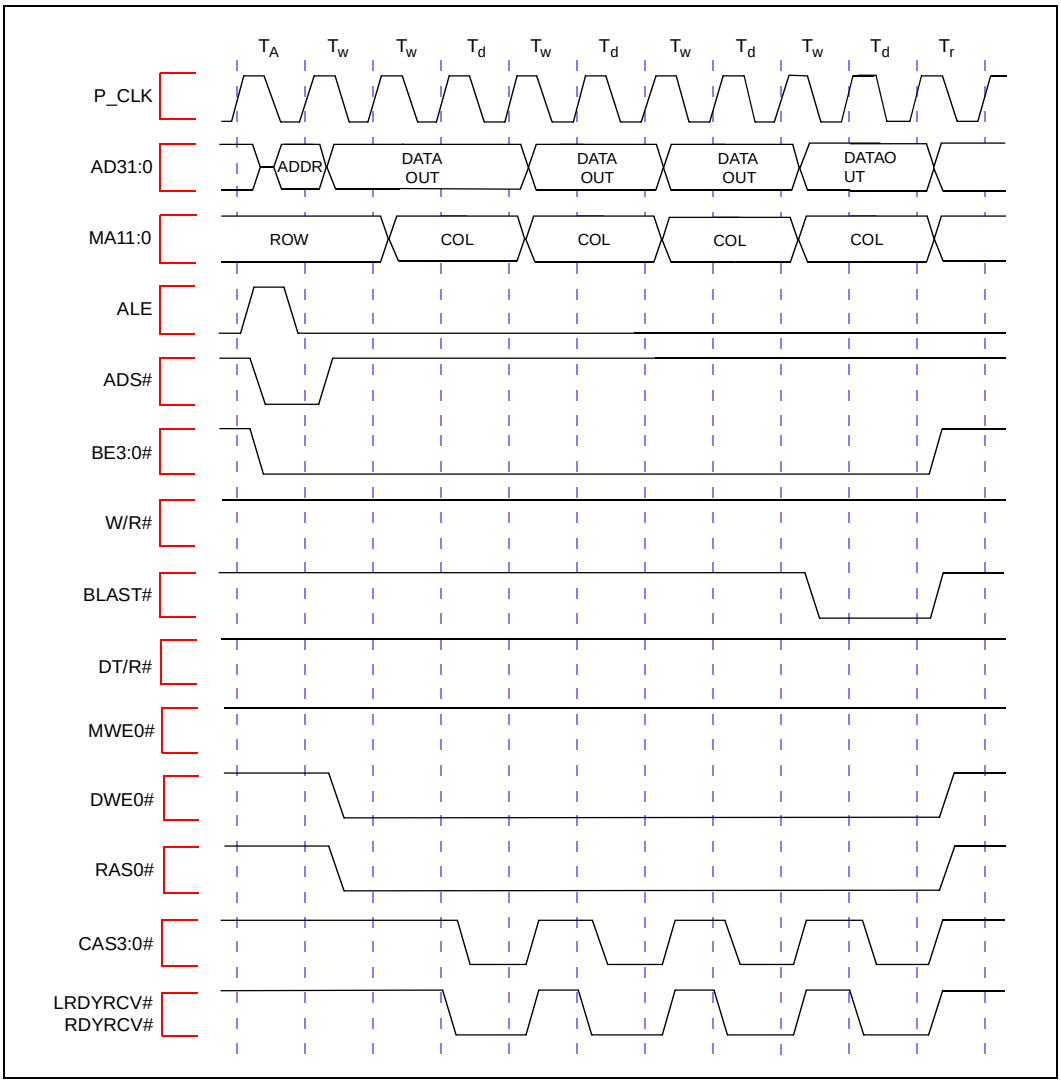


Figure 18. FPM DRAM System Read Access, Interleaved, 2,0,0,0 Wait States

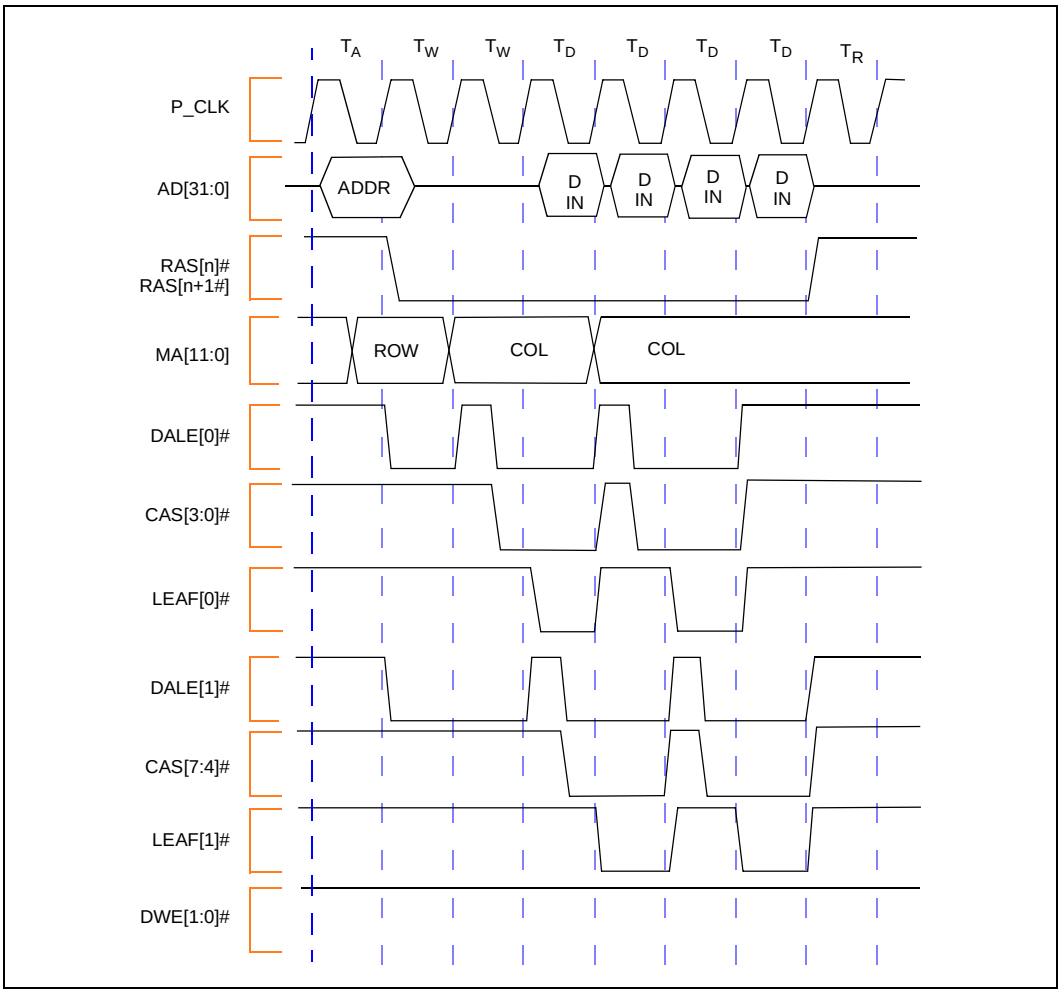


Figure 19. FPM DRAM System Write Access, Interleaved, 1,0,0,0 Wait States

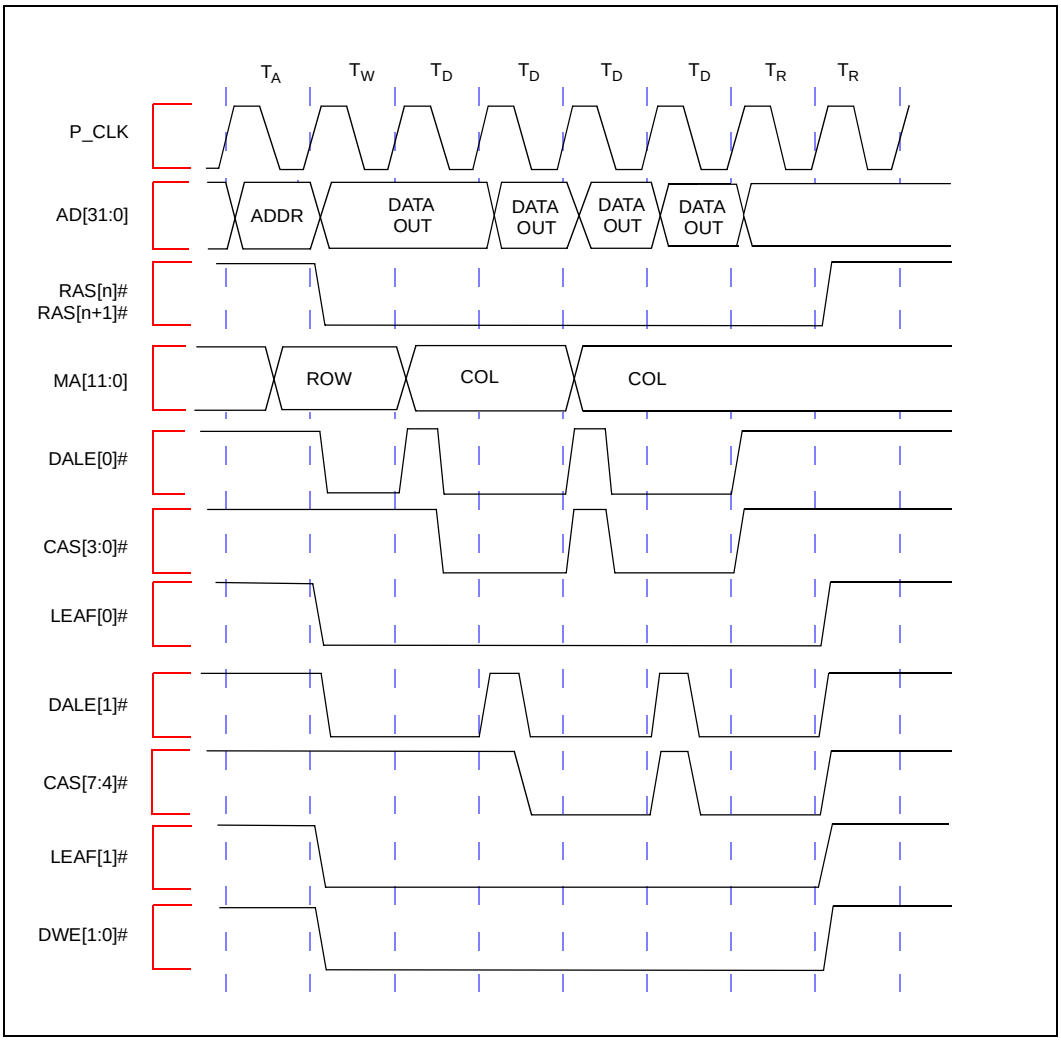


Figure 20. EDO DRAM, Read Cycle

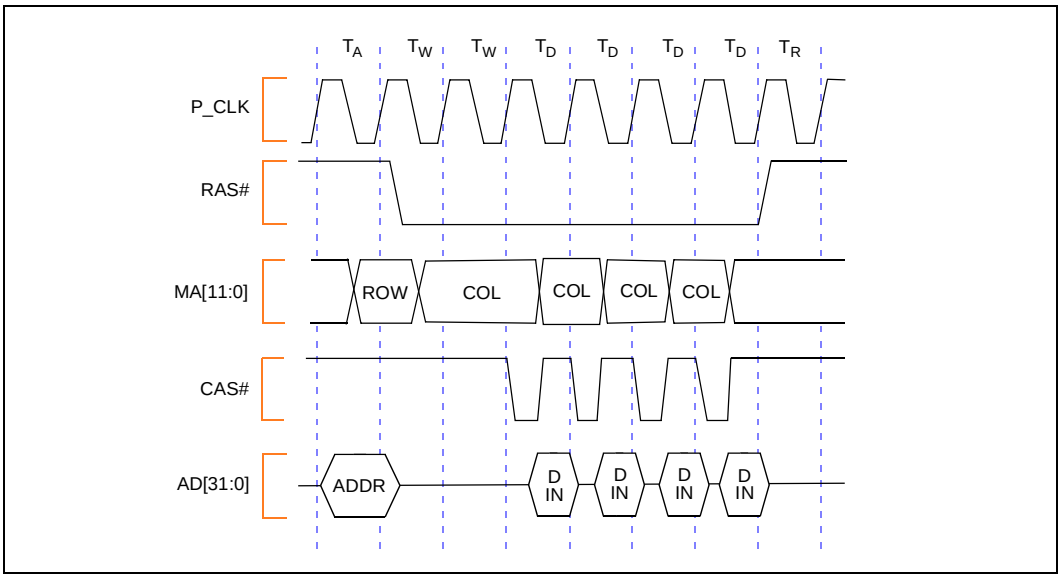


Figure 21. EDO DRAM, Write Cycle

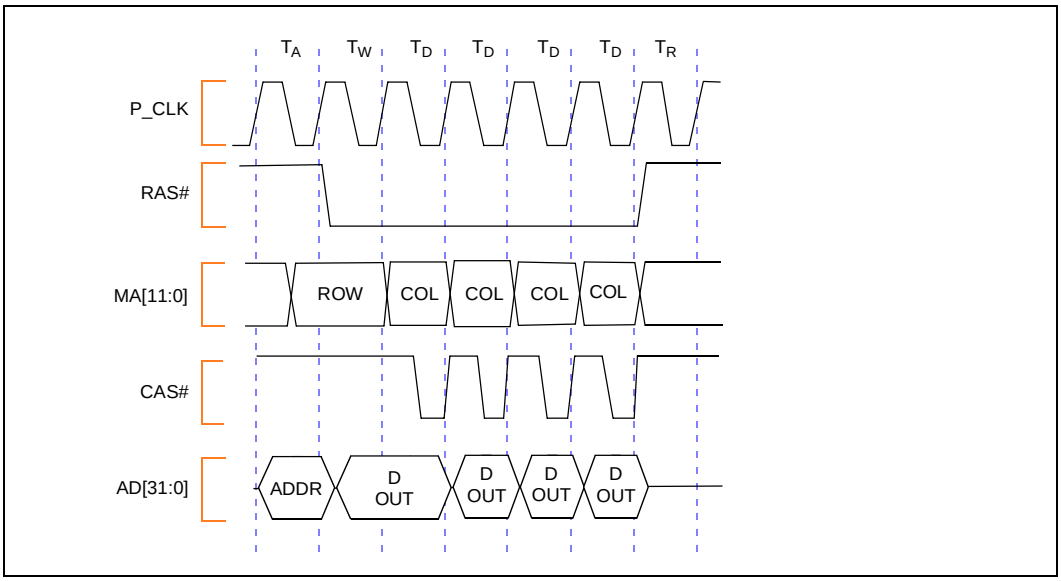


Figure 22. 32-Bit Bus, SRAM Read Accesses with 0 Wait States

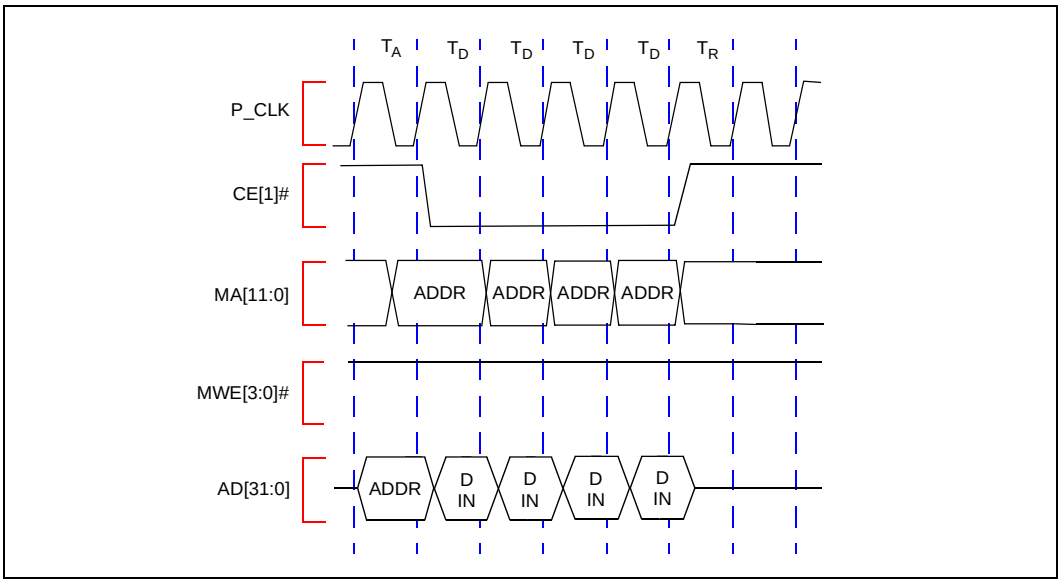
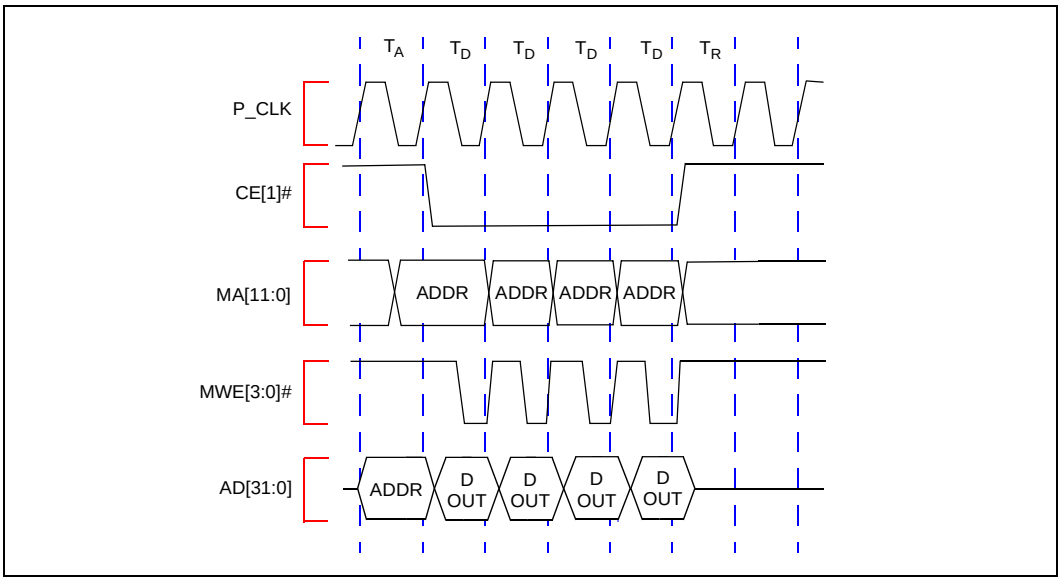


Figure 23. 32-Bit Bus, SRAM Write Accesses with 0 Wait States



5.0 Bus Functional Waveforms

Figure 24. Non-Burst Read and Write Transactions without Wait States, 32-Bit 80960 Local Bus

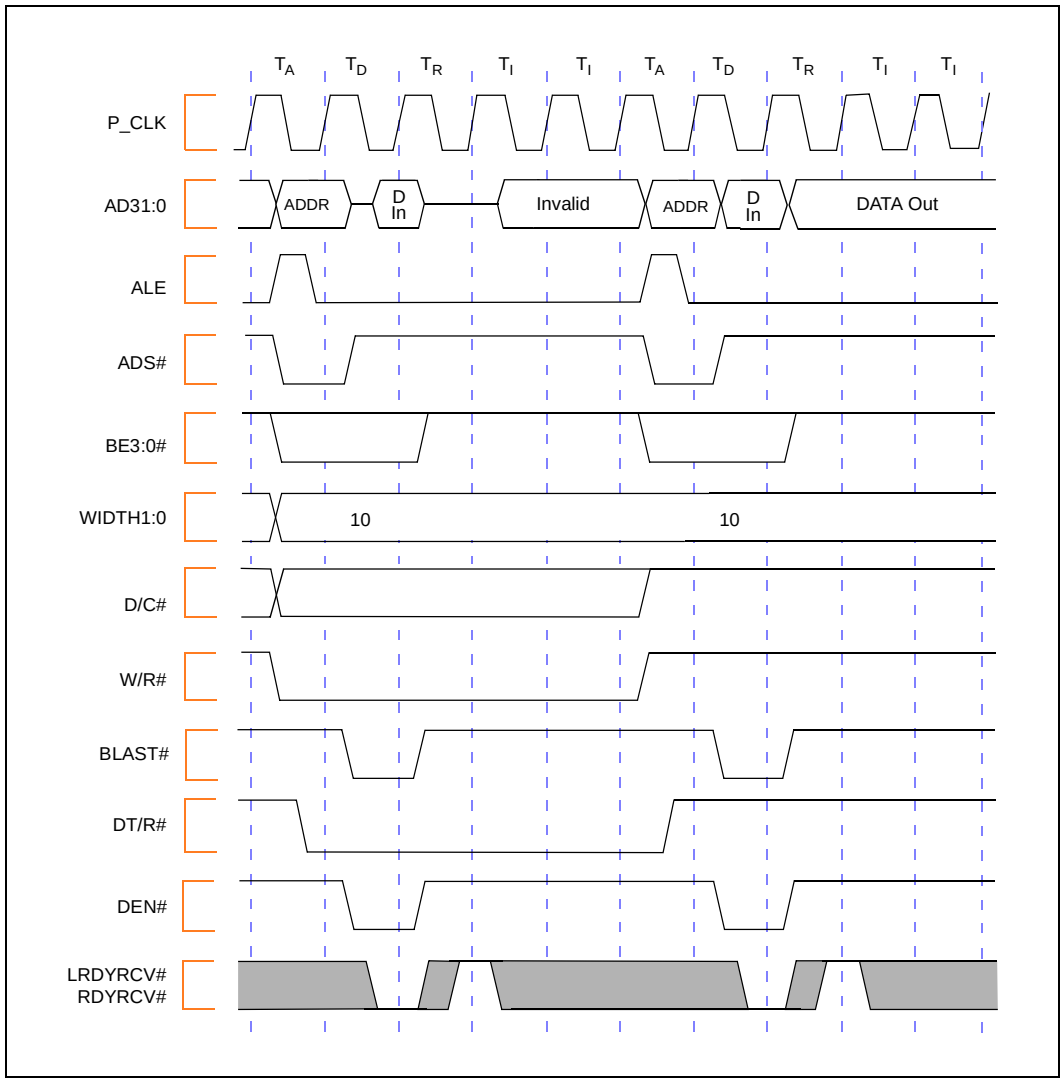


Figure 25. Burst Read and Write Transactions without Wait States, 32-Bit 80960 Local Bus

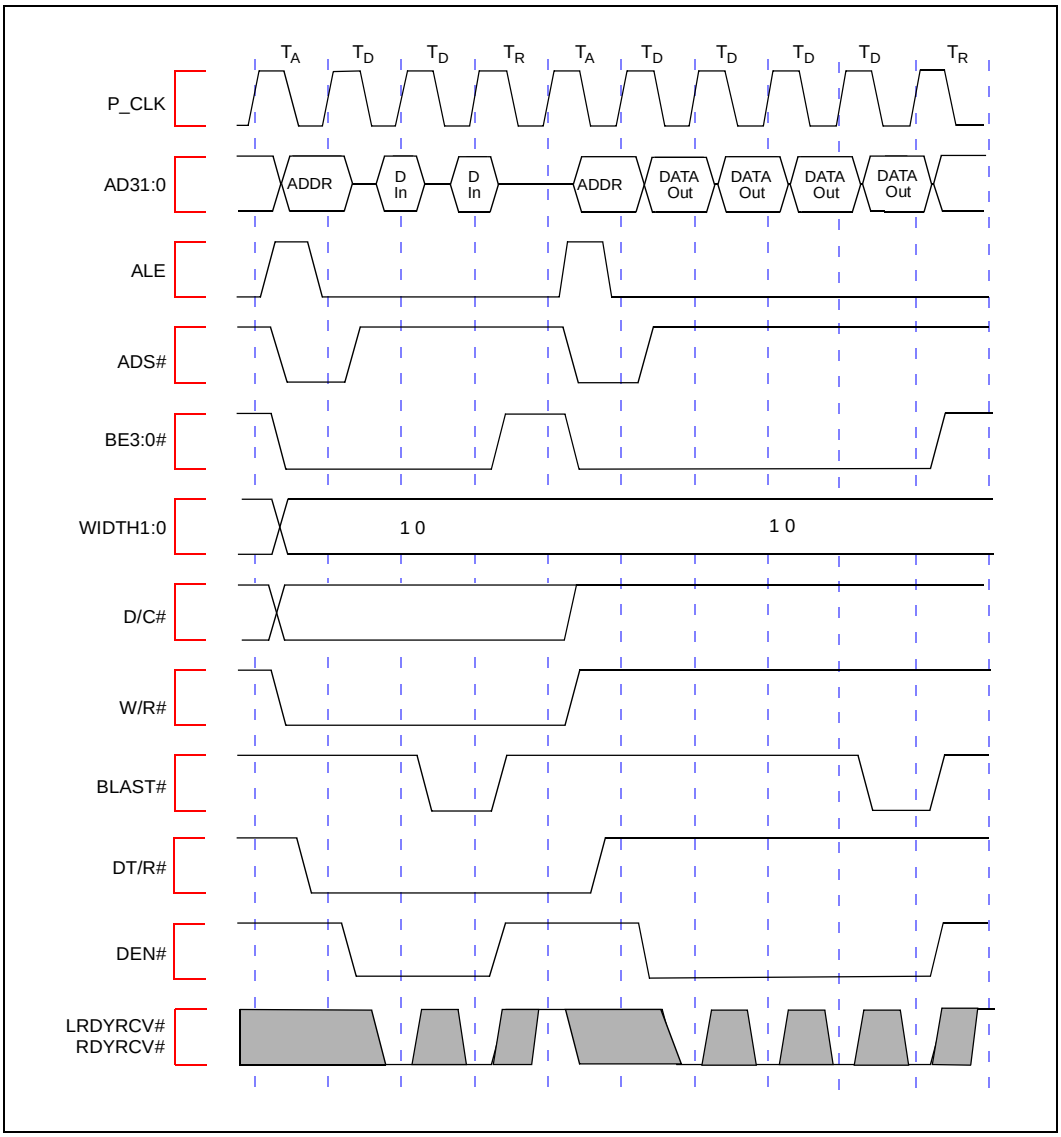


Figure 26. Burst Write Transactions with 2,1,1,1 Wait States, 32-Bit 80960 Local Bus

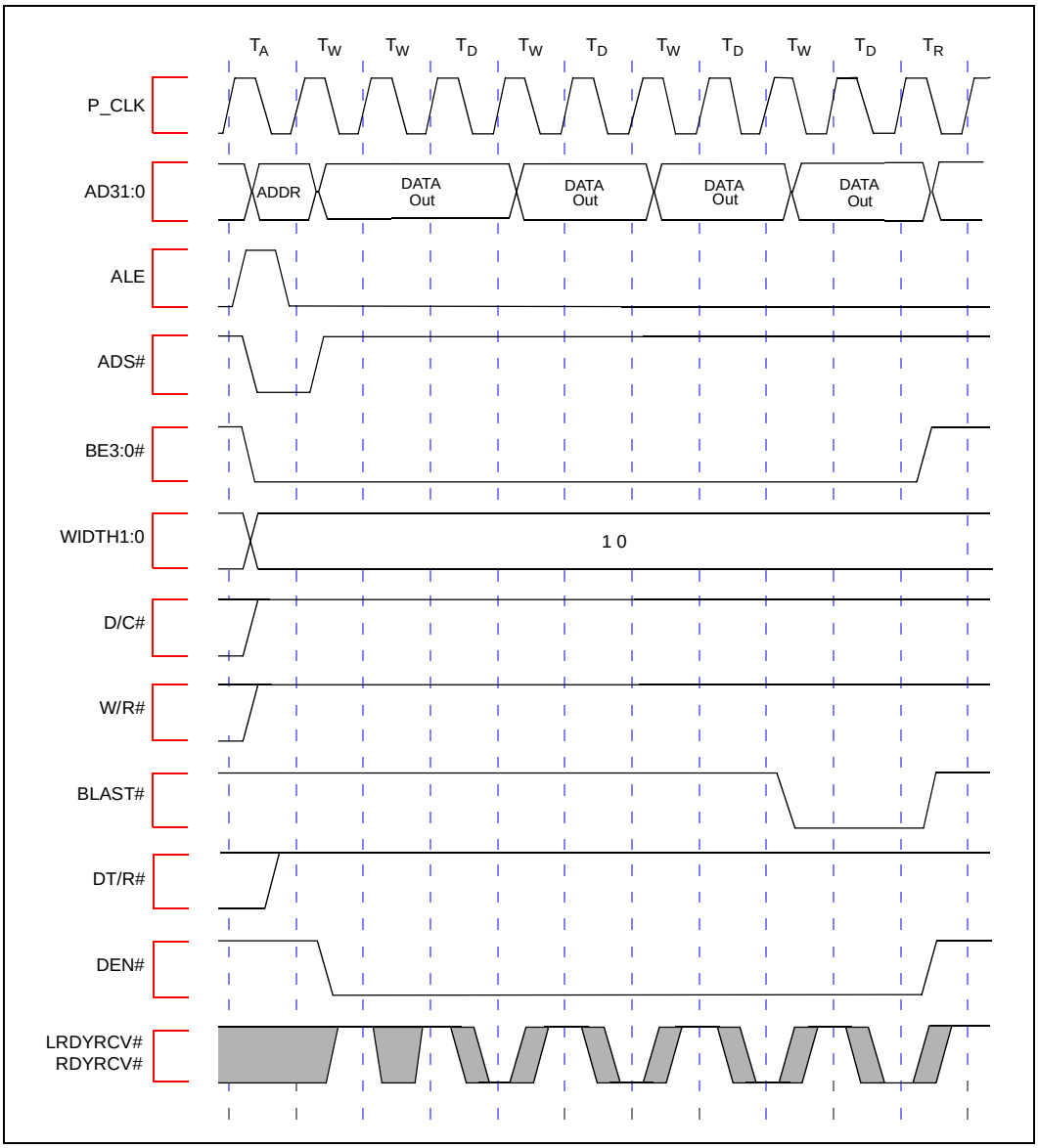


Figure 27. Burst Read and Write Transactions without Wait States, 8-Bit 80960 Local Bus

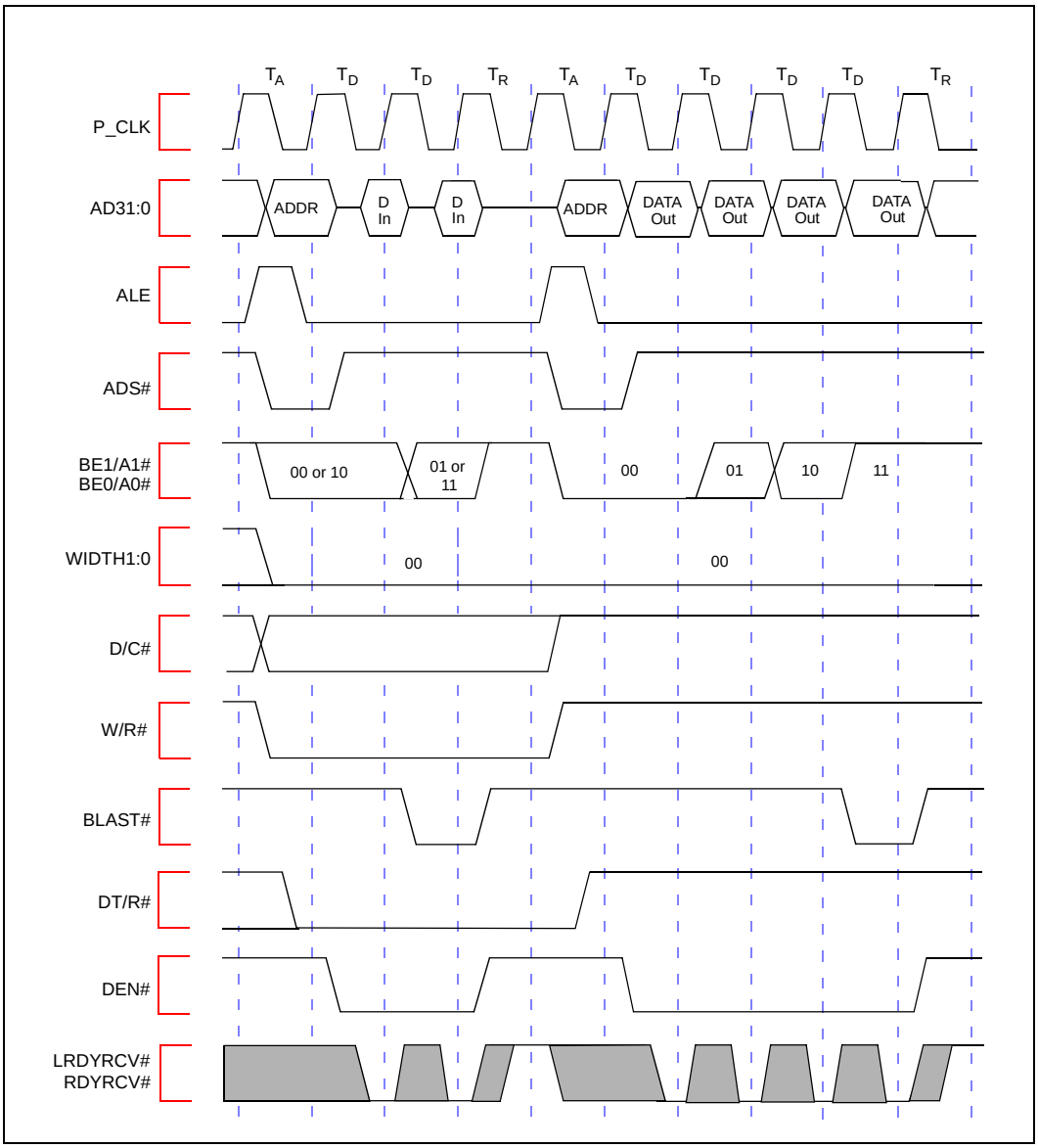


Figure 28. Burst Read and Write Transactions with 1, 0 Wait States and Extra Tr State on Read, 16-Bit 80960 Local Bus

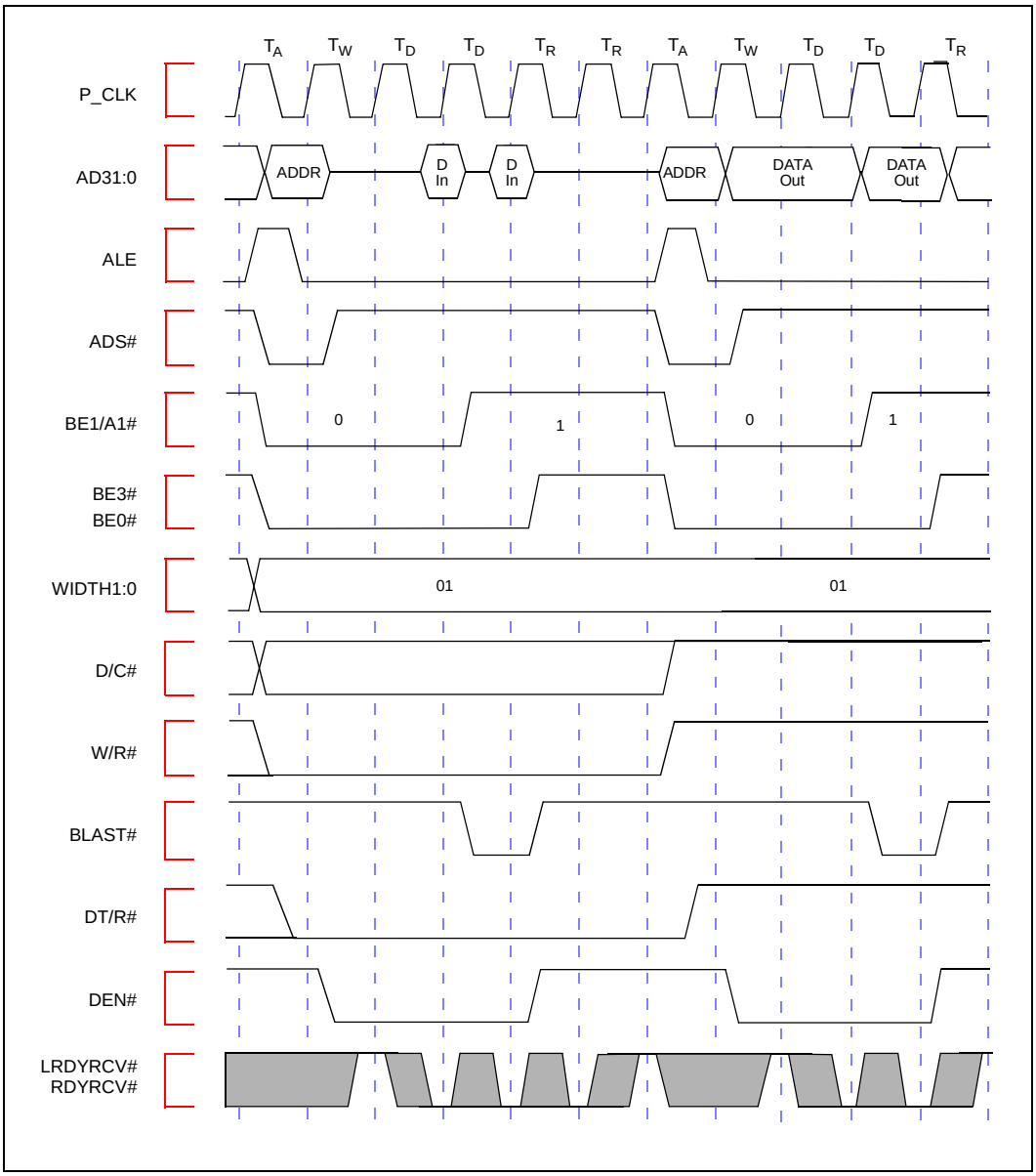


Figure 29. Bus Transactions Generated by Double Word Read Bus Request, Misaligned One Byte From Quad Word Boundary, 32-Bit 80960 Local Bus

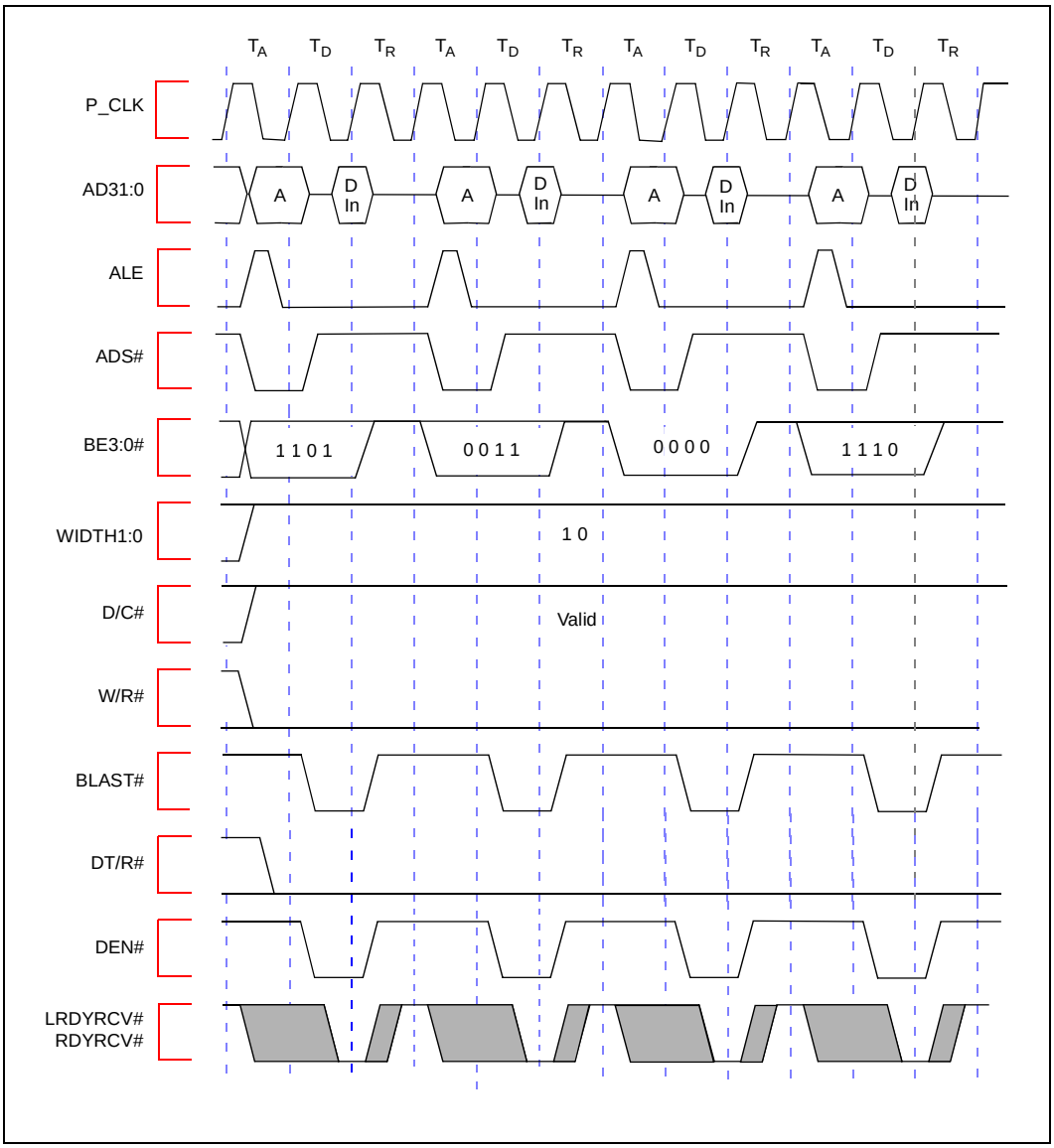
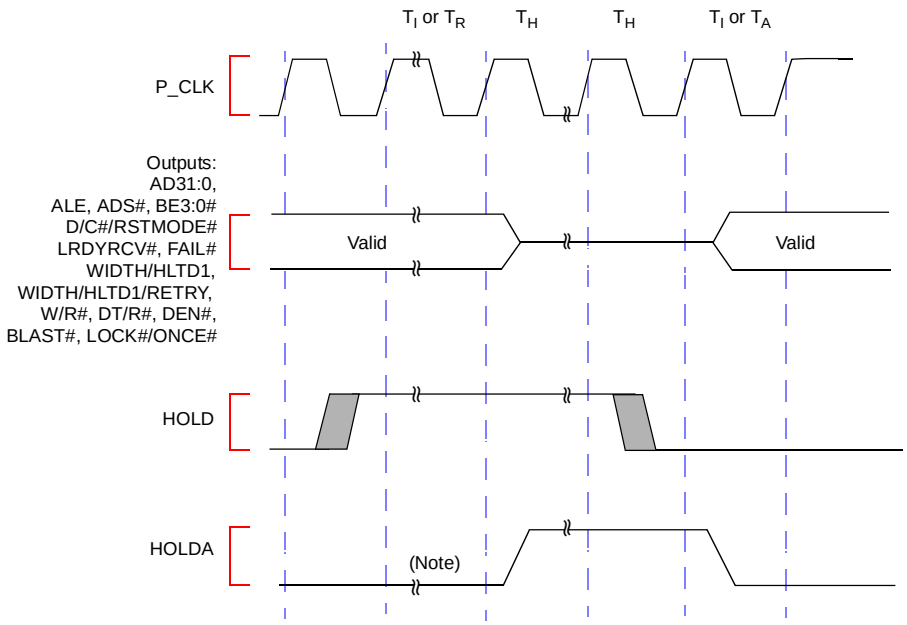
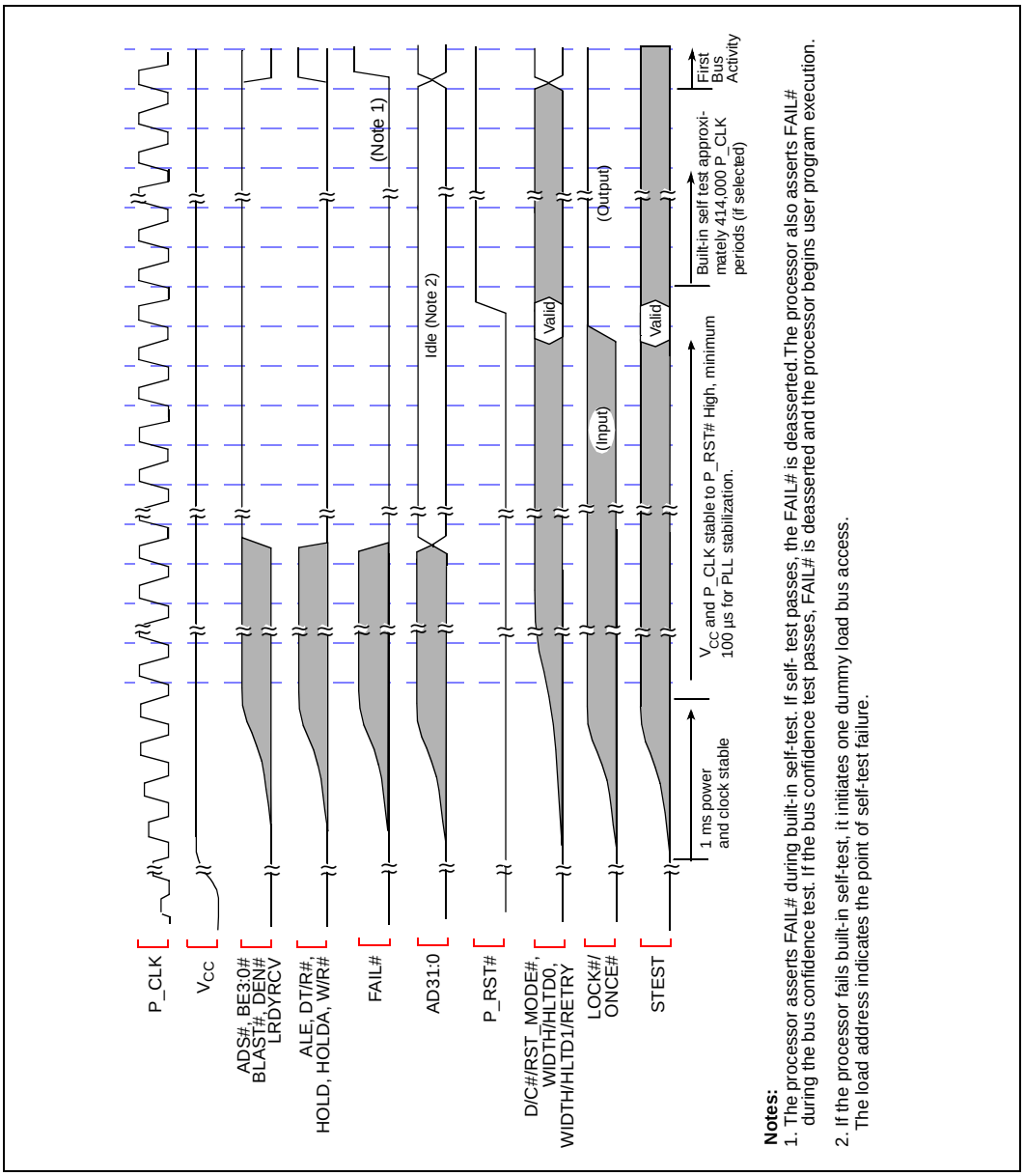


Figure 30. HOLD/HOLDA Waveform For Bus Arbitration



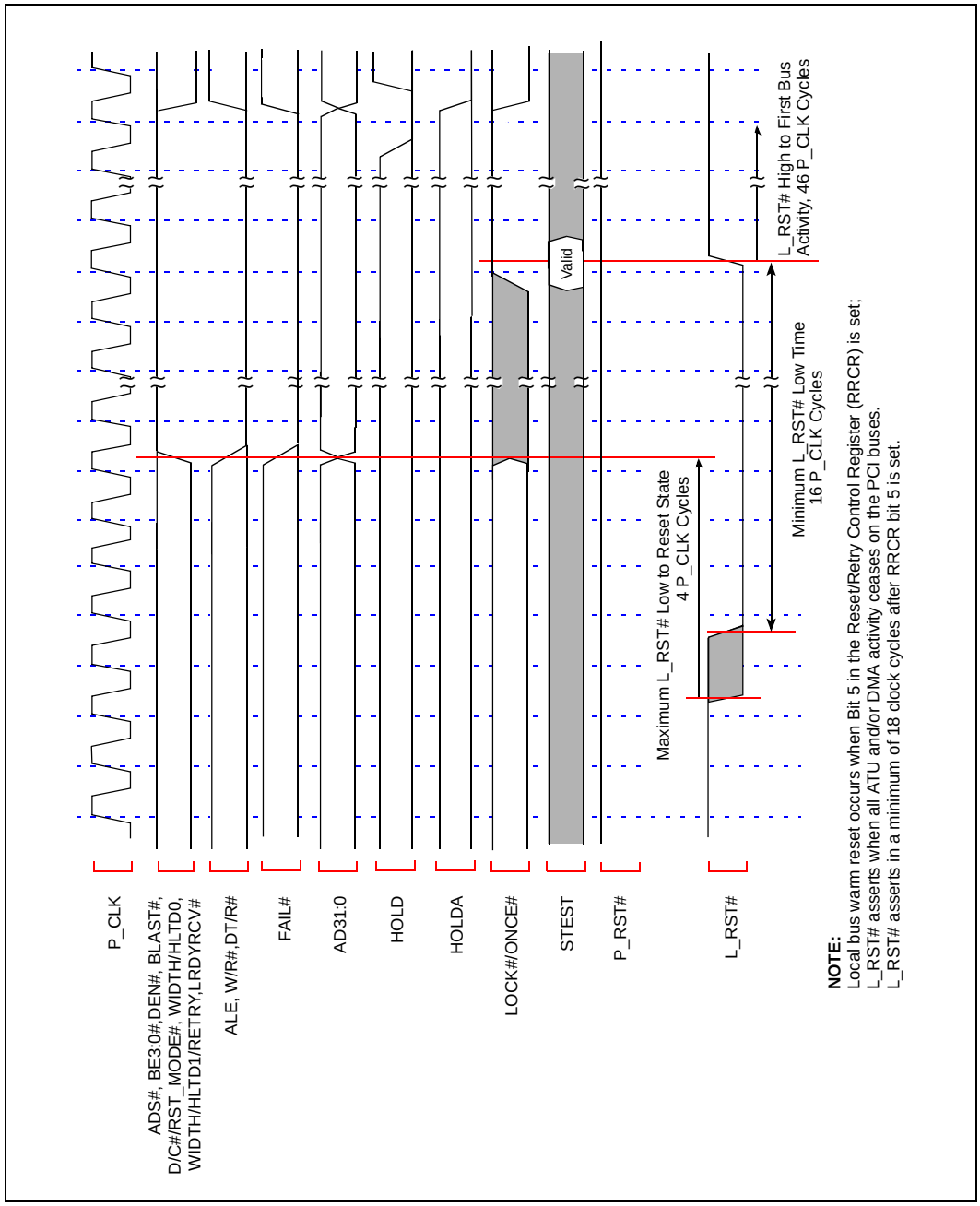
NOTE: HOLD is sampled on the rising edge of P_CLK. HOLDA is granted after the latency counter in the local bus arbiter expires. The processor asserts HOLDA to grant the bus on the same edge in which it recognizes HOLD if the last state was T_i or the last T_r of a bus transaction. Similarly, the processor deasserts HOLDA on the same edge in which it recognizes the deassertion of HOLD.

Figure 31. 80960 Core Cold Reset Waveform



Notes:
1. The processor asserts FAIL# during built-in self-test. If self- test passes, the FAIL# is deasserted.The processor also asserts FAIL# during the bus confidence test. If the bus confidence test passes, FAIL# is deasserted and the processor begins user program execution.
2. If the processor fails built-in self-test, it initiates one dummy load bus access. The load address indicates the point of self-test failure.

Figure 32. 80960 Local Bus Warm Reset Waveform

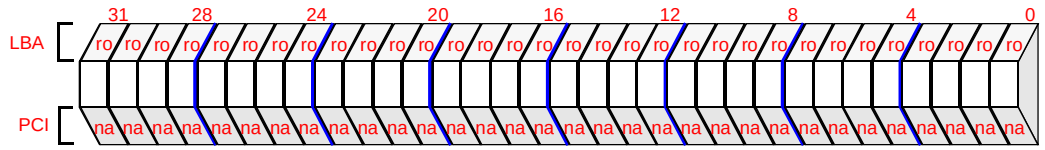


6.0 Device Identification On Reset

During the manufacturing process, values characterizing the i960® VH processor type and stepping are programmed into the memory-mapped registers. The 80960VH contains two read-only device ID MMRs. One holds the Processor Device ID (PDIDR - 0000 1710H) and the other holds the i960 Core Processor Device ID (DEVICEID - FF00 8710H). During initialization, the PDIDR is placed in g0.

The device identification values are compliant with the IEEE 1149.1 specification and Intel standards. Table 30 describes the fields of the two Device IDs.

Table 30. Processor Device ID Register - PDIDR



LBA: 1710H **PCI:** NA		**Legend:**NA = Not AccessibleRO = Read Only RV = ReservedPR = PreservedRW = Read/Write RS = Read/SetRC = Read Clear LBA = 80960 Local Bus Address PCI = PCI Configuration Address Offset
Bit	**Default**	**Description**
31:28	X	Version - Indicates stepping changes.
27	X	V_{CC} - Indicates device voltage type. 0 = 5.0 V 1 = 3.3 V
26:21	X	Product Type - Indicates the generation or “family member”.
20:17	X	Generation Type - Indicates the generation of the device.
16:12	X	Model Type - Indicates member within a series and specific model information.
11:01	X	Manufacturer ID - Indicates manufacturer ID assigned by IEEE. 0000 0001 001 = Intel Corporation
0	X	Constant

NOTE: Values programmed into this register vary with stepping. Refer to the i960® VH processor Specification Update (273174-001) for the correct value.