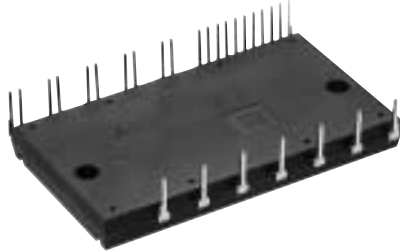


PS22054

TRANSFER-MOLD TYPE
INSULATED TYPE

PS22054



INTEGRATED POWER FUNCTIONS

1200V/15A low-loss 4th generation IGBT inverter bridge
for 3 phase DC-to-AC power conversion

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

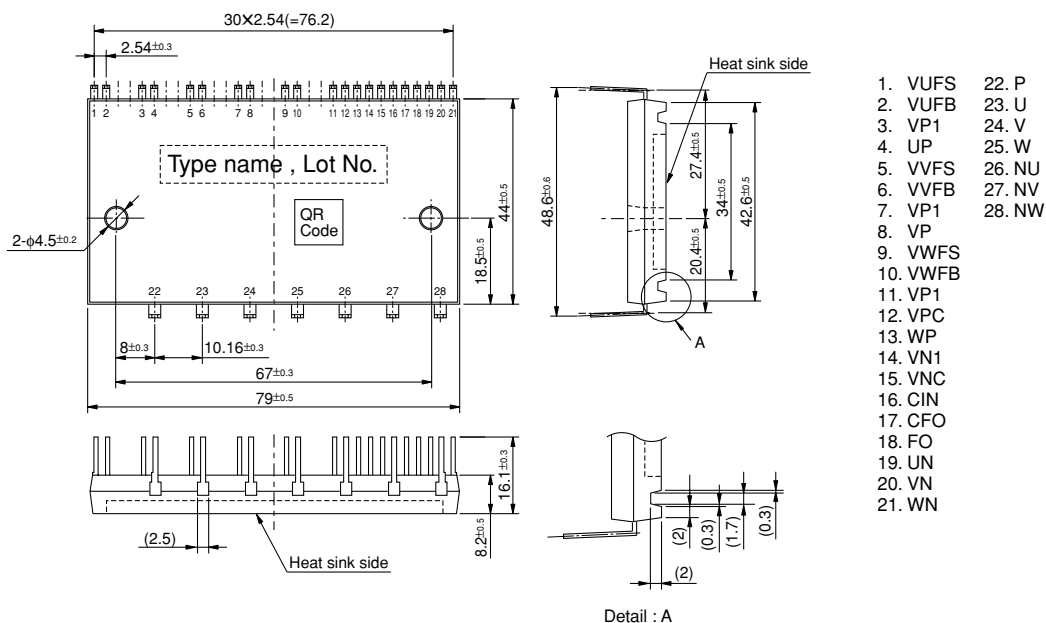
- For upper-leg IGBTs : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-side IGBT) or a UV fault (Lower-side supply).
- Input interface : 5V line CMOS/TTL compatible (High active logic).

APPLICATION

AC400V 0.2kW~2.2kW inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



All external terminals are treated with lead free solder (ingredient : Sn-Cu) plating.

Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

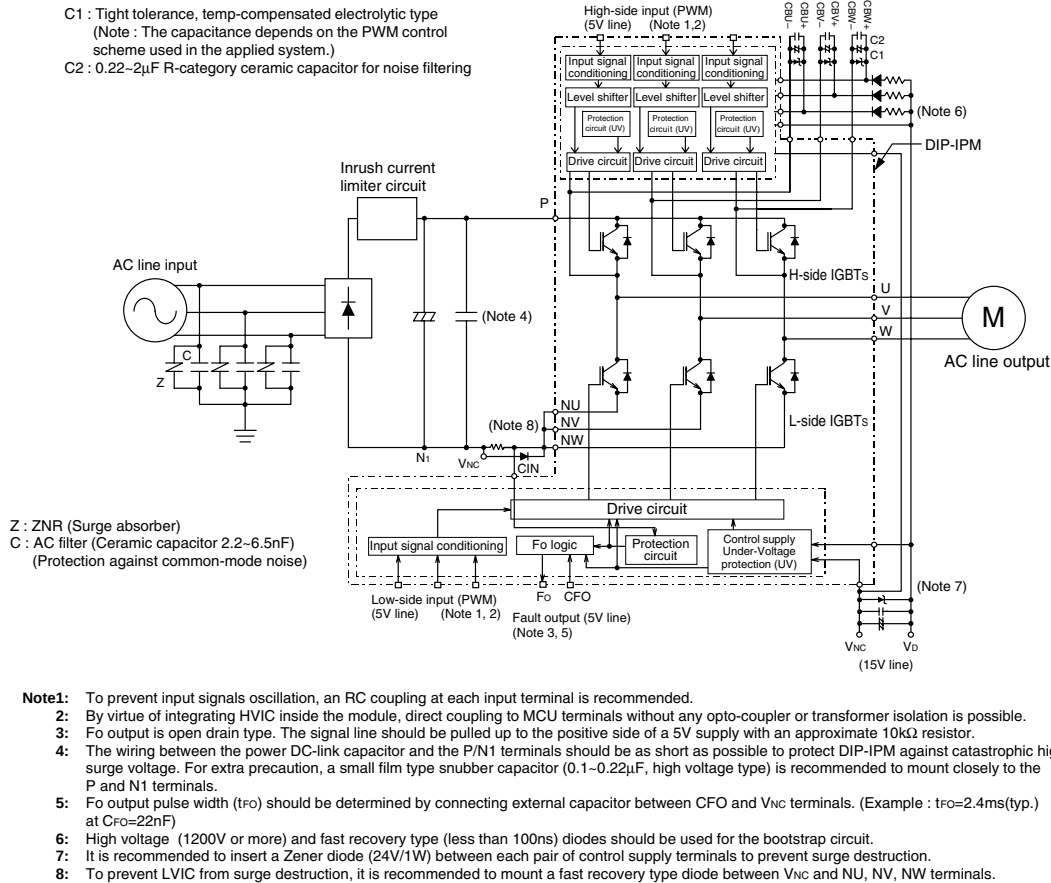
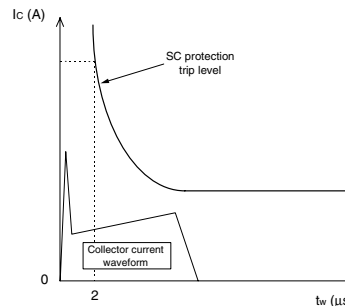
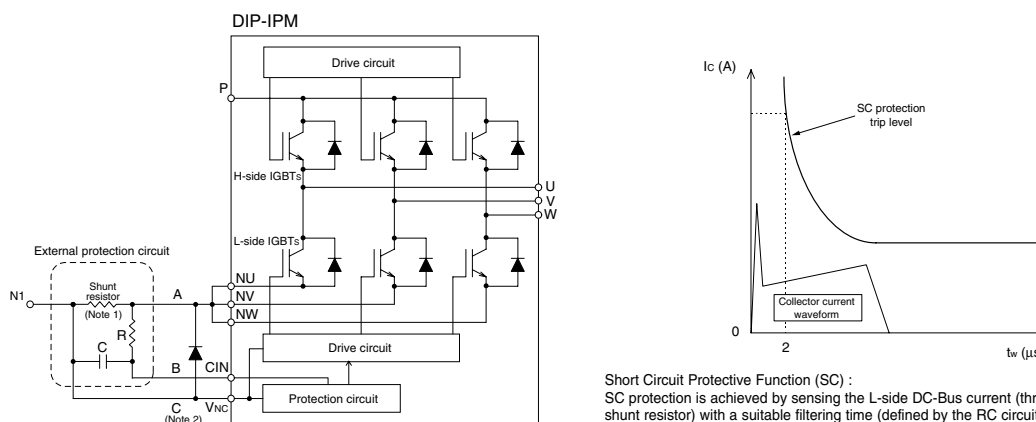


Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



Short Circuit Protective Function (SC) :
SC protection is achieved by sensing the L-side DC-Bus current (through the external shunt resistor) with a suitable filtering time (defined by the RC circuit).
When the sensed shunt voltage exceeds the SC trip-level, all the L-side IGBTs are turned OFF and a fault signal (Fo) is output.
Since the SC fault may be repetitive, it is recommended to stop the system and check the fault, when the Fo signal is received.

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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CC}	Supply voltage	Applied between P-NU, NV, NW	900	V
V _{CC(surge)}	Supply voltage (surge)	Applied between P-NU, NV, NW	1000	V
V _{CES}	Collector-emitter voltage		1200	V
±I _C	Each IGBT collector current	T _C = 25°C	15	A
±I _{CP}	Each IGBT collector current (peak)	T _C = 25°C, less than 1ms	30	A
P _C	Collector dissipation	T _C = 25°C, per 1 chip	56.8	W
T _j	Junction temperature	(Note 1)	-20~+125	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ T_C ≤ 100°C) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to T_{j(ave)} ≤ 125°C (@ T_C ≤ 100°C).

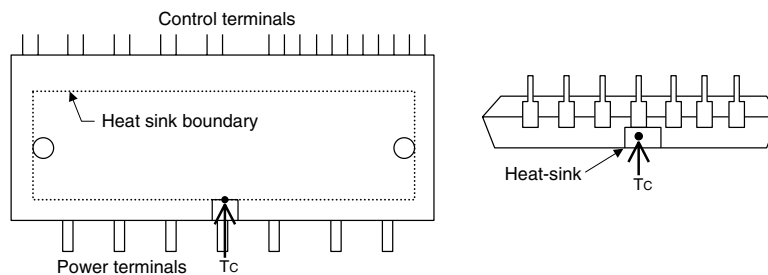
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VP1-VPC, VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V _{IN}	Input voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	-0.5~V _D +0.5	V
V _{FO}	Fault output supply voltage	Applied between FO-VNC	-0.5~V _D +0.5	V
I _{FO}	Fault output current	Sink current at FO terminal	1	mA
V _{SC}	Current sensing input voltage	Applied between CIN-Vnc	-0.5~V _D +0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(PROT)}	Self protection supply voltage limit (short circuit protection capability)	V _D = 13.5~16.5V, Inverter part T _j = 125°C, non-repetitive, less than 2 μs	800	V
T _C	Module case operation temperature	(Note 2)	-20~+100	°C
T _{stg}	Storage temperature		-40~+125	°C
V _{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	2500	V _{rms}

Note 2 : T_C MEASUREMENT POINT



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	1.76	°C/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	—	—	2.41	°C/W
$R_{th(c-f)}$	Contact thermal resistance	Case to fin, (per 1 module) thermal grease applied	—	—	0.047	°C/W

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100 μ m~+200 μ m on the contacting surface of DIP-IPM and heat-sink.

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB} = 15\text{V}$ $V_{IN} = 5\text{V}$, $I_C = 15\text{A}$	—	2.7	3.4	V
V_{EC}	FWDi forward voltage	$-I_C = 15\text{A}$, $V_{IN} = 0\text{V}$	—	2.5	3.0	V
t_{on}	Switching times	$V_{CC} = 600\text{V}$, $V_D = V_{DB} = 15\text{V}$ $I_C = 15\text{A}$, $T_j = 125^\circ\text{C}$, $V_{IN} = 0 \leftrightarrow 5\text{V}$ Inductive load (upper-lower arm)	0.8	1.5	2.2	μs
t_{rr}			—	0.2	—	μs
$t_{c(on)}$			—	0.4	0.7	μs
t_{off}			—	2.8	3.8	μs
$t_{c(off)}$			—	0.4	0.7	μs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$	—	—	1	mA
		$T_j = 125^\circ\text{C}$	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
I_D	Circuit current	$V_D = V_{DB} = 15\text{V}$ $V_{IN} = 5\text{V}$	Total of V_{P1-VPC} , V_{N1-VNC}		3.70	mA
			$V_{UFB-VUFS}$, $V_{VFB-VVFS}$, $V_{WFB-VWFS}$		1.30	
		$V_D = V_{DB} = 15\text{V}$ $V_{IN} = 0\text{V}$	Total of V_{P1-VPC} , V_{N1-VNC}		3.50	mA
			$V_{UFB-VUFS}$, $V_{VFB-VVFS}$, $V_{WFB-VWFS}$		1.30	
V_{FOH}	Fault output voltage	$V_{SC} = 0\text{V}$, F_O circuit pull-up to 5V with 10k Ω	4.9	—	—	V
V_{FOL}		$V_{SC} = 1\text{V}$, $I_{FO} = 1\text{mA}$	—	—	1.10	V
$V_{SC(ref)}$	Short circuit trip level	$T_j = 25^\circ\text{C}$, $V_D = 15\text{V}$ (Note 4)	0.43	0.48	0.53	V
I_{IN}	Input current	$V_{IN} = 5\text{V}$	0.7	1.5	2.0	mA
UV_{DBt}	Supply circuit under-voltage protection	$T_j \leq 125^\circ\text{C}$	Trip level		12.0	V
UV_{DBr}			Reset level		12.5	V
UV_{Dt}			Trip level		12.5	V
UV_{Dr}			Reset level		13.0	V
t_{FO}	Fault output pulse width	$C_{FO} = 22\text{nF}$ (Note 5)	1.6	2.4	—	ms
$V_{th(on)}$	ON threshold voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	2.0	3.0	4.2	V
$V_{th(off)}$	OFF threshold voltage		0.8	1.4	2.0	V

Note 4: Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 1.7 times device current rating.

5: Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : $C_{FO} = 9.3 \times 10^{-6} \times t_{FO} [\text{F}]$.

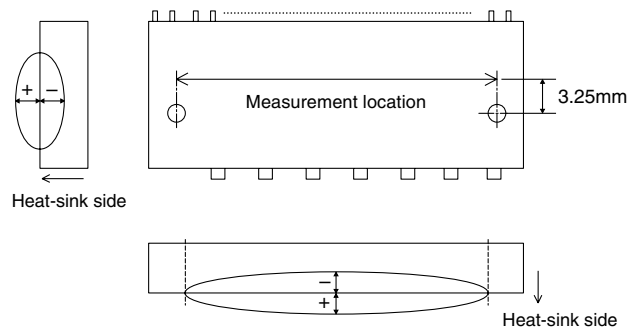
PS22054

TRANSFER-MOLD TYPE
INSULATED TYPE

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4	Recommended 1.18 N·m	0.98	—	1.47	N·m
Weight			—	77	—	g
Heat-sink flatness	(Note 6)		-50	—	100	μm

Note 6: Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
VCC	Supply voltage	Applied between P-NU, NV, NW		350	600	800	V
VD	Control supply voltage	Applied between VP1-VPC, VN1-VNC		13.5	15.0	16.5	V
VDB	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS		13.5	15.0	16.5	V
ΔVD, ΔVDB	Control supply variation			−1	—	1	V/μs
tdead	Arm shoot-through blocking time	For each input signal, TC ≤ 100°C		3.3	—	—	μs
fPWM	PWM input frequency	TC ≤ 100°C, TJ ≤ 125°C		—	—	15	kHz
Io	Output r.m.s. current	VCC = 600V, VD = 15V, fc = 15kHz P.F = 0.8, sinusoidal Tj ≤ 125°C, TC ≤ 100°C (Note 7)		—	—	5.5	Arms
PWIN(on)	Minimum input pulse width	(Note 8)		1.5	—	—	μs
PWIN(off)		350 ≤ VCC ≤ 800V, 13.5 ≤ VD ≤ 16.5V, 13.5 ≤ VDB ≤ 16.5V, −20°C ≤ TC ≤ 100°C, N line wiring inductance less than 10nH (Note 9)	Ic ≤ 15A	2.5	—	—	
			15 < Ic ≤ 25.5A	2.7	—	—	
VNC	VNC variation	Between VNC-NU, NV, NW (including surge)		−5.0	—	5.0	V

Note 7 : The output r.m.s. current value depends on the actual application conditions.

8 : DIP-IPM might not make response to the input on signal with pulse width less than PW_{IN} (on).

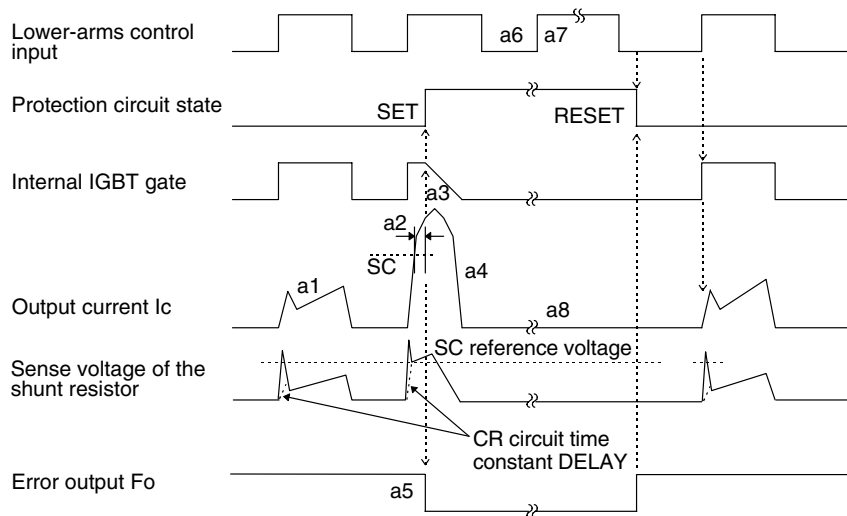
9 : DIP-IPM might not make response or work properly if the input off signal pulse width is less than PW_{IN} (off).

The diagram illustrates a 3-phase inverter with a 4th leg, featuring four HVIC (High Voltage Integrated Circuit) modules (HVIC1, HVIC2, HVIC3, and LVIC) and six IGBTs (IGBT1 through IGBT6) with anti-parallel diodes (Di1 through Di6). The inverter is powered by a 48V battery (V_B) and has a common source (V_S). The output terminals are P, U, V, W, NU, NV, and NW. The input pins include V_{UFB}, V_{UFS}, V_{P1}, U_P, V_{WFB}, V_{WFS}, V_{P1}, V_P, V_{WFB}, V_{WFS}, V_{P1}, W_P, V_{PC}, V_{N1}, U_N, V_N, W_N, F_O, V_{NC}, C_{FO}, and C_{IN}. The LVIC module is connected to V_{CC}, U_{OUT}, UV_{NO}, V_{OUT}, VV_{NO}, W_{OUT}, WV_{NO}, CIN, and GND. The HVIC modules are connected to V_{CC}, V_B, IN, HO, and COM. The IGBTs are connected to V_B, V_S, and the output terminals. The diodes are connected to the output terminals and the common source.

Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS

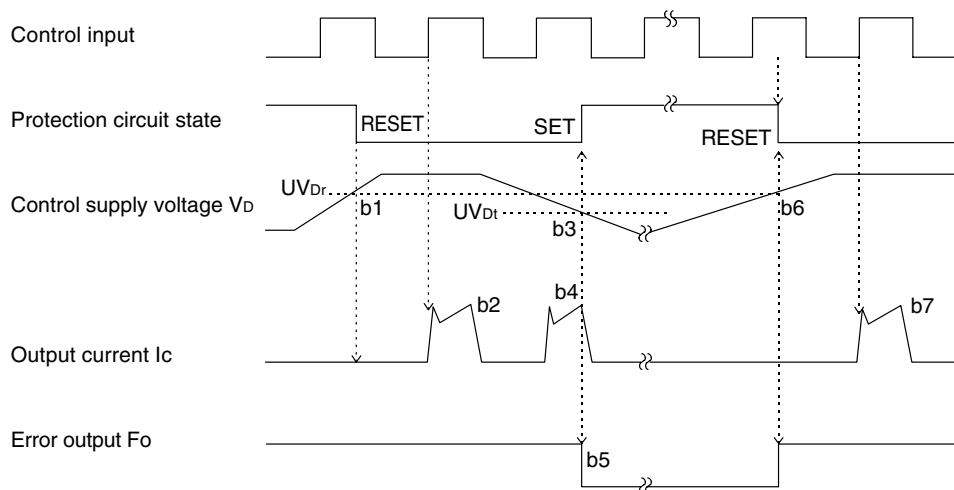
[A] Short-Circuit Protection (Lower-arms only with the external shunt resistor and CR filter)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. IGBT gate hard interruption.
- a4. IGBT turns OFF.
- a5. Fo output with a fixed pulse width determined by the external capacitor C_{FO}.
- a6. Input = "L" : IGBT OFF
- a7. Input = "H" :
- a8. IGBT OFF state in spite of input "H".



[B] Under-Voltage Protection (Lower-arm, UVd)

- b1. Control supply voltage rising : After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV_{Dt}).
- b4. IGBT OFF in spite of control input condition.
- b5. Fo keeps output during the UV period, however, Fo pulse is not less than the fixed width for very short UV interval.
- b6. Under voltage reset (UV_{Dr}).
- b7. Normal operation : IGBT ON and carrying current.



[C] Under-Voltage Protection (Upper-side, UVDB)

- c1. Control supply voltage rises : After the voltage reaches UVDBr, the circuits start to operate when next input is applied.
- c2. Normal operation : IGBT ON and carrying current.
- c3. Under voltage trip (UVDBt).
- c4. IGBT OFF in spite of control input signal level, but there is no Fo signal output.
- c5. Under voltage reset (UVDBr).
- c6. Normal operation : IGBT ON and carrying current.

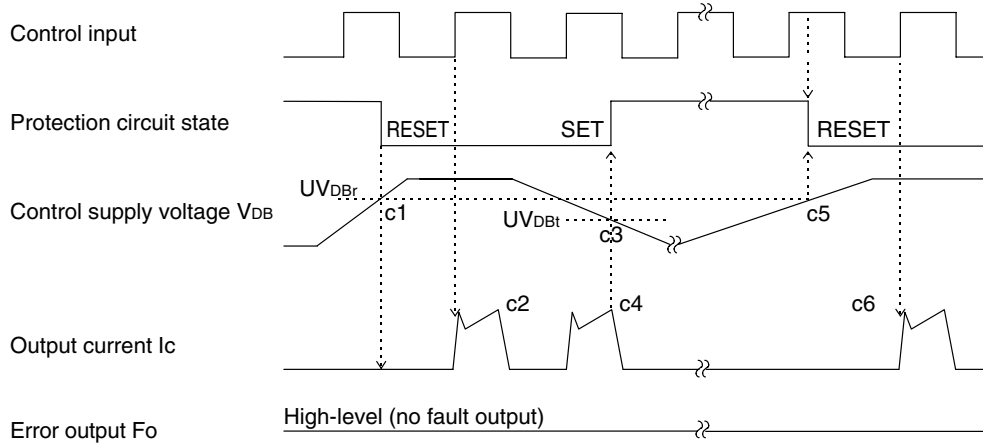
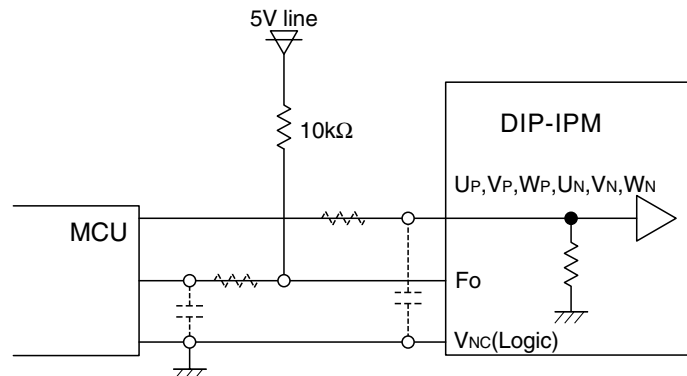
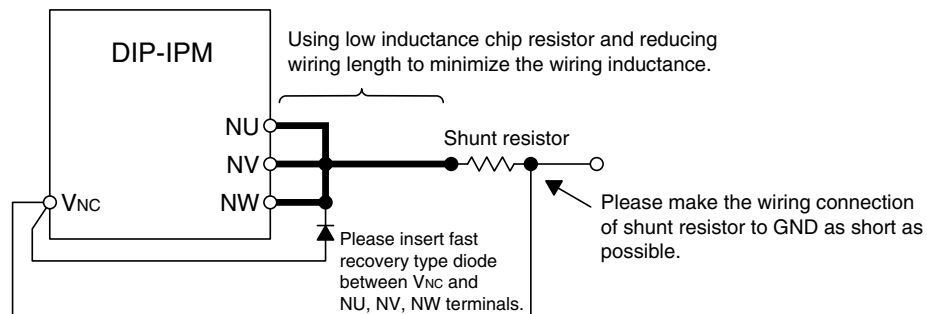


Fig. 6 MCU I/O INTERFACE CIRCUIT



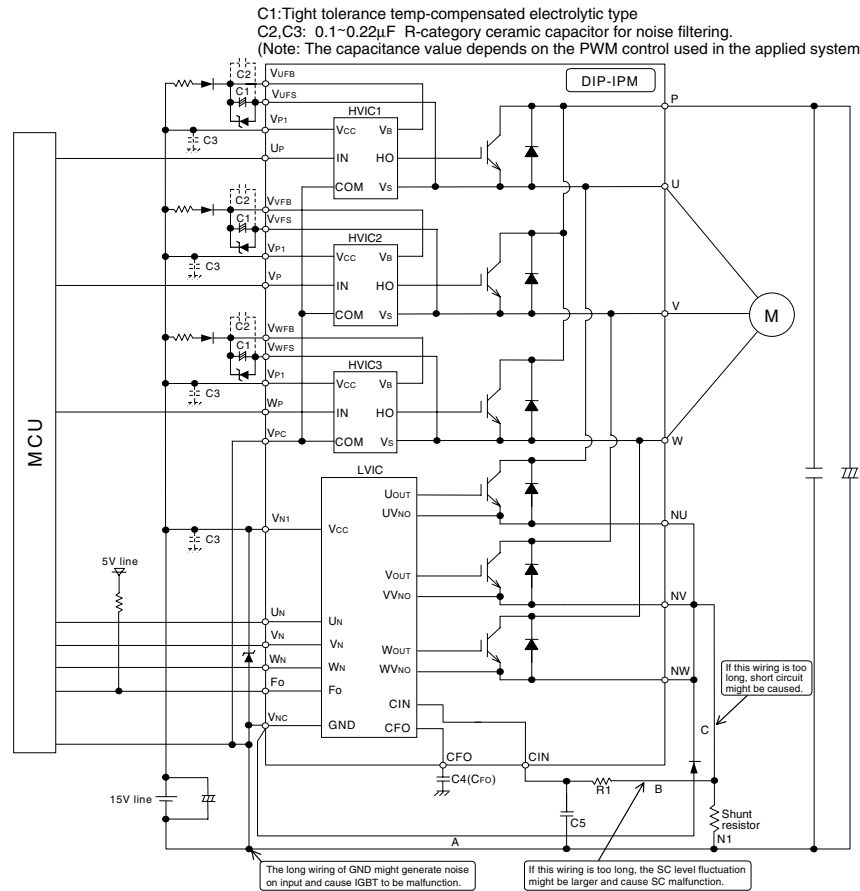
Note : RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board.
The DIP-IPM input signal section integrates a 2.5kΩ(min) pull-down resistor. Therefore, when using a external filtering resistor, pay attention to the turn-on threshold voltage requirement.

Fig. 7 WIRING CONNECTION WITH 1 SHUNT RESISTOR



For 3 shunt resistors connection, please refer to Fig.9.

Fig. 8 AN EXAMPLE OF TYPICAL DIP-IPM APPLICATION CIRCUIT WITH 1 SHUNT RESISTOR



- Note 1:** To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)
- 2:** By virtue of integrating HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.
- 3:** Fo output is open drain type. The signal line should be pulled up to the positive side of a 5V supply with an approximate 10k Ω resistor.
- 4:** Fo output pulse width (tFO) should be determined by connecting external capacitor C4 between CFO and Vnc terminals. (Example : tFO=2.4ms(typ.) at CFO=22nF)
- 5:** Input signal is High-Active type. There is a 2.5k Ω (Min.) resistor inside IC to pull down each input signal line to GND.
- 6:** When employing RC coupling circuits at each input, set up RC couple such that input signal agree with turn-off/turn-on threshold voltage.
- 7:** To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.
- 8:** The time constant R5C1 of the protection circuit should be selected in the range of 1.5~2 μ s. SC interrupting time might vary with the wiring pattern.
- 9:** All capacitors should be mounted as close to the terminals of the DIP-IPM as possible.
- 10:** To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 terminals should be as short as possible. Generally a 0.1~0.22 μ F snubber between the P&N1 terminals is recommended.
- 11:** It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
- 12:** To prevent LVIC from surge destruction, it is recommended to mount a fast recovery type diode between Vnc and NU, NV, NW terminals.

Fig. 9 EXAMPLE OF EXTERNAL PROTECTION CIRCUIT WITH 3 SHUNT RESISTORS

