

DUAL 15-Ω SPDT ANALOG SWITCH

Check for Samples: [TS5A23157-Q1](#)

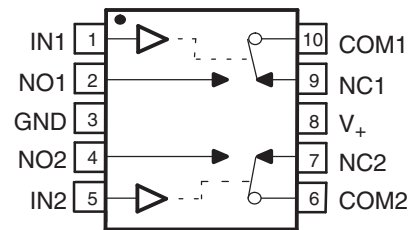
FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: –40°C to 125°C
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C4B
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Specified Break-Before-Make Switching
- Low ON-State Resistance (15 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-Resistance Matching

- Low Total Harmonic Distortion
- 1.8-V to 5.5-V Single-Supply Operation

APPLICATIONS

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits



DESCRIPTION

The TS5A23157 is a dual, single-pole, double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. The device can transmit signals up to 5.5 V (peak) in either direction.

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Table 1. FUNCTION TABLE

INPUT IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 2. SUMMARY OF CHARACTERISTICS

Configuration	2:1 Multiplexer and Demultiplexer (2 × SPDT)
Number of channels	2
r_{on}	15 Ω
Δr_{on}	0.15 Ω
$r_{on(flat)}$	4 Ω
t_{ON}	8.7 ns
t_{OFF}	6.8 ns
t_{BBM}	0.5 ns
Charge injection	7 pC
Bandwidth	220 MHz
OFF isolation	–65 dB at 10 MHz
Crosstalk	–66 dB at 10 MHz
Total harmonic distortion	0.01%
$I_{COM(off)}/I_{NC(off)}$	± 1 μ A
Package option	10-pin DGS

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Supply voltage range ⁽²⁾	–0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage range ^{(2) (3) (4)}	–0.5	$V_+ + 0.5$	V
$I_{I/OK}$	Analog port diode current $V_{NC}, V_{NO}, V_{COM} < 0$ or $V_{NC}, V_{NO}, V_{COM} > V_+$		± 50	mA
I_{NC} I_{NO} I_{COM}	On-state switch current $V_{NC}, V_{NO}, V_{COM} = 0$ to V_+		± 50	mA
V_{IN}	Digital input voltage range ^{(2) (3)}	–0.5	6.5	V
I_{IK}	Digital input clamp current $V_{IN} < 0$		–50	mA
	Continuous current through V_+ or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽⁵⁾		165.36	°C/W
T_{stg}	Storage temperature range	–65	150	°C
ESD	Electrostatic discharge rating	Human-body model H2		2
		Charged-device model C4B		750

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) This value is limited to 5.5 V maximum.

(5) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply

 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NO} , V _{NC}					0		V ₊	V
ON-state resistance	r _{on}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −30 mA,	Switch ON, See Figure 6	Full	4.5 V			15	Ω
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 3.15 V, I _{COM} = −30 mA,	Switch ON, See Figure 6	25°C	4.5 V	0.15			Ω
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −30 mA,	Switch ON, See Figure 6	25°C	4.5 V	4			Ω
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 0 to V ₊ , V _{COM} = 0 to V ₊ ,	Switch OFF, See Figure 7	25°C	5.5 V	−1	0.05	1	μA
				Full		−1	1		
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 0 to V ₊ , V _{COM} = Open,	Switch ON, See Figure 7	25°C	5.5 V	−0.1		0.1	μA
				Full		−1	1		
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 0 to V ₊ ,	Switch ON, See Figure 7	25°C	5.5 V	−0.1		0.1	μA
				Full		−1	1		
Digital Inputs (IN1, IN2) ⁽²⁾									
Input logic high	V _{IH}			Full		V ₊ × 0.7			V
Input logic low	V _{IL}			Full		V ₊ × 0.3			V
Input leakage current	I _{IH} , I _{IL}	V _{IN} = 5.5 V or 0		25°C	5.5 V	−1	0.05	1	μA
				Full		−1	1		

(1) $T_A = 25^\circ\text{C}$

(2) Hold all unused digital inputs of the device at V_+ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

Electrical Characteristics for 5-V Supply (continued)

$V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
Dynamic								
Turnon time	t_{ON}	$V_{NC} = \text{GND and } V_{NO} = V_+$, or $V_{NC} = V_+$ and $V_{NO} = \text{GND}$, $R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, See Figure 9	Full	4.5 V to 5.5 V	1.2		8.7	ns
Turnoff time	t_{OFF}	$V_{NC} = \text{GND and } V_{NO} = V_+$, or $V_{NC} = V_+$ and $V_{NO} = \text{GND}$, $R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, See Figure 9	Full	4.5 V to 5.5 V	0.5		6.8	ns
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 10	25°C	4.5 V to 5.5 V	0.5			ns
Charge injection	Q_C	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$, See Figure 14	25°C	5 V		7		pC
NC, NO OFF capacitance	$C_{NC(OFF)},$ $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF, See Figure 8	25°C	5 V		5.5		pF
NC, NO ON capacitance	$C_{NC(ON)},$ $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON, See Figure 8	25°C	5 V		17.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 8	25°C	5 V		17.5		pF
Digital input capacitance	C_{IN}	$V_{IN} = V_+$ or GND, See Figure 8	25°C	5 V		2.8		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON, See Figure 11	25°C	4.5 V		220		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch OFF, See Figure 12	25°C	4.5 V		–65		dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch ON, See Figure 13	25°C	4.5 V		–66		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 600\text{ Hz to }20\text{ kHz}$, See Figure 15	25°C	4.5 V		0.01		%
Supply								
Positive supply current	I_+	$V_{IN} = V_+$ or GND, Switch ON or OFF	25°C	5.5 V			1	μA
			Full				10	
Change in supply current	ΔI_+	$V_{IN} = V_+ - 0.6\text{ V}$	Full	5.5 V			500	μA

Electrical Characteristics for 3.3-V Supply

 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NO} , V _{NC}					0		V ₊	V
ON-state resistance	r _{on}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −24 mA,	Switch ON, See Figure 6	Full	3 V			23	Ω
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 2.1 V, I _{COM} = −24 mA,	Switch ON, See Figure 6	25°C	3 V	0.2			Ω
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −24 mA,	Switch ON, See Figure 6	25°C	3 V	9			Ω
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 0 to V ₊ , V _{COM} = 0 to V ₊ ,	Switch OFF, See Figure 7	25°C	3.6 V	−1	0.05	1	μA
				Full		−1	1		
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 0 to V ₊ , V _{COM} = Open,	Switch ON, See Figure 7	25°C	3.6 V	−0.1		0.1	μA
				Full		−1	1		
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 0 to V ₊ ,	Switch ON, See Figure 7	25°C	3.6 V	−0.1		0.1	μA
				Full		−1	1		
Digital Inputs (IN1, IN2) ⁽²⁾									
Input logic high	V _{IH}			Full		V ₊ × 0.7			V
Input logic low	V _{IL}			Full		V ₊ × 0.3			V
Input leakage current	I _{IH} , I _{IL}	V _{IN} = 5.5 V or 0		25°C	3.6 V	−1	0.05	1	μA
				Full		−1	1		
Dynamic									
Turnon time	t _{ON}	V _{NC} = GND and V _{NO} = V ₊ , or V _{NC} = V ₊ and V _{NO} = GND,	R _L = 500 Ω, C _L = 50 pF, See Figure 9	Full	3 V to 3.6 V	2.0		10.6	ns
Turnoff time	t _{OFF}	V _{NC} = GND and V _{NO} = V ₊ , or V _{NC} = V ₊ and V _{NO} = GND,	R _L = 500 Ω, C _L = 50 pF, See Figure 9	Full	3 V to 3.6 V	1.0		8.3	ns
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	C _L = 35 pF, See Figure 10	25°C	3 V to 3.6 V	0.5			ns
Charge injection	Q _C	R _L = 50 Ω, C _L = 0.1 nF,	See Figure 14	25°C	3.3 V	3			pC
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 11	25°C	3 V	220			MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 12	25°C	3 V	−65			dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 13	25°C	3 V	−66			dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 15	25°C	3 V	0.015			%
Supply									
Positive supply current	I ₊	V _{IN} = V ₊ or GND,	Switch ON or OFF	25°C	3.6 V	1		μA	
				Full		10			
Change in supply current	ΔI ₊	V _{IN} = V ₊ − 0.6 V		Full	3.6 V	500		μA	

(1) $T_A = 25^\circ\text{C}$

(2) Hold all unused digital inputs of the device at V_+ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

Electrical Characteristics for 2.5-V Supply

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NO} , V _{NC}					0		V ₊	V
ON-state resistance	r _{on}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −8 mA,	Switch ON, See Figure 6	Full	2.3 V			50	Ω
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 1.6 V, I _{COM} = −8 mA,	Switch ON, See Figure 6	25°C	2.3 V	0.5			Ω
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −8 mA,	Switch ON, See Figure 6	25°C	2.3 V	27			Ω
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 0 to V ₊ , V _{COM} = 0 to V ₊ ,	Switch OFF, See Figure 7	25°C	2.7 V	−1	0.05	1	μA
				Full		−1	1		
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 0 to V ₊ , V _{COM} = Open,	Switch ON, See Figure 7	25°C	2.7 V	−0.1		0.1	μA
				Full		−1	1		
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 0 to V ₊ ,	Switch ON, See Figure 7	25°C	2.7 V	−0.1		0.1	μA
				Full		−1	1		
Digital Inputs (IN1, IN2) ⁽²⁾									
Input logic high	V _{IH}			Full		V ₊ × 0.7			V
Input logic low	V _{IL}			Full		V ₊ × 0.3			V
Input leakage current	I _{IH} , I _{IL}	V _{IN} = 5.5 V or 0		25°C	2.7 V	−1	0.05	1	μA
				Full		−1	1		
Dynamic									
Turnon time	t _{ON}	V _{NC} = GND and V _{NO} = V ₊ , or V _{NC} = V ₊ and V _{NO} = GND,	R _L = 500 Ω, C _L = 50 pF, See Figure 9	Full	2.3 V to 2.7 V	2.5		17	ns
Turnoff time	t _{OFF}	V _{NC} = GND and V _{NO} = V ₊ , or V _{NC} = V ₊ and V _{NO} = GND,	R _L = 500 Ω, C _L = 50 pF, See Figure 9	Full	2.3 V to 2.7 V	1.5		10.5	ns
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	C _L = 35 pF, See Figure 10	25°C	2.3 V to 2.7 V	0.5			ns
Bandwidth	BW	R _L = 50 Ω,	Switch ON, See Figure 11	25°C	2.3 V	220			MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 12	25°C	2.3 V	−65			dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 13	25°C	2.3 V	−66			dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 15	25°C	2.3 V	0.025			%
Supply									
Positive supply current	I ₊	V _{IN} = V ₊ or GND,	Switch ON or OFF	25°C	2.7 V	1		μA	
				Full		10			
Change in supply current	ΔI ₊	V _{IN} = V ₊ − 0.6 V		Full	2.7 V	500		μA	

(1) $T_A = 25^\circ\text{C}$

(2) Hold all unused digital inputs of the device at V_+ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

Electrical Characteristics for 1.8-V Supply

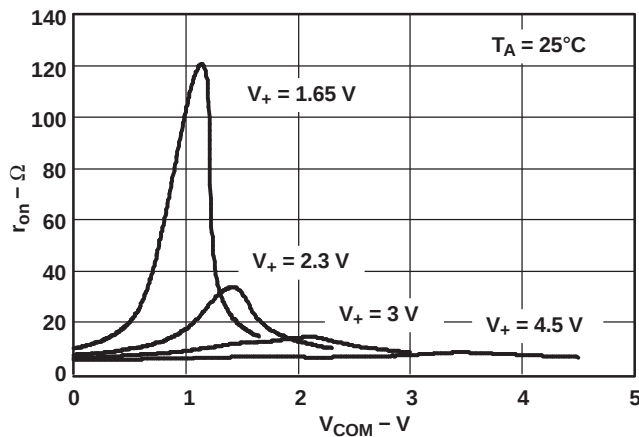
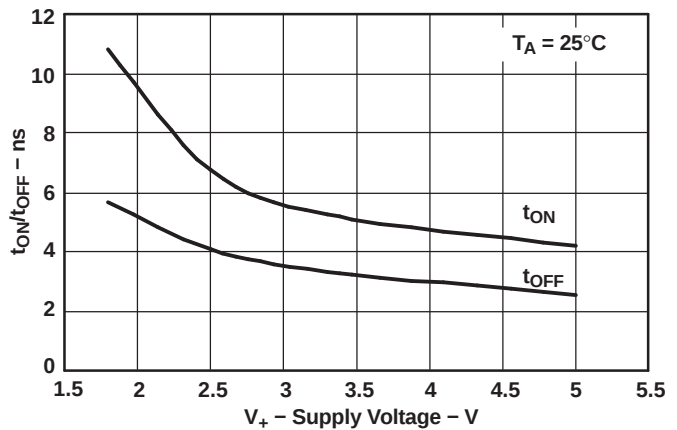
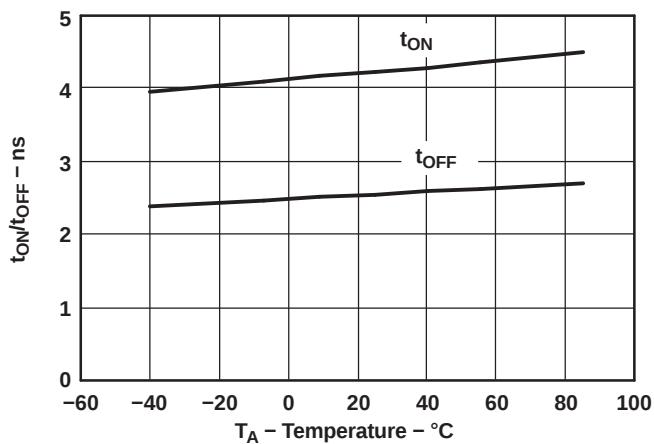
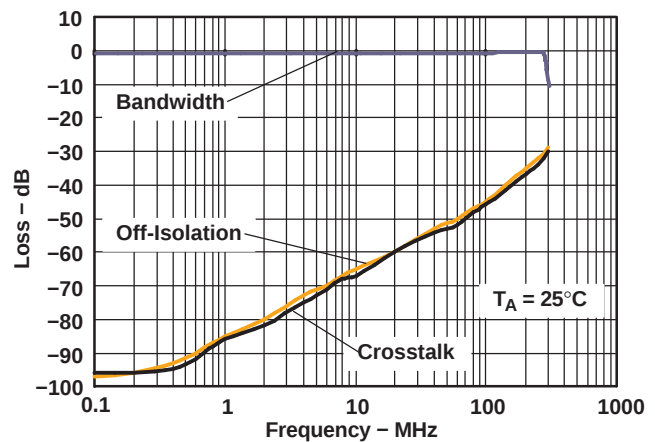
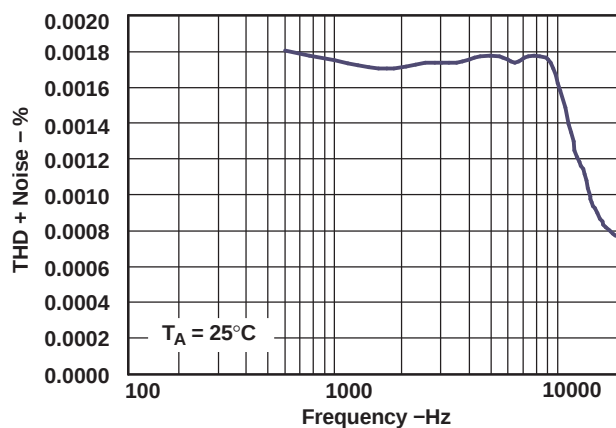
 $V_+ = 1.65 \text{ V to } 1.95 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NO} , V _{NC}					0		V ₊	V
ON-state resistance	r _{on}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −4 mA,	Switch ON, See Figure 6	Full	1.65 V			180	Ω
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 1.15 V, I _{COM} = −4 mA,	Switch ON, See Figure 6	25°C	1.65 V	1			Ω
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −4 mA,	Switch ON, See Figure 6	25°C	1.65 V	110			Ω
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 0 to V ₊ , V _{COM} = 0 to V ₊ ,	Switch OFF, See Figure 7	25°C	1.95 V	−1	0.05	1	μA
				Full		−1		1	
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 0 to V ₊ , V _{COM} = Open,	Switch ON, See Figure 7	25°C	1.95 V	−0.1		0.1	μA
				Full		−1		1	
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 0 to V ₊ ,	Switch ON, See Figure 7	25°C	1.95 V	−0.1		0.1	μA
				Full		−1		1	
Digital Inputs (IN1, IN2) ⁽²⁾									
Input logic high	V _{IH}			Full		V ₊ × 0.75			V
Input logic low	V _{IL}			Full		V ₊ × 0.25			V
Input leakage current	I _{IH} , I _{IL}	V _{IN} = 5.5 V or 0		25°C	1.95 V	−1	0.05	1	μA
				Full		−1		1	
Dynamic									
Turnon time	t _{ON}	V _{NC} = GND and V _{NO} = V ₊ , or V _{NC} = V ₊ and V _{NO} = GND,	R _L = 500 Ω, C _L = 50 pF, See Figure 9	Full	1.65 V to 1.95 V	5.5		27	ns
Turnoff time	t _{OFF}	V _{NC} = GND and V _{NO} = V ₊ , or V _{NC} = V ₊ and V _{NO} = GND,	R _L = 500 Ω, C _L = 50 pF, See Figure 9	Full	1.65 V to 1.95 V	2		16	ns
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	C _L = 35 pF, See Figure 10	25°C	1.65 V to 1.95 V	0.5			ns
Bandwidth	BW	R _L = 50 Ω,	Switch ON, See Figure 11	25°C	1.8 V	220			MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 12	25°C	1.8 V	−60			dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 13	25°C	1.8 V	−66			dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 15	25°C	1.8 V	0.015			%
Supply									
Positive supply current	I ₊	V _{IN} = V ₊ or GND,	Switch ON or OFF	25°C	1.95 V	1		μA	
				Full		10			
Change in supply current	ΔI ₊	V _{IN} = V ₊ − 0.6 V		Full	1.95 V	500		μA	

(1) $T_A = 25^\circ\text{C}$

(2) Hold all unused digital inputs of the device at V_+ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

TYPICAL CHARACTERISTICS

Figure 1. r_{on} versus V_{COM} Figure 2. t_{ON} and t_{OFF} versus V_+ Figure 3. t_{ON} and t_{OFF} versus Temperature
($V_+ = 5$ V)Figure 4. Frequency Response ($V_+ = 3$ V)Figure 5. Total Harmonic Distortion (THD)
versus Frequency ($V_+ = 3$ V)

PIN DESCRIPTION

NAME	PIN NO.	DESCRIPTION
COM1	10	Common
COM2	6	Common
GND	3	Digital ground
IN1	1	Digital control to connect COM to NO or NC
IN2	5	Digital control to connect COM to NO or NC
NC1	9	Normally closed
NC2	7	Normally closed
NO1	2	Normally open
NO2	4	Normally open
V ₊	8	Power supply

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V _{COM}	Voltage at COM
V _{NC}	Voltage at NC
V _{NO}	Voltage at NO
r _{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr _{on}	Difference of r _{on} between channels
r _{on(flat)}	Difference between the maximum and minimum value of r _{on} in a channel over the specified range of conditions
I _{NC(OFF)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
I _{NC(ON)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (NO to COM or NC to COM) in the ON state and the output (NC or NO) being open
V _{IH}	Minimum input voltage for logic high for the control input (IN)
V _{IL}	Minimum input voltage for logic low for the control input (IN)
V _{IN}	Voltage at IN
I _{IH} , I _{IL}	Leakage current measured at IN
t _{ON}	Turnon time for the switch. Measure this parameter under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM/NC/NO) signal when the switch is turning ON.
t _{OFF}	Turnoff time for the switch. Measure this parameter under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM/NC/NO) signal when the switch is turning OFF.
t _{BBM}	Break-before-make time. Measure this parameter under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q _C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This measure is in coulombs (C) and is the total charge induced due to switching of the control input. Charge injection, Q _C = C _L × ΔV _O , C _L is the load capacitance and ΔV _O is the change in analog output voltage.
C _{NC(OFF)}	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NC to COM) is OFF
C _{NC(ON)}	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NC to COM) is ON
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C _{IN}	Capacitance of IN
O _{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This measure is in dB at a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. OFF isolation, O _{ISO} = 20 LOG (V _{NC} /V _{COM}) dB, V _{COM} is the input and V _{NC} is the output.

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This measure is at a specific frequency and in dB. Crosstalk, $X_{\text{TALK}} = 20 \log (V_{\text{NC1}}/V_{\text{NO1}})$, V_{NO1} is the input and V_{NC1} is the output.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the dc gain. Gain is measured from the equation, $20 \log (V_{\text{NC}}/V_{\text{COM}})$ dB, where V_{NC} is the output and V_{COM} is the input.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

PARAMETER MEASUREMENT INFORMATION

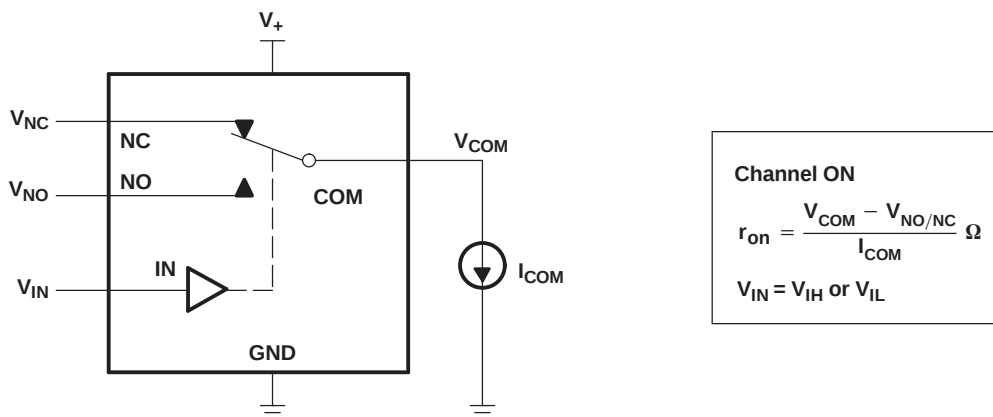


Figure 6. ON-State Resistance (R_{on})

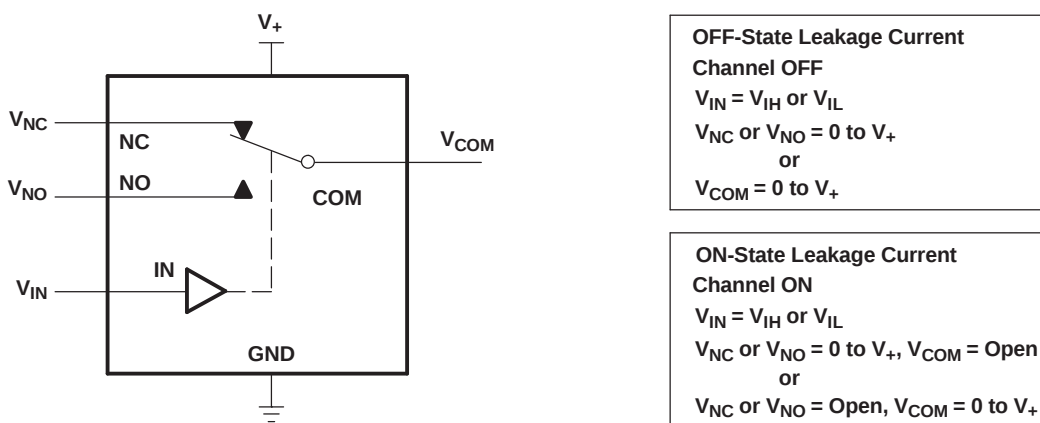


Figure 7. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

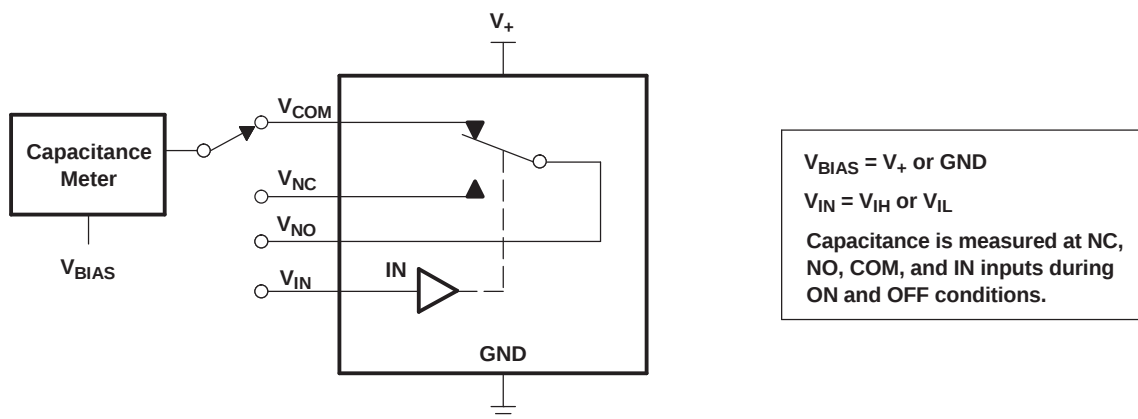
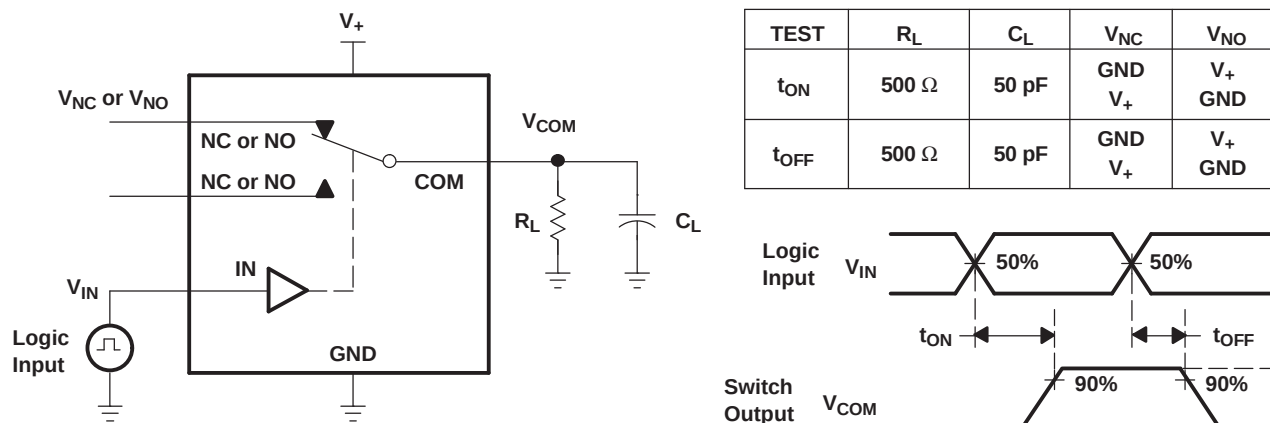
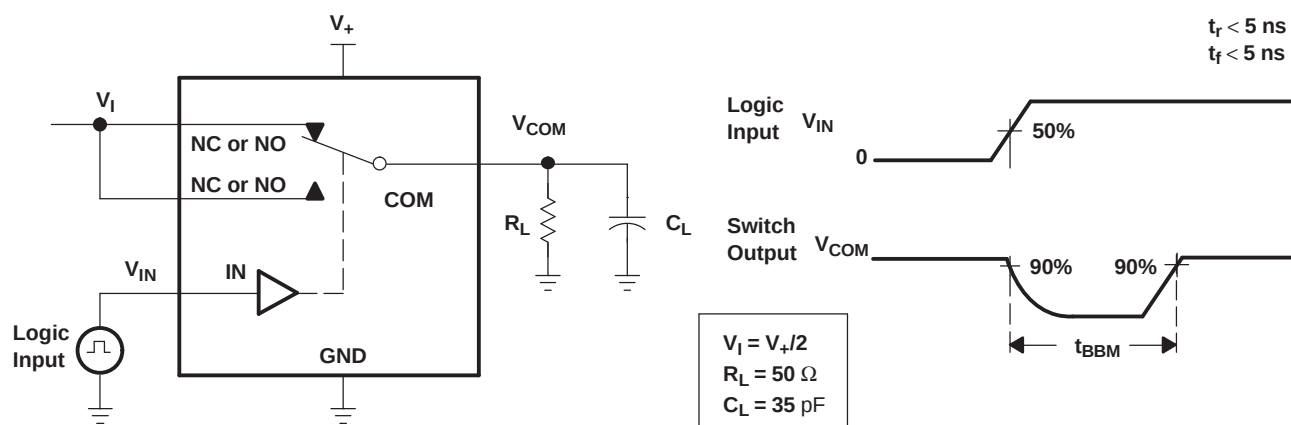
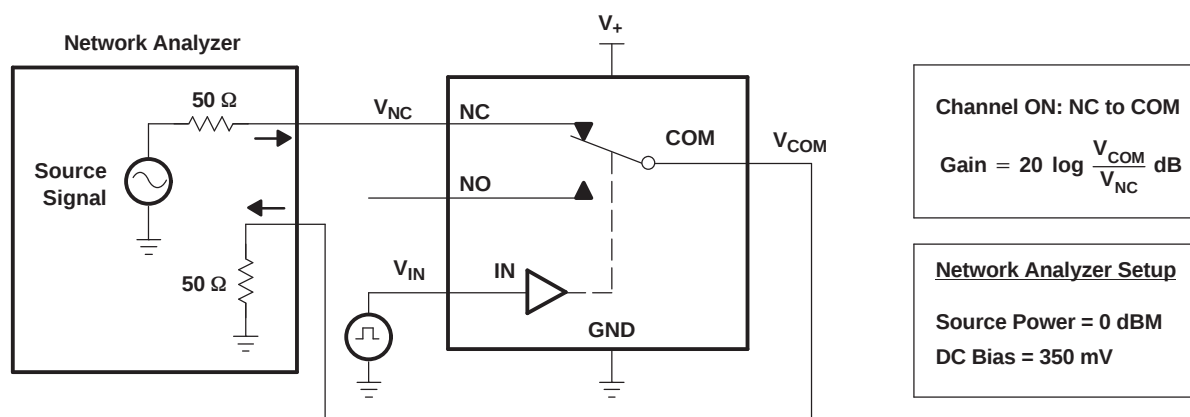


Figure 8. Capacitance (C_{IN} , $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)**Figure 9. Turn-On Time (t_{ON}) and Turn-Off Time (t_{OFF})****Figure 10. Break-Before-Make Time (t_{BBM})****Figure 11. Frequency Response (BW)**

PARAMETER MEASUREMENT INFORMATION (continued)

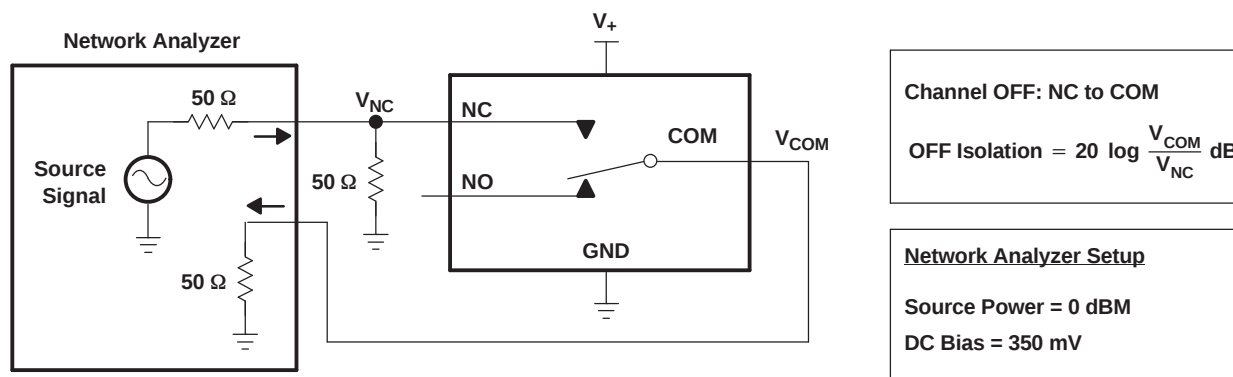


Figure 12. OFF Isolation (O_{ISO})

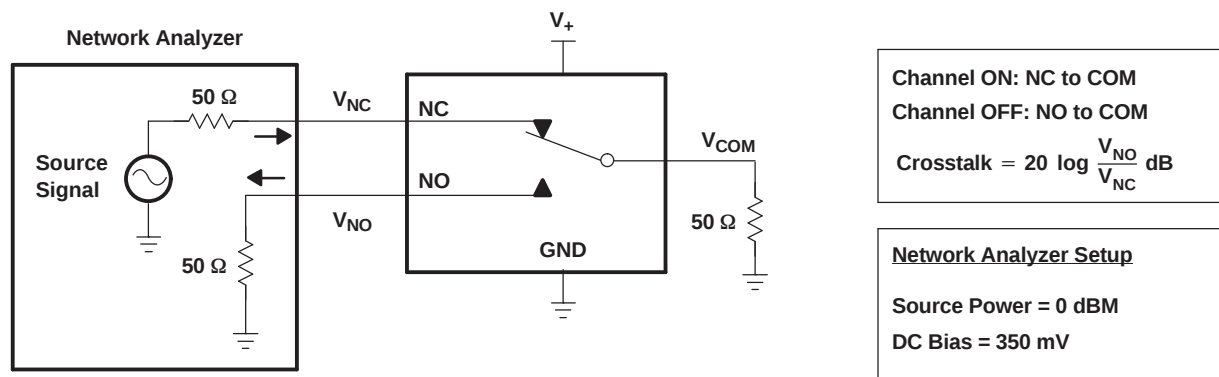


Figure 13. Crosstalk (X_{TALK})

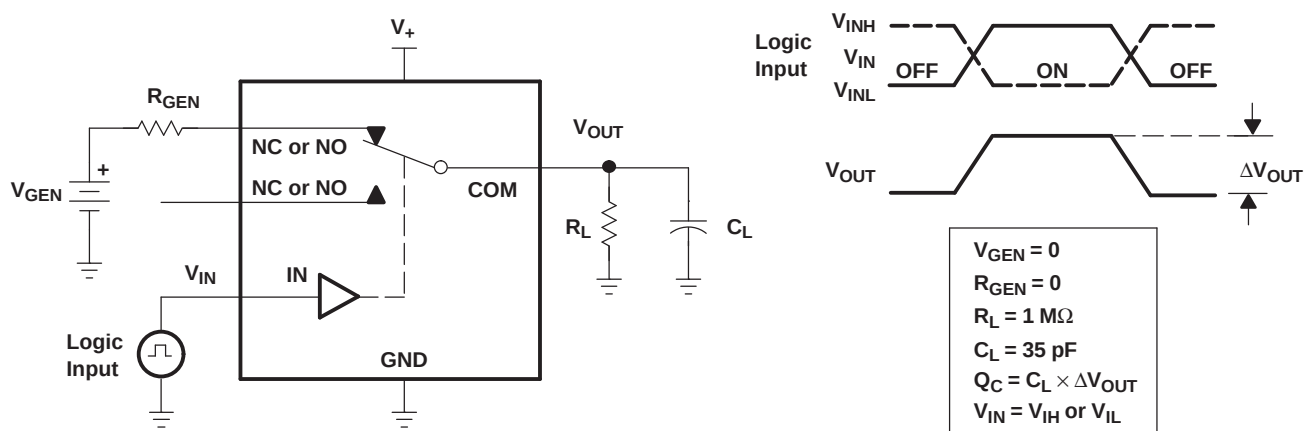
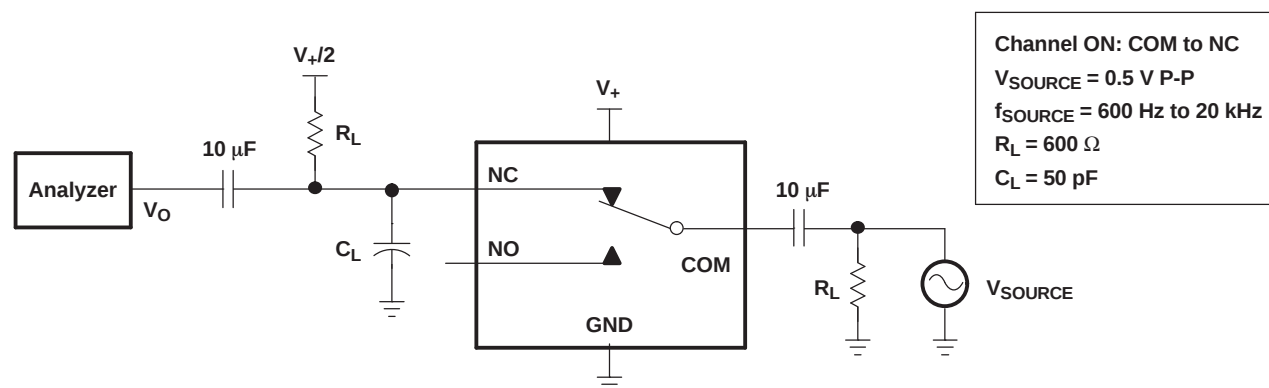


Figure 14. Charge Injection (Q_C)

PARAMETER MEASUREMENT INFORMATION (continued)**Figure 15. Total Harmonic Distortion (THD)**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A23157QDGSRQ1	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	SJC	Samples
TS5A23157TDGSRQ1	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	JBR	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TS5A23157-Q1 :

- Catalog: [TS5A23157](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

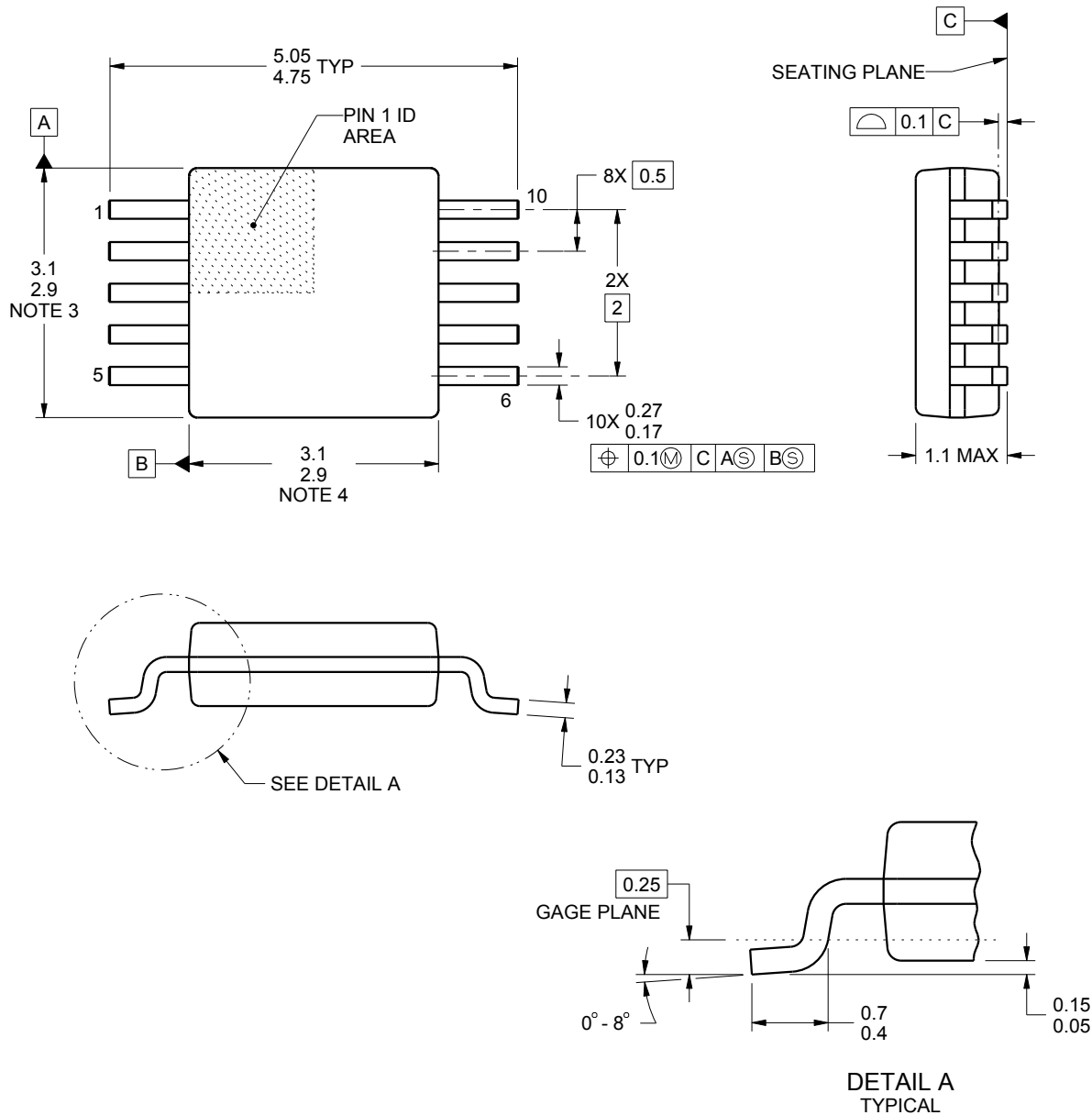
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23157QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A23157TDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23157QDGSRQ1	VSSOP	DGS	10	2500	346.0	346.0	29.0
TS5A23157TDGSRQ1	VSSOP	DGS	10	2500	346.0	346.0	29.0



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NOTES:

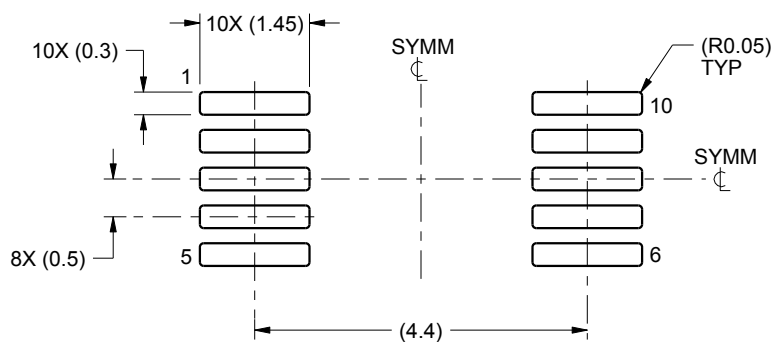
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

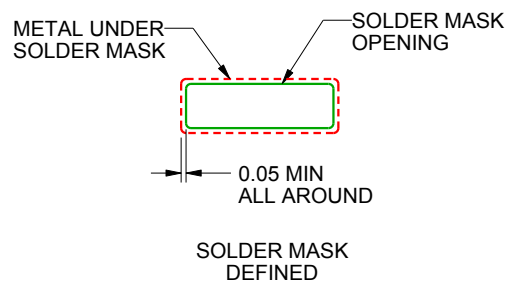
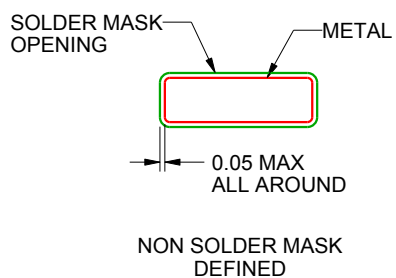
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

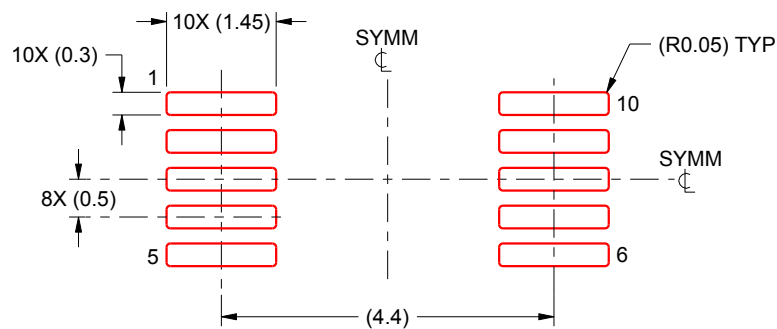
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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