

ADG711/ADG712/ADG713

FEATURES

1.8 V to 5.5 V Single Supply
Low On Resistance (2.5 Ω Typ)
Low On Resistance Flatness
-3 dB Bandwidth > 200 MHz
Rail-to-Rail Operation
16-Lead TSSOP and SOIC Packages
Fast Switching Times
 t_{ON} 16 ns
 t_{OFF} 10 ns
Typical Power Consumption (< 0.01 μ W)
TTL/CMOS Compatible

APPLICATIONS

USB 1.1 Signal Switching Circuits
Cell Phones
PDA's
Battery-Powered Systems
Communication Systems
Sample Hold Systems
Audio Signal Routing
Video Switching
Mechanical Reed Relay Replacement

GENERAL DESCRIPTION

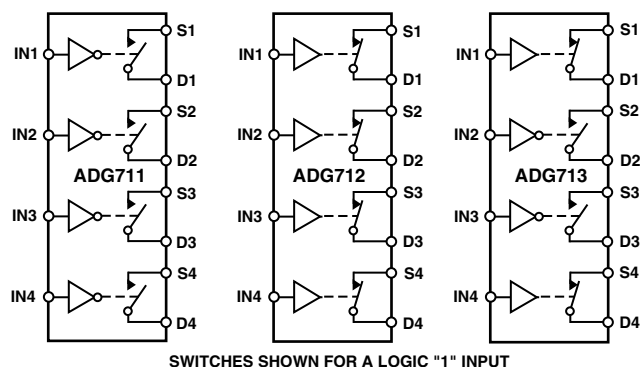
The ADG711, ADG712, and ADG713 are monolithic CMOS devices containing four independently selectable switches. These switches are designed on an advanced submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents, and high bandwidth.

They are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices. Fast switching times and high bandwidth make the parts suitable for switching USB 1.1 data signals and video signals.

The ADG711, ADG712, and ADG713 contain four independent single-pole/single-throw (SPST) switches. The ADG711 and ADG712 differ only in that the digital control logic is inverted. The ADG711 switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the ADG712. The ADG713 contains two switches whose digital control logic is similar to the ADG711, while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON. The ADG713 exhibits break-before-make switching action.

FUNCTIONAL BLOCK DIAGRAMS



The ADG711/ADG712/ADG713 are available in 16-lead TSSOP and 16-lead SOIC packages.

PRODUCT HIGHLIGHTS

- 1.8 V to 5.5 V Single-Supply Operation.
The ADG711, ADG712, and ADG713 offer high performance and are fully specified and guaranteed with 3 V and 5 V supply rails.
- Very Low R_{ON} (4.5 Ω max at 5 V, 8 Ω max at 3 V). At supply voltage of 1.8 V, R_{ON} is typically 35 Ω over the temperature range.
- Low On Resistance Flatness.
- 3 dB Bandwidth >200 MHz.
- Low Power Dissipation.
CMOS construction ensures low power dissipation.
- Fast t_{ON}/t_{OFF} .
- Break-Before-Make Switching.
This prevents channel shorting when the switches are configured as a multiplexer (ADG713 only).
- 16-Lead TSSOP and 16-Lead SOIC Packages.

REV. A

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ADG711/ADG712/ADG713—SPECIFICATIONS¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^{\circ}\text{C}$ unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	
On Resistance (R _{ON})	2.5		Ω typ	V _S = 0 V to V _{DD} , I _S = −10 mA;
	4	4.5	Ω max	Test Circuit 1
On Resistance Match Between Channels (ΔR _{ON})		0.05	Ω typ	V _S = 0 V to V _{DD} , I _S = −10 mA
		0.3	Ω max	
On Resistance Flatness (R _{FLAT(ON)})	0.5		Ω typ	V _S = 0 V to V _{DD} , I _S = −10 mA
		1.0	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01		nA typ	V _{DD} = +5.5 V;
	±0.1	±0.2	nA max	V _S = 4.5 V/1 V, V _D = 1 V/4.5 V;
Drain OFF Leakage I _D (OFF)	±0.01		nA typ	Test Circuit 2
	±0.1	±0.2	nA max	V _S = 4.5 V/1 V, V _D = 1 V/4.5 V;
Channel ON Leakage I _D , I _S (ON)	±0.01		nA typ	Test Circuit 2
	±0.1	±0.2	nA max	V _S = V _D = 1 V, or 4.5 V;
				Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.4	V min	
Input Low Voltage, V _{INL}		0.8	V max	
Input Current				
I _{INL} or I _{INH}	0.005		μA typ	V _{IN} = V _{INL} or V _{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS ²				
t _{ON}	11		ns typ	R _L = 300 Ω, C _L = 35 pF,
		16	ns max	V _S = 3 V; Test Circuit 4
t _{OFF}	6		ns typ	R _L = 300 Ω, C _L = 35 pF,
		10	ns max	V _S = 3 V; Test Circuit 4
Break-Before-Make Time Delay, t _D (ADG713 Only)	6		ns typ	R _L = 300 Ω, C _L = 35 pF,
		1	ns min	V _{S1} = V _{S2} = 3 V; Test Circuit 5
Charge Injection	3		pC typ	V _S = 2 V; R _S = 0 Ω, C _L = 1 nF; Test Circuit 6
Off Isolation	−58		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz
	−78		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	−90		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz; Test Circuit 8
Bandwidth −3 dB	200		MHz typ	R _L = 50 Ω, C _L = 5 pF; Test Circuit 9
C _S (OFF)	10		pF typ	
C _D (OFF)	10		pF typ	
C _D , C _S (ON)	22		pF typ	
POWER REQUIREMENTS				
I _{DD}	0.001		μA typ	V _{DD} = +5.5 V
		1.0	μA max	Digital Inputs = 0 V or 5 V

NOTES

¹Temperature range: B Version: -40°C to $+85^{\circ}\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS¹

($V_{DD} = +3\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^{\circ}\text{C}$ unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range	5	0 V to V _{DD}	V	V _S = 0 V to V _{DD} ; I _S = −10 mA; Test Circuit 1
On Resistance (R _{ON})		5.5	Ω typ	
On Resistance Match Between Channels (ΔR _{ON})	0.1	8	Ω max	V _S = 0 V to V _{DD} ; I _S = −10 mA
		0.3	Ω typ	
		0.3	Ω max	
On Resistance Flatness (R _{FLAT(ON)})		2.5	Ω typ	V _S = 0 V to V _{DD} ; I _S = −10 mA
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01	±0.2	nA typ	V _{DD} = +3.3 V; V _S = 3 V/1 V, V _D = 1 V/3 V; Test Circuit 2
	±0.1		nA max	
Drain OFF Leakage I _D (OFF)	±0.01	±0.2	nA typ	V _S = 3 V/1 V, V _D = 1 V/3 V; Test Circuit 2
	±0.1		nA max	
Channel ON Leakage I _D , I _S (ON)	±0.01	±0.2	nA typ	V _S = V _D = 1 V, or 3 V; Test Circuit 3
	±0.1		nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.0	V min	V _{IN} = V _{INL} or V _{INH}
Input Low Voltage, V _{INL}		0.4	V max	
Input Current	0.005		μA typ	
I _{INL} or I _{INH}		±0.1	μA max	
DYNAMIC CHARACTERISTICS ²				
t _{ON}	13	20	ns typ	R _L = 300 Ω, C _L = 35 pF, V _S = 2 V; Test Circuit 4
			ns max	
t _{OFF}	7	12	ns typ	R _L = 300 Ω, C _L = 35 pF, V _S = 2 V; Test Circuit 4
			ns max	
Break-Before-Make Time Delay, t _D (ADG713 Only)	7	1	ns typ	R _L = 300 Ω, C _L = 35 pF, V _{S1} = V _{S2} = 2 V; Test Circuit 5
			ns min	
Charge Injection	3		pC typ	V _S = 1.5 V; R _S = 0 Ω, C _L = 1 nF; Test Circuit 6
Off Isolation	−58		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 7
	−78		dB typ	
Channel-to-Channel Crosstalk	−90		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz; Test Circuit 8
Bandwidth −3 dB	200		MHz typ	R _L = 50 Ω, C _L = 5 pF; Test Circuit 9
C _S (OFF)	10		pF typ	
C _D (OFF)	10		pF typ	
C _D , C _S (ON)	22		pF typ	
POWER REQUIREMENTS				
I _{DD}	0.001	1.0	μA typ	V _{DD} = +3.3 V Digital Inputs = 0 V or 3 V
			μA max	

NOTES

¹Temperature range: B Version: -40°C to $+85^{\circ}\text{C}$.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG711/ADG712/ADG713

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V _{DD} to GND	−0.3 V to +6 V
Analog, Digital Inputs ²	−0.3 V to V _{DD} +0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package, Power Dissipation	430 mW
θ _{JA} Thermal Impedance	150°C/W
θ _{JC} Thermal Impedance	27°C/W

SOIC Package, Power Dissipation	520 mW
θ _{JA} Thermal Impedance	125°C/W
θ _{JC} Thermal Impedance	42°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	2 kV

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG711/ADG712/ADG713 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG711BR	−40°C to +85°C	Standard Small Outline (SOIC)	R-16
ADG711BR-REEL	−40°C to +85°C	Standard Small Outline (SOIC)	R-16
ADG711BR-REEL7	−40°C to +85°C	Standard Small Outline (SOIC)	R-16
ADG711BRU	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG711BRU-REEL	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG711BRU-REEL7	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG712BR	−40°C to +85°C	Standard Small Outline (SOIC)	R-16
ADG712BR-REEL	−40°C to +85°C	Standard Small Outline (SOIC)	R-16
ADG712BR-REEL7	−40°C to +85°C	Standard Small Outline (SOIC)	R-16
ADG712BRU	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG712BRU-REEL	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG712BRU-REEL7	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG712BRUZ*	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG712BRUZ-REEL*	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG712BRUZ-REEL7*	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG713BR	−40°C to +85°C	Standard Small Outline (SOIC)	R-16
ADG713BR-REEL	−40°C to +85°C	Standard Small Outline (SOIC)	R-16
ADG713BR-REEL7	−40°C to +85°C	Standard Small Outline (SOIC)	R-16
ADG713BRU	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG713BRU-REEL	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16
ADG713BRU-REEL7	−40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16

*Z = Pb-free part.

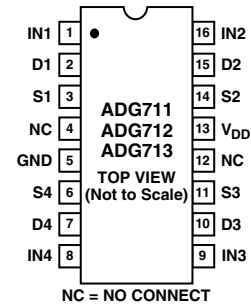
Table I. Truth Table (ADG711/ADG712)

ADG711 In	ADG712 In	Switch Condition
0	1	ON
1	0	OFF

Table II. Truth Table (ADG713)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

**PIN CONFIGURATION
(TSSOP/SOIC)**



TERMINOLOGY

V_{DD}	Most positive power supply potential.	t_{OFF}	Delay between applying the digital control input and the output switching off.
GND	Ground (0 V) reference.	t_D	“OFF” time or “ON” time measured between the 90% points of both switches, when switching from one address state to another. (ADG713 only).
S	Source terminal. May be an input or output.	Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
D	Drain terminal. May be an input or output.	Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
IN	Logic control input.	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
R_{ON}	Ohmic resistance between D and S.	Bandwidth	The frequency at which the output is attenuated by 3 dB.
ΔR_{ON}	On resistance match between any two channels, i.e., $R_{ONmax} - R_{ONmin}$.	On Response	The frequency response of the “ON” switch.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.	On Loss	The voltage drop across the “ON” switch, seen on the on response vs. frequency plot as how many dBs the signal is away from 0 dB at very low frequencies.
I_S (OFF)	Source leakage current with the switch “OFF.”		
I_D (OFF)	Drain leakage current with the switch “OFF.”		
I_D, I_S (ON)	Channel leakage current with the switch “ON.”		
V_D (V_S)	Analog voltage on terminals D, S.		
C_S (OFF)	“OFF” switch source capacitance.		
C_D (OFF)	“OFF” switch drain capacitance.		
C_D, C_S (ON)	“ON” switch capacitance.		
t_{ON}	Delay between applying the digital control input and the output switching on.		

ADG711/ADG712/ADG713—Typical Performance Characteristics

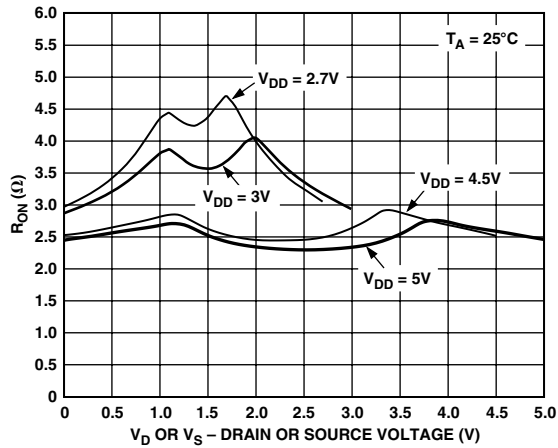


Figure 1. On Resistance as a Function of V_D (V_S)

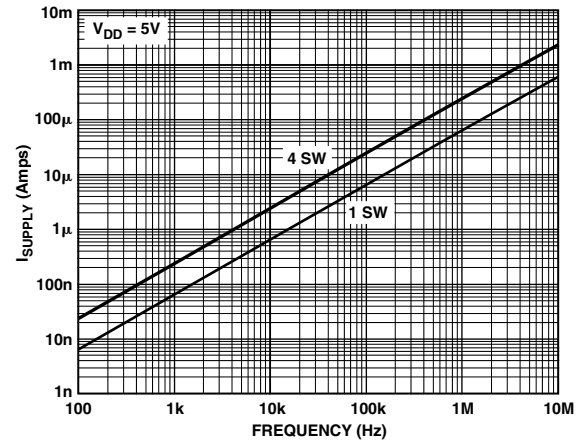


Figure 4. Supply Current vs. Input Switching Frequency

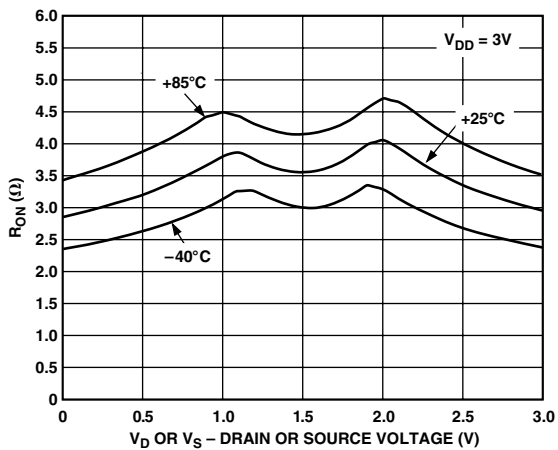


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures $V_{DD} = 3V$

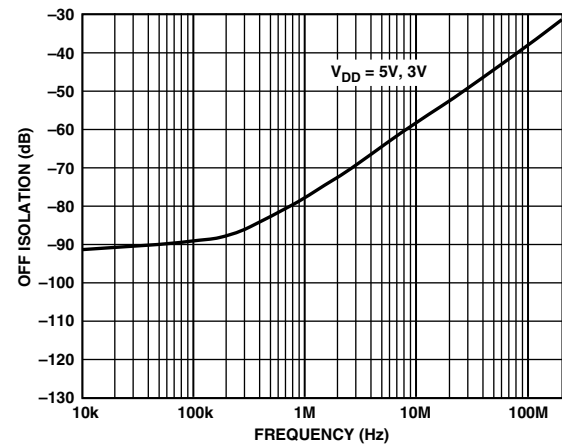


Figure 5. Off Isolation vs. Frequency

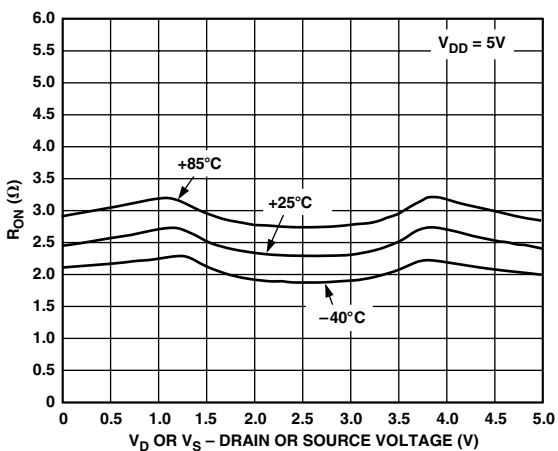


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures $V_{DD} = 5V$

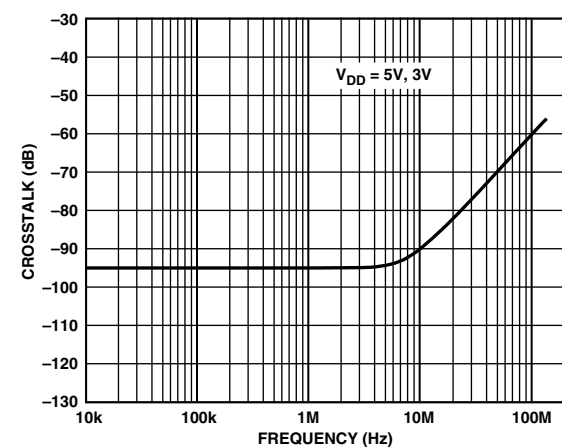


Figure 6. Crosstalk vs. Frequency

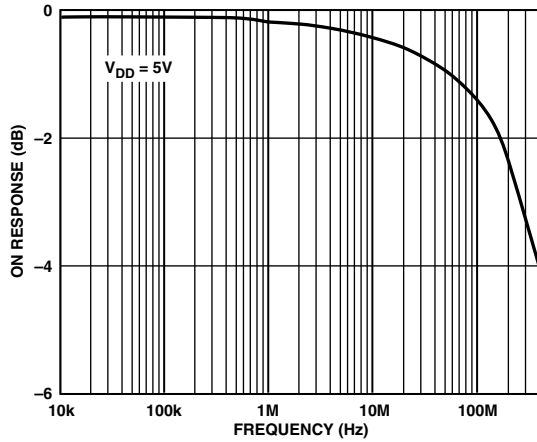


Figure 7. On Response vs. Frequency

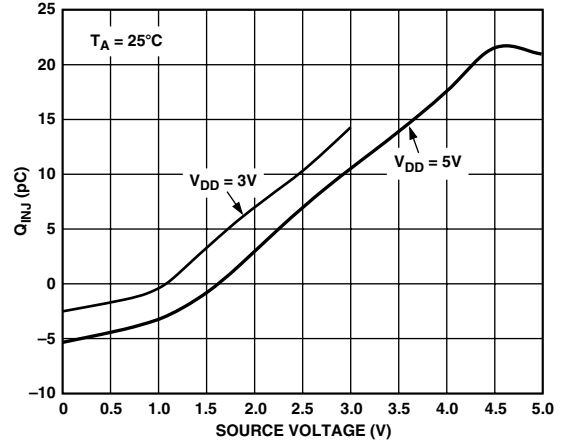


Figure 8. Charge Injection vs. Source Voltage

APPLICATIONS

Figure 9 illustrates a photodetector circuit with programmable gain. An AD820 is used as the output operational amplifier. With the resistor values shown in the circuit, and using different combinations of the switches, gain in the range of 2 to 16 can be achieved.

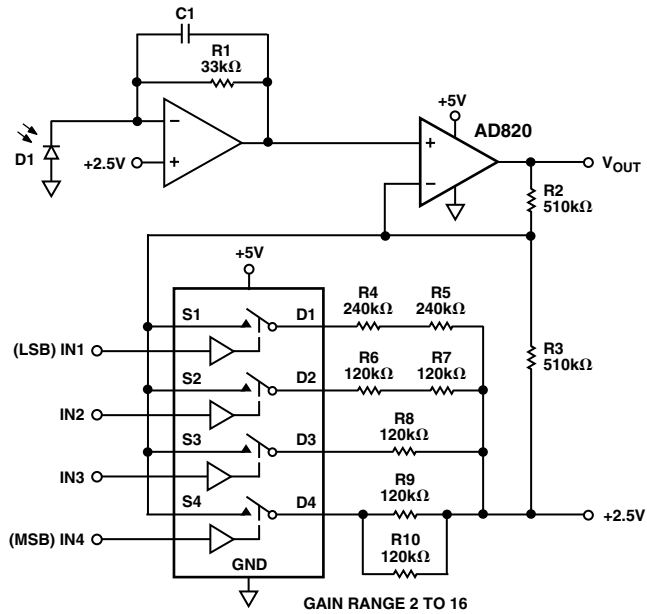
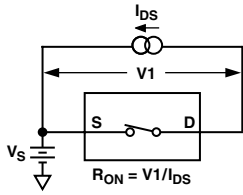


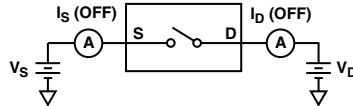
Figure 9. Photodetector Circuit with Programmable Gain

ADG711/ADG712/ADG713

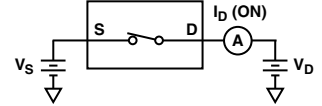
Test Circuits



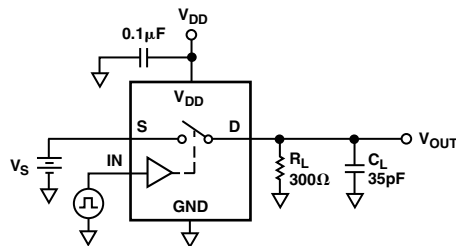
Test Circuit 1. On Resistance



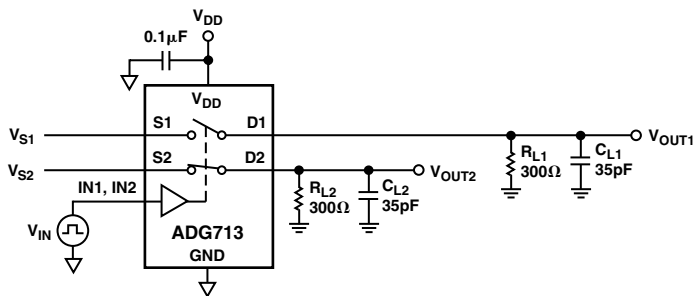
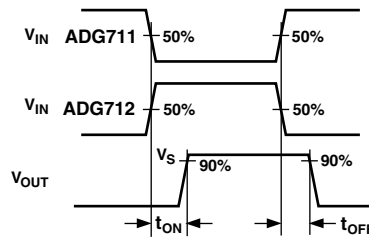
Test Circuit 2. Off Leakage



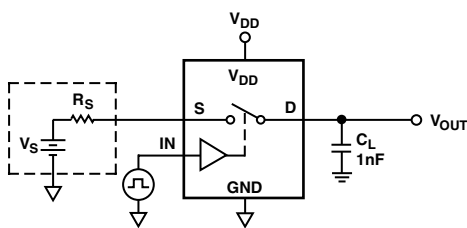
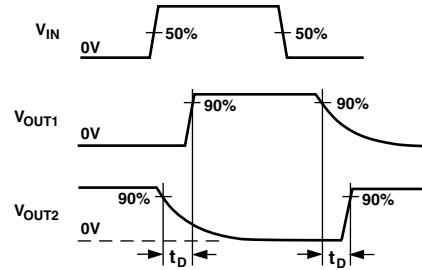
Test Circuit 3. On Leakage



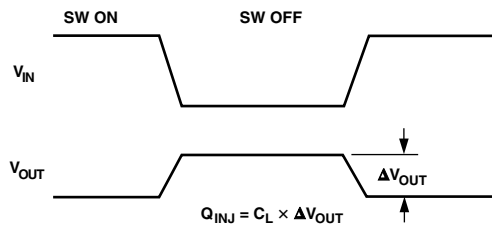
Test Circuit 4. Switching Times

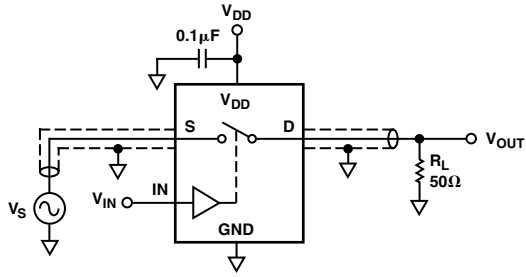


Test Circuit 5. Break-Before-Make Time Delay, t_D

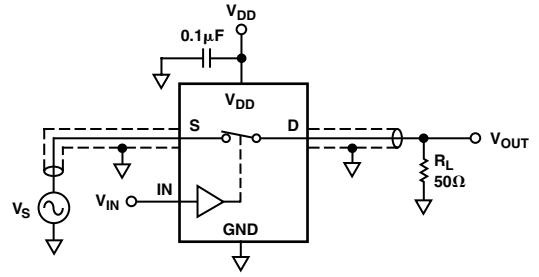


Test Circuit 6. Charge Injection

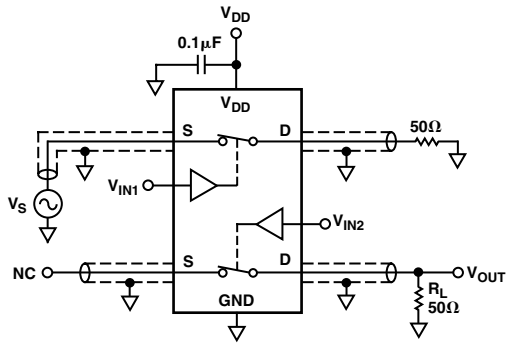




Test Circuit 7. Off Isolation



Test Circuit 9. Bandwidth



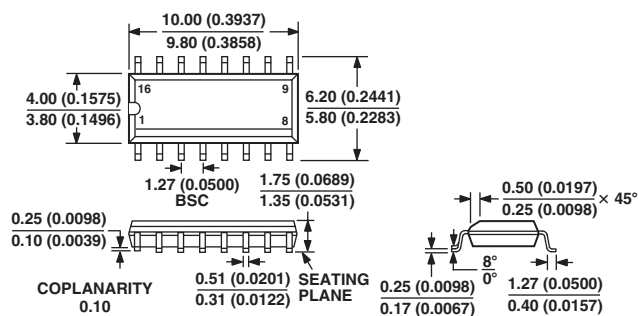
$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \times \text{LOG} |V_S/V_{OUT}|$$

Test Circuit 8. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS

16-Lead Standard Small Outline Package [SOIC] Narrow Body (R-16)

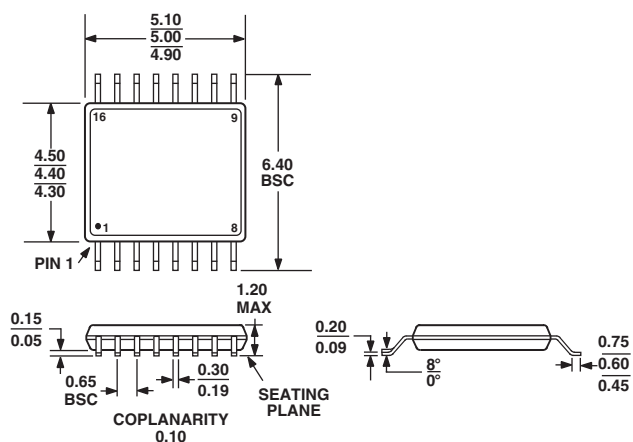
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB

Revision History

Location	Page
3/04—Data Sheet changed from REV. 0 to REV. A.	
Added APPLICATIONS	1
Changes to ORDERING GUIDE	4
Updated OUTLINE DIMENSIONS	10

