

AMD Athlon™ X2

Dual-Core Processor

Product Data Sheet



- **Compatible with Existing 32-Bit Code Base**
 - Including support for SSE, SSE2, SSE3, MMX™, 3DNow!™ technology and legacy x86 instructions
 - Runs existing operating systems and drivers
 - Local APIC on-chip
 - **AMD64 Technology**
 - AMD64 technology instruction set extensions
 - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
 - Eight additional 64-bit integer registers (16 total)
 - Eight additional 128-bit SSE/SSE2/SSE3 registers (16 total)
 - **Dual-Core Architecture**
 - Discrete L1 and L2 cache structures for each core
 - **HyperTransport™ Technology to I/O Devices**
 - One 16-bit link supporting speeds up to 1 GHz (2000 MT/s) or 4 Gigabytes/s in each direction
 - **64-Kbyte 2-Way Associative ECC-Protected L1 Data Caches**
 - Two 64-bit operations per cycle, 3-cycle latency
 - **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Caches**
 - With advanced branch prediction
 - **16-Way Associative ECC-Protected L2 Caches**
 - Exclusive cache architecture—storage in addition to L1 caches
 - Up to 1 Mbyte per L2 cache
 - **Machine Check Architecture**
 - Includes hardware scrubbing of major ECC-protected arrays
 - **Power Management**
 - Multiple low-power states including C1E
 - System Management Mode (SMM)
 - ACPI-compliant, including support for processor performance states
-
- ### Socket AM2 Specific Features
- **Refer to the *Socket AM2 Processor Functional Data Sheet*, order# 31117, for functional and mechanical details of socket AM2 processors.**
 - **Refer to the *AMD NPT 0Fh Family Processor Electrical Data Sheet*, order# 31119, for electrical details of socket AM2 processors.**
 - **Electrical Interfaces**
 - HyperTransport™ technology: LVDS-like differential, unidirectional
 - DDR2 SDRAM: SSTL_1.8 per JEDEC specification
 - Clock, reset, and test signals also use DDR2 SDRAM-like electrical specifications
 - **Packaging**
 - Lidded micro PGA
 - 31 x 31 grid array
 - 1.27-mm pin pitch
 - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
 - **Integrated Memory Controller**
 - Low-latency, high-bandwidth
 - 144-bit DDR2 SDRAM controller operating at up to 400 MHz
 - Supports up to four unbuffered DIMMs
 - ECC checking with double-bit detect and single-bit correct

Publication #	43042	Revision:	3.00
Issue Date:	May 2007		

Revision History

Date	Revision	Description
May 2007	3.00	Initial public release.

© 2007 Advanced Micro Devices, Inc. All rights reserved.

The contents of this document are provided in connection with Advanced Micro Devices, Inc. (“AMD”) products. AMD makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. The information contained herein may be of a preliminary or advance nature and is subject to change without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in AMD’s Standard Terms and Conditions of Sale, AMD assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

AMD’s products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of AMD’s product could create a situation where personal injury, death, or severe property or environmental damage may occur. AMD reserves the right to discontinue or make changes to its products at any time without notice.

Trademarks

AMD, the AMD Arrow logo, AMD Athlon and combinations thereof, and 3DNow! are trademarks of Advanced Micro Devices, Inc.

HyperTransport is a licensed trademark of the HyperTransport Technology Consortium.

MMX is a trademark of Intel Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.