

MOS INTEGRATED CIRCUIT

μ PD16732A, 16732B

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μ PD16732A, 16732B are a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ -corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as $V_{SS2} + 0.1$ V to $V_{DD2} - 0.1$ V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 65 MHz when driving at 3.0 V, 45 MHz when driving at 2.3 V, this driver is applicable to XGA-standard TFT-LCD panels and SXGA TFT-LCD panels by input display signal 2 systems (Clock divide).

FEATURES

- CMOS level input (2.3 V to 3.6 V)
- 384 Outputs
- Input of 6 bits (gradation data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter (R-DAC)
- High-speed data transfer: $f_{MAX.} = 65$ MHz (internal data transfer speed when operating at $V_{DD1} = 3.0$ V)
- Output dynamic range $V_{SS2} + 0.1$ V to $V_{DD2} - 0.1$ V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output Voltage polarity inversion function (POL)
- Display data inversion function (POL2)
- Low power control function (LPC)
- Logic power supply voltage (V_{DD1}) : 2.3 V to 3.6 V
- Driver power supply voltage (V_{DD2}) : 8.5 ± 0.5 V
- Different point between μ PD16732A, 16732B : The ladder resistors value(Refer to **5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE**)

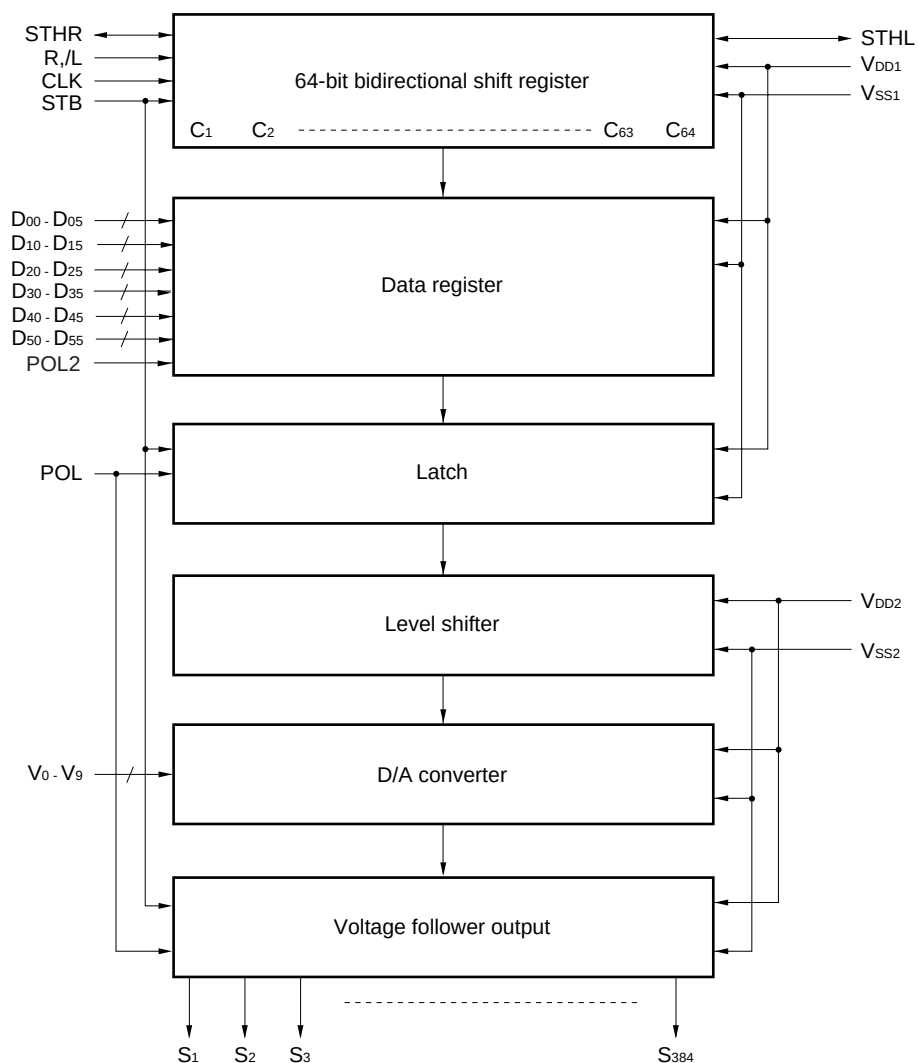
ORDERING INFORMATION

Part Number	Package
μ PD16732AN-xxx	TCP (TAB package)
μ PD16732BN-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, please contact an NEC salesperson.

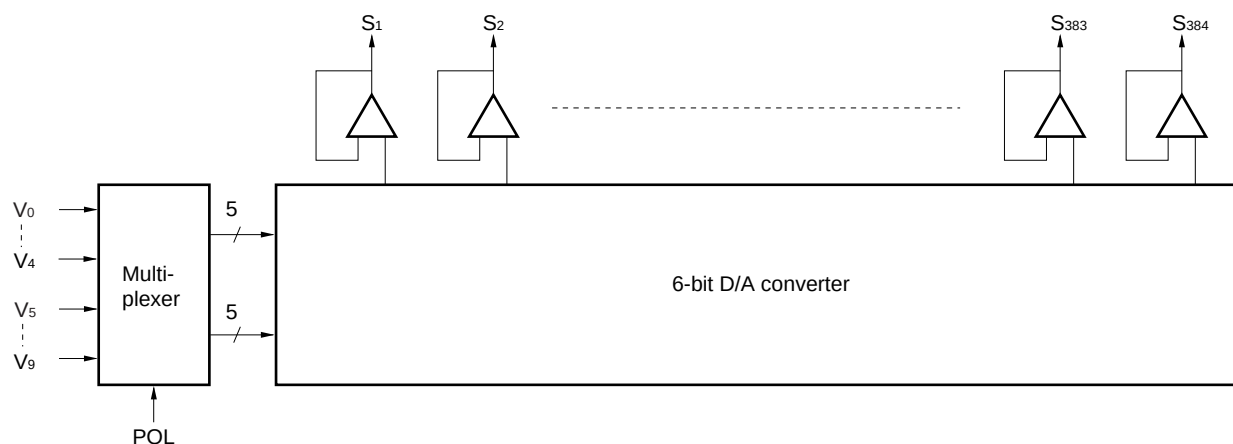
The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM

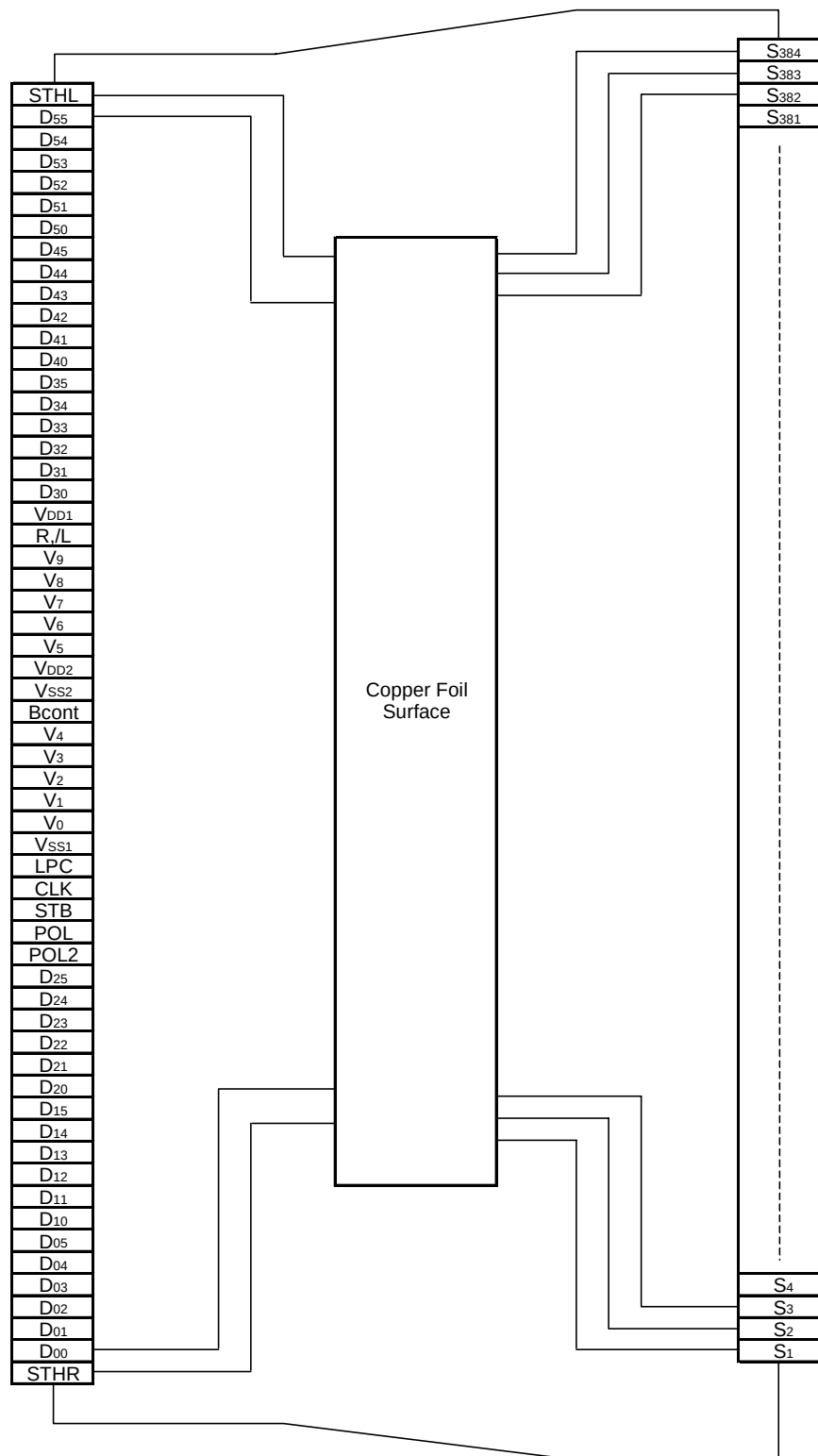


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μ PD16732AN-xxx, μ PD16732BN-xxx : TCP (TAB package))



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	Description
S ₁ to S ₃₈₄	Driver output	The D/A converted 64-gray-scale analog voltage is output.
D ₀₀ to D ₀₅	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D _{X0} : LSB, D _{X5} : MSB
D ₁₀ to D ₁₅		
D ₂₀ to D ₂₅		
D ₃₀ to D ₃₅		
D ₄₀ to D ₄₅		
D ₅₀ to D ₅₅		
R,/L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H : STHR input, S ₁ → S ₃₈₄ , STHL output R,/L = L : STHL input, S ₃₈₄ → S ₁ , STHR output
STHR	Right shift start pulse input/output	R,/L = H : Becomes the start pulse input pin. R,/L = L : Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R,/L = H : Becomes the start pulse output pin. R,/L = L : Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver.
STB	Latch input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L : The S _{2n-1} output uses V ₀ to V ₄ as the reference supply. The S _{2n} output uses V ₅ to V ₉ as the reference supply. POL = H : The S _{2n-1} output uses V ₅ to V ₉ as the reference supply. The S _{2n} output uses V ₀ to V ₄ as the reference supply. S _{2n-1} indicates the odd output: and S _{2n} indicates the even output. Input of the POL signal is allowed the setup time (t _{POL-STB}) with respect to STB's rising edge.
POL2	Data inversion	POL2 = H : Display data is inverted. POL2 = L : Display data is not inverted
LPC	Low power control input	The current consumption is lowered by controlling the constant current source of the output amplifier. In low power mode (LPC = "L"), the V _{DD2} of static current consumption can be reduced to two thirds of the normal current consumption. This pin is pulled up to the V _{DD1} power supply inside the IC. LPC = H or Open : Normal power mode LPC = L : Low power mode

★

(2/2)

Pin Symbol	Pin Name	Description
Bcont	Bias control	This pin can be used to finely control the bias current inside the output amplifier. In cases when fine-control is necessary, connect this pin to the stabilized ground potential (V_{SS2}) via an external resistor of 10 to 100kΩ (per IC). When this fine-control function is not required, leave this pin open. Refer to 9. CURRENT CONSUMPTION REDUCTION FUNCTION
V_0 to V_9	γ -corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\text{ V} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1\text{ V}$
V_{DD1}	Logic power supply	2.3 V to 3.6 V
V_{DD2}	Driver power supply	8.5 V $\pm$ 0.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

Cautions 1. The power start sequence must be V_{DD1} , logic input, and V_{DD2} & V_0 to V_9 in that order.

Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.)

2. To stabilize the supply voltage, please be sure to insert a 0.1 μ F bypass capacitor between V_{DD1} - V_{SS1} and V_{DD2} - V_{SS2} . Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μ F is also advised between the γ -corrected power supply terminals (V_0 , V_1 , V_2 , ..., V_9) and V_{SS2} .

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel γ -compensated voltages to $V_{0'}$ to $V_{63'}$ and $V_{0''}$ to $V_{63''}$ is almost equivalent. For the 2 sets of five γ -compensated power supplies, V_0 to V_4 and V_5 to V_9 , respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine-gray scale voltage precision is not necessary, there is no need to connect a voltage follower circuit to the γ -compensated power supplies V_1 to V_3 and V_6 to V_8 .

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2} , common electrode potential V_{COM} , and γ -corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of $V_{DD2} - 0.1\text{ V} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1\text{ V}$.

Figures 5–2 and 5–3 show the relationship between the input data and the output data. This driver IC is designed for only single-sided mounting. Therefore, please do not use it for γ -corrected power supply level inversion in double-sided mounting.

Figure 5–1. Relationship between Input Data and γ -corrected Power Supply

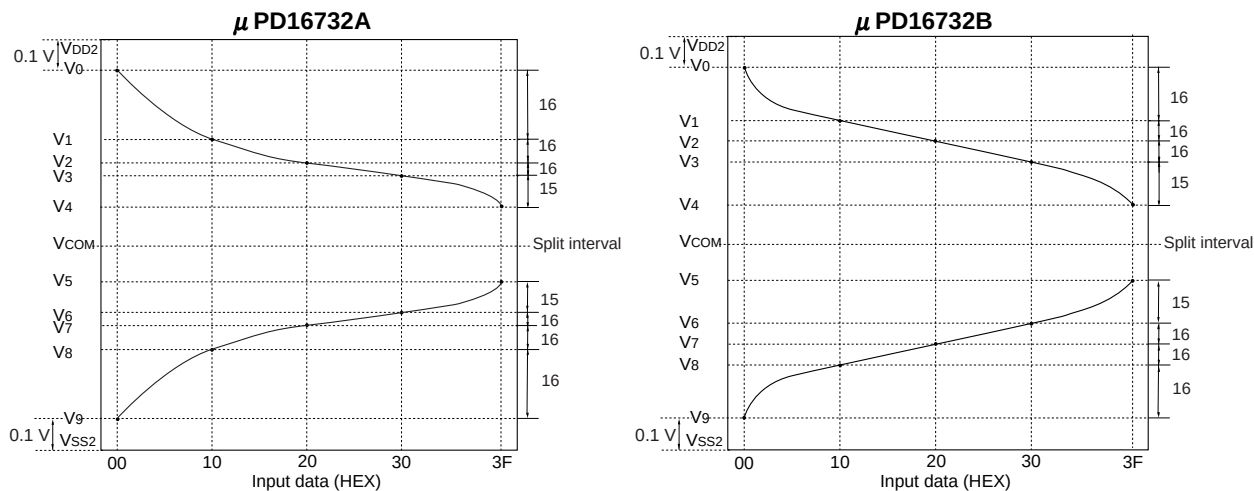


Figure 5-2. Relationship between Input Data and Output Voltage (1/2)

$V_{DD2} - 0.1\text{ V} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5$, POL2 = L

		Data	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output Voltage			rn	(Ω)	
										732A	732B		732A 732B	
V ₀	r0	00H	0	0	0	0	0	0	V _{0'}	V ₀		r0	800 1766	
	r1	01H	0	0	0	0	0	1	V _{1'}	V ₁ +(V ₀ -V ₁)×	7250/8050	4585/6351	r1	750 736
		02H	0	0	0	0	1	0	V _{2'}	V ₁ +(V ₀ -V ₁)×	6500/8050	3849/6351	r2	700 566
		03H	0	0	0	0	1	1	V _{3'}	V ₁ +(V ₀ -V ₁)×	5800/8050	3283/6351	r3	650 509
		04H	0	0	0	1	0	0	V _{4'}	V ₁ +(V ₀ -V ₁)×	5150/8050	2774/6351	r4	600 396
		05H	0	0	0	1	0	1	V _{5'}	V ₁ +(V ₀ -V ₁)×	4550/8050	2378/6351	r5	550 340
		06H	0	0	0	1	1	0	V _{6'}	V ₁ +(V ₀ -V ₁)×	4000/8050	2038/6351	r6	550 283
		07H	0	0	0	1	1	1	V _{7'}	V ₁ +(V ₀ -V ₁)×	3450/8050	1755/6351	r7	500 283
		08H	0	0	1	0	0	0	V _{8'}	V ₁ +(V ₀ -V ₁)×	2950/8050	1472/6351	r8	500 226
		09H	0	0	1	0	0	1	V _{9'}	V ₁ +(V ₀ -V ₁)×	2450/8050	1246/6351	r9	400 226
V ₁	0AH	0	0	1	0	1	0	V _{10'}	V ₁ +(V ₀ -V ₁)×	2050/8050	1020/6351	r10	400 170	
	0BH	0	0	1	0	1	1	V _{11'}	V ₁ +(V ₀ -V ₁)×	1650/8050	850/6351	r11	350 170	
	0CH	0	0	1	1	0	0	V _{12'}	V ₁ +(V ₀ -V ₁)×	1300/8050	680/6351	r12	350 170	
	0DH	0	0	1	1	0	1	V _{13'}	V ₁ +(V ₀ -V ₁)×	950/8050	510/6351	r13	350 170	
	0EH	0	0	1	1	1	0	V _{14'}	V ₁ +(V ₀ -V ₁)×	600/8050	340/6351	r14	300 170	
	0FH	0	0	1	1	1	1	V _{15'}	V ₁ +(V ₀ -V ₁)×	300/8050	170/6351	r15	300 170	
	10H	0	1	0	0	0	0	V _{16'}	V ₁		r16	300 152		
	11H	0	1	0	0	0	1	V _{17'}	V ₂ +(V ₁ -V ₂)×	2450/2750	2280/2432	r17	250 152	
	12H	0	1	0	0	1	0	V _{18'}	V ₂ +(V ₁ -V ₂)×	2200/2750	2128/2432	r18	250 152	
	13H	0	1	0	0	1	1	V _{19'}	V ₂ +(V ₁ -V ₂)×	1950/2750	1976/2432	r19	250 152	
V ₂	14H	0	1	0	1	0	0	V _{20'}	V ₂ +(V ₁ -V ₂)×	1700/2750	1824/2432	r20	200 152	
	15H	0	1	0	1	0	1	V _{21'}	V ₂ +(V ₁ -V ₂)×	1500/2750	1672/2432	r21	200 152	
	16H	0	1	0	1	1	0	V _{22'}	V ₂ +(V ₁ -V ₂)×	1300/2750	1520/2432	r22	200 152	
	17H	0	1	0	1	1	1	V _{23'}	V ₂ +(V ₁ -V ₂)×	1100/2750	1368/2432	r23	150 152	
	18H	0	1	1	0	0	0	V _{24'}	V ₂ +(V ₁ -V ₂)×	950/2750	1216/2432	r24	150 152	
	19H	0	1	1	0	0	1	V _{25'}	V ₂ +(V ₁ -V ₂)×	800/2750	1064/2432	r25	150 152	
	1AH	0	1	1	0	1	0	V _{26'}	V ₂ +(V ₁ -V ₂)×	650/2750	912/2432	r26	150 152	
	1BH	0	1	1	0	1	1	V _{27'}	V ₂ +(V ₁ -V ₂)×	500/2750	760/2432	r27	100 152	
	1CH	0	1	1	1	0	0	V _{28'}	V ₂ +(V ₁ -V ₂)×	400/2750	608/2432	r28	100 152	
	1DH	0	1	1	1	0	1	V _{29'}	V ₂ +(V ₁ -V ₂)×	300/2750	456/2432	r29	100 152	
V ₃	1EH	0	1	1	1	1	0	V _{30'}	V ₂ +(V ₁ -V ₂)×	200/2750	304/2432	r30	100 152	
	1FH	0	1	1	1	1	1	V _{31'}	V ₂ +(V ₁ -V ₂)×	100/2750	152/2432	r31	100 152	
	20H	1	0	0	0	0	0	V _{32'}	V ₂		r32	100 156		
	21H	1	0	0	0	0	1	V _{33'}	V ₃ +(V ₂ -V ₃)×	1500/1600	2340/2496	r33	100 156	
	22H	1	0	0	0	1	0	V _{34'}	V ₃ +(V ₂ -V ₃)×	1400/1600	2184/2496	r34	100 156	
	23H	1	0	0	0	1	1	V _{35'}	V ₃ +(V ₂ -V ₃)×	1300/1600	2028/2496	r35	100 156	
	24H	1	0	0	1	0	0	V _{36'}	V ₃ +(V ₂ -V ₃)×	1200/1600	1872/2496	r36	100 156	
	25H	1	0	0	1	0	1	V _{37'}	V ₃ +(V ₂ -V ₃)×	1100/1600	1716/2496	r37	100 156	
	26H	1	0	0	1	1	0	V _{38'}	V ₃ +(V ₂ -V ₃)×	1000/1600	1560/2496	r38	100 156	
	27H	1	0	0	1	1	1	V _{39'}	V ₃ +(V ₂ -V ₃)×	900/1600	1404/2496	r39	100 156	
V ₄	28H	1	0	1	0	0	0	V _{40'}	V ₃ +(V ₂ -V ₃)×	800/1600	1248/2496	r40	100 156	
	29H	1	0	1	0	0	1	V _{41'}	V ₃ +(V ₂ -V ₃)×	700/1600	1092/2496	r41	100 156	
	2AH	1	0	1	0	1	0	V _{42'}	V ₃ +(V ₂ -V ₃)×	600/1600	936/2496	r42	100 156	
	2BH	1	0	1	0	1	1	V _{43'}	V ₃ +(V ₂ -V ₃)×	500/1600	780/2496	r43	100 156	
	2CH	1	0	1	1	0	0	V _{44'}	V ₃ +(V ₂ -V ₃)×	400/1600	624/2496	r44	100 156	
	2DH	1	0	1	1	0	1	V _{45'}	V ₃ +(V ₂ -V ₃)×	300/1600	468/2496	r45	100 156	
	2EH	1	0	1	1	1	0	V _{46'}	V ₃ +(V ₂ -V ₃)×	200/1600	312/2496	r46	100 156	
	2FH	1	0	1	1	1	1	V _{47'}	V ₃ +(V ₂ -V ₃)×	100/1600	156/2496	r47	100 156	
	30H	1	1	0	0	0	0	V _{48'}	V ₃		r48	100 175		
	31H	1	1	0	0	0	1	V _{49'}	V ₄ +(V ₃ -V ₄)×	3350/3450	4397/4572	r49	100 175	
V ₅	32H	1	1	0	0	1	0	V _{50'}	V ₄ +(V ₃ -V ₄)×	3250/3450	4222/4572	r50	100 175	
	33H	1	1	0	0	1	1	V _{51'}	V ₄ +(V ₃ -V ₄)×	3150/3450	4047/4572	r51	100 175	
	34H	1	1	0	1	0	0	V _{52'}	V ₄ +(V ₃ -V ₄)×	3050/3450	3872/4572	r52	100 175	
	35H	1	1	0	1	0	1	V _{53'}	V ₄ +(V ₃ -V ₄)×	2950/3450	3697/4572	r53	150 232	
	36H	1	1	0	1	1	0	V _{54'}	V ₄ +(V ₃ -V ₄)×	2800/3450	3465/4572	r54	150 232	
	37H	1	1	0	1	1	1	V _{55'}	V ₄ +(V ₃ -V ₄)×	2650/3450	3233/4572	r55	150 232	
	38H	1	1	1	0	0	0	V _{56'}	V ₄ +(V ₃ -V ₄)×	2500/3450	3001/4572	r56	200 232	
	39H	1	1	1	0	0	1	V _{57'}	V ₄ +(V ₃ -V ₄)×	2300/3450	2769/4572	r57	200 289	
	3AH	1	1	1	0	1	0	V _{58'}	V ₄ +(V ₃ -V ₄)×	2100/3450	2480/4572	r58	250 345	
	3BH	1	1	1	0	1	1	V _{59'}	V ₄ +(V ₃ -V ₄)×	1850/3450	2135/4572	r59	250 402	
V ₆	3CH	1	1	1	1	0	0	V _{60'}	V ₄ +(V ₃ -V ₄)×	1600/3450	1733/4572	r60	300 402	
	3DH	1	1	1	1	0	1	V _{61'}	V ₄ +(V ₃ -V ₄)×	1300/3450	1331/4572	r61	500 459	
	3EH	1	1	1	1	1	0	V _{62'}	V ₄ +(V ₃ -V ₄)×	800/3450	872/4572	r62	800 872	
	3FH	1	1	1	1	1	1	V _{63'}	V ₄		rtotal	15850 15851		

Caution There is no connection between V₄ and V₅ terminal in the chip.

Figure 5-3. Relationship between Input Data and Output Voltage (2/2)

$$V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1 V, \text{POL2} = L$$

		Data						Output Voltage				rn		(Ω)	
		Dx5	Dx4	Dx3	Dx2	Dx1	Dx0								

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × 2 RGBs (6 dots)

Input width: 36 bits (2-pixel data)

R,/L = H (Right shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₅	D ₁₀ to D ₁₅	D ₂₀ to D ₂₅	D ₃₀ to D ₃₅	...	D ₄₀ to D ₄₅	D ₅₀ to D ₅₅

R,/L = L (Left shift)

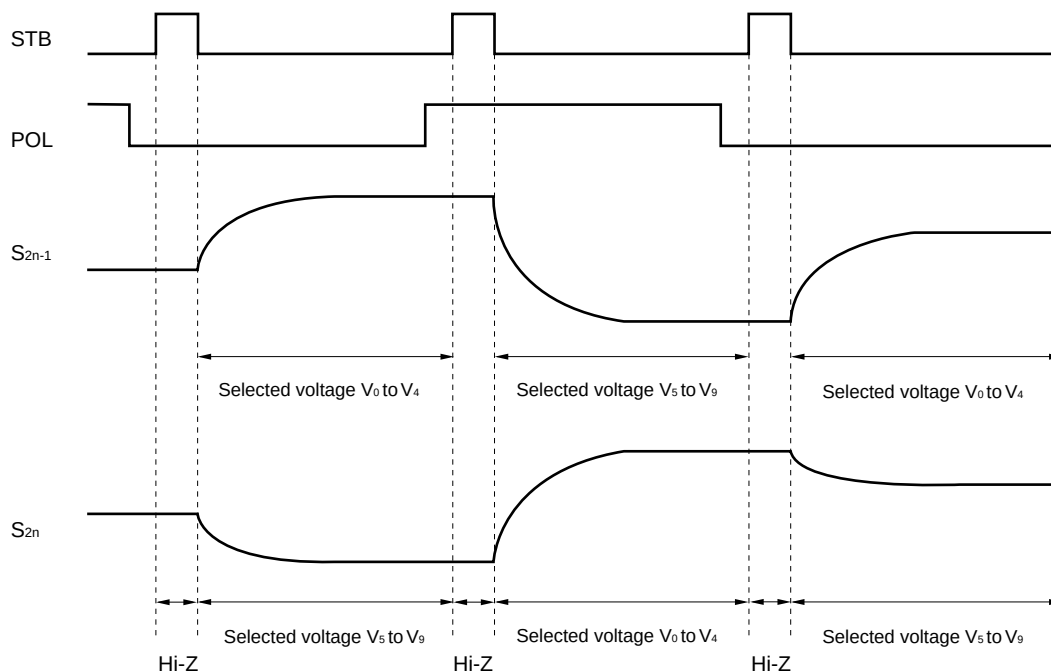
Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₅	D ₁₀ to D ₁₅	D ₂₀ to D ₂₅	D ₃₀ to D ₃₅	...	D ₄₀ to D ₄₅	D ₅₀ to D ₅₅

POL	S _{2n-1} ^{Note}	S _{2n} ^{Note}
L	V ₀ to V ₄	V ₅ to V ₉
H	V ₅ to V ₉	V ₀ to V ₄

Note S_{2n-1} (Odd output), S_{2n} (Even output)

★ 7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



8. RELATIONSHIP BETWEEN STB, CLK, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

Figure 8-1. Output Circuit Block Diagram

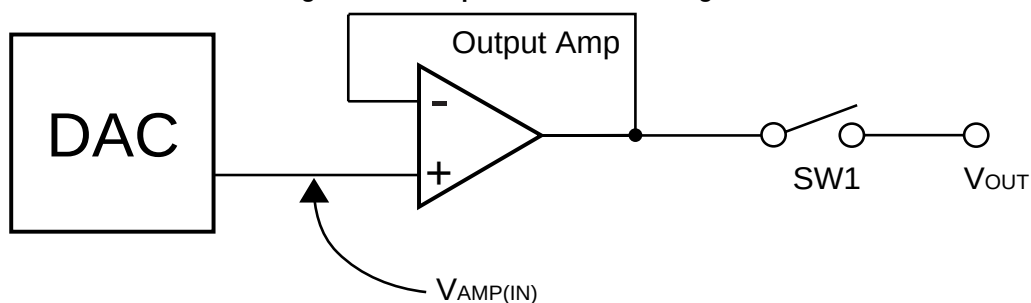
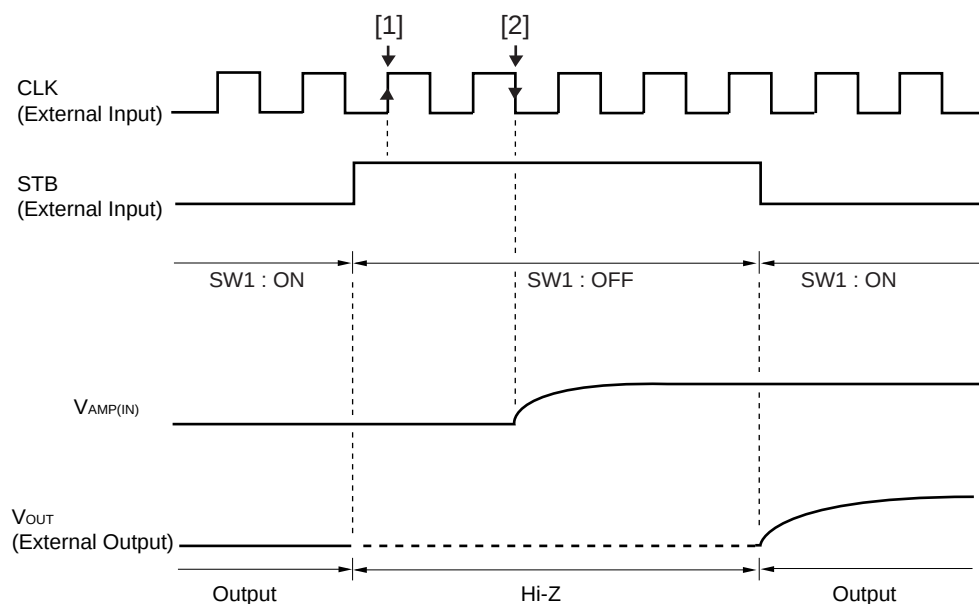


Figure 8-2. Output Circuit Timing Waveform



Remarks 1. STB = L : SW1 = ON

STB = H : SW1 = OFF

2. STB = "H" is acknowledged at timing [1].

3. The display data latch is completed at timing [2] and the input voltage (Vamp (in) : gray-scale level voltage) of the output amplifier changes.

9. CURRENT CONSUMPTION REDUCTION FUNCTION

The μ PD16732A and 16732B have a low power control function (LPC) which can switch the bias current of the output amplifier between two levels and a bias control function (Bcont) which can be used to finely control the bias current.

<Low power control function (LPC)>

The bias current of the output amplifier can be switched between two levels using this pin. (Bcont: Open)

LPC = H or Open: Normal power mode

LPC = L: Low power mode

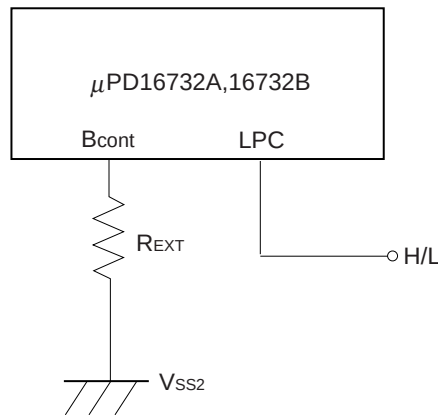
- ★ The V_{DD2} of static current consumption can be reduced to two thirds of that in normal mode. Input a stable DC current (V_{DD1}/V_{SS1}) to this pin.

<Bias Current Control Function (Bcont)>

It is possible to fine-control the current consumption by using the bias current control function (Bcont pin). When using this function, connect this pin to the stabilized ground potential (V_{SS2}) via an external resistor (R_{EXT}). When not using this function, leave this pin open.

Refer to the table below for the percentage of current regulation when using the bias current control function.

Figure9–1. Bias Current Control Function (Bcont)



Refer to the table below for the percentage of current regulation when using the bias current control function.

★ Talbe9–1. Current Consumption Regulation Percentage Compared to Normal Mode

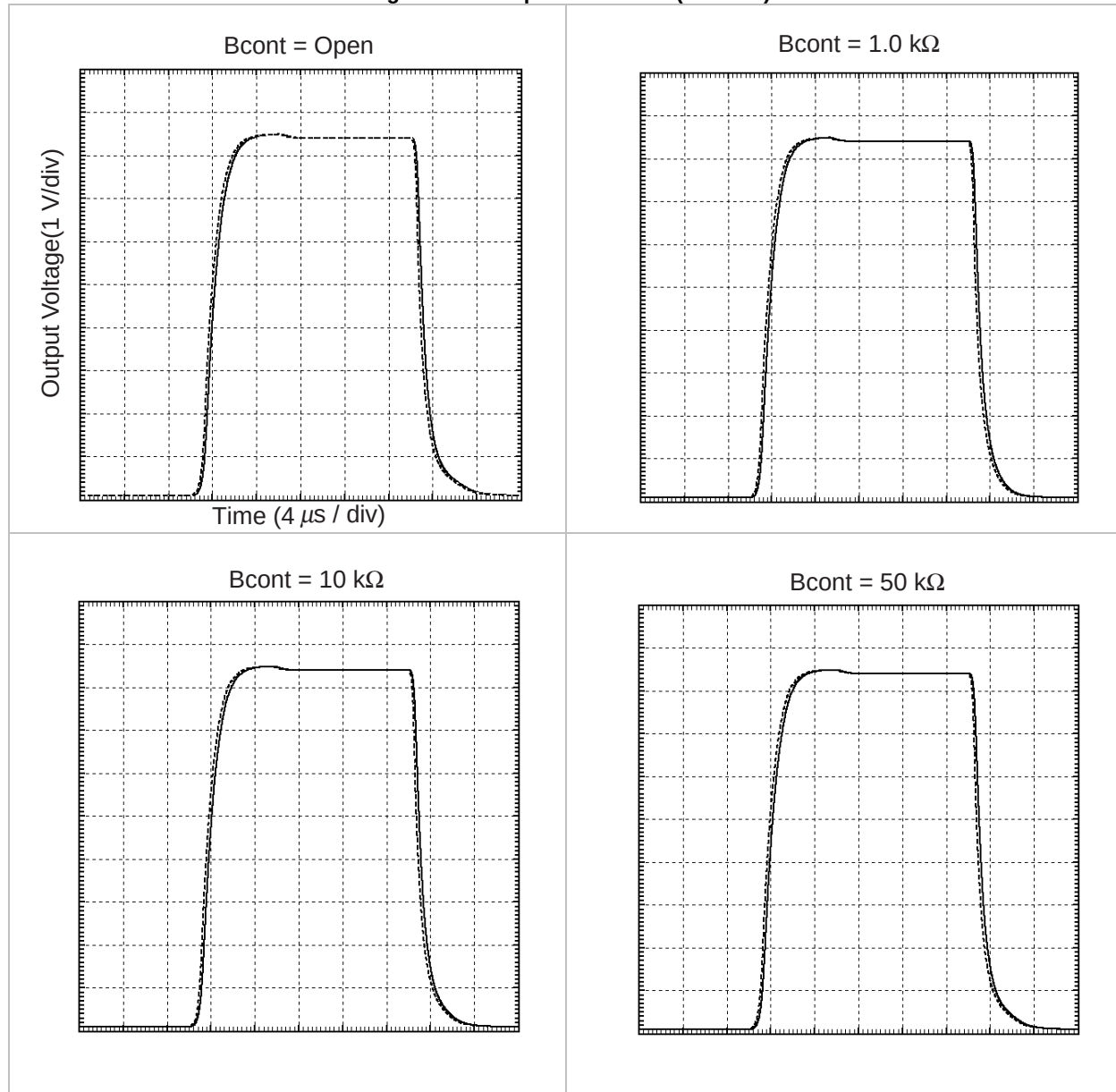
R_{EXT}	Current Consumption Regulation Percentage	
	LPC = H	LPC = L
∞ (Open)	100 %	65 %
50 kΩ	110 %	70 %
20 kΩ	115 %	80 %
10 kΩ	120 %	85 %

$V_{DD1} = 3.3 \text{ V}$
 $V_{DD2} = 8.7 \text{ V}$
 $LPC = 3.3 \text{ V}/0 \text{ V}$

Remark The above current consumption regulation percentages are not product-characteristic guaranteed as they are based on the results of simulation.

Caution Because the low-power and bias-current control functions control the bias current in the output amplifier and regulate the over-all current consumption of the driver IC, when this occurs, the characteristics of the output amplifier will simultaneously change. Therefore, when using these functions, be sure to sufficiently evaluate the picture quality.

Figure9-2. Output wave form (LPC = L)



----- [1]
 _____ [2]

<Test Condition>

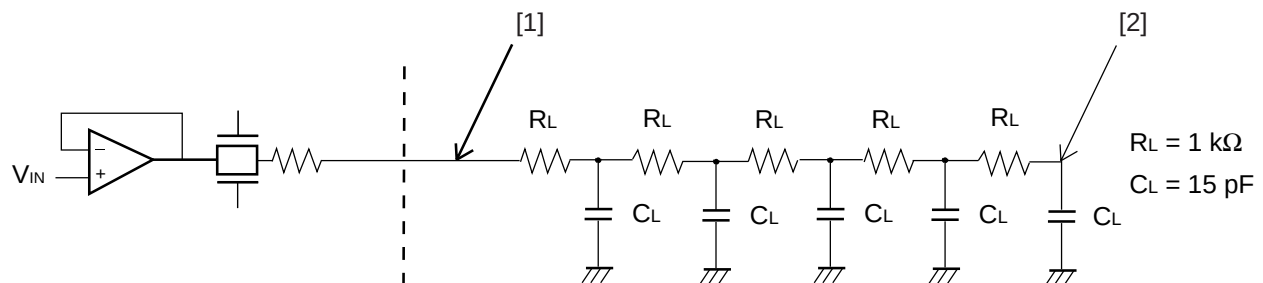
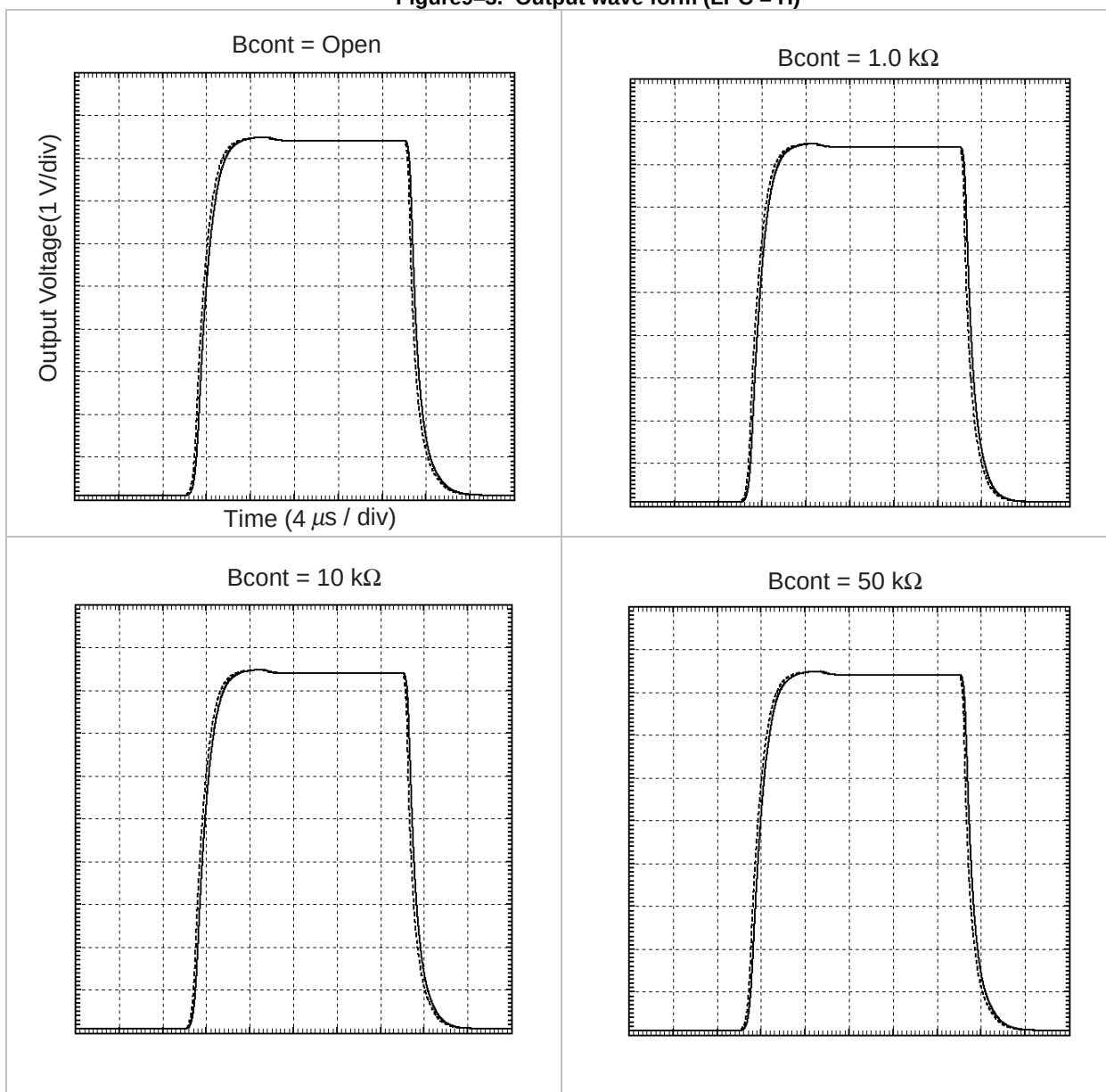


Figure9-3. Output wave form (LPC = H)



10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ($T_A = +25\text{ }^\circ\text{C}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	-0.5 to +4.0	V
Driver Part Supply Voltage	V_{DD2}	-0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	-0.5 to $V_{DD1} + 0.5$	V
Driver Part Input Voltage	V_{I2}	-0.5 to $V_{DD2} + 0.5$	V
Logic Part Output Voltage	V_{O1}	-0.5 to $V_{DD1} + 0.5$	V
Driver Part Output Voltage	V_{O2}	-0.5 to $V_{DD2} + 0.5$	V
Operating Ambient Temperature	T_A	-10 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range ($T_A = -10\text{ to }+75\text{ }^\circ\text{C}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.3		3.6	V
Driver Part Supply Voltage	V_{DD2}		8.0	8.5	9.0	V
High-Level Input Voltage	V_{IH}		$0.7 V_{DD1}$		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		$0.3 V_{DD1}$	V
γ -Corrected Voltage	V_0 to V_9		$V_{SS2} + 0.1$		$V_{DD2} - 0.1$	V
Driver Part Output Voltage	V_O		$V_{SS2} + 0.1$		$V_{DD2} - 0.1$	V
Maximum Clock Frequency	$f_{MAX.}$	$V_{DD1} = 2.3\text{ V to }3.6\text{ V}$	45			MHz
		$V_{DD1} = 3.0\text{ V to }3.6\text{ V}$	65			MHz

Electrical Characteristics ($T_A = -10$ to $+75$ °C, $V_{DD1} = 2.3$ V to 3.6 V, $V_{DD2} = 8.5$ V $\pm$ 0.5 V, $V_{SS1} = V_{SS2} = 0$ V,
Unless otherwise specified, the input level is defined to be LPC = H or Open,
Bcont = Open)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}					± 1.0	μ A
High-Level Output Voltage	V_{OH}	STHR (STHL), $I_{OH} = 0$ mA		$V_{DD1} - 0.1$			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), $I_{OL} = 0$ mA				0.1	V
γ -Corrected Supply Current	I_γ	V_0 to $V_4 =$	V_0 pin, V_5 pin	126	252	504	μ A
		V_5 to $V_9 = 4.0$ V	V_4 pin, V_9 pin	-504	-252	-126	μ A
Driver Output Current	I_{VOH}	$V_X = 7.0$ V, $V_{OUT} = 6.5$ V ^{Note}				-30	μ A
	I_{VOL}	$V_X = 1.0$ V, $V_{OUT} = 1.5$ V ^{Note}		30			μ A
Output Voltage Deviation	ΔV_O	$V_{DD1} = 3.3$ V, $V_{DD2} = 8.5$ V,			± 7	± 20	mV
Output swing difference deviation	ΔV_{P-P}	$V_{OUT} = 2.0$ V, 4.25 V, 6.5 V			± 2	± 15	mV
Output Voltage Range	V_O	All Input data		0.1		$V_{DD2} - 0.1$	V
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1} , with no load			3.0	6.0	mA
Driver Part Dynamic Current Consumption	I_{DD21}	$V_{DD2} = 8.5$ V $\pm$ 0.5 V, with no load LPC = H, Bcont = Open			3.0	6.0	mA
	I_{DD22}	$V_{DD2} = 8.5$ V $\pm$ 0.5 V, with no load LPC = L, Bcont = Open			2.0	4.0	mA

Notes1. V_X refers to the output voltage of analog output pins S_1 to S_{384} .

2. V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{384} .

Cautions 1. The STB cycle is defined to be 20 μ s at $f_{CLK} = 40$ MHz.

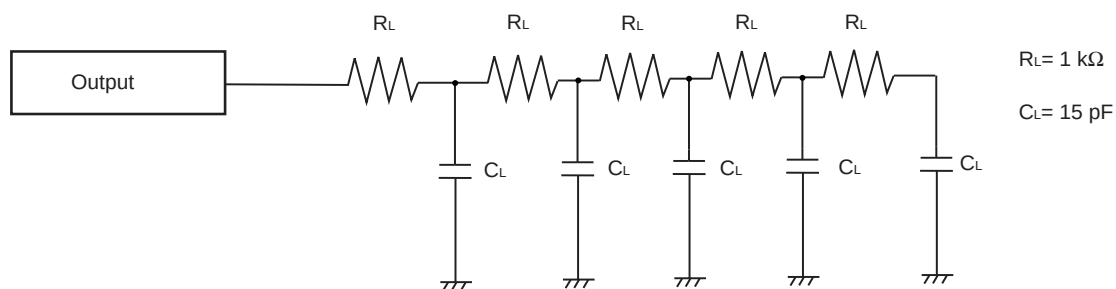
2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics ($T_A = -10$ to $+75$ °C, $V_{DD1} = 2.3$ V to 3.6 V, $V_{DD2} = 8.5$ V $\pm$ 0.5 V, $V_{SS1} = V_{SS2} = 0$ V,
Unless otherwise specified, the input level is defined to be LPC = H or Open,
Bcont = Open)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	$C_L = 10$ pF, $V_{DD1} = 2.3$ V to 3.6 V		10	17	ns
		$C_L = 10$ pF, $V_{DD1} = 3.0$ V to 3.6 V		7	10.5	ns
Driver Output Delay Time	t_{PLH2}	$C_L = 75$ pF, $R_L = 5$ k Ω		2.5	5	μ s
	t_{PLH3}			5	8	μ s
	t_{PHL2}			2.5	5	μ s
	t_{PHL3}			5	8	μ s
Input Capacitance	C_{i1}	STHR (STHL) excluded, $T_A = +25$ °C		5	10	pF
	C_{i2}	STHR (STHL), $T_A = +25$ °C		8	10	pF

<Measurement Condition>

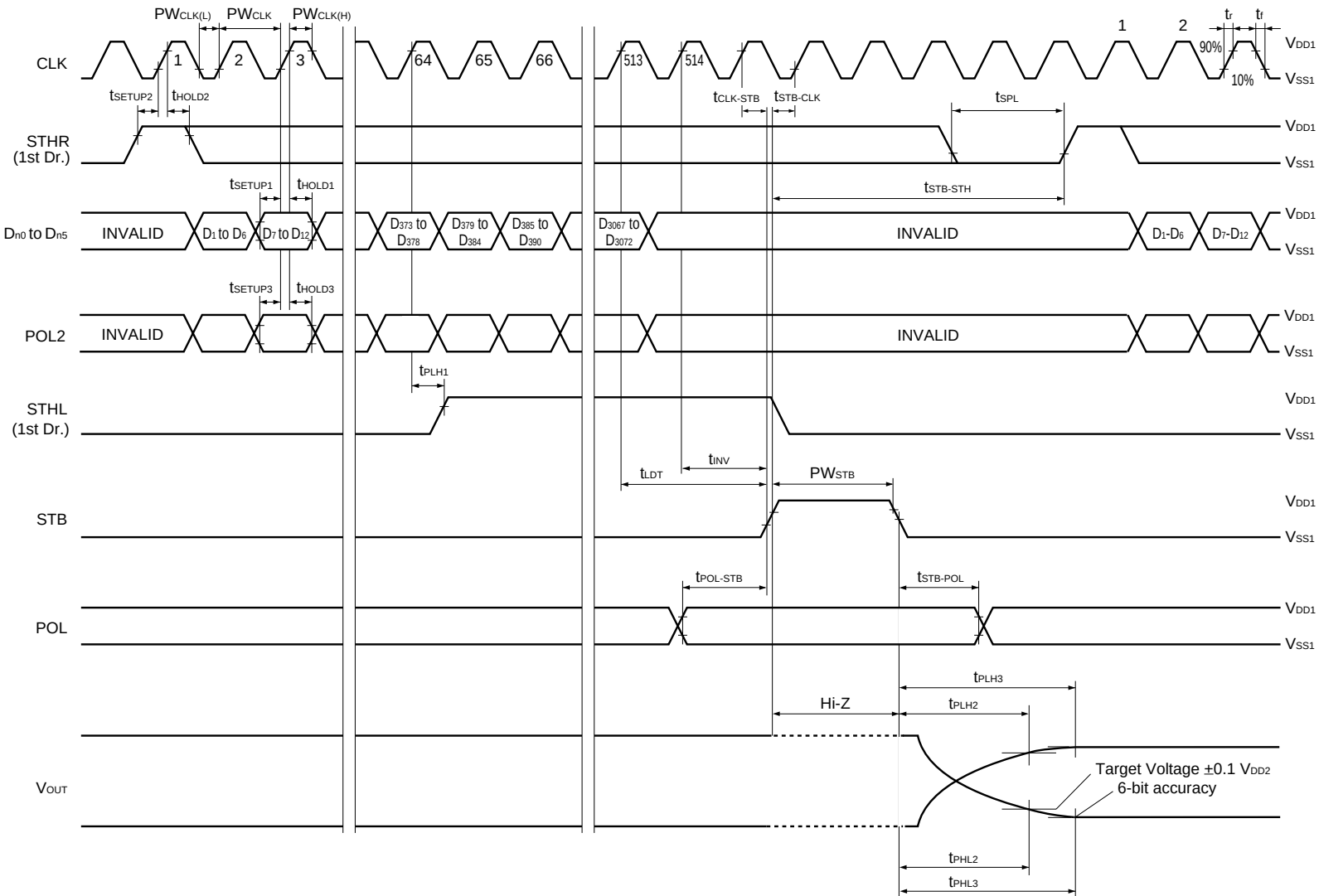


Timing Requirement ($T_A = -10$ to $+75$ °C, $V_{DD1} = 2.3$ V to 3.6 V, $V_{SS1} = V_{SS2} = 0$ V, $t_r = t_f = 8.0$ ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}	$V_{DD1} = 2.3$ V to 3.6 V	22			ns
		$V_{DD1} = 3.0$ V to 3.6 V	15			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$	$V_{DD1} = 2.3$ V to 3.6 V	6			ns
		$V_{DD1} = 3.0$ V to 3.6 V	4			ns
Data Setup Time	t_{SETUP1}		4			ns
Data Hold Time	t_{HOLD1}		0			ns
Start Pulse Setup Time	t_{SETUP2}		4			ns
Start Pulse Hold Time	t_{HOLD2}		0			ns
POL2 Setup Time	t_{SETUP3}		4			ns
POL2 Hold Time	t_{HOLD3}		0			ns
Start Pulse Low Period	t_{SPL}		6			ns
STB Pulse Width	PW_{STB}		2			CLK
					4	μs
Data Invalid Period	t_{INV}		1			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	$CLK \uparrow \rightarrow STB \uparrow$	6			ns
STB-CLK Time	$t_{STB-CLK}$	$STB \uparrow \rightarrow CLK \uparrow$ $V_{DD1} = 2.3$ V to 3.6 V	9			ns
		$STB \uparrow \rightarrow CLK \uparrow$ $V_{DD1} = 3.0$ V to 3.6 V	6			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	$STB \uparrow \rightarrow STHR(STHL) \uparrow$	2			CLK
POL-STB Time	$t_{POL-STB}$	$POL \uparrow$ or $\downarrow \rightarrow STB \uparrow$	-5			ns
★ STB-POL Time	$t_{STB-POL}$	$STB \downarrow \rightarrow POL \downarrow$ or $\uparrow$	6			ns

★ 11. SWITCHING CHARACTERISTICS WAVEFORM

Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$.



12. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μ PD16732A, 16732B.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

μ PD16732AN-xxx, μ PD16732BN-xxx : TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm ² : time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm ² : time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability / Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

- **The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
 - No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
 - NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
 - Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
 - While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
 - NEC devices are classified into the following three quality grades:
"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
 - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
 - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
- The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.