XN1872

Silicon N-channel • Enhancement MOS FET

For switching

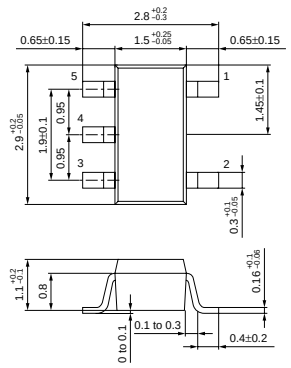
Features

- Two elements incorporated into one package. (Source-coupled FETs)
- Reduction of the mounting area and assembly cost by one half.

Basic Part Number of Element

- 2SK621 × 2 elements

Unit: mm



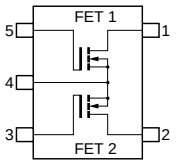
1 : Drain (Tr1)
2 : Drain (Tr2)
3 : Gate (Tr2)
4 : Source
5 : Gate (Tr1)
EIAJ : SC–74A
Mini Type Pakage (5–pin)

Marking Symbol: 5U

Absolute Maximum Ratings (Ta=25˚C)

Parameter		Symbol	Ratings	Unit
Rating of element	Drain to source voltage	V_{DSS}	50	V
	Gate to source voltage	V_{GSO}	8	V
	Drain current	I_D	100	mA
		I_{DM}	200	mA
Overall	Total power dissipation	P_T	300	mW
	Channel temperature	T_{ch}	150	˚C
	Storage temperature	T_{stg}	–55 to +150	˚C

Internal Connection



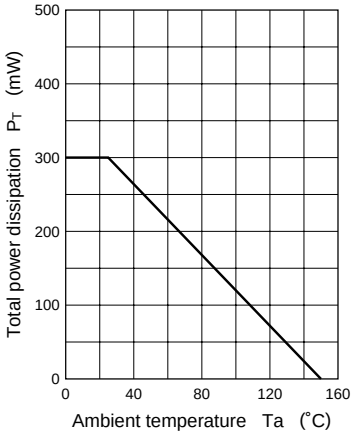
Electrical Characteristics (Ta=25˚C)

Parameter	Symbol	Conditions	min	typ	max	Unit
Drain to source voltage	V_{DSS}	I_D = 100μA, V_{GS} = 0	50			V
Drain current	I_{DSS}	V_{DS} = 10V, V_{GS} = 0			10	μA
Gate cutoff current	I_{GSS}	V_{GS} = 8V, V_{DS} = 0	40		80	μA
Gate threshold voltage	V_{th}	I_D = 100μA, V_{DS} = V_{GS}	1.5		3.5	V
Drain resistance	$R_{DS(on)}$	I_D = 20mA, V_{GS} = 5V			50	Ω
Forward transfer admittance	$\|Y_{fs}\|$	I_D = 20mA, V_{DS} = 5V, f = 1kHz	20	30		mS
Output voltage high level	V_{OH}	V_{DS} = 5V, V_{GS} = 1V, R_L = 200Ω	4.5			V
Output voltage low level	V_{OL}	V_{DS} = 5V, V_{GS} = 5V, R_L = 200Ω			1.0	V
Input resistance	R_1+R_2 *1		100		200	kΩ
Turn-on time	t_{on} *2	V_{DD} = 5V, V_{GS} = 0 to 5V, R_L = 200Ω			1.0	μs
Turn-off time	t_{off} *2	V_{DD} = 5V, V_{GS} = 5 to 0V, R_L = 200Ω			1.0	μs
Common source short-circuit input capacitance	C_{iss}	V_{DS} = 5V, V_{GS} = 0, f = 1MHz		9	15	pF

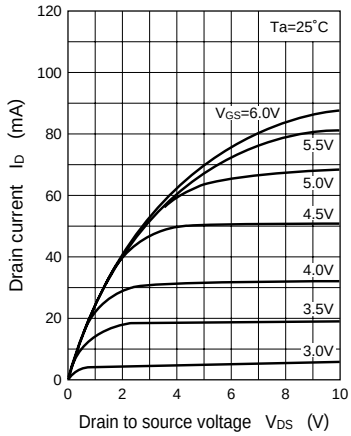
*1 Pulse measurement

*2 Resistance ratio R_1/R_2 = 1/50

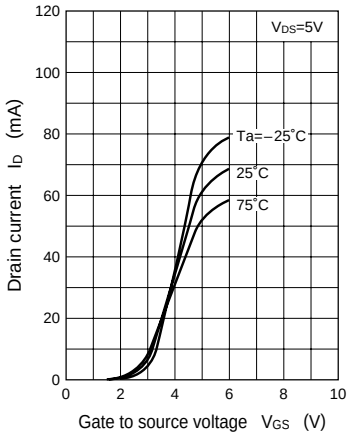
P_T — Ta



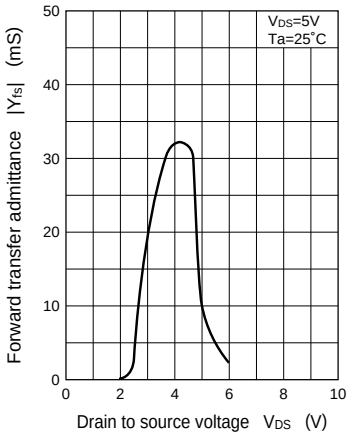
I_D — V_{DS}



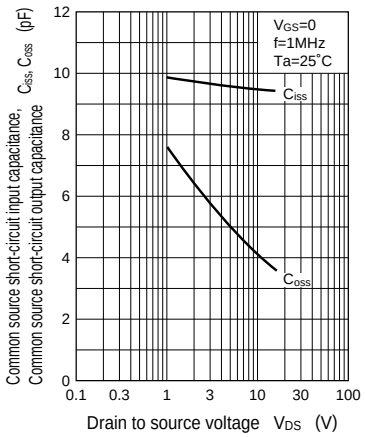
I_D — V_{GS}



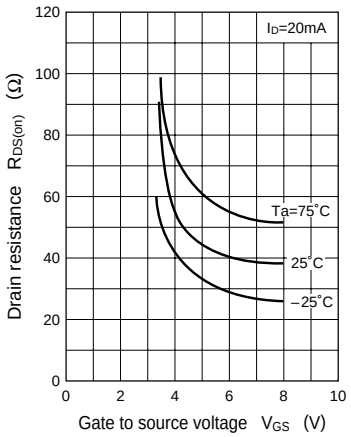
$|Y_{fs}|$ — V_{DS}



C_{iss}, C_{oss} — V_{DS}



$R_{DS(ON)}$ — V_{GS}



V_{IN} — I_O