

Am2964B

Dynamic Memory Controller



Advanced
Micro
Devices

DISTINCTIVE CHARACTERISTICS

- Dynamic Memory Controller for 16K and 64K MOS dynamic RAMs
- 8-Bit Refresh Counter for refresh address generation, has clear input and terminal count output
- Refresh Counter terminal count selectable at 256 or 128
- Latch input $\overline{RAS}$ Decoder provides 4 $\overline{RAS}$ outputs, all active during refresh
- Dual 8-Bit Address Latches plus separate $\overline{RAS}$ Decoder Latches
- Burst mode, distributed refresh or transparent refresh mode determined by user

GENERAL DESCRIPTION

The Am2964B Dynamic Memory Controller (DMC) replaces a dozen MSI devices by grouping several unique functions. Two 8-bit latches capture and hold the memory address. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX for output to the dynamic RAM address lines.

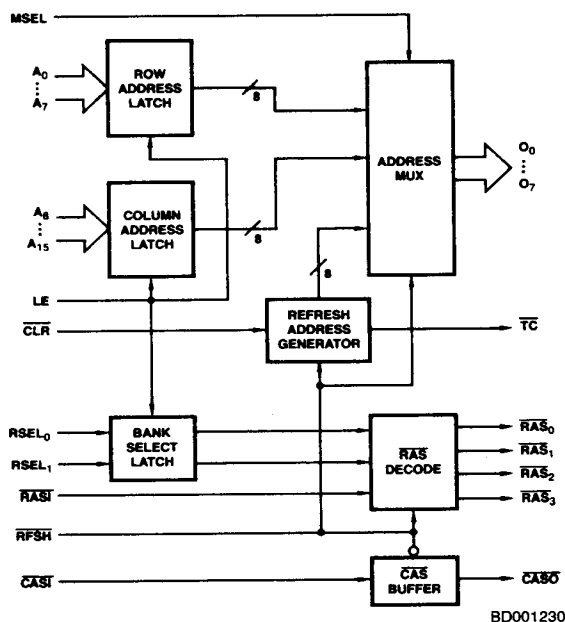
The same silicon chip also includes a special $\overline{RAS}$ decoder and $\overline{CAS}$ buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore allows a faster memory cycle time by the amount of skew eliminated.

The $\overline{RAS}$ Decoder allows upper addresses to select one-of-four banks of RAM by determining which bank receives a $\overline{RAS}$ input. During refresh ($\overline{RFSH} = \text{LOW}$) the decoder mode is changed to four-of-four and all banks of memory receive a $\overline{RAS}$ input for refresh in response to a $\overline{RAS}$ active LOW input. $\overline{CAS}$ is inhibited during refresh.

Burst mode refresh is accomplished by holding $\overline{RFSH}$ LOW and toggling $\overline{RAS}$.

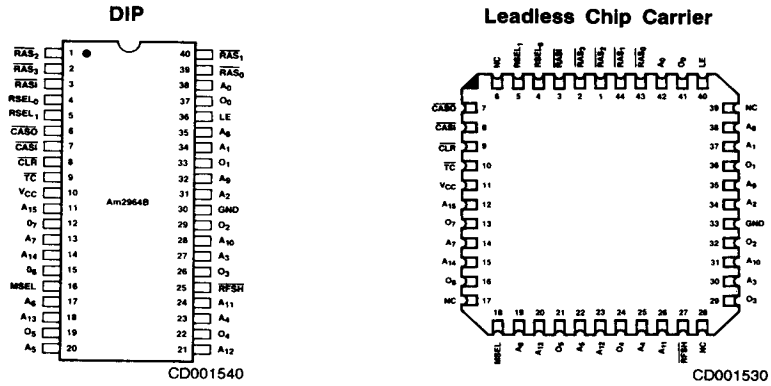
A_{15} is a dual function input which controls the refresh counter's range. For 64K RAMs it is an address input. For 16K RAMs it can be pulled to +12V through 1K Ω to terminate the refresh count at 128 instead of 256.

BLOCK DIAGRAM



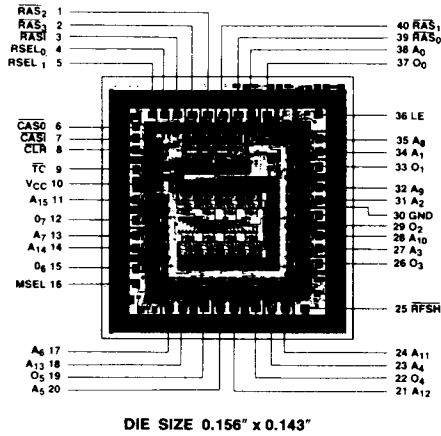
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CONNECTION DIAGRAM **Top View**

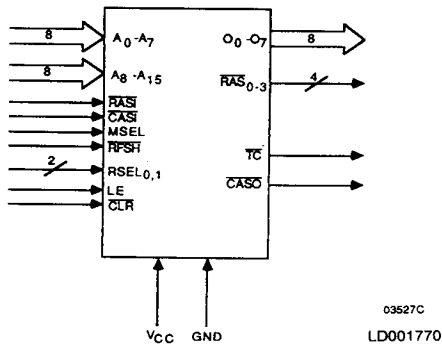


Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT



LOGIC SYMBOL



Am2964B

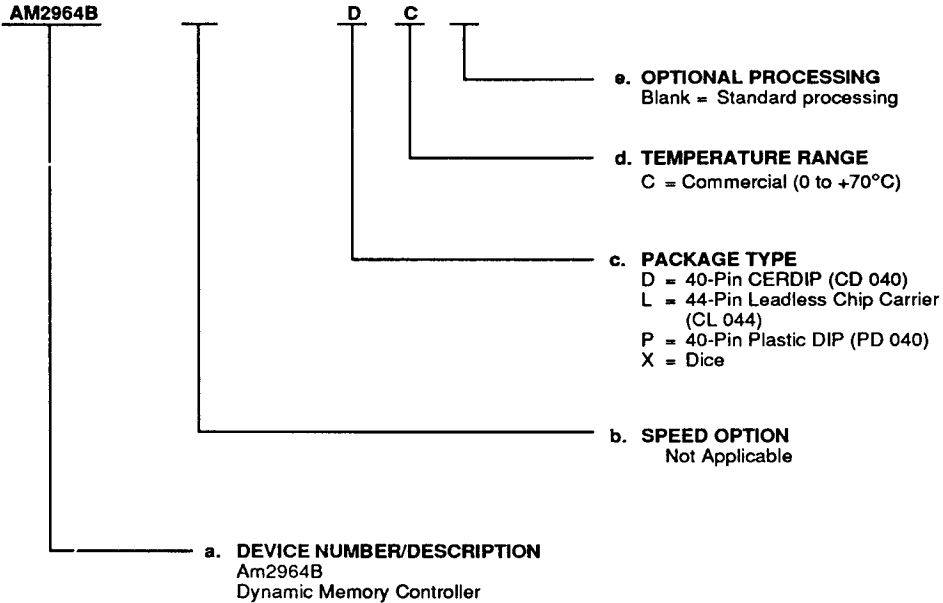
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM2964B	DC, LC, PC, XC

Valid Combinations

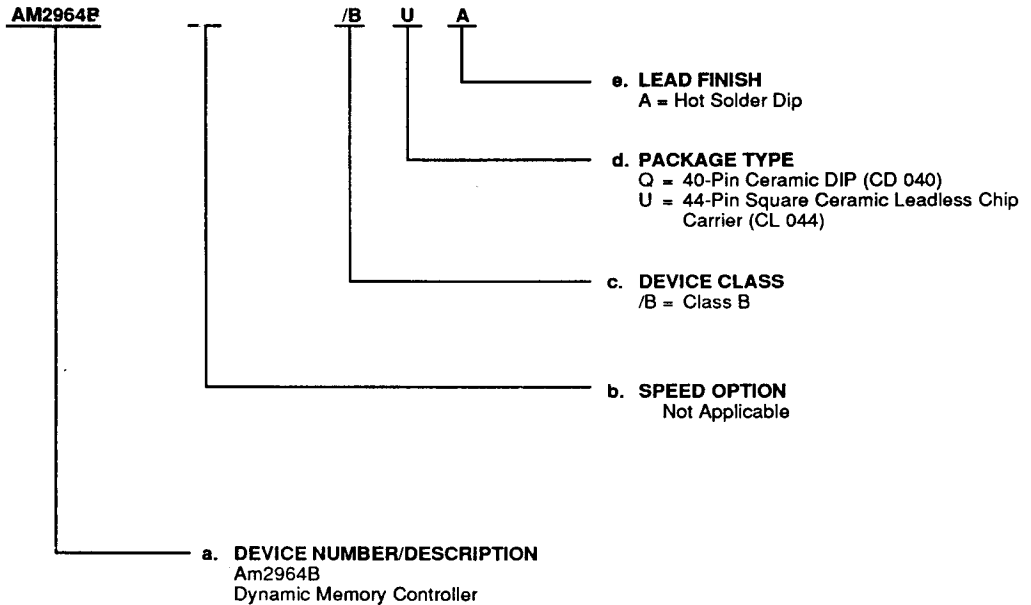
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (If applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM2964B	/BQA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A ₀ – A ₇	I	The low order Address inputs are used to latch eight Row Address inputs for the RAM. These inputs drive the outputs O ₀ – O ₇ when MSEL is HIGH.
	A ₈ – A ₁₅	I	The high order Address inputs are used to latch eight Column Address inputs for the RAM. These inputs drive the outputs O ₀ – O ₇ when MSEL is LOW.
11	A ₁₅	I	A ₁₅ is a dual input. With normal TTL level inputs A ₁₅ acts as address input A ₁₅ for 64K RAMs. If A ₁₅ is pulled up to +12V through a 1K Ω resistor, the terminal count output, TC, will go LOW every 128 counts (for 16K RAMs) instead of every 256 counts.
	O ₀ – O ₇	O	The RAM address outputs. The eight-bit width is designed for dynamic RAMs up to 64K.
16	MSEL	I	The Multiplexer-SElect input determines whether low order or high order address inputs appear at the multiplexer outputs O ₀ – O ₇ . When MSEL is HIGH the low order address latches (A ₀ – A ₇) are connected to the outputs. When MSEL is LOW the high order address latches are connected to the outputs.
25	RFSH	I	The Refresh control input. When active LOW the RFSH input switches the address output multiplexer to output the inverted contents of the 8-bit refresh counter. RFSH LOW also inhibits the CAS buffer and changes the mode of the RAS decoder from one-of-four to four-of-four so that all four RAS decoder outputs, RAS ₀ , RAS ₁ , RAS ₂ and RAS ₃ , go LOW in response to a LOW input at RAS _I . This action refreshes one row address in each of the four RAS decoded memory banks. The refresh counter is advanced at the end of each refresh cycle by the LOW-to-HIGH transition of RFSH or RAS _I (whichever occurs first). In burst mode refresh, RFSH may be held LOW and refresh accomplished by toggling RAS _I .
9	TC	O	The Terminal Count output. A LOW output at TC indicates that the refresh counter has been sequenced through either 128 or 256 refresh addresses depending on A ₁₅ . The TC output remains active LOW until the refresh counter is advanced by the rising edge of RAS _I or RFSH.
8	CLR	I	The refresh counter Clear input. An active LOW input at CLR resets the refresh counter to all LOW (refresh address output to all HIGH).
36	LE	I	The address latch enable input. An active HIGH input at LE causes the two 8-bit address latches and the 2-bit RAS Select input latch to go transparent, accepting new input data. A LOW input on LE latches the input data which meets set-up and hold time requirements.
4, 5	RSEL ₀ and RSEL ₁	I	The RAS decoder Select inputs. Data (latched) at these inputs (normally higher order addresses) is decoded by the RAS Decoder to "RAS Select" one of four banks of memory with RAS ₀ , RAS ₁ , RAS ₂ or RAS ₃ .
3	RAS _I	I	The Row Address Strobe Input. During normal memory cycles the selected RAS Decoder output RAS ₀ , RAS ₁ , RAS ₂ or RAS ₃ will go active LOW in response to an active LOW input at RAS _I . During refresh (RFSH = LOW), all RAS outputs go LOW in response to RAS _I = LOW.
39, 40, 1, 2	RAS ₀ , RAS ₁ , RAS ₂ , RAS ₃	O	Row Address Strobe outputs (RAS). Each provides a Row Address Strobe for one of the four banks of memory. Each will go active LOW only when selected by RSEL ₀ and RSEL ₁ and only when RAS _I goes active LOW. All RAS ₀ – ₃ outputs go active low in response RAS _I when RFSH goes LOW.
7	CAS _I	I	The Column Address Strobe. An active LOW input at CAS _I will result in an active LOW output at CAS ₀ , unless a refresh cycle is in progress (RFSH = LOW).
6	CAS ₀	O	The Column Address Strobe output. The active LOW CAS ₀ output strobes the Column Address into the dynamic RAM. CAS ₀ is inhibited during refresh (RFSH = LOW).

RAS OUTPUT FUNCTION TABLE

RFSH	RAS _I	RSEL ₁	RSEL ₀	RAS ₀	RAS ₁	RAS ₂	RAS ₃
L	H	X	X	H	H	H	H
L	L	X	X	L	L	L	L
H	H	X	X	H	H	H	H
H	L	L	L	L	H	H	H
H	L	L	H	H	L	H	H
H	L	H	L	H	H	L	H
H	L	H	H	H	H	H	L

CAS₀ FUNCTION TABLE

RFSH	CAS _I	CAS ₀
H	L	L
H	H	H
L	X	H

ADDRESS OUTPUT FUNCTION TABLE

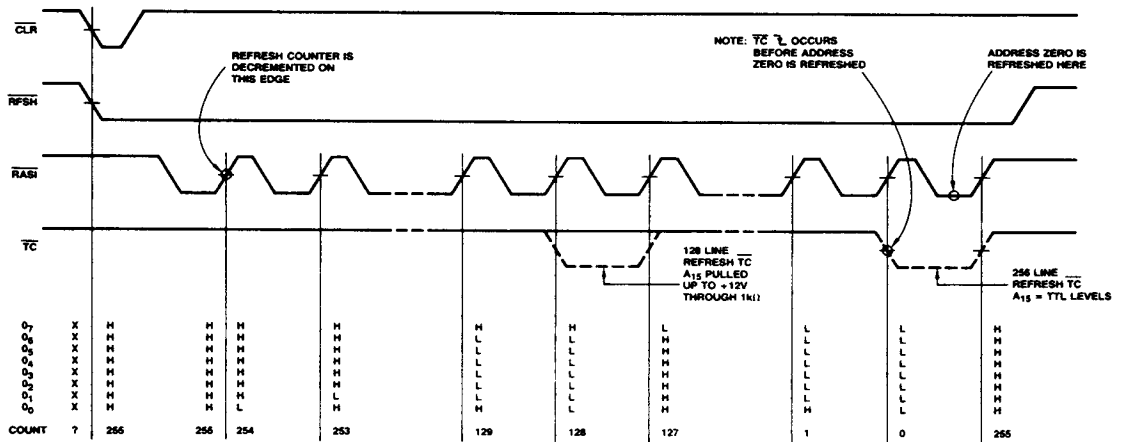
MSEL	RFSH	O ₀ -O ₇
H	H	A ₀ -A ₇
L	H	A ₈ -A ₁₅
X	L	Refresh Address

REFRESH ADDRESS COUNTER FUNCTION TABLE

A ₁₅	CLR	RFSH	RAS _i	T _C	REFRESH COUNT	FUNCTION
X	L	X	X	X	FF _H	Clear Counter
X	H		X	X	NC	Output Refresh Address No Change for Counter
X	H		L	X	Count - 1	Return to Memory Cycle Mode and Decrement Counter
X	H	L		X	NC	Output all RAS _i to RAM No Change for Counter
X	H	L		X	Count - 1	Return RAS _i to HIGH and Decrement Counter
L or H	H	X	X	L	00 _H	Terminal Count for 256 Line Refresh
+12V*	H	X	X	L	00 _H and 80 _H	Terminal Count for 128 Line Refresh

* Through 1K Ω resistor.

BURST REFRESH TIMING



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The timing shown assumes that burst mode applications may power-down the Am2964B with the RAM. Therefore the counter is cleared prior to executing the refresh sequence.

FUNCTIONAL DESCRIPTION

Architecture

The Dynamic Memory Controller (DMC) provides address multiplexing, refresh address generation and RAS/CAS control for the MOS dynamic RAM memories of any data width. The eight bit address path is designed for 64K RAMs and can be used with 16K RAMs.

Sixteen address input latches and two RAS Select latches (for higher order addresses) allow the DMC to control up to 256K words of memory (with 64K RAMs) by using the internal RAS decoder to select from one-of-four banks of RAMs.

Speed With Minimum Skew

The DMC provides Schottky speed in all of the critical paths. In addition, time skew between the Address, RAS and CAS paths is minimized (and specified) by placing these function on the same chip. The inclusion of the CAS buffer allows matching of its propagation delay, plus provides the CAS inhibit function during RAS - only refresh.

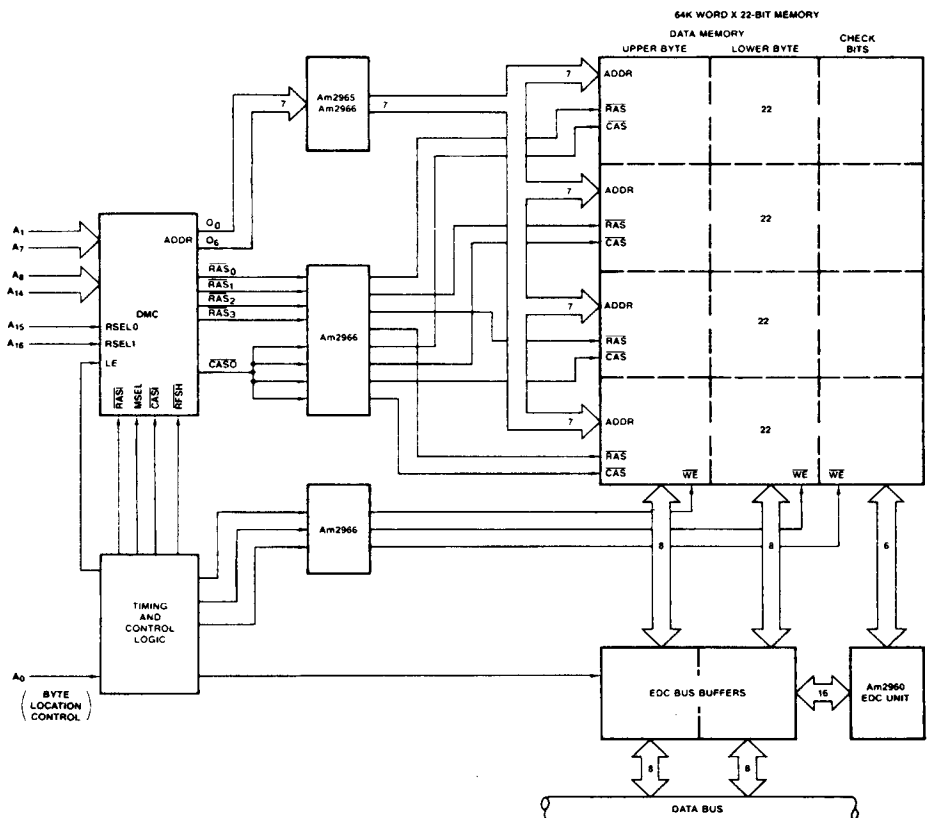
Input Latches

The eighteen input latches are transparent when LE is HIGH and latch the input data meeting set-up and hold time requirements when LE goes LOW. In systems with separate address and data buses, LE may be permanently enabled HIGH.

Refresh Counter

The 8-bit refresh counter provides both 128 and 256 line refresh capability. Refresh control is external to allow maximum user flexibility. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

The refresh counter is advanced at the LOW-to-HIGH transition of RFSH (or RASI). This assures a stable counter output for the next refresh cycle. The counter will continue to cycle through 256 addresses unless reset to zero by CLR. This actually causes all outputs to go HIGH since the output MUX is inverting. (Address inputs to outputs are non-inverting since both the input latches and output MUX are inverting).



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Address and RAS/CAS drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for RAS/CAS, spreading the CAS loading over four drivers to equalize the capacitive load on each driver.

Figure 1. Dynamic Memory Control with Error Detection and Correction

Refresh Terminal Count

The refresh counter also provides a Terminal Count output for burst mode refresh applications. $\overline{TC}$ normally occurs at count 255 (0₀ to 0₇ all LOW when $\overline{RFSH}$ is LOW). $\overline{TC}$ can be made to occur at count 127 for 128 line burst mode refresh by pulling A₁₅ up to +12V through a 1K Ω ±10% resistor. The counter actually cycles through 256 with $\overline{TC}$ determined by A₁₅. Otherwise, A₁₅ functions as an address input when driven at normal TTL levels.

Three Input 8-Bit Address Multiplexer

The address MUX is 8-bits wide (for 64K RAMs) and has three data sources: the lower address input latch (A₀ to A₇), the upper address input latch (A₈ to A₁₅) and the internal refresh counter. The lower address latch is selected when MSEL is HIGH. This is normally the Row address. The upper address latch is selected when MSEL is LOW. This is normally the Column address. The third source, the refresh counter, is selected when $\overline{RFSH}$ is LOW and overrides MSEL.

When $\overline{RFSH}$ goes LOW, the MUX selects the refresh counter address and $\overline{CAS0}$ is inhibited. Also, the $\overline{RAS}$ Decoder

function is changed from one-of-four to four-of-four so all $\overline{RAS}$ outputs $\overline{RAS_0}$ - $\overline{RAS_3}$ go LOW to refresh all banks of memory when $\overline{RAS_1}$ goes LOW. When $\overline{RFSH}$ is HIGH only one $\overline{RAS}$ output goes low. This is determined by the $\overline{RAS}$ Select inputs, RSEL₀ and RSEL₁. In either case the $\overline{RAS}$ Decoder output timing is controlled by $\overline{RAS_1}$ to make sure the refresh count appears at 0₀-0₇ before $\overline{RAS_0}$ - $\overline{RAS_3}$ go LOW. This assures meeting Row address Set-up time requirement of the RAM (t_{ASR}).

Maximum Performance System

The typical organization of a maximum performance 16-bit system including Error Detection and Correction is shown in Figure 1. Delay lines provide the most accurate timing and are recommended for $\overline{RAS}$ /MSEL/ $\overline{CAS}$ timing in this type of system.

Controlling 16K RAMs or Smaller Systems

16K RAMs require seven address inputs and 128 line refresh. Also, A₀ is often used to designate upper or lower byte transactions in 16-bit systems. These modifications are shown in Figure 2.

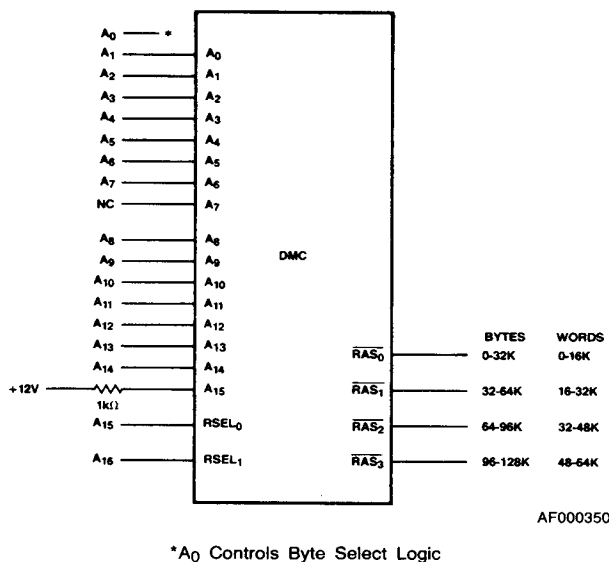


Figure 2. Word Organized Memory Using 16K RAMs

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Supply Voltage to Ground Potential	
Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs For	
High Output State	-0.5V to V_{CC} Max
DC Input Voltage	-0.5V to +5.5V
Output Current, Into Outputs	20mA
DC Input Current	-30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature	0°C to +70°C
Supply Voltage	+4.75V to +5.25V

Military (M) Devices

Temperature	-55°C to +125°C
Supply Voltage	+4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -1\text{mA}$	TC	2.5			Volts
			Others	3.0			Volts
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -15\text{mA}$	All outputs except TC	2.0			Volts
V_{OL}	Output LOW Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL}	All outputs except TC, $I_{OL} = 16\text{mA}$			0.5	Volts
			TC, $I_{OL} = 8\text{mA}$			0.5	Volts
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{IN} = -18\text{mA}$				-1.5	Volts
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX}$ $V_{IN} = 0.4\text{V}$	RASI			-3.2	mA
			CASI, MSEL, RFSH			-1.6	mA
			A ₀ - A ₁₅ , CLR RSEL _{0,1} , LE			-0.4	mA
I_{IH}	Input HIGH Current	$V_{CC} = \text{MAX}$ $V_{IN} = 2.7\text{V}$	RASI			100	μA
			CASI, MSEL, RFSH			50	μA
			A ₀ -A ₁₅ , CLR RSEL _{0,1} , LE			20	μA
I_I	Input HIGH Current	$V_{CC} = \text{MAX}$ $V_{IN} = 5.5\text{V}$	RASI			2.0	mA
			CASI, MSEL, RFSH			1.0	mA
		$V_{CC} = \text{MAX}$ $V_{IN} = 5.5\text{V}$	A ₀ -A ₁₅ , CLR RSEL _{0,1} , LE			0.1	mA
I_{SC}	Output Short Circuit Current	$V_{CC} = \text{MAX}$ (Note 3)		-40		-100	mA
I_{CC}	Power Supply Current (Note 4)	25°C, 5V			122		mA
		0°C to 70°C				173	mA
		70°C	COM'L				
		-55°C to +125°C				164	mA
		+125°C	MIL			150	mA
I_T	A ₁₅ Enable Current	A ₁₅ connected to +12V through 1KΩ±10%				5	mA

- Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is worst case when the Address inputs are latched HIGH, the refresh counter is at terminal count (255), RASI and CASI are HIGH and all other inputs are LOW.

SWITCHING CHARACTERISTICS over operating range for $C_L = 50\text{pF}$ **Am2964B** (Notes 5, 6)

Parameter	Description	Test Conditions	Typ	COMMERCIAL		MILITARY		Units
				Min	Max	Min	Max	
1	t_{PD}	A_i to O_i Delay	14		19		23	ns
2	t_{PHL}	RAS_i to RAS_i (RFSH = H)	14		20		23	ns
3	t_{PHL}	RAS_i to RAS_i (RFSH = L)	14		20		23	ns
4	t_{PD}	MSEL to O_i	17	9		9		ns
5	t_{PD}	MSEL to O_i	17		21		25	ns
6	t_{PHL}	CAS_i to CAS_i (RFSH = H)	12		17		19	ns
7	t_{PHL}	$RSEL_i$ to RAS_i (LE = H, RAS_i = L)	15		20		24	ns
8	t_{PLH}	RFSH to TC (RAS_i = L)	30		40		50	ns
9	t_{PLH}	RAS_i to TC (RFSH = L)	25		35		40	ns
10	t_{PW}	RAS_i = L (RFSH = L)	10	50		50		ns
11	t_{PW}	RAS_i = H (RFSH = L)	10	50		50		ns
12	t_{PD}	RFSH to O_i (RAS_i = X)	17		21		25	ns
13	t_{PHL}	RFSH to RAS_i (RAS_i = L)	19		26		29	ns
14	t_{PW}	CLR = L	10	30		35		ns
15	t_{PLH}	RFSH to CAS_i (RAS_i = L, CAS_i = L, Note 7)	16		21		25	ns
16	t_{PD}	LE to O_i	25		35		40	ns
17	t_{PHL}	LE to RAS_i	30		40		45	ns
18	t_{PLH}	CLR to TC	35		45		56	ns
19	t_{PLH}	CLR to O_i (RFSH = L)	31		44		54	ns
20	t_S	A_i to LE Set-Up Time	0	5		5		ns
21	t_H	A_i to LE Hold Time	5	12		15		ns
22	t_S	$RSEL_i$ to LE Set-Up Time	0	5		5		ns
23	t_H	$RSEL_i$ to LE Hold Time	10	17		25		ns
24	t_S	CLR Recovery Time	10	16		18		ns
25	t_{SKEW}	O_i to RAS_i (RFSH = H, Note 8)	2		5		6	ns
26	t_{SKEW}	O_i to CAS_i (Note 8)	6		8		8	ns
27	t_{SKEW}	O_i to RAS_i (RFSH = L, Note 9)	6		8		10	ns
28	t_{SKEW}	O_i to RAS_i (MSEL = $\overline{L}$, Note 10)	1		5		5	ns

Notes: 5. Minimum spec limits for t_{pw} , t_s and t_H are minimum system operating requirements. Limits for t_{SKEW} and t_{PD} are guaranteed test limits for the device.

6. All AC parameters are specified at the 1.5V level.

7. RFSH inhibits CAS_i during refresh. Specification is for CAS_i inhibit time.

8. O_i to RAS_i (RFSH = HIGH) skew is guaranteed maximum difference between fastest RAS_i to RAS_i delay and slowest A_i to O_i delay within a single device. O_i to CAS_i skew is maximum difference between fastest CAS_i to CAS_i delay and slowest MSEL to O_i delay within a single device. See application section entitled Memory Cycle Timing for correlation to System Timing requirements.

9. O_i to RAS_i (RFSH = LOW) skew is guaranteed maximum difference between fastest RAS_i to RAS_i delay and slowest RFSH to O_i delay within a single device. See application section on Refresh Timing for correlation to system refresh timing requirements.

10. O_i to RAS_i (MSEL = $\overline{L}$) skew is guaranteed maximum difference between fastest MSEL $\overline{L}$ to O_i delay and slowest RAS_i to RAS_i delay within a single device.

SWITCHING CHARACTERISTICS over operating range for $C_L = 50pF$
Am2964B (Notes 5, 6)

Parameter		Description	Test Conditions	Typ	COMMERCIAL		MILITARY		Units
					Min	Max	Min	Max	
1	t_{PD}	A_i to O_i Delay	$C_L = 150pF$	20		25		30	ns
2	t_{PHL}	$\overline{RAS}_i$ to $\overline{RAS}_i$ (RFSH = H)		18		24		27	ns
3	t_{PHL}	$\overline{RAS}_i$ to $\overline{RAS}_i$ (RFSH = L)		18		24		27	ns
4	t_{PD}	MSEL to O_i		23	12		12		ns
5	t_{PD}	MSEL to O_i		23		27		31	ns
6	t_{PHL}	$\overline{CAS}_i$ to $\overline{CAS}_i$ (RFSH = H)		17		24		26	ns
7	t_{PHL}	$RSEL_i$ to $\overline{RAS}_i$ (LE = H, $\overline{RAS}_i$ = L)		19		27		30	ns
8	t_{PLH}	RFSH to $\overline{TC}$ ($\overline{RAS}_i$ = L)		34		45		55	ns
9	t_{PLH}	$\overline{RAS}_i$ to $\overline{TC}$ (RFSH = L)		32		45		55	ns
10	t_{PW}	$\overline{RAS}_i$ = L (RFSH = L)		10	50		50		ns
11	t_{PW}	$\overline{RAS}_i$ = H (RFSH = L)		10	50		50		ns
12	t_{PD}	RFSH to O_i ($\overline{RAS}_i$ = X)		21		27		30	ns
13	t_{PHL}	RFSH to $\overline{RAS}_i$ ($\overline{RAS}_i$ = L)		25		33		36	ns
14	t_{PW}	$\overline{CLR}$ = L		10	30		35		ns
15	t_{PLH}	RFSH to $\overline{CAS}_i$ ($\overline{RAS}_i$ = L, $\overline{CAS}_i$ = L, Note 7)		21		27		31	ns
16	t_{PD}	LE to O_i		30		40		50	ns
17	t_{PHL}	LE to $\overline{RAS}_i$		34		45		54	ns
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$		39		55		60	ns
19	t_{PLH}	$\overline{CLR}$ to O_i (RFSH = L)		38		50		62	ns
20	t_S	A_i to LE Set-Up Time		0	5		5		ns
21	t_H	A_i to LE Hold Time		5	12		12		ns
22	t_S	$RSEL_i$ to LE Set-Up Time		0	5		5		ns
23	t_H	$RSEL_i$ to LE Hold Time		10	17		25		ns
24	t_S	$\overline{CLR}$ Recovery Time		10	16		18		ns
25	t_{SKEW}	O_i to $\overline{RAS}_i$ (RFSH = H, Note 8)		3		6		7	ns
26	t_{SKEW}	O_i to $\overline{CAS}_i$ (Note 8)		6		8		8	ns
27	t_{SKEW}	O_i to $\overline{RAS}_i$ (RFSH = L, Note 9)		6		9		10	ns
28	t_{SKEW}	O_i to $\overline{RAS}_i$ (MSEL = $\overline{L}$, Note 10)		1		5		5	ns

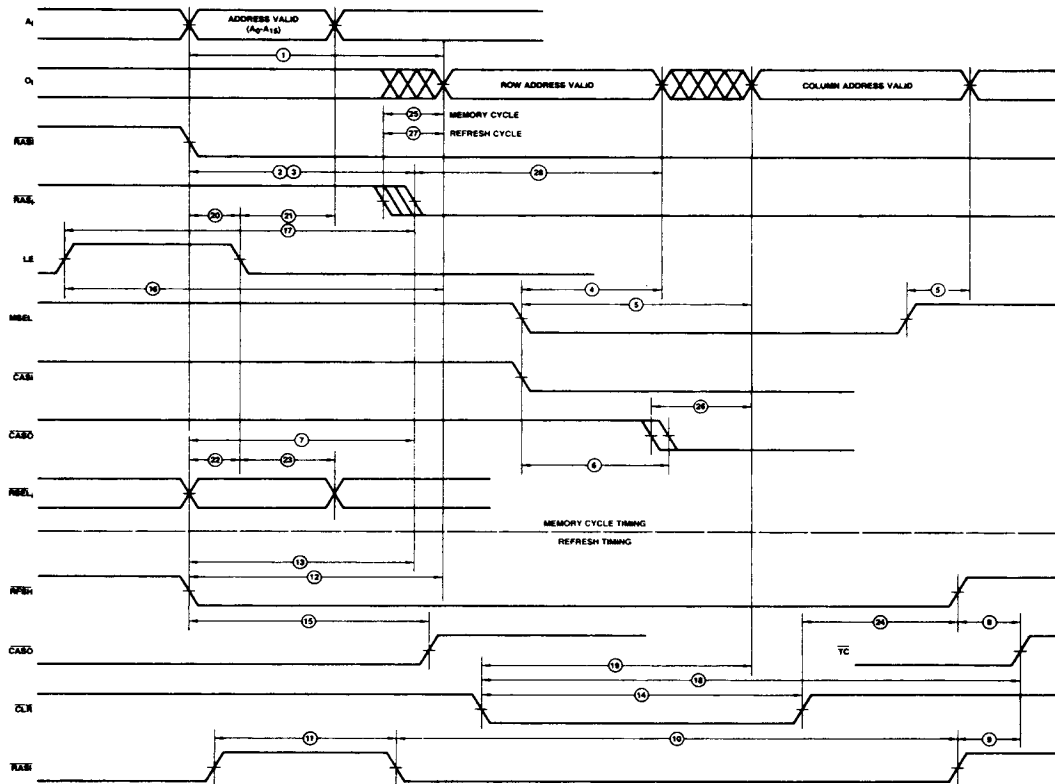
Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable

may allow the ground pin at the device to rise by 100s of millivolts momentarily.

4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures.



WF001990

Am2964B Dynamic Memory Controller Timing

MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 3. T_1 , T_2 and T_3 represent the minimum timing requirements at the DMC inputs to guarantee that RAM timing requirements are met and that maximum system performance is achieved.

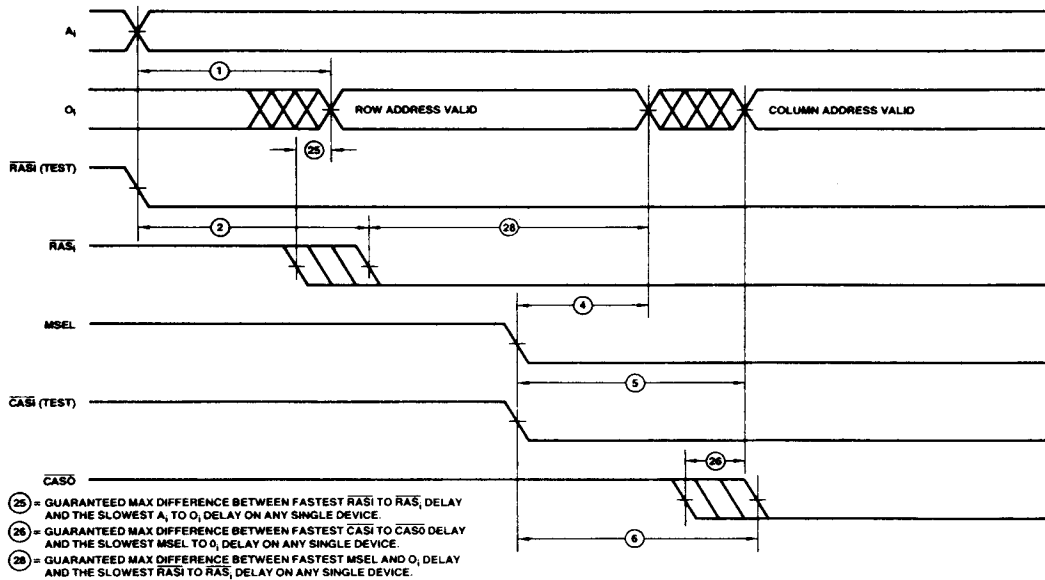
The minimum requirement for T_1 , T_2 and T_3 are as follows:

$$T_1 \text{ MIN} = t_{\text{RAH}} + t_{28}$$

$$T_2 \text{ MIN} = T_1 + t_{26} + t_{\text{ASC}}$$

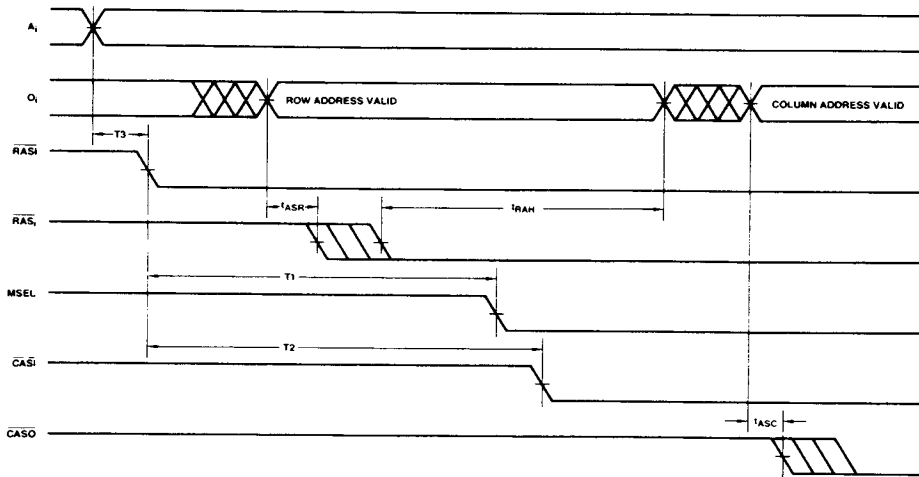
$$T_3 \text{ MIN} = t_{\text{ASR}} + t_{25}$$

See RAM data sheet for applicable values for t_{RAH} , t_{ASC} and t_{ASR} .



WF001920

a. Specifications Applicable to Memory Cycle Timing

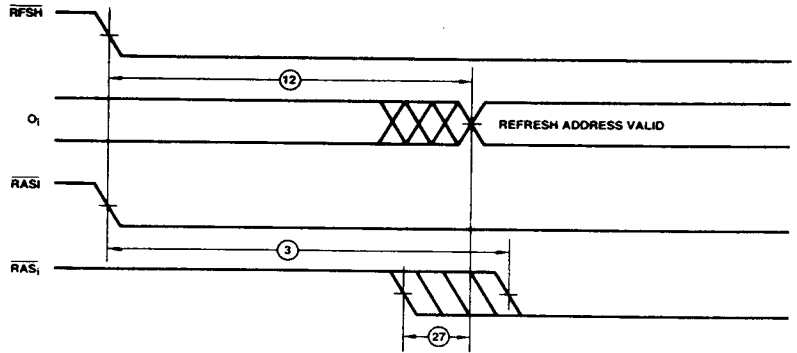


WF001930

b. Desired System Timing Figure 3. Memory Cycle Timing

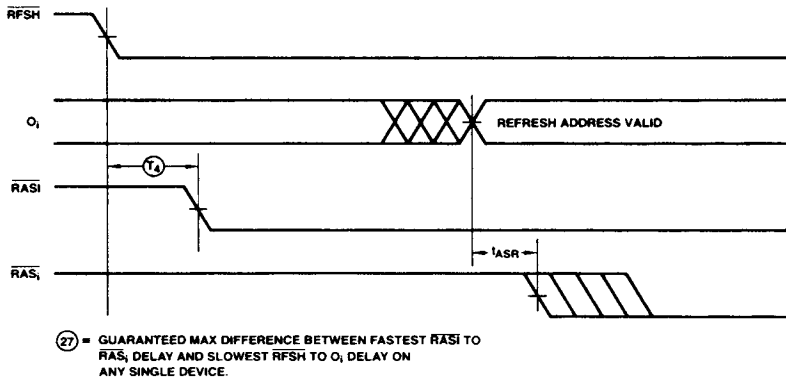
REFRESH CYCLE TIMING

The timing relationships for refresh are shown in Figure 4.
 T_4 minimum is calculated as follows: $T_4 = t_{ASR} + t_{27}$



WF001940

a. Test Waveforms



WF001880

b. Desired System Timing

Figure 4. Refresh Timing