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AK4145

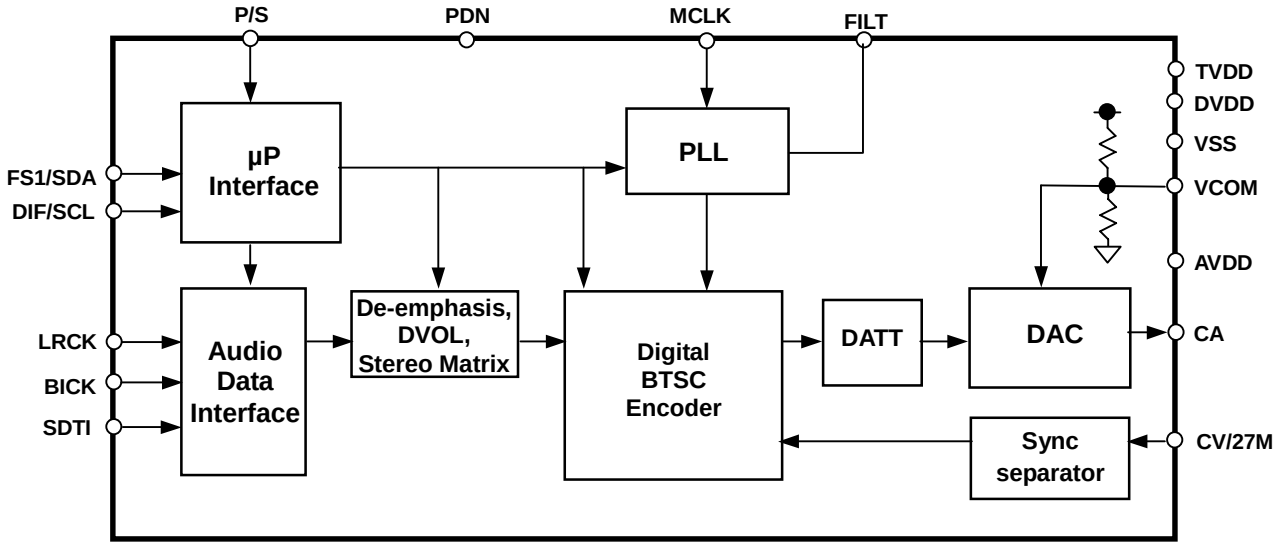
Digital BTSC Stereo Encoder

GENERAL DESCRIPTION

The AK4145 is a BTSC Encoder with D/A Converter, which is optimized for Digital AV application. The AK4145 achieves high audio performance using the digital BTSC encoding architecture requires no alignment of external parts. The AK4145 supports major audio data formats (MSB justified, I^2S, TDM) to interface with usual DSP. Therefore, the AK4145 is suitable for the systems such as Digital STB/TV, digital recorder.

FEATURES

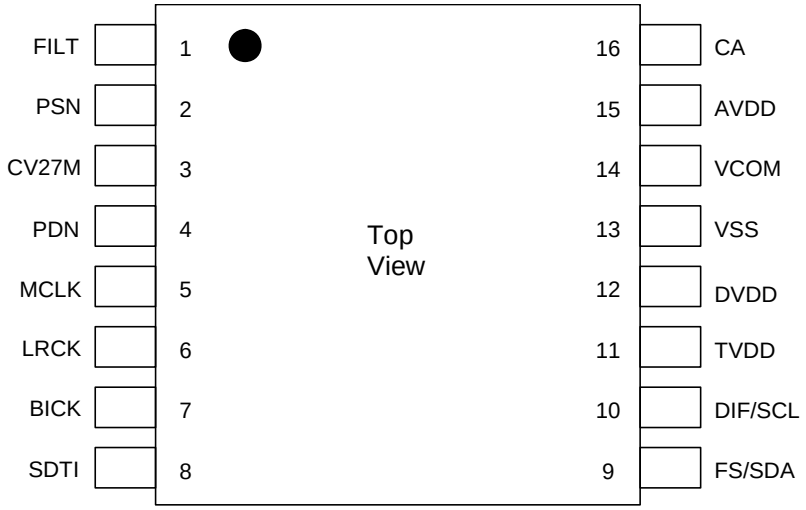
- ☐ **Alignment Free Digital BTSC Stereo Encoding**
- ☐ **Base band Composite Audio Output (Mono/Stereo)**
- ☐ **Digital Volume for Composite Audio Output**
- ☐ **Digital De-emphasis filter (32k/44.1k/48kHz)**
- ☐ **Stereo Digital Volume Control for Audio Input Data**
- ☐ **Soft Mute**
- ☐ **Sampling Rate (fs): 32k/44.1k/48kHz**
- ☐ **Master Clock: 256fs/384fs/512fs/768fs**
- ☐ **I/F format: 24-Bit MSB justified, 24/20/16-Bit LSB justified or I^2S**
- ☐ **Control: Standalone/I^2C-bus Selectable**
- ☐ **Video Input for Pilot Synchronization**
- ☐ **S/(N+D): 0.01%**
- ☐ **S/N: 82dB**
- ☐ **Channel Separation: 47dB**
- ☐ **Power Supply: 1.7V ~ 1.9V, 2.7 ~ 3.6V**
- ☐ **Ta: -20 ~ 85°C**



■ Ordering Guide

AK4145ET	-20 ~ +85°C	16pinTSSOP
AKD4145	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	FILT	-	Filter Pin, 4.7nF should be connected between FILT pin and VSS pin.
2	PSN	I	Parallel/Serial Select Pin (Internal pull-up pin) "L": Serial control mode, "H": Parallel control mode
3	CV27M	I	Composite Video or 27MHz Signal Input Pin.
4	PDN	I	Power-Down Mode Pin When at "L", the AK4145 is in the power-down mode and is held in reset. The AK4145 must be reset once upon power-up.
5	MCLK	I	Master Clock Input Pin
6	LRCK	I	Channel Clock Input Pin
7	BICK	I	Audio Serial Data Clock Input Pin
8	SDTI	I	Audio Serial Data Input Pin
9	FS	I	Sampling Rate Control Pin in parallel control mode
	SDA	I/O	Control Data Pin in serial control mode
10	DIF	I	Audio Data Interface Format Pin in parallel control mode
	SCL	I	Control Data Clock Pin in serial control mode
11	TVDD	-	Digital I/O Power Supply Pin, DVDD(min:1.7V) ~ 3.6V
12	DVDD	-	Digital Power Supply Pin, 1.7 ~ 1.9V
13	VSS	-	Ground Pin
14	VCOM	O	Common Voltage Pin, AVDD/2 Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
15	AVDD	-	Analog Power Supply Pin, 2.7 ~ 3.6V
16	CA	O	Baseband Composite Audio Output Pin

Note: All input pins except pull-up pin should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	CV	Connect to VSS.
Digital	FS(Parallel mode), DIF(Parallel mode)	Connect to VDD or VSS.

■ Output Status at PDN pin = "L"

Below is the output status of each output pin when the PDN pin = "L".

Pin#	Pin Name	Status
1	FILT	VSS
9	SDA	Hi-Z
14	VCOM	VSS
16	CA	VCOM(=VSS)

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	AVDD	-0.3	4.3	V
	DVDD	-0.3	2.4	V
	TVDD	-0.3	4.3	V
Input Current, Any Pin Except Supply	IIN	-	±10	mA
Input Voltage (All input pins)	VIND	-0.3	TVDD+0.3	V
Ambient Temperature (powered applied)	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. PSN, CV27M, PDN, MCLK, LRCK, BICK, SDTI, FS/SDA, DIF/SCL pin

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	AVDD	2.7	3.3	3.6	V
	DVDD	1.7	1.8	1.9	V
	TVDD	DVDD	3.3	3.6	V

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=TVDD=3.3V; DVDD=1.8V; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=50Hz ~ 13kHz; unless otherwise specified)

Parameter			min	typ	max	Units
Resolution					16	Bits
Composite Audio Output Characteristics						
	Output Voltage			2.2		Vp-p
	Load Resistance	(Note 4)	5			kΩ
	Load Capacitance				25	pF
BTSC Encoder Characteristics (Note 5)						
	S/(N+D)	Mono (1kHz, 100%EIM)		0.01	TBD	%
		Stereo (1kHz, 100%EIM. L or R)		0.01	TBD	%
	S/N (A-weighted)	Mono (input off)	75	82		dB
		Stereo (input off)	75	82		dB
	Stereo Separation	1kHz		47		dB
		20Hz~500Hz	30			dB
		500Hz~5kHz	27			dB
		5kHz~13kHz	23			dB
	Frequency response	Mono (20~13kHz)	-1		1	dB
		Stereo (20~13kHz)	-1		1	dB
Video Sync Input Characteristics						
	Video Input Sync Level		100			mVp-p
	Video Input Impedance			1		MΩ
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H"):						
AVDD				13	TBD	mA
DVDD				8	TBD	mA
TVDD				0.1	TBD	mA
Power down mode (PDN pin = "L"): (Note 3)						
AVDD				10	100	μA
DVDD				10	100	μA
TVDD				10	100	μA

Note 3. All digital input pins are held to VSS.

Note 4. AC-load.

Note 5. Received by the Belar TVM230 (BTSC Decoder) and measured by the Audio Precision (System Two). Refer to the evaluation board manual.

DC CHARACTERISTICS

(Ta=-20~ 85°C; AVDD=TVDD=1.7~3.6V, DVDD=1.7~1.9V)

Parameter	Symbol	min	typ	Max	Units
High-Level Input Voltage					
TVDD < 2.7V	VIH	80%TVDD	-	-	V
TVDD ≥ 2.7V	VIH	70%TVDD	-	-	V
Low-Level Input Voltage					
TVDD < 2.7V	VIL	-	-	20%TVDD	V
TVDD ≥ 2.7V	VIL	-	-	30%TVDD	V
Low-Level Output Voltage (SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	± 10	μA

SWITCHING CHARACTERISTICS

(Ta=-20~ 85°C; AVDD=2.7 ~ 3.6V, TVDD=1.7~3.6V, DVDD=1. 7~1.9V)

Parameter		Symbol	min	typ	max	Units
Master Clock Frequency		fCLK	8.192		36.8640	MHz
Duty Cycle		dCLK	40		60	%
LRCK Frequency		fs	32		48	kHz
Duty Cycle		Duty	45		55	%
Audio Interface Timing						
BICK Period		tBCK	1/128fs			ns
BICK Pulse Width Low		tBCKL	30			ns
Pulse Width High		tBCKH	30			ns
BICK rising to LRCK Edge	(Note 6)	tBLR	20			ns
LRCK Edge to BICK rising	(Note 6)	tLRB	20			ns
SDTI Hold Time		tSDH	20			ns
SDTI Setup Time		tSDS	20			ns
Control Interface Timing (I^2C Bus)						
SCL Clock Frequency		fSCL	-		400	kHz
Bus Free Time Between Transmissions		tBUF	1.3		-	μs
Start Condition Hold Time (prior to first clock pulse)		tHD:STA	0.6		-	μs
Clock Low Time		tLOW	1.3		-	μs
Clock High Time		tHIGH	0.6		-	μs
Setup Time for Repeated Start Condition		tSU:STA	0.6		-	μs
SDA Hold Time from SCL Falling	(Note 7)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising		tSU:DAT	0.1		-	μs
Rise Time of Both SDA and SCL Lines		tR	-		0.3	μs
Fall Time of Both SDA and SCL Lines		tF	-		0.3	μs
Setup Time for Stop Condition		tSU:STO	0.6		-	μs
Pulse Width of Spike Noise Suppressed by Input Filter		tSP	-		50	ns
Capacitive load on bus		Cb	0		400	pF
Reset Timing						
PDN Pulse Width	(Note 8)	tPD	150			ns

Note 6. BICK rising edge must not occur at the same time as LRCK edge.
Note 7. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 8. The AK4145 can be reset by bringing the PDN pin = "L".
Note 9. I^2C is a registered trademark of Philips Semiconductors.

■ Timing Diagram

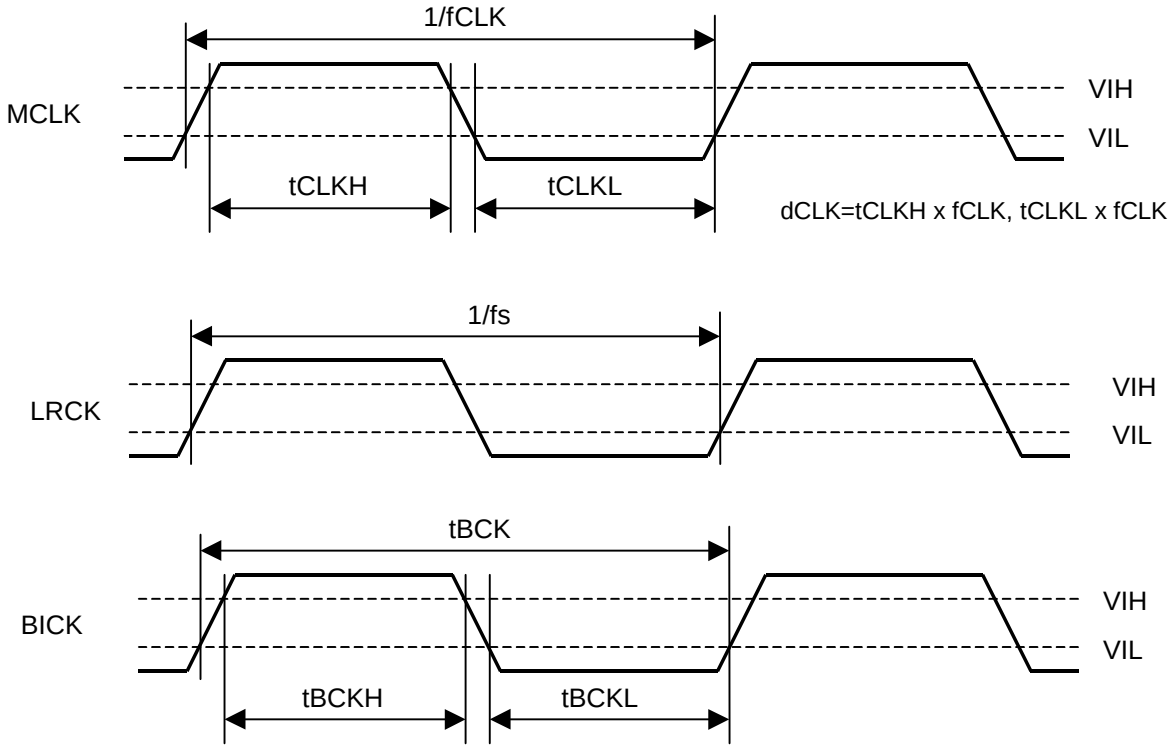


Figure 1. Clock Timing

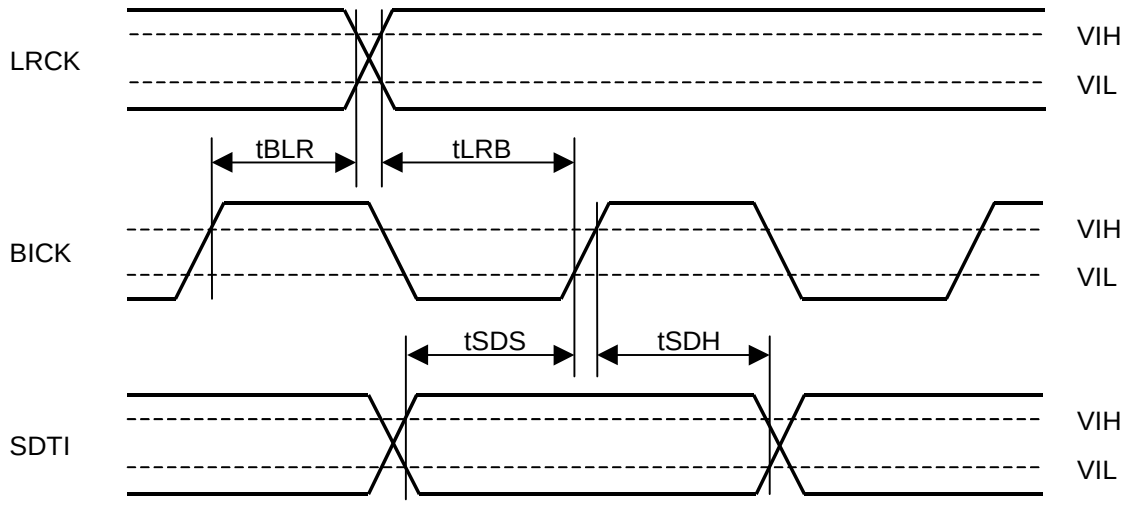


Figure 2. Serial Interface Timing

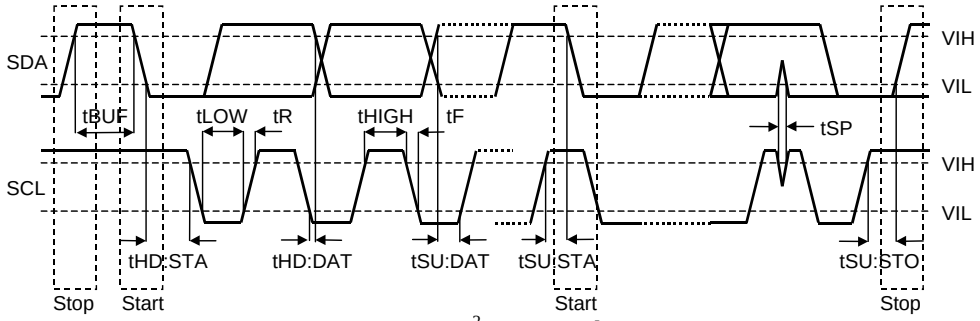


Figure 3. I^{2}C Bus mode Timing

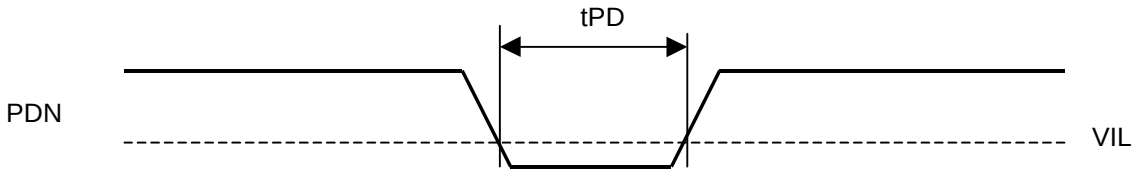
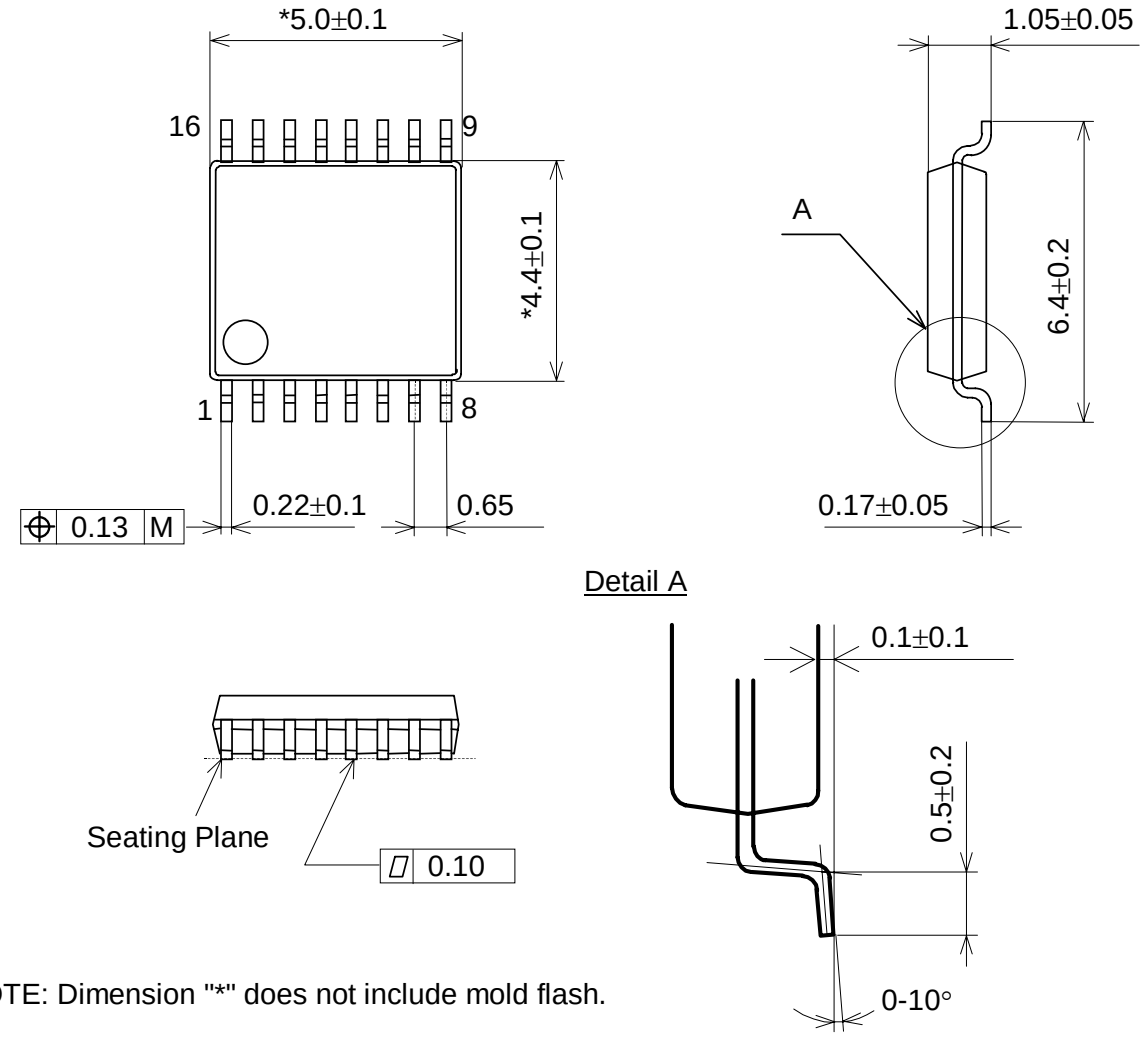


Figure 4. Power-down Timing

PACKAGE

16pin TSSOP (Unit: mm)

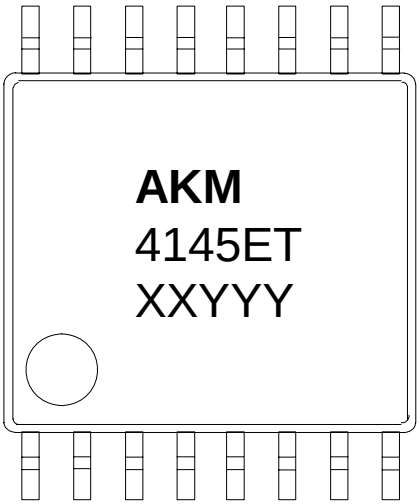


NOTE: Dimension "*" does not include mold flash.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate (Pb Free)

MARKING



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code : 4145ET
4) Asahi Kasei Logo

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More detail product informations are available, please contact our sales office or authorized distributors.