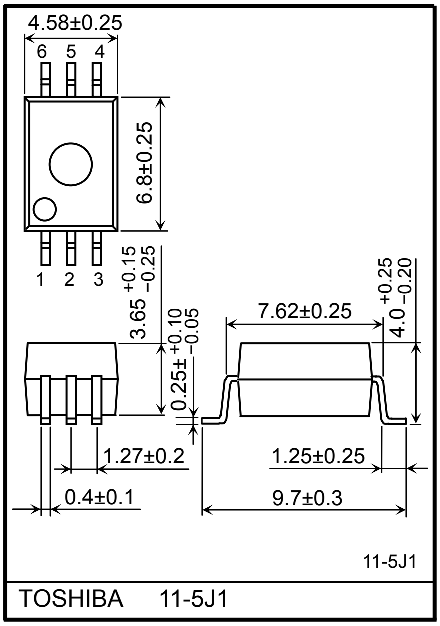
TOSHIBA PHOTOCOUPLER GaAℓAs IRED & PHOTO-IC

TLP702

Intelligent power module signal isolation
Industrial inverters
Motor drive

Unit in mm



Weight:0.26 g (typ.)

The Toshiba TLP702 consists of a GaAℓAs light-emitting diode and an integrated high-gain, high-speed photodetector. The TLP702 is suitable for isolating input control signals to intelligent power modules. This unit is a 6-pin SDIP. The TLP702 is 50% smaller than the 8-PIN DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

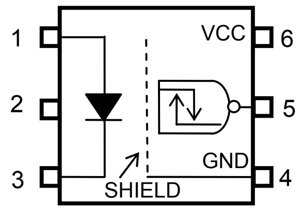
The detector has a totem pole output stage to provide both source and sink driving. The detector IC has an internal shield that provides a guaranteed common-mode transient immunity of 10 kV/μs.

The TLP702 is inverter logic type. For buffer logic type, the TLP706 is in line-up.

- Inverter logic type (totem pole output)
- Guaranteed performance over temperature : −40~100°C
- Power supply voltage : 4.5~20 V
- Input current: I_{FHL} = 5 mA (Max.)
- Switching time (t_{pHL} / t_{pLH}) : 600 ns (Max.)
- Common-mode transient immunity : ±10 kV/μs (Min)
- Isolation voltage : 5000 Vrms (Min)
- UL Recognized :UL1577, File No.E67349
- Option (D4)
  TÜV Approved : DIN EN60747-5-2
  No.R50033433
  Maximum Operating Insulation Voltage : 890V_{PK}
  Highest Permissible Over Voltage : 8000V_{PK}
  (Note) : When a EN60747-5-2 approved type is needed, Please designate “Option(D4)”
- Construction Mechanical Rating

	7.62 mm pich standard type	10.16 mm pich TLPXXXF type
Creepage Distance	7.0 mm (Min)	8.0 mm (Min)
Clearance	7.0 mm (Min)	8.0 mm (Min)
Insulation Thickness	0.4 mm (Min)	0.4 mm (Min)

Pin Configuration (Top View)

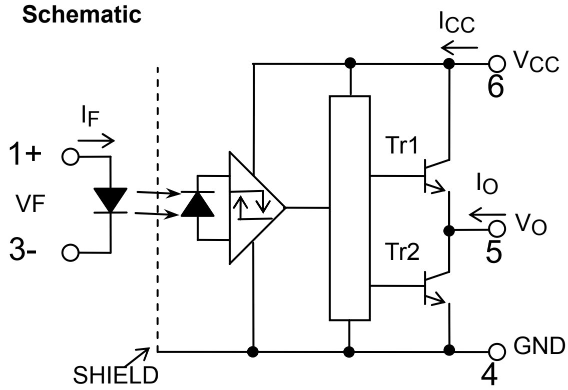


1:ANODE
2:N.C.
3:CATHODE
4:GND
5:Vo
6:Vcc

Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

Schematic



0.1 μF bypass capacitor must be connected between pins 6 and 4. (Note 4)

Absolute Maximum Ratings (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Ta ≤ 85°C)	I_F	20	mA
	Forward Current Derating (Ta > 85°C)	$\Delta I_F/\Delta Ta$	−0.5	mA/°C
	Peak Transient Forward Current (Note 1)	I_{FPT}	1	A
	Reverse Voltage	V_R	5	V
	Junction Temperature	Tj	125	°C
DETECTOR	Output Current 1 (Ta ≤ 25°C)	I_{O1}	15/−15	mA
	Output Current 2 (Ta ≤ 100°C)	I_{O2}	4.5/−4.5	mA
	Peak Output Current	I_{OP}	20/−20	mA
	Output Voltage	V_O	−0.5~20	V
	Supply Voltage	V_{CC}	−0.5~20	V
	Junction Temperature	Tj	125	°C
Operating Temperature Range		Topr	−40~100	°C
Storage Temperature Range		Tstg	−55~125	°C
Lead Solder Temperature (10 s)		Tsol	260	°C
Isolation Voltage (AC,1 min., R.H. ≤ 60%, Ta = 25°C) (Note 2)		BVs	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current, ON	$I_{F\ (ON)}$	7	−	12	mA
Input Voltage, OFF	$V_{F\ (OFF)}$	0	−	0.8	V
Supply Voltage (*) (Note 3, Note 4)	V_{CC}	4.5	−	20	V

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

(*) This item denotes operating ranges, not meaning of recommended operating conditions.

Note 1: Pulse width PW≤1us,300pps.

Note 2: Device Considered a two terminal device : pins 1,2 and 3 shorted together and pins 4,5 and 6 shorted together.

Note 3: The detector of this product requires a power supply voltage (VCC) of 4.5 V or higher for stable operation.
If the VCC is lower than this value, an output may be unstable. Be sure to use the product after checking the supply current, and the operation of a power−on/−off.

Note 4: A ceramic capacitor(0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Electrical Characteristics
(Unless otherwise specified, Ta =−40~100°C, Vcc = 4.5~20 V.)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN.	TYP. *	MAX.	UNIT
Input forward voltage	V_F	—	I_F = 5 mA , Ta = 25°C	—	1.6	1.7	V
Temperature coefficient of forward voltage	$\Delta V_F/\Delta Ta$	—	I_F = 5 mA	—	−2.0	—	mV/°C
Input reverse current	I_R	—	V_R = 5 V , Ta = 25°C	—	—	10	μA
Input capacitance	C_T	—	V = 0 V, f = 1 MHz, Ta = 25°C	—	30	—	pF
Logic LOW output voltage	V_{OL}	1	I_{OL} = 3.5 mA , I_F = 5 mA	—	0.1	0.35	V
Logic HIGH output voltage	V_{OH}	2	I_{OH} = −3.5 mA, VF = 0.8 V; V_{CC} = 5 V	2.4	3.1	—	V
			I_{OH} = −3.5 mA, VF = 0.8 V; V_{CC} = 20 V	17.4	18.1	—	
Logic LOW supply current	I_{CCL}	3	I_F = 5 mA; V_{CC} = 20 V, Ta =−40~100°C	—	4.0	6.0	mA
			I_F = 5 mA; V_{CC} = 5 V, Ta = 25°C	—	3.6	4.5	
Logic HIGH supply current	I_{CCH}	4	V_F=0V; V_{CC} = 20 V, Ta =−40~100°C	—	3.1	6.0	mA
			V_F=0V; V_{CC} = 5 V, Ta = 25°C	—	2.8	4.5	
Logic LOW short circuit output current	I_{OSL}	5	I_F = 5 mA, V_{CC} = V_O = 20 V	7	37	—	mA
Logic HIGH short circuit output current	I_{OSH}	6	V_F = 0 V, V_O = GND, V_{CC} = 20 V	−7	-40	—	mA
Input current logic LOW output	I_{FHL}	—	I_O = 3.5 mA, V_O < 0.4 V	—	0.5	5	mA
Input voltage logic HIGH output	V_{FLH}	—	I_O = −3.5 mA, V_O > 2.4V, V_{CC} = 5 V	0.8	—	—	V
Input current hysteresis	I_{HYS}	—	V_{CC} = 5 V	—	0.05	—	mA

*All typical values are at Ta = 25°C.

Isolation Characteristics (Ta = 25°C)

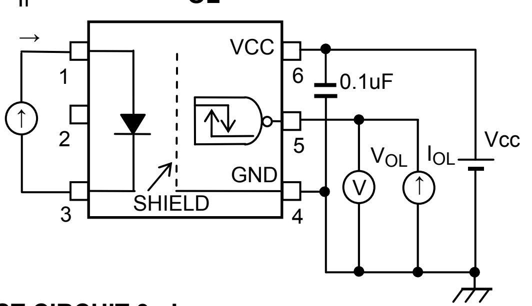
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Capacitance input to output	C_S	V = 0V, f = 1 MHz (Note 2)	—	1.0	—	pF
Isolation resistance	R_S	R.H. ≤ 60%, V_S = 500 V (Note 2)	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 1 minute	5000	—	—	V_{rms}
		AC, 1 second, in oil	—	10000	—	Vdc
		DC, 1 minute, in oil	—	10000	—	

Switching Characteristics
(Unless otherwise specified, Ta = −40~100°C,Vcc = 4.5~20 V.)

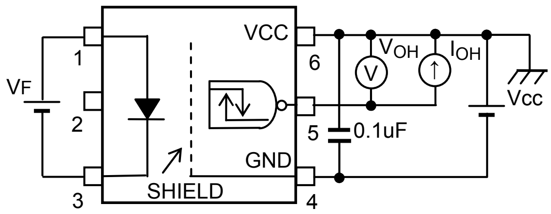
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN.	TYP. *	MAX.	UNIT
Propagation delay time to logic LOW output	t_{pHL}		I_F = 0→5 mA, C_L = 100 pF V_{CC} = 20 V	50	250	600	ns
Propagation delay time to logic HIGH output	t_{pLH}		I_F = 5→0 mA, C_L = 100 pF V_{CC} = 20 V	50	260	600	ns
Switching time dispersion Between ON and OFF	$\|t_{pLH}-t_{pHL}\|$	7	I_F = 0⇔5 mA, C_L = 100 pF V_{CC} = 20 V	—	—	550	ns
Output fall time	tf		I_F = 0→5 mA, V_{CC} = 20 V	—	95	—	ns
Output rise time	tr		I_F = 5→0 mA, V_{CC} = 20 V	—	175	—	ns
Propagation delay time to logic LOW output	t_{pHL}	8	I_F = 0→5 mA	50	—	600	ns
Propagation delay time to logic HIGH output	t_{pLH}		I_F = 5→0 mA	50	—	600	ns
Common-mode transient Immunity at HIGH level output	CM_H	9	V_{CM} = 1000 Vp-p, I_F = 0 mA, V_{CC} = 20 V, Ta = 25°C	10000	—	—	V/us
Common-mode transient Immunity at LOW level output	CM_L		V_{CM} = 1000 Vp-p, I_F = 5 mA, V_{CC} = 20 V, Ta = 25°C	−10000	—	—	V/us

*All typical values are at Ta = 25°C.

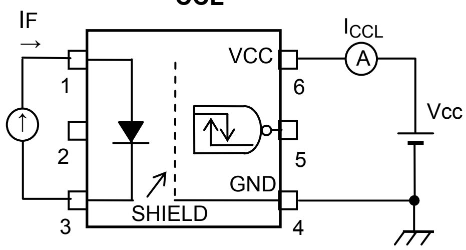
TEST CIRCUIT 1 : V_{OL}



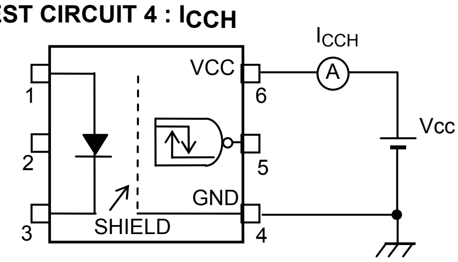
TEST CIRCUIT 2 : V_{OH}



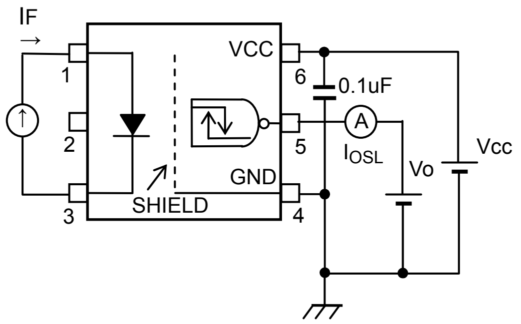
TEST CIRCUIT 3 : I_{CCL}



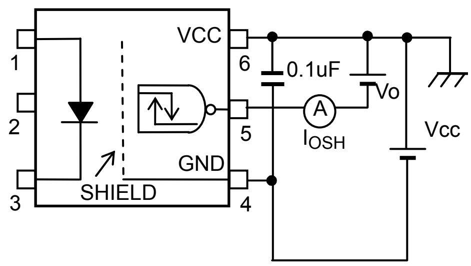
TEST CIRCUIT 4 : I_{CCH}



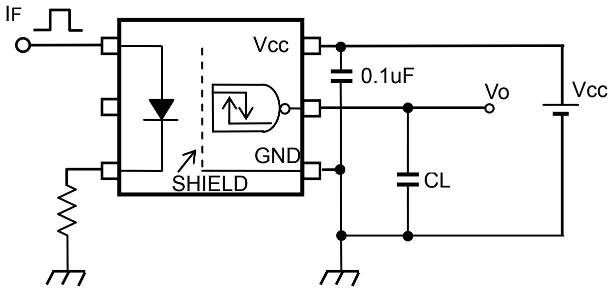
TEST CIRCUIT 5 : I_{OSL}

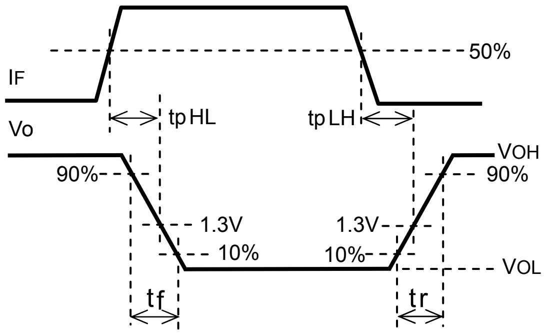


TEST CIRCUIT 6 : I_{OSH}



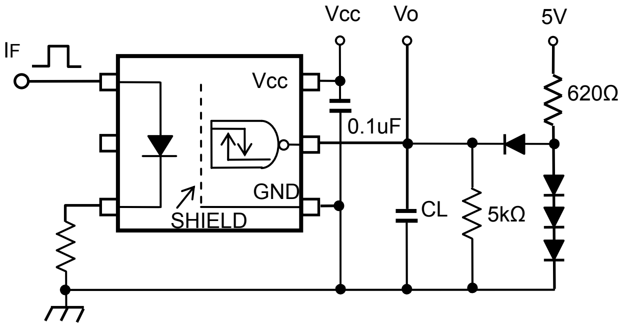
TEST CIRCUIT 7: Switching Time Test Circuit

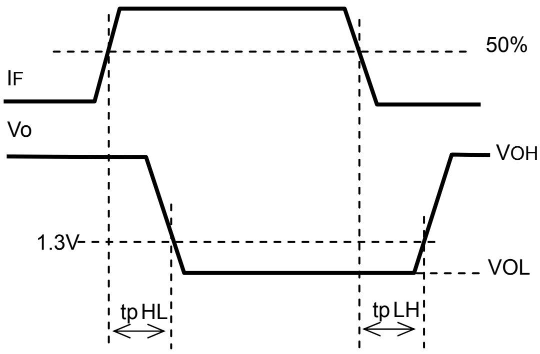




CL: total capacitance

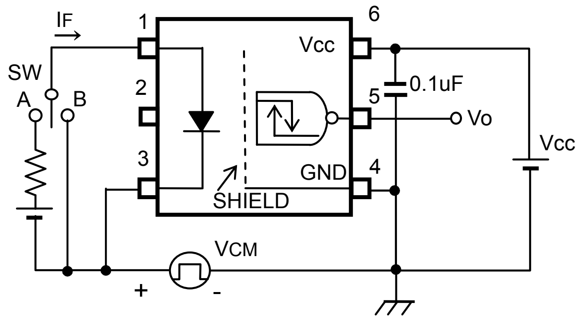
TEST CIRCUIT 8: Switching Time Test Circuit

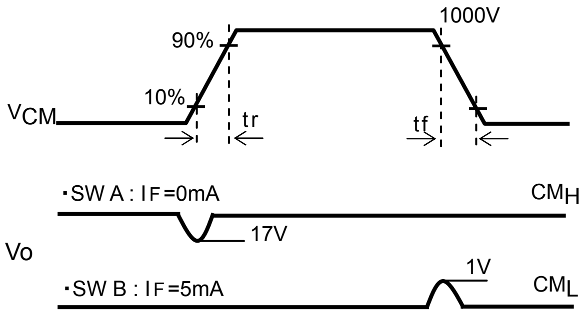




CL: stray capacitance of probe and wiring (to 15 pF)

TEST CIRCUIT 9: Common-Mode Transient Immunity Test Circuit





$$CM_H = \frac{800(V)}{t_r(\mu s)} \qquad CM_L = -\frac{800(V)}{t_f(\mu s)}$$

CM_H (CM_L) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the high (low) state.

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