19-0402; Rev 0; 6/95

EVALUATION KIT AVAILABLE

330MHz Buffered Video Switches/ Crosspoint Building Blocks

General Description

The MAX4111/MAX4121/MAX4221 wideband video switches are optimized for high-definition, broadcast-quality, composite (HDTV, NTSC, PAL, SECAM, and RGB) video switching arrays. Their open-loop buffer amplifiers offer 0.1dB gain flatness to 150MHz. They operate from ±5V supplies and feature differential phase and gain error of only 0.01°/0.01%, respectively. The ultra-low switching glitch (13mV) is positive to avoid confusion with any sync pulse.

Ideal as building blocks in large arrays, these devices feature a constant, high input impedance and a disable function that puts the outputs into a high-impedance state and reduces the operating current to only 250µA. The open-loop architecture allows the outputs to drive capacitive loads without oscillation. Other key features include -92dB crosstalk and -78dB isolation (MAX4121).

The MAX4111/MAX4121/MAX4221 are offered in narrow plastic DIP and SO packages. See the table below for key features:

PART	DESCRIPTION	PINS
MAX4111	SPST, single-input, single-output switch	8
MAX4121	SPDT, 2-input, single-output switch	8
MAX4221	Dual, SPDT, 2-input, single-output switch	16

Applications

Video-Router and Crosspoint Arrays
Broadcast/HDTV-Quality Color Signal Multiplexing
RF and IF Routing
Graphics Color-Signal Routing
Telecom Routing
Data Acquisition

Features

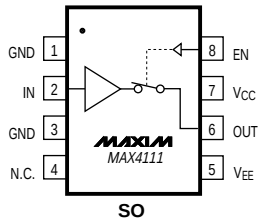
- **-3dB Bandwidth of 330MHz**
- **0.1dB Gain Flatness of 150MHz**
- **700V/µs Slew Rate**
- **0.01°/0.01% Differential Phase/Gain**
- **Low Power: 5.5mA Max**
- **-92dB Crosstalk and -78dB Off Isolation at 30MHz**
- **High-Z Outputs when Disabled**
- **3pF Input Capacitance**
- **Ultra-Low Switching Glitch**
- **On-Board Control Logic**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4111CSA	0°C to +70°C	8 SO
MAX4121CSA	0°C to +70°C	8 SO
MAX4221CSE	0°C to +70°C	16 Narrow SO

Pin Configurations/Functional Diagrams

TOP VIEW



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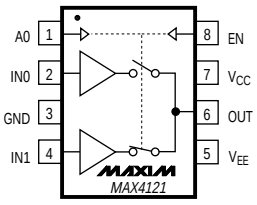

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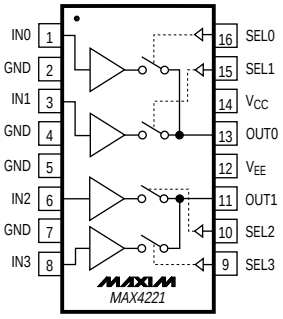


Narrow SO

330MHz Buffered Video Switches/ Crosspoint Building Blocks

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{CC} .....+6V
- V_{EE} .....-6V
- V_{CC}-V_{EE} .....+12V

Analog Input Voltage .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Digital Input Voltage.....-0.3V to (V_{CC} + 0.3V)
Duration of Short Circuit to Ground.....Continuous

Continuous Power Dissipation (T_A = +70°C)
- 8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
- 16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ...696mW

Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-65°C to +160°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±5V, -2.5V ≤ V_{IN} ≤ +2.5V, R_L = 5kΩ, C_L ≤ 5pF, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PARAMETERS							
Operating Supply Voltage	V_S			±4.5	±5.0	±5.5	V
Operating Supply Current	I_{CC}, I_{EE}	Per channel	T_A = +25°C		4.0	5.5	mA
			T_A = T_{MIN} to T_{MAX}			6.5	
Disabled Supply Current	I_{CC}, I_{EE}	MAX4111/MAX4121			150	200	µA
		MAX4221			250	350	
Input Voltage Range	V_{IN}			±2.5			V
Input Bias Current	I_B	V_{IN} = 0V	Channel selected		±2.5	±4.0	µA
			Channel disabled		±0.02		
Input Resistance	R_{IN}	Channel selected			0.4		MΩ
		Channel disabled			100		
Input Capacitance	C_{IN}	V_{IN} = 0V, channel enabled or disabled			3		pF
Output Offset Voltage	V_{OS}	T_A = +25°C			±5	±10	mV
		T_A = T_{MIN} to T_{MAX}				±15	
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V		50			dB
Voltage Gain	A_V	V_{IN} = ±2.5V	T_A = +25°C	0.98		1.0	V/V
			T_A = T_{MIN} to T_{MAX}	0.97		1.0	
Output Resistance	R_{OUT}	f = DC to 50MHz			20		Ω
Disabled Output Current	$I_{OUT(OFF)}$	V_{OUT} = 0V			10		nA
Disabled Output Resistance	$R_{OUT(OFF)}$				30		MΩ
Disabled Output Capacitance	$C_{OUT(OFF)}$				5		pF
Logic Input High Voltage	V_{INH}	V_S = ±4.5V to ±5.5V		2.0			V
Logic Input Low Voltage	V_{INL}	V_S = ±4.5V to ±5.5V				0.8	V
Logic Input High Current	I_{INH}	V_S = ±4.5V to ±5.5V				10	µA
Logic Input Low Current	I_{INL}	V_S = ±4.5V to ±5.5V				10	µA

ELECTRICAL CHARACTERISTICS

(V_S = ±5V, -2.5V ≤ V_{IN} ≤ +2.5V, R_L = 5kΩ, C_L ≤ 5pF, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC PARAMETERS							
Slew Rate	SR	V_{OUT} = 5Vp-p			700		V/µs
		V_{OUT} = 1.4Vp-p			500		
Full-Power Bandwidth (Note 1)	FPBW	V_{IN} = 1.4Vp-p			110		MHz
		V_{IN} = 5Vp-p			45		
-3dB Bandwidth	f_{3dB}	V_{IN} = 0.1Vp-p			330		MHz
Gain Flatness		DC to 30MHz			0.02		dB
		DC to 150MHz			0.1		
Gain Peaking					0.08		dB
Small-Signal Rise Time	t_r/t_f	V_{IN} = 0.1Vp-p			950		ps
Differential Gain (Note 2)	DG	f = 3.58MHz			0.01		%
Differential Phase (Note 2)	DP	f = 3.58MHz			0.01		degrees
All-Hostile Crosstalk		V_{IN} = 1Vp-p, f = 30MHz	MAX4121		-92		dB
			MAX4221		-70		
Off Isolation		V_{IN} = 1Vp-p, f = 30MHz, see test circuit	MAX4111		86		dB
			MAX4121		78		
			MAX4221		84		
Channel Switching Off Time	t_{OFF}				1.0		µs
Channel Switching On Time	t_{ON}				500		ns
Switching Transient					13		mVp-p
Group Delay					860		ps
Input-Output Delay Matching		Chip-to-chip, f = 3.58MHz			±0.2		degrees
Second Harmonic		f = 30MHz, V_{IN} = 1.4Vp-p			-65		dBc
Third Harmonic		f = 30MHz, V_{IN} = 1.4Vp-p			-70		dBc

Note 1: Full-Power Bandwidth is inferred from Slew Rate (SR) testing by the equation SR = ωE_P, where E_P is the peak output voltage and $\omega = 2\pi f$.

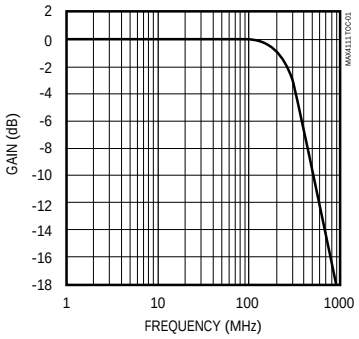
Note 2: Differential Gain and Phase are tested using a modulated ramp, 100IRE (0.714V).

330MHz Buffered Video Switches/ Crosspoint Building Blocks

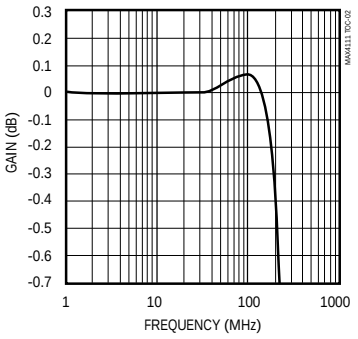
Typical Operating Characteristics

(V_S = ±5V, R_L = 5kΩ, C_L ≤ 5pF, T_A = +25°C, unless otherwise noted.)

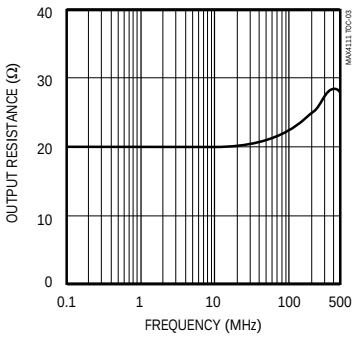
GAIN vs. FREQUENCY



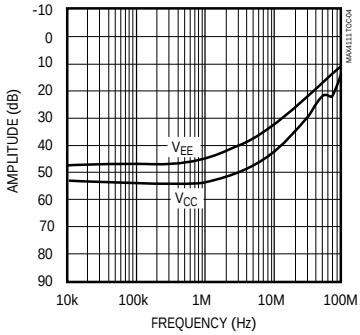
GAIN FLATNESS



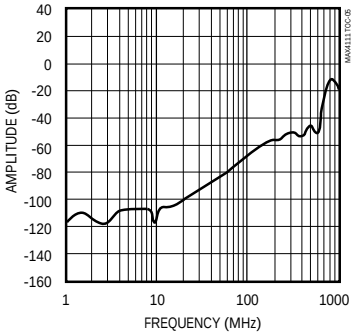
OUTPUT RESISTANCE vs. FREQUENCY



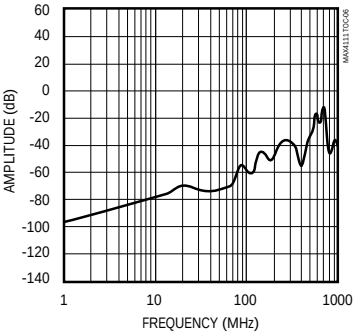
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



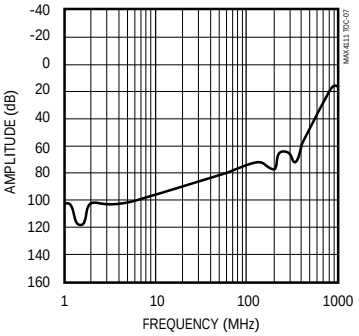
MAX4121 ALL-HOSTILE CROSSTALK vs. FREQUENCY



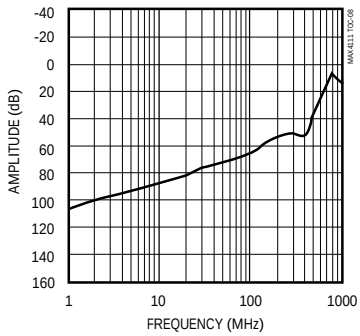
MAX4221 ALL-HOSTILE CROSSTALK vs. FREQUENCY



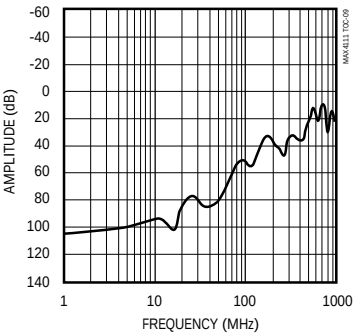
MAX4111 OFF ISOLATION vs. FREQUENCY



MAX4121 OFF ISOLATION vs. FREQUENCY



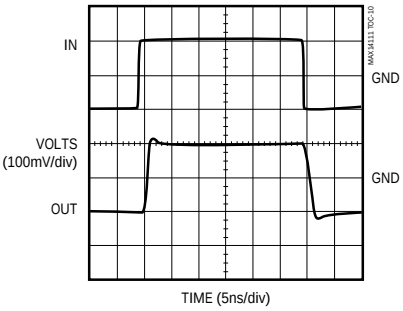
MAX4221 OFF ISOLATION vs. FREQUENCY



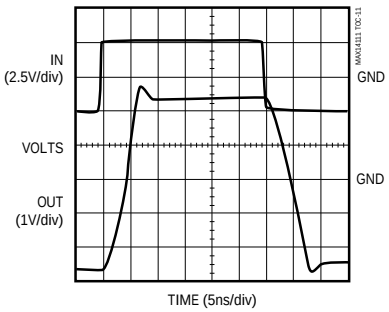
Typical Operating Characteristics (continued)

(V_S = ±5V, R_L = 5kΩ, C_L ≤ 5pF, T_A = +25°C, unless otherwise noted.)

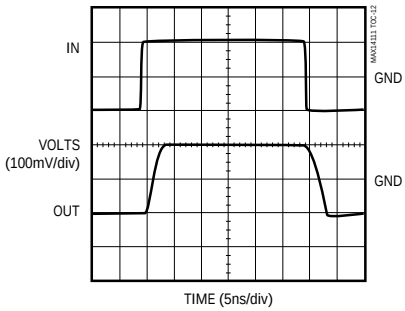
SMALL-SIGNAL PULSE RESPONSE
(R_L = 5kΩ)



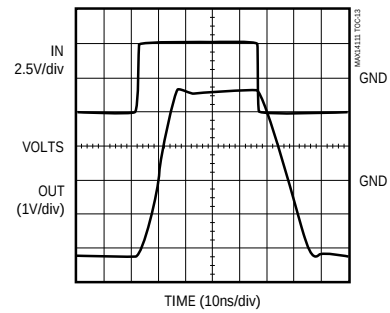
LARGE-SIGNAL PULSE RESPONSE
(R_L = 5kΩ)



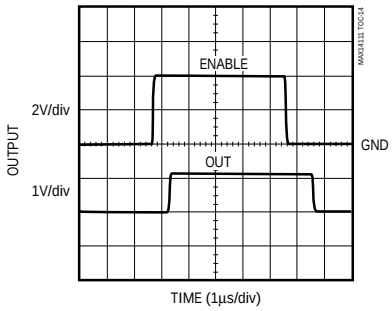
SMALL-SIGNAL PULSE RESPONSE
(C_L = 47pF, R_L = open)



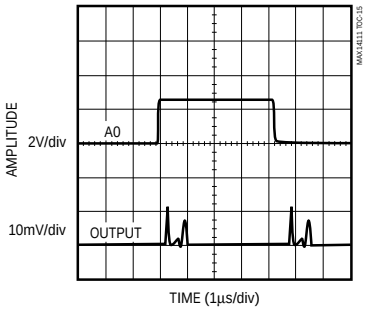
LARGE-SIGNAL PULSE RESPONSE
(C_L = 47pF, R_L = open)



ENABLE/DISABLE DELAY TIME
(INPUT = 1.1V)



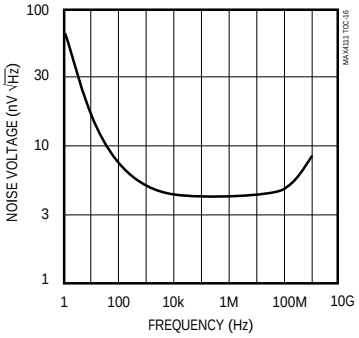
OUTPUT GLITCH AMPLITUDE



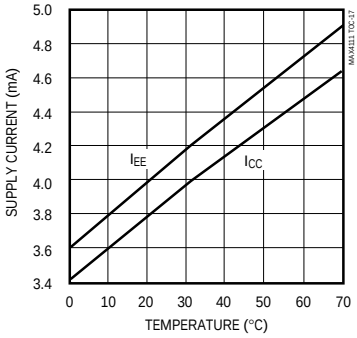
Typical Operating Characteristics (continued)

(V_S = ±5V, R_L = 5kΩ, C_L ≤ 5pF, T_A = +25°C, unless otherwise noted.)

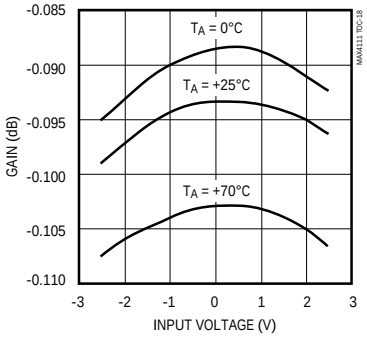
NOISE VOLTAGE vs. FREQUENCY



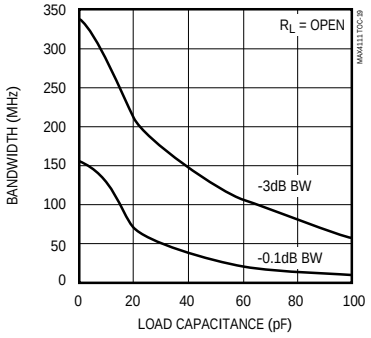
SUPPLY CURRENT vs. TEMPERATURE



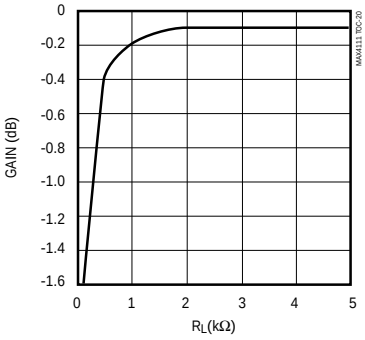
GAIN vs. INPUT VOLTAGE AND TEMPERATURE



BANDWIDTH vs. LOAD CAPACITANCE



GAIN vs. LOAD RESISTANCE



Pin Description

PIN			NAME	FUNCTION
MAX4111	MAX4121	MAX4221		
1, 3	3	2, 4, 5, 7	GND	Analog (signal) ground. Since inputs are isolated by these grounds, GND should be as noise-free as possible.
—	1	—	A0	Logic Input. Channel Selection Bit for the 2x1. See Table 2.
2	—	—	IN	Signal Input
—	2, 4	1, 3	IN0, IN1	Signal Input
4	—	—	N.C.	No Connect—not internally connected
5	5	12	V_{EE}	Negative Power-Supply Voltage. Connect to -5V. Decouple to power ground.
6	6	—	OUT	Signal Output
—	—	6, 8	IN2, IN3	Signal Inputs for the dual 2x1 switch
7	7	14	V_{CC}	Positive Power-Supply Voltage. Connect to +5V. Decouple to power ground.
8	8	—	EN	Logic Input. Output Enable for the 1x1, 2x1 switches. A logic high on this pin enables the output. A logic low causes the output to assume a high-impedance state, and reduces supply current.
—	—	9, 10	SEL3, SEL2	Logic Inputs. Channel Selection Bits for OUT1 of the dual 2x1 (MAX4221). See Table 3.
—	—	11, 13	OUT1, OUT0	Signal Outputs
—	—	15, 16	SEL1, SEL0	Logic Inputs. Channel Selection Bits for OUT0 of the dual 2x1 (MAX4221). See Table 3.

Detailed Description

The MAX4111/MAX4121/MAX4221 video switches are manufactured with Maxim's proprietary, ultra-high frequency, complementary bipolar process that yields high bandwidth and low capacitance. Make-before-break switching is used to reduce noise and glitches, even when switching from part to part in large arrays. The input buffers provide a constant high input impedance, and prevent the make-before-break action from feeding back to the input.

The design of the switching mechanism limits the inevitable glitch to less than 13mVp-p. In addition, the glitch pulse is positive to avoid confusion with negative sync pulses.

Unity-gain buffers isolate other inputs from the switching action of large multiplex arrays. These buffers can drive 5kΩ resistive loads. In addition, these devices drive capacitive loads without oscillation. Load capacitance is limited only by system bandwidth requirements.

The MAX4111/MAX4121/MAX4221 do not contain buffer latches. The digital inputs are transparent.

Table 1. MAX4111 Truth Table

EN	OUT
0	High-Z
1	IN

Table 2. MAX4121 Truth Table

A0	EN	OUT
X	0	High-Z
0	1	IN0
1	1	IN1

Table 3. MAX4221 Truth Table

SEL0	SEL1	OUT0
0	0	High-Z
1	0	IN0
0	1	IN1
1	1	NA

SEL2	SEL3	OUT1
0	0	High-Z
1	0	IN2
0	1	IN3
1	1	NA

Note: SEL0 = SEL1 = 1 and/or SEL2 = SEL3 = 1 is not allowed. Enabling these states will not damage the device, but may cause excessive supply currents and distortion.

Applications Information

Grounding, Bypassing, and PC Board Layout

To obtain the full 330MHz bandwidth of these switches, Microstrip and Stripline techniques are recommended. To ensure your PC board does not degrade the switch's performance, it's wise to design the board for a frequency greater than 1GHz. Even with very short runs, it's good practice to use this technique at critical points such as inputs and outputs.

Use the following guidelines when designing the board:

- Do not use wire-wrap boards, because they are too inductive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.
- In general, surface-mount components have shorter leads and lower parasitic reactance, and give better high-frequency performance than through-hole components.
- The PC board should have at least two layers, with one side a signal side and the other a ground plane.
- Keep signal lines as short and straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.

Bypass Components—Capacitors

Surface-mount ceramic capacitors are recommended to achieve good high-frequency bypassing. A 0.1µF capacitor in parallel with a 1000pF capacitor should be used for each supply. The capacitors should be located as close to the ICs supply pins as possible, with the smaller value capacitor being closer to the IC than the other.

Creating Larger Arrays

The MAX4111/MAX4121/MAX4221 were designed as building blocks for larger arrays. The single-pole switch allows the system designer much greater control over crosstalk than multiple switches in a single IC. For this reason, cable drivers have not been included in the switch design because of the high-power drive required (see Figure 6).

Even though the stability of these devices is not worsened by adding capacitance, you may want to limit the number of switches connected together. The MAX4111/MAX4121/MAX4221 have a finite input capacitance of about 3pF and a dynamic output resistance of about 20Ω. This causes a pole at a little more than 2.7GHz. However, in a large array with many switch inputs, the total capacitance is N x 3pF, where "N" is the number of switches connected in parallel. The pole will be located at:

$$\frac{1}{2\pi \times (N \times 3pF + C_{STRAY}) \times 20\Omega} MHz$$

C_{STRAY} = Stray capacitance at the interconnect

If the maximum number of switches that may be connected while still maintaining bandwidth is less than your system requirements, use a unity-gain buffer amplifier to isolate the switch from the remainder of the inputs.

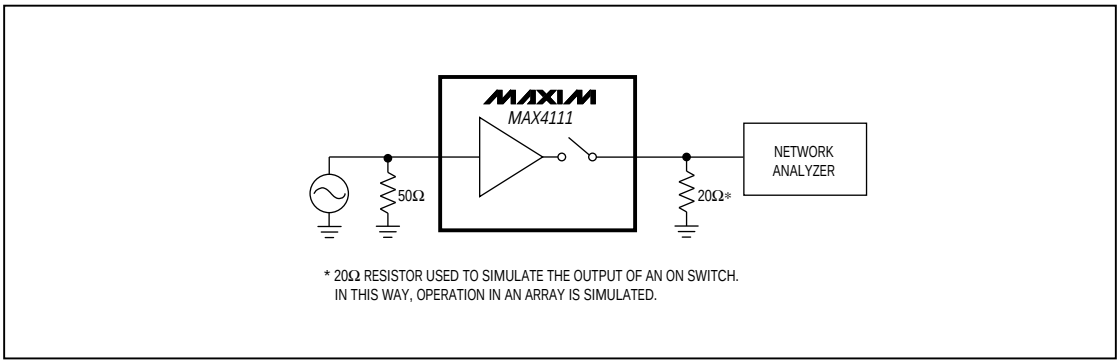


Figure 1. MAX4111 Off Isolation

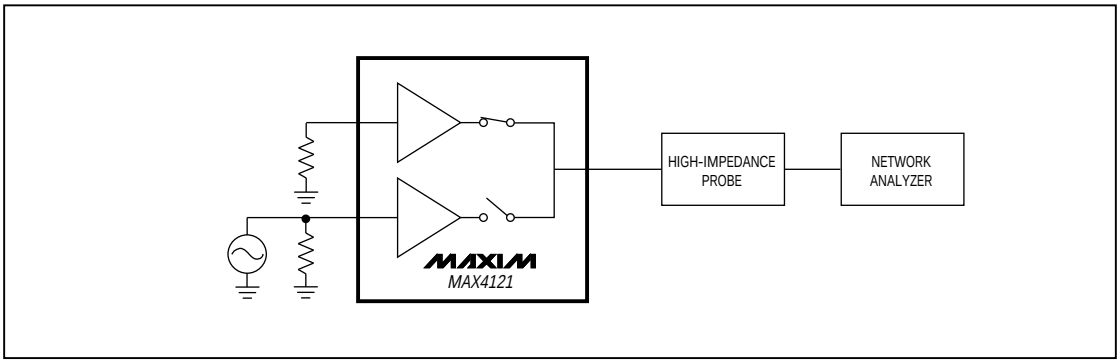


Figure 2. MAX4121 All-Hostile Crosstalk

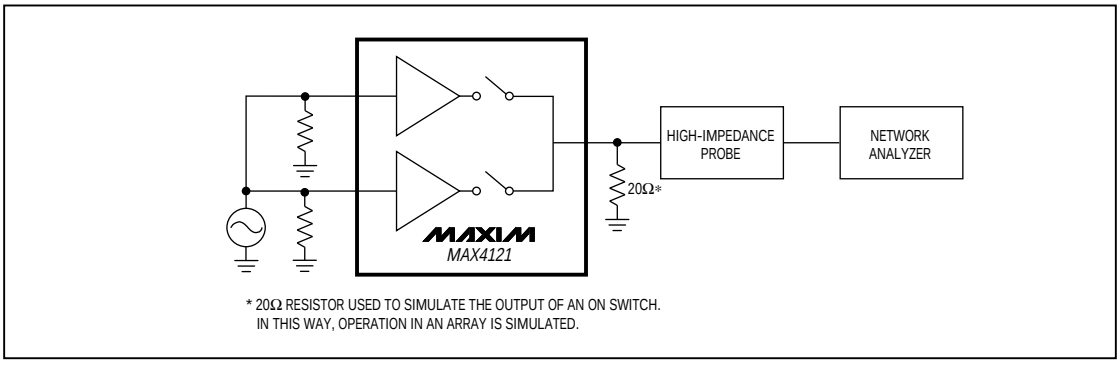


Figure 3. MAX4121 Off Isolation

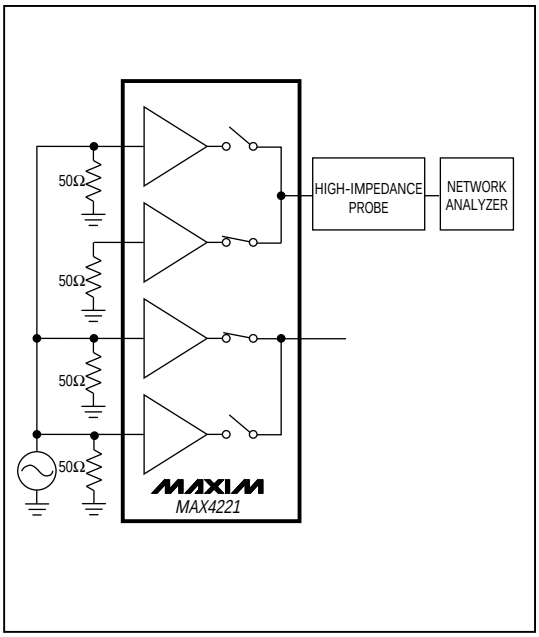


Figure 4. MAX4221 All-Hostile Crosstalk

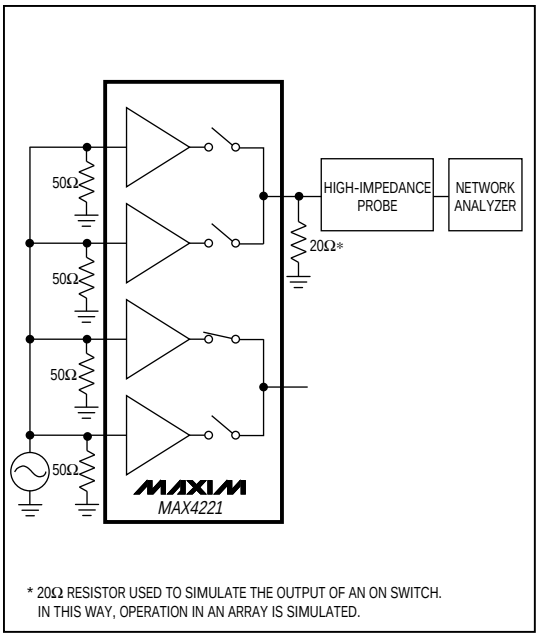


Figure 5. MAX4221 Off Isolation

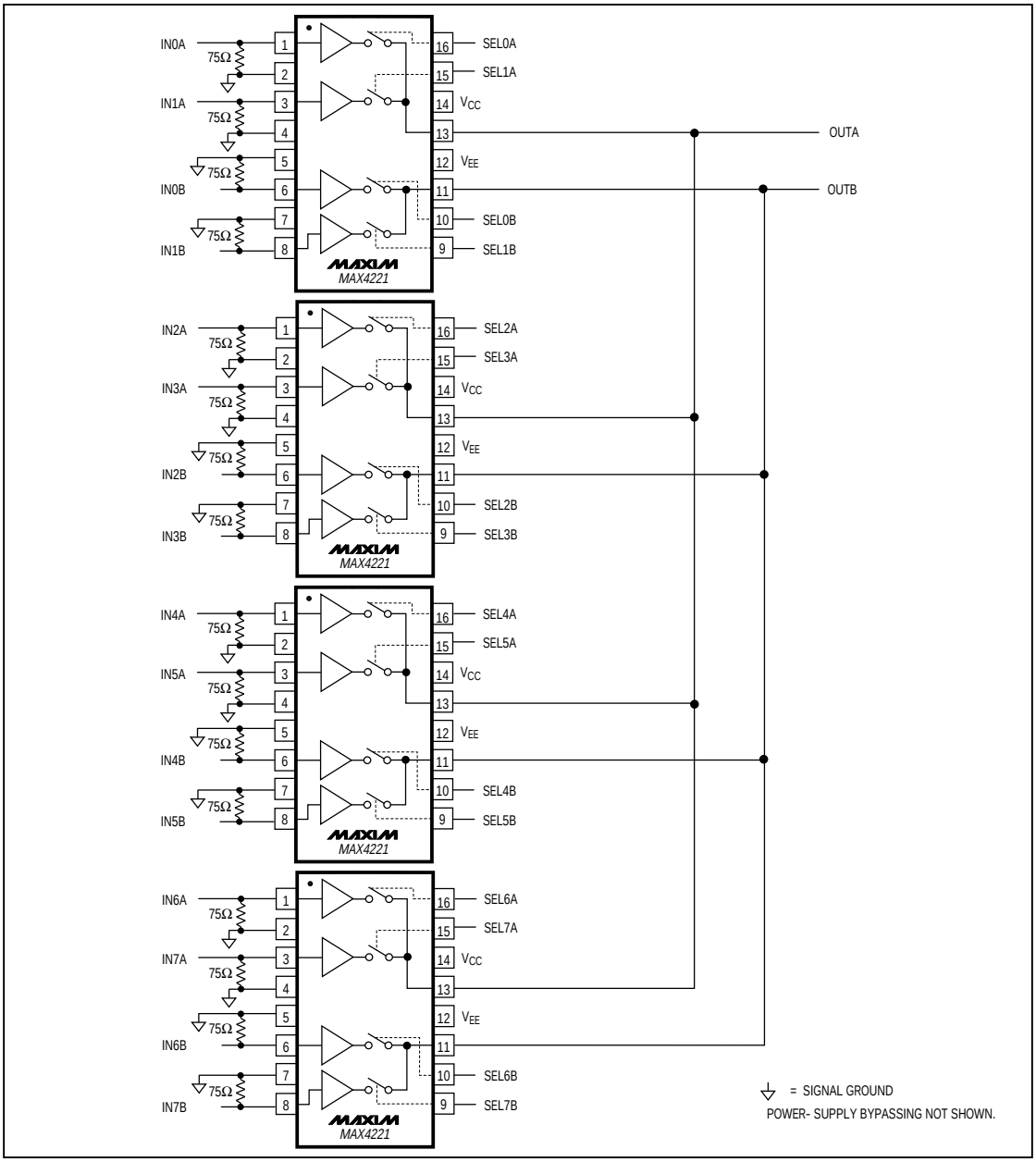
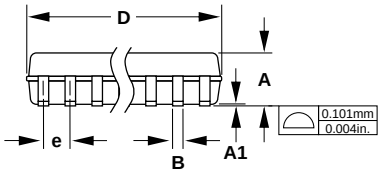
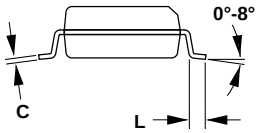
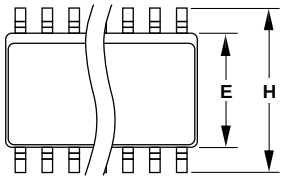


Figure 6. 8x2 Multiplexer Using MAX4221

Package Information







Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

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