

10–43.5 GHz GaAs MMIC Voltage Variable Attenuator

Alpha

AV850M2-00

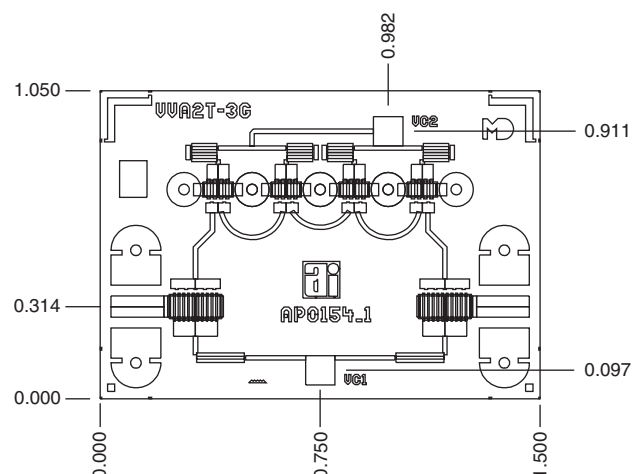
Features

- Dual Voltage Control
- 35 dB Attenuation Range
- +10 dBm $P_{1\text{ dB}}$ All Attenuation States
- 100% On-Wafer RF and DC Testing
- 100% Visual Inspection to MIL-STD-883 MT 2010
- Ideal for Ka Band SatCom, Point to Point and Point to Multi-Point Applications

Description

Alpha's AV850M2-00 MMIC voltage variable attenuator is a standard TEE configuration incorporating triple-gate 0.25 μm power MESFETs. The attenuator has a typical insertion loss of 3 dB over the 10–40 GHz band. The attenuation range is 35 dB while typical I/P and O/P return loss is better than 6 dB. The MMICs employ surface passivation to ensure a rugged, reliable part with through-substrate via holes and gold-based backside metallization to facilitate a conductive epoxy or solder die attach process. This chip incorporates triple-gate FETs which results in less attenuation variation over temperature as well as better power handling performance at all attenuation states. All chips are screened for insertion loss, full attenuation and I/P and O/P match over the 10–43.5 GHz band for guaranteed performance.

Chip Outline



Dimensions indicated in mm.

All DC (V) pads are 0.1 x 0.1 mm and RF In, Out pads are 0.07 mm wide.
Chip thickness = 0.1 mm.

Absolute Maximum Ratings

Characteristic	Value
Operating Temperature (T_C)	-55°C to +90°C
Storage Temperature (T_{ST})	-65°C to +150°C
Control Voltage (V_C)	-7 V_{DC}
Power In (P_{IN})	30 dBm
Junction Temperature (T_J)	175°C

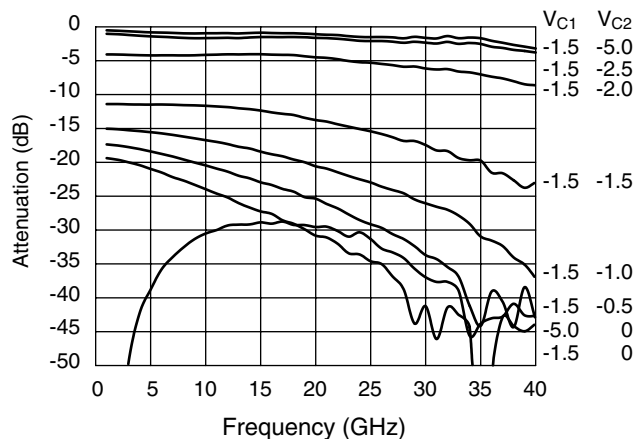
Electrical Specifications at 25°C

Parameter	Condition		Frequency (GHz)	Symbol	Min.	Typ. ²	Max.	Unit
	V_{C1}	V_{C2}						
Maximum Attenuation	-1	-0.25	10.0–18.0	ISO	15	22		dB
	-1	-0.25	18.0–26.0	ISO	20	26		dB
	-1	-0.25	26.0–35.0	ISO	25	32		dB
	0	-0.80	35.0–43.5	ISO	34	44		dB
Minimum Attenuation	-1	-2.50	10.0–18.0	I_L		1.0	2.0	dB
	-1	-2.50	18.0–26.0	I_L		2.0	2.5	dB
	-1	-2.50	26.0–35.0	I_L		2.5	3.0	dB
	0	-2.50	35.0–43.5	I_L		4.0	5.0	dB
Input/Output Return Loss			10.0–43.5	RL		-10		dB
Input Power at 1 dB Compression (For All Attenuation Levels) ¹			10.0–43.5	$P_{1\text{ dB}}$		10		dB
Thermal Resistance				θ_{JC}		101		°C/W

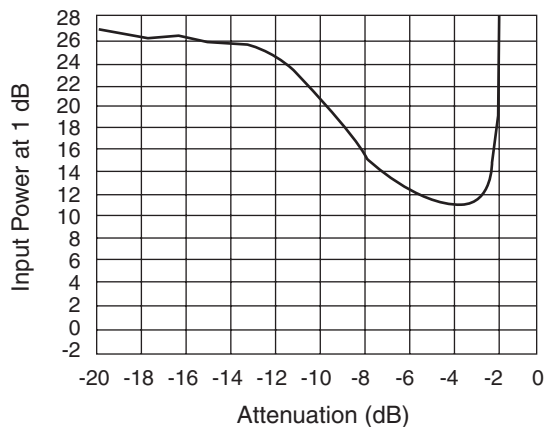
1. Not measured on a 100% basis.

2. Typical represents the median parameter value across the specified frequency range for the median chip.

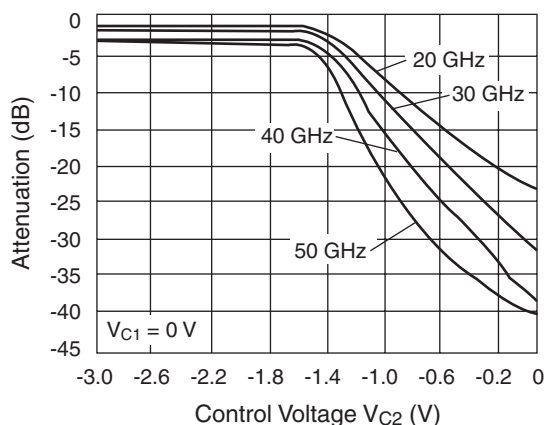
Typical Performance Data



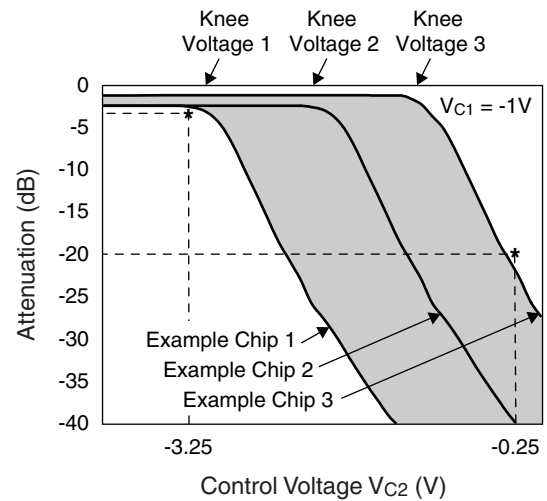
Attenuation vs. Frequency



Attenuation vs. 1.0 dB Compression



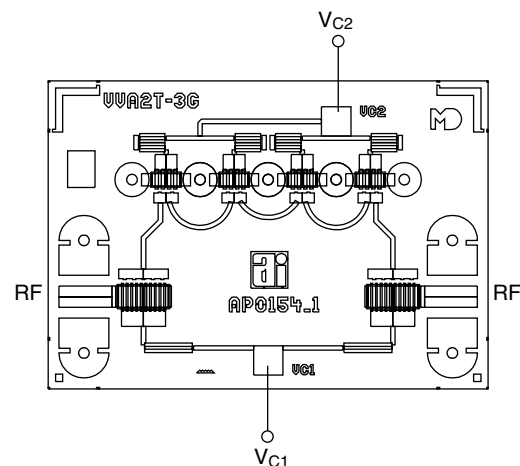
Attenuation vs. Control Voltage



Example Chip-to-Chip Variation for Any Single-Frequency of Operation (Low-Frequency Band)

* Asterisk in graph indicates guaranteed attenuation limits from the Electrical Specification table (knee voltage can vary from -3.25 V to approximately -1.0 V).

Bias Arrangement



V_{C1} controls the series devices, adjust for optimum VSWR.

V_{C2} controls the shunt devices, adjust to set attenuation.

Recommended Control Voltages:

For frequency 18–35 GHz: $V_{C1} = -1$ V, $V_{C2} = -0.25$ to -3.25 V.

For frequency 35–43.5 GHz: $V_{C1} = 0$ V, $V_{C2} = -0.8$ to -3.25 V.

Circuit Schematic

